IPC-2292

Design Standard for Printed Electronics on Flexible Substrates

Developed by the D-61 Printed Electronics Design Subcommittee of the D-60 Printed Electronics Committee of IPC

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 105N
Bannockburn, Illinois
60015-1249
Tel 847 615.7100
Fax 847 615.7105

TABLE OF CONTENTS

1 SCOPE 1
1.1 Printed Electronics Types 1
1.2 Standard Printed Electronics Design 1
1.2.2 Standard Printed Electronic Design (SPED) 2
1.2.3 Standard Printed Electronic Design (SPED) 2
1.2.4 Standard Printed Electronics Design (SPED) Example .3
1.3 Definition of Requirements 3
1.4 Classification of Product 3

2 APPLICABLE DOCUMENTS 3
2.1 IPC 3
2.2 Joint Standards 4
2.5 NCSL International 4

3 GENERAL REQUIREMENTS 4
3.1 Terms and Definitions 4
3.1.1 Crease 4
3.1.2 Panelization 4
3.1.3 Substrate 4
3.1.4 Printed Electronics 4
3.1.5 Printed Electronics Process 5
3.2 Information Hierarchy 5
3.2.1 Order of Precedence 5
3.2.2 End-Product Performance Requirements 5
3.3 Design Considerations 5
3.4 Schematic/Logic Diagram 6
3.5 Density Evaluation 6
3.6 Parts List 6
3.7 Test Requirement Considerations 6
3.7.1 Electrical 6
3.7.2 Printed Electronic Assembly Testability 9
3.7.3 Functional Testing 10
3.7.4 Test Points and Connectors 10
3.8 Layout Evaluation 10
3.8.1 Layout Design 10
3.8.2 Feasibility Density Evaluation 11

4 MATERIALS 11
4.1 Material Selection 11
4.1.2 Functional Conductive Material Options 13
4.2 Flex Applications 13
4.2.1 Stretch and Elongation 13
4.2.2 Crease and Crumple 13
4.2.3 Gap Bridging Applications 13
4.2.4 Via Hole Aspect Ratio/Material Deposit Aspect Ratio .13
4.2.5 Process Compatibility 14
4.2.6 Vertical Transition Angles 14
4.3 Materials Deposition Methods 14
4.3.1 Analog Printing Methods 17
4.3.2 Digital Printed Electronics Material Deposition Methods 17
4.3.3 Dispense Method Considerations 17
4.3.4 Contact Resistance 18
4.3.6 Ink-to-Substrate Compatibility 18
4.3.7 Ink Properties 18
4.4 Dielectric Materials 18
4.4.1 Dielectric Filaments 18
4.4.2 Dielectric Ink Materials 18
4.5 Adhesives 18
4.5.1 Liquid Adhesives 18
4.5.2 Flexible Adhesive Bonding Films (Dry-Film Adhesive) 18
4.5.3 Pressure-Sensitive Adhesives (PSAs) 19
4.6 Conductive Materials 19
4.6.1 Conductive Inks Functioning by Percolation 19
4.6.3 Conductive Filaments (Wires, Coated Wires or Conductive Filaments) 20
4.6.4 Conductive Films, Foils and Grids 20
4.6.5 Printed Conductive Seed Layers for Plating (Print and Plate) 20
4.6.6 Conductive Interfaces and Out-of-Plane Interconnects 21
4.6.7 Isotropic Conductive Adhesives 21
4.6.8 Anisotropic Conductive Adhesives 21
4.7 Operations Following Plating 21
4.8 Coatings 21
4.8.1 Carbon for Printed Ag 21
4.8.2 Conductive Coatings for Shielding 21
4.8.3 Organic Protective Coatings 21
4.8.4 Conformal Coating, Spray Coats 21
4.9 Other Cover Materials 21
4.9.1 Coverlay 21
4.9.2 Coverfilm 22
4.9.3 Covercoat 22
4.10 Other Printed Materials 22
4.11 Marking and Legend 22

5 MECHANICAL AND PHYSICAL PROPERTIES 22
5.1 Fabrication Requirements 22
5.1.1 Printed Flex Fabrication – Sheet Form 22
5.1.2 Printed Flex Roll-to-Roll Fabrication 22
5.2 Product/Printed Flex Configuration 22
5.2.1 Circuit Profile (Outline) 22
5.2.2 Flexible Areas 23
5.2.3 Forming Bends 25

6 ELECTRICAL PROPERTIES 26
6.1 Electrical Considerations 26
6.1.1 Electrical Performance 26
6.1.2 Power Distribution Considerations 26
6.1.3 Circuit Type Considerations 26
6.2 Conductive Material Requirements 27
6.3 Electrical Clearance 27
6.4 Impedance Controls 28
6.5 Formed Components 28
6.5.1 Formed Resistors 28
6.5.2 Formed Capacitors 28
6.5.3 Formed Inductors 29
6.5.4 Formed Active Components 29

7 THERMAL MANAGEMENT 29
7.1 Cooling Mechanisms 29
7.1.1 Conduction 29
7.1.2 Radiation 30
7.1.3 Convection 30
7.1.4 Altitude Effects 31
7.2 Heat Dissipation Considerations 31

8 COMPONENT AND ASSEMBLY ISSUES 31
8.1 Lands for Surface-Mount Components 32
8.2 Constraints on Mounting to Flexible Sections 32
8.3 General Placement Requirements 32
8.3.1 Automatic Assembly 32
8.3.2 Orientation 33
8.3.3 Accessibility 33
8.3.4 Design Envelope 33
8.3.5 Flush Mounting Over Conductive Areas 34
8.3.6 Clearances 34
8.3.7 Physical Support 34
8.4 General Attachment Requirements 34
8.4.1 Thermal Processing Considerations 34
8.4.2 Fastening Hardware 34
8.4.3 Stiffeners 34
8.4.4 Wire Assembly 34
8.4.5 Bus Bar 35
8.4.6 Component Selection Considerations 35

9 HOLES/INTERCONNECTIONS 36
9.1 Printed Land Requirements 36
9.2 Holes 36
9.2.1 Unsupported Holes 36
9.2.2 Printed Through-Holes 36

10 DOCUMENTATION 36
10.1 Special Tooling 37
10.2 Layout 37
10.2.1 Viewing 37
10.2.2 Accuracy and Scale 37
10.2.3 Model and Drawing Notes 37
10.2.4 Automated-Layout Techniques 37
10.3 Deviation Requirements 38
10.4 Phototool Considerations 38
10.4.1 Artwork Master Files 38
10.4.2 Coating Phototools 38

11 QUALITY ASSURANCE 38
11.1 Material Quality Assurance 38
11.2 Statistical Process Control (SPC) 38
11.3 Build and Manufacturing Controls 39
11.4 Conformance Test Coupons 39
11.4.1 Individual Coupon Design 39
11.4.2 Coupon Quantity and Location 39
11.4.3 Process Control Test Coupon 39
11.4.5 Coupon Identification 40
11.5 Responsibility for Inspection 40
11.6 Test Equipment and Inspection Facilities 40
11.7 Preparation of Samples 40
11.8 Standard Laboratory Conditions 40
11.9 Tolerances 40
11.10 Qualification Inspection 40
11.11 Failures 40
11.12 User Sampling Plan 40
11.13 Noncompliance 40
11.14 Reduction of Quality Conformance Testing 40
11.15 Inspection Methodology 40
11.15.1 Process Verification Inspection 40
11.15.2 Visual Inspection 41
11.15.3 Magnification Aids 41
11.15.4 Acceptance and Test Activities 41
11.16 Storage Conditions 41

APPENDIX A Fabrication and Design Features Benefits and Drawbacks 42

APPENDIX B Testability Requirements Considerationsand Design Complexity 51
B.1 Test Requirement Considerations 51
B.2 Design Complexity 51
B.3 Test Equipment Interfaces 51
B.4 Circuit Test Methods 51

APPENDIX C Sample Layout Views for Printed Electronic Designs 53

Figures

Figure 1-1 Standard Printed Electronic Design (SPED) 1 2
Figure 1-2 Standard Printed Electronic Design (SPED) 2 2
Figure 1-3 Standard Printed Electronics Design (SPED) 3 2
Figure 1-4 Example of Printed Electronic Using Every Standard Printed Electronic Design (SPED) Type in One Device 3
Figure 3-1 Rounded Probe and Pin Probe 9
Figure 4-1 Cross-Sectional View of a Representative Construction Identifying Material Types 11
Figure 4-2 Meander Pattern 13
Figure 4-3 Hole Aspect Ratio 14
Figure 4-4 Material Deposit Aspect Ratio 14
Figure 4-5 Printed Conductive Network and Microstructure for Polymer Thick Film (PTF) Inks (Top) and Metalorganic Inks (Bottom) 20
Figure 5-1 Circuits Nested on a Panel Sheet 22
Figure 5-2 Relief Radii 23
Figure 5-3 Material Added for Increased Tear Resistance 23
Figure 5-4 Conductors in Bend Areas 24
Figure 5-5 Neutral Axis Ideal Construction 24
Figure 5-6 Irregular Folds 25
Figure 6-1 Voltage/Ground Distribution Concepts 26
Figure 8-1 Printed Conductor-to-Hole Interface 34
Figure 8-2 Two Examples of Ramps 36
Figure 11-1 Systematic Path for Implementation of Statistical Process Control (SPC) 39
Figure B-1 In-Circuit Test (ICT) Pads 51
Figure B-2 Connectors/Tails 51
Figure B-3 Test Header Pins 51
Figure B-4 Example of Test Starting Points 52

Tables

Table 3-1 Comparisons of Test and Inspection Methods 10
Table 4-1 Characteristics of Analog Printing Processes 15
Table 6-1 Electrical Conductor Spacing Guidelines 28
Table 7-1 Effects of Material Type on Construction 30
Table 7-2 Emissivity Ratings for Certain Materials 30

DESIGN STANDARD FOR PRINTED ELECTRONICS ON FLEXIBLE SUBSTRATES

1 SCOPE

This standard establishes specific requirements for the design of printed electronic applications and their forms of component mounting and interconnecting structures on flexible substrates. Flexible substrates, as pertain to this standard, are materials or devices which have some amount of flexibility or bendability (not rigid) but are not considered to be stretchable (e.g., fabrics, textiles, stretchable polymers, etc.).

1.1 Printed Electronics Types Any printed electronics design will be incumbent on requirements from the customer, materials to be used and the printing processes. The following printed electronics types represent the known variations of printed electronics. These types cover all known processes for printing electronics (e.g., screen, aerosol, 3D, etc.). As other types or printing processes are made known, they will be added to this standardized list of types.

The printed electronics type **shall** be specified on the procurement document as agreed upon between user and supplier (AABUS). If the printed electronics type is not designated below, a unique type designation will be used.

- *Printed electronics — Type 1: Using printed electronics processes on a planar substrate*
- *Printed electronics — Type 2: Using printed electronics processes on a nonplanar substrate*
- *Printed electronics — Type 3: Using printed electronics processes to fully build and functionalize a device in a 3D space (no starting substrate)*

1.2 Standard Printed Electronics Design (SPED) Classifications Standard print electronics design (SPED) types **shall** be in accordance with 1.2.1 through 1.2.3. For purposes of explanation, a basic variation of each SPED is shown in 1.2.1 through 1.2.3.

Each IPC-2292 SPED consists of the following components:

- *Substrate* — Any flexible nonconductive and/or conductive (e.g., flexible printed board or other manufactured functional part) material
- *Printed element* — Any conductive, semiconductive or dielectric material applied using additive/printing processes
- *Surfaces* — Top and bottom sides of the substrate
  - First surface is top
  - Second surface is bottom

Each additive process required to manufacture the finished flexible printed electronic is identified by an alphanumeric designation. The letter F (first/top surface) or S (second/bottom surface) indicates the side of the substrate. The number indicates the print/process step.

For example:

F1 = first print on the first/top surface

F2 = second print on the first/top surface

S1 = first print on the second/bottom surface

S2 = second print on the second/bottom surface

It is important to note that the print/process step numbers can be repeated on each side, because the numbers only apply to printing elements on a specific side.

1.2.1 Standard Printed Electronic Design (SPED) 1 SPED 1 has printed element(s), which can include vias between printed conductive elements, on one or both surfaces of a substrate. SPED 1 does not have electrical/electronic interconnections from printed element(s) to the substrate.