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Design and Assembly Process Implementation of 3D Components

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Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC

Tel 847 615.7100
Fax 847 615.7105

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Design and Assembly Process Implementation of 3D Components

1 SCOPE

This document describes the design and assembly challenges and ways to address those challenges for implementing 3D component technology. Recognizing the effects of combining multiple uncased semiconductor die elements in a single-package format can impact individual component characteristics and can dictate suitable assembly methodology. The information contained in this standard focuses on achieving optimum functionality, process assessment, end-product reliability and repair issues associated with 3D semiconductor package assembly and processing.

1.1 Purpose Performance-driven electronic systems continue to challenge companies in search of more innovative semiconductor package methodologies. The key market driver for semiconductor package technology is to provide greater functionality and improved performance without increasing package size. The package interposer is the key enabler. Although glass-reinforced epoxy-based materials and high-density Cu interconnect capability will continue to have a primary role for array-configured packaging, there is a trend toward alternative dielectric platforms as well as toward combining multiple functions within the same die element. To address this movement, an increasing number of semiconductor die developed for advanced applications now require higher I/O with contact pitch variations that are significantly smaller than the mainstream semiconductor products previously in the market. For these applications, companies are developing interposer technologies that can provide interconnect densities far superior to organic-based counterparts.

1.1.1 Target Audience The target audiences for this standard are managers, design/process engineers and operators who deal with:

- Implementing 3D semiconductor packaging
- Interposer, substrate and printed board design
- Board-level assembly, inspection and repair processes

1.1.2 Intent This standard intends to provide useful and practical information to those who are designing, developing or using 3D-packaged semiconductor components or those who are considering 3D package implementation. The 3D semiconductor package may include multiple die elements—some homogeneous and some heterogeneous. The package may also include several discrete passive SMT devices, some of which are surface mounted and some of which are integrated (embedded) within the components' substrate structure.

1.2 Classification IPC standards recognize that electrical and electronic assemblies are subject to classifications by intended end-item use. Three general end-product classes have been established to reflect differences in manufacturability, complexity, functional performance requirements, and verification (inspection/test) frequency. It should be recognized that there may be overlaps of equipment between classes.

CLASS 1 General Electronic Products

Includes products suitable for applications where the major requirement is function of the completed assembly.

CLASS 2 Dedicated Service Electronic Products

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically, the end-use environment would not cause failures.

CLASS 3 High Performance/Harsh Environment Electronic Products

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

1.3 Measurement Units All dimensions and tolerances in this specification are expressed in hard SI (metric) units and bracketed soft imperial [inch] units. Users of this specification are expected to use metric dimensions. All dimensions ≥ 1 mm [0.0394 in] will be expressed in millimeters and inches. All dimensions < 1 mm [0.0394 in] will be expressed in micrometers and microinches.

1.4 Use of "Lead" For readability and translation, this document uses the noun lead only to describe leads of a component. The metallic element lead is always written as Pb.

1.5 Abbreviations and Acronyms Periodic table elements are abbreviated in the standard. See Appendix A for full spellings of abbreviations (including elements) and acronyms used in this standard.

1.6 Terms and Definitions Other than those terms listed below, the definitions of terms used in this standard are in accordance with IPC-T-50.

1.6.1 Die* Separated piece(s) of a semiconductor wafer that constitutes a discrete semiconductor or integrated circuit (IC). They are normally uncased and leadless forms of an electronic component.

*singular or plural

1.6.2 Electronic Element A bare die/wafer or discrete component (resistor, capacitor, inductor, transistor, diode, fuse, etc.) with metallized terminals or terminations ready for mounting. The element can be an IC or a discrete electrical, optical or microelectronic mechanical system (MEMS) element. Individual elements cannot be further reduced without destroying their stated function.

1.6.3 Interposer A material placed between two surfaces to provide electrical insulation, redistribution of electrical connections, mechanical strength and/or controlled mechanical and thermal separation between the two surfaces.

1.6.4 Substrate The insulating material upon which a conductive pattern may be formed. (The base material may be rigid or flexible. It may be a dielectric or insulated metal sheet.) For this document, the term substrate refers to an interconnect platform fabricated from organic dielectric materials (rigid, flexible or a combination of rigid and flexible materials). Sometimes referred to as package substrate.

1.6.5 Electronic Package An individual electronic element or elements in a container that protect the contents to ensure integrity and provide terminals to interconnect the container to an outer circuit. Package outline is generally standardized or meets guideline documents. A package may function as electronic, optoelectronic or MEMS, and it may include bioelectronic elements (e.g., sensors).

1.6.6 Electronic Module A functional block that contains individual electronic elements and/or electronic packages to be used in a next-level assembly. An individual module may include an application-specific function or multiple electronic functions (e.g., optoelectronic, mechanical). The module typically provides protection of its elements and packages to ensure the required level of reliability.

1.6.7 Three-Dimensional (3D) Packaging Three-dimensional (3D) integration of heterogeneous elements, using traditional interconnection processes, to achieve vertically configured interconnections.

1.7 Implementation Challenges The next generation of 3D assembly has many implementation challenges, since the technology is complex and requires process expertise that may require foundries, outsourced semiconductor assembly and test (OSAT) providers and original design manufacturers (ODMs). There is no clear direction where 3D packages will be built, tested and assembled. The type of process to be used and the order of assembly and stacking is not defined and depends on the assembler's expertise.

Figure 1-1 illustrates the technological complexity of 3D assembly.

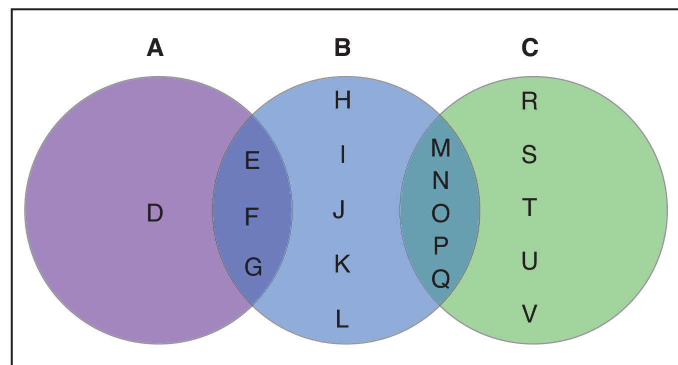

Figure 1-1 3D Technology Complexity

A – Foundry
B – Outsourced semiconductor assembly and test (OSAT)
C – Original design manufacturer (ODM)
D – Wafer process
E – Wafer test known good die (KGD)
F – Through-silicon via (TSV) interposer
G – Micro bumping
H – Package assembly
I – Wire bond
J – Wafer-level packaging (WLP)
K – Package mold
L – Wafer bumping
M – Package bumping
N – Die attach
O – 2.5D assembly
P – Underfill
Q – Prestacked
R – Printed board assembly
S – Package-on-package (PoP) assembly
T – Rework
U – Corner glue
V – System test

As mobile electronics markets continue to see significant growth, there will be an increasing demand for product miniaturization and higher product performance expectation. Developers of personal communication and computing products, for example, have already adopted multicore processors. Furthermore, these high-performance processors will require greater memory bandwidth. To meet these market trends, manufacturers are predicting faster process capability and anticipate reduced power requirements to extend battery life. Next-generation semiconductor package solutions also are projected to be physically robust. While materials for organic-substrate-based applications will meet most commercial applications, more severe operating environments may require a more robust (nonorganic) base substrate material.

Industry may continue to rely on organic-based platforms for a majority of semiconductor packaging applications. When