Role of Surface Finish for Next Generation PCB Technologies – 5G, HDI, RF-Microwave, High Frequencies

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Outline/Agenda

- **Introduction**
- **Results of Experiments**
- **Conclusions**
- **Acknowledgements**
- **Q & A**

High Frequency PCBs Application

- Tremendous growth mobile phones/devices led to enormous increase in amount of data transfer

- High speed-high frequency electronic signals necessary in the electronic assemblies-PCBs

- Choice of materials used to fabricate PCBs is critical to realize the optimum performance for high speed-high frequency applications

High Frequency PCBs’ Needs

- Surface Finish Selection
  - Low insertion loss- No Nickel
  - High reliability- Robust solder joints
  - Long shelf-life (Gold based final finish)
  - Cost-effective- lower thickness of precious metals (Au, Pd, etc.)

Insertion Loss

- Insertion loss of a high-frequency PCB can decrease the usage signal levels of a system

Total insertion loss (α_T)

$$\alpha_T = \boldsymbol{\alpha_C} + \alpha_D + \alpha_R + \alpha_L$$

α_C = Conductor Loss

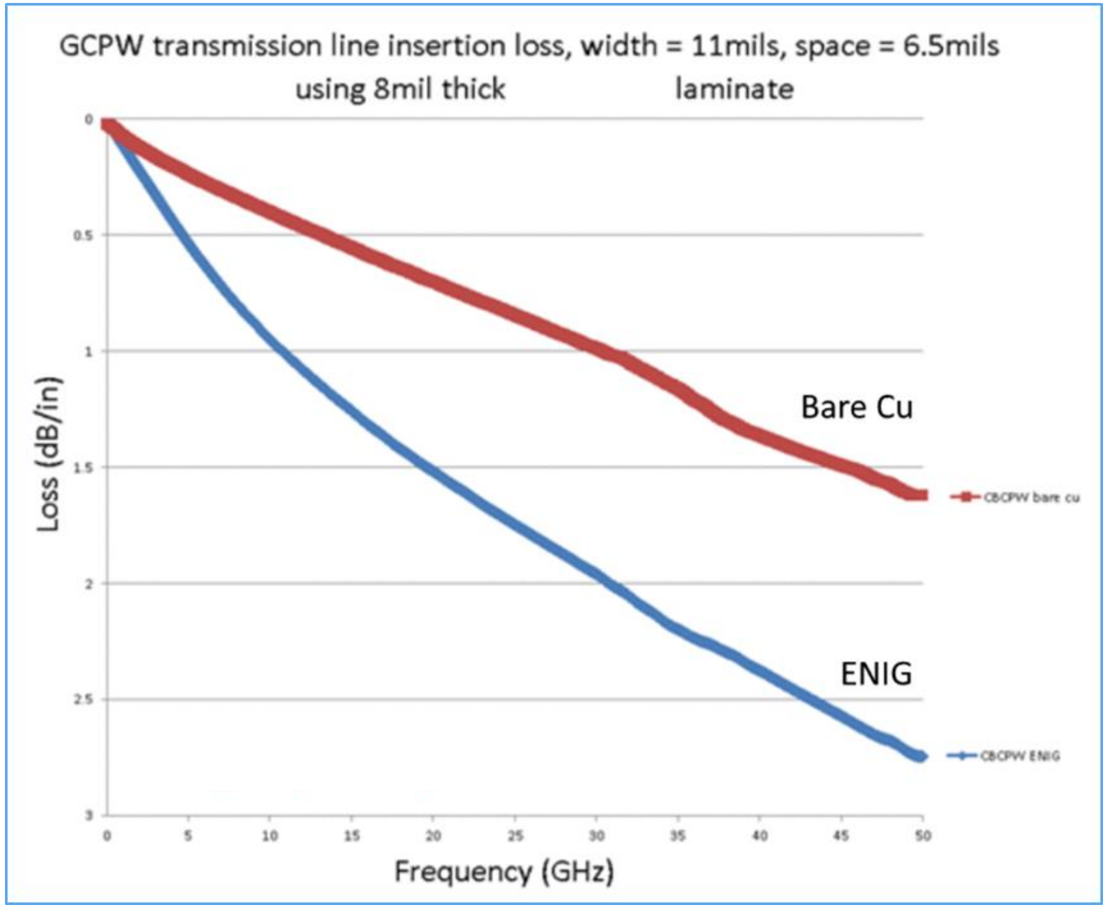
α_D = Dielectric Loss

α_R = Radiation Loss

α_L = Leakage Loss

Conductor loss is correlated to the selection of the surface finish

Prevalent Solution: ENIG



- Electroless Ni/Immersion Gold: (ENIG) Most widely used
  - *Long shelf life (Au based)*
  - *Low surface roughness*

However,

  - *High insertion loss due to Ni (high frequency applications)*
  - *Black pads- hyper corrosion issues*
  - *Brittle solder joints failures*

REF: Insertion Loss Performance Differences Due to Plated Finish and Different Circuit Structures., John Coonrod Rogers Corporation, IPC APEX 2019 Conference Proceedings.

Immersion Tin (Sn)

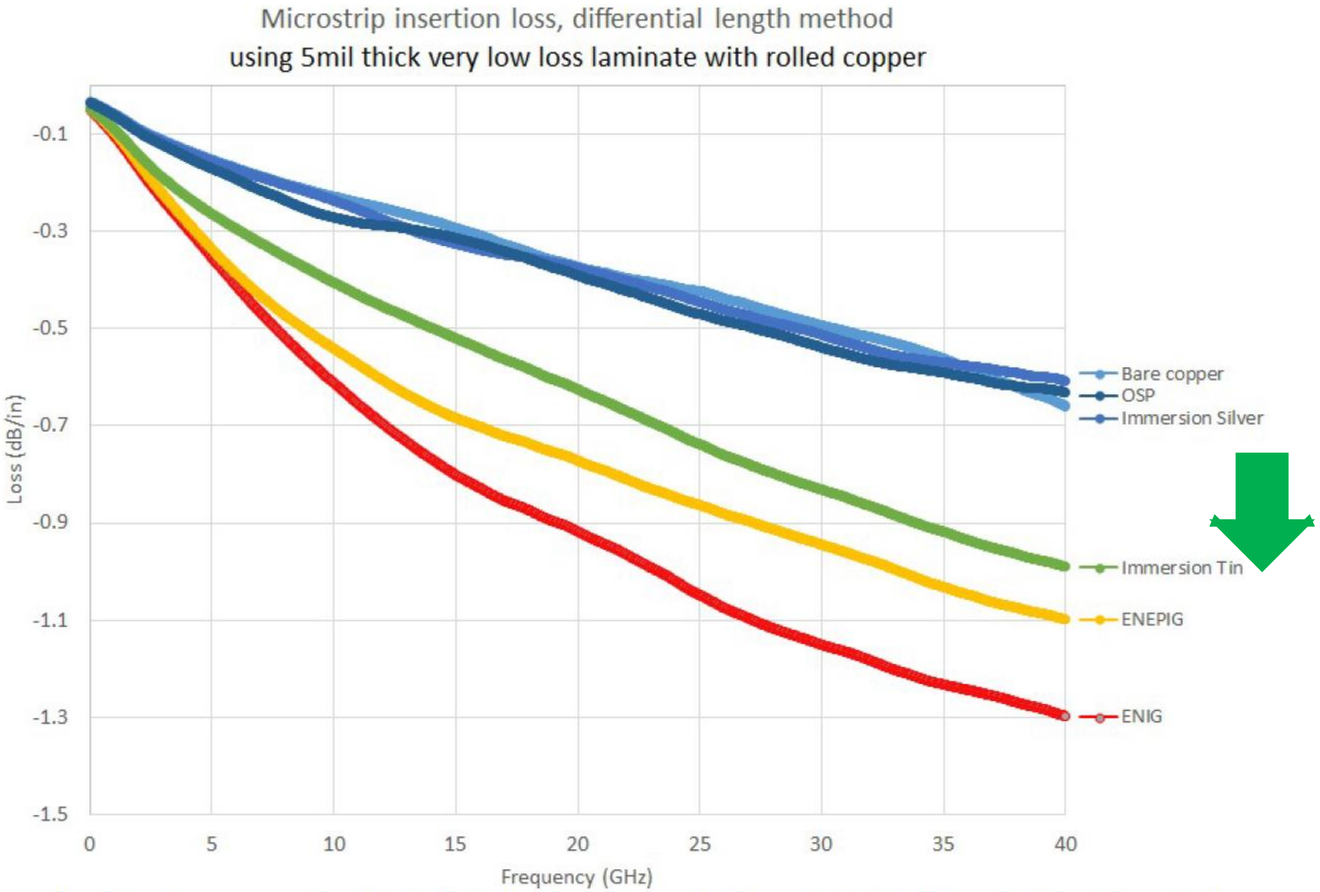


Figure 6. Insertion loss curves of multiple final plated finishes using the microstrip differential length method

- Immersion Sn:
  - *Very good solderability*

However,

  - *Higher insertion loss*
  - *Shelf life (3-6 months)*
  - *Tin whiskers/ Corrosion concerns*
  - *Sensitive to handling*

REF: Insertion Loss Performance Differences Due to Plated Finish and Different Circuit Structures., John Coonrod Rogers Corporation, IPC APEX 2019 Conference Proceedings.

Immersion Silver (Ag)

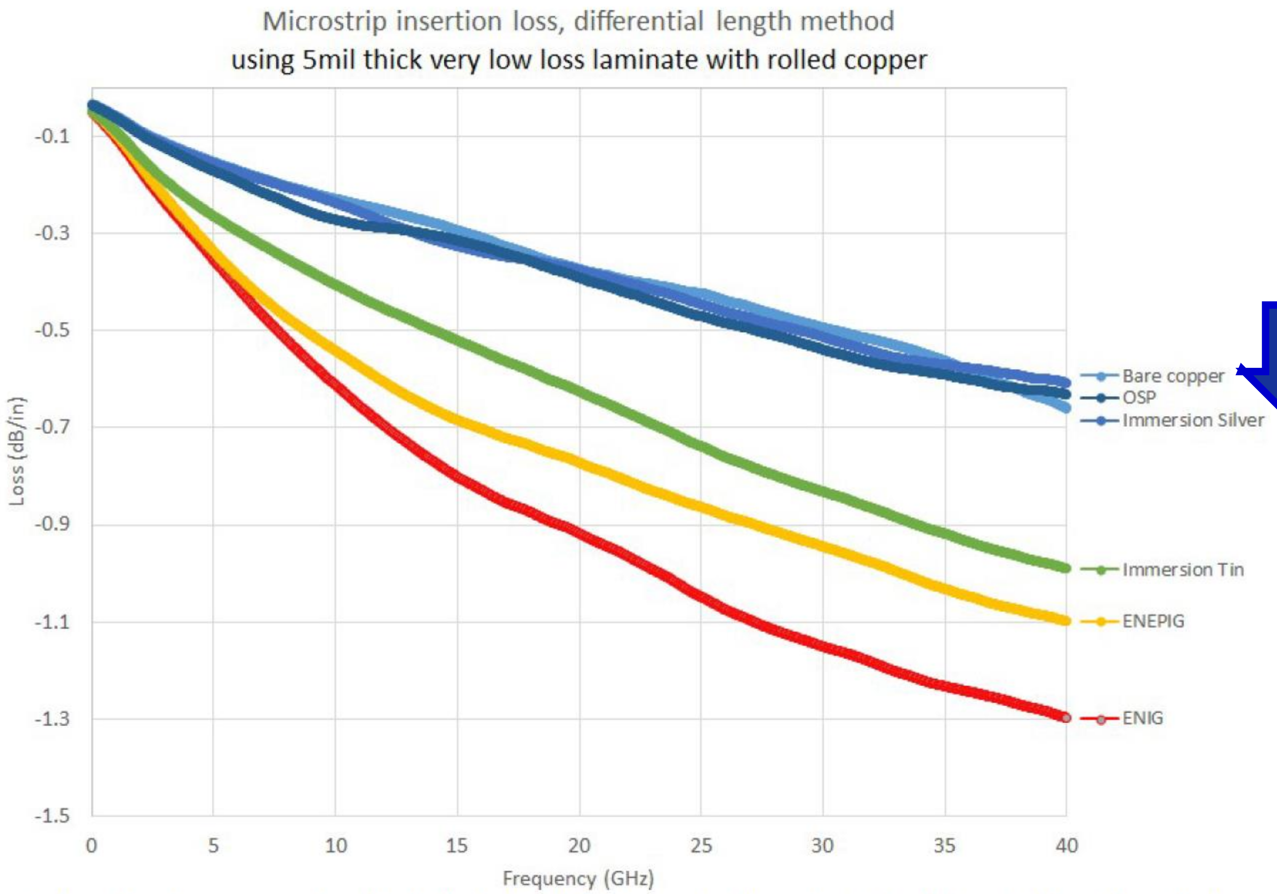


Figure 6. Insertion loss curves of multiple final plated finishes using the microstrip differential length method

- Immersion Ag:
  - *Lower insertion loss*
  - *Low surface roughness*

However,

  - *Shelf life (6-12 months)*
  - *Corrosion concerns/tarnishing*
  - *Sensitive to handling*

REF: Insertion Loss Performance Differences Due to Plated Finish and Different Circuit Structures., John Coonrod Rogers Corporation, IPC APEX 2019 Conference Proceedings.

OSP: Organic Solderability Preservative

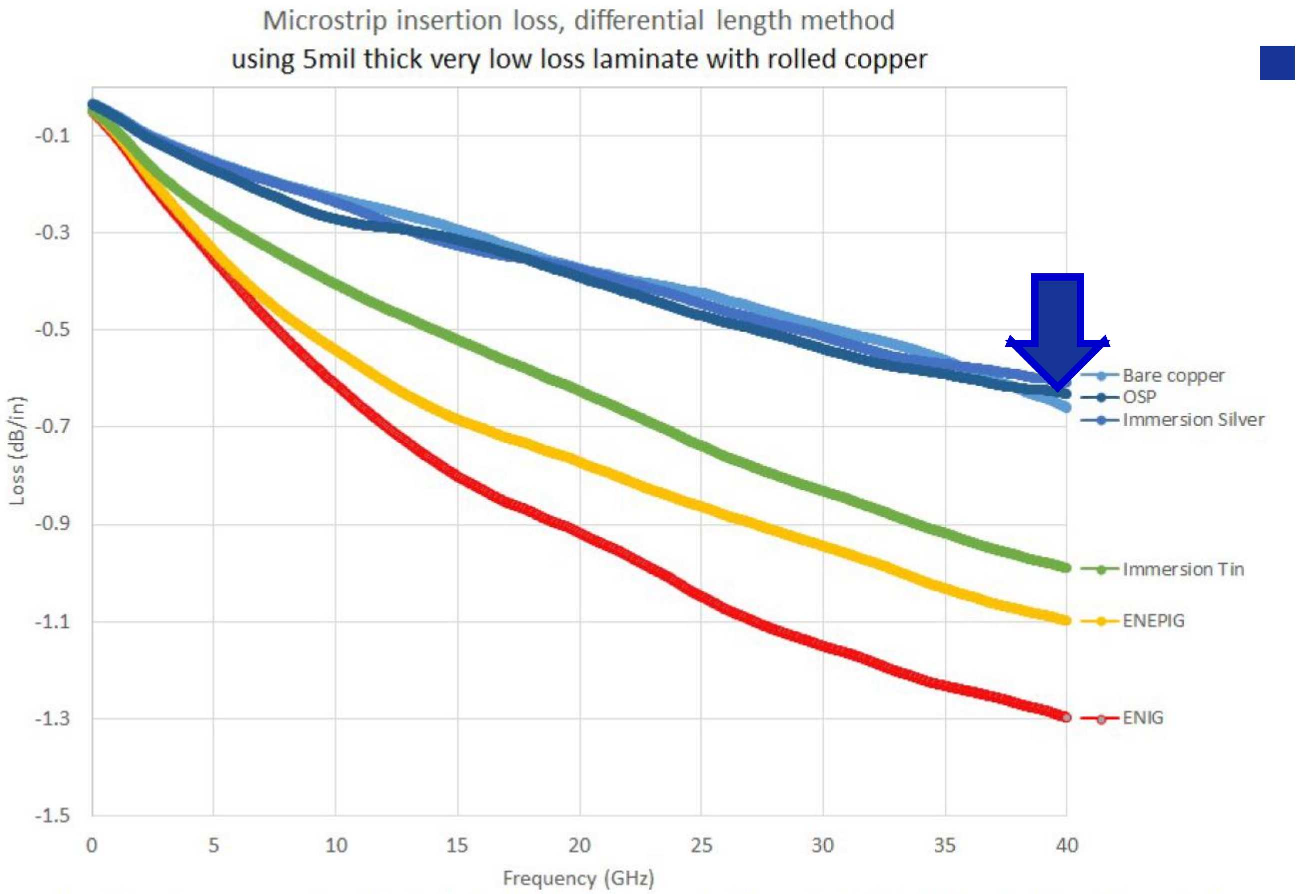


Figure 6. Insertion loss curves of multiple final plated finishes using the microstrip differential length method

- OSP: widely used
  - *Lower insertion loss*
  - *Low surface roughness*

However,

  - *Poor shelf life (3-6 months)*
  - *Concerns over multiple reflow cycles*
  - *Sensitive to handling*

REF: Insertion Loss Performance Differences Due to Plated Finish and Different Circuit Structures., John Coonrod Rogers Corporation, IPC APEX 2019 Conference Proceedings.

Current Ni-free Options: DIG, EPIG, EPAG

Gold based (longer shelf life)

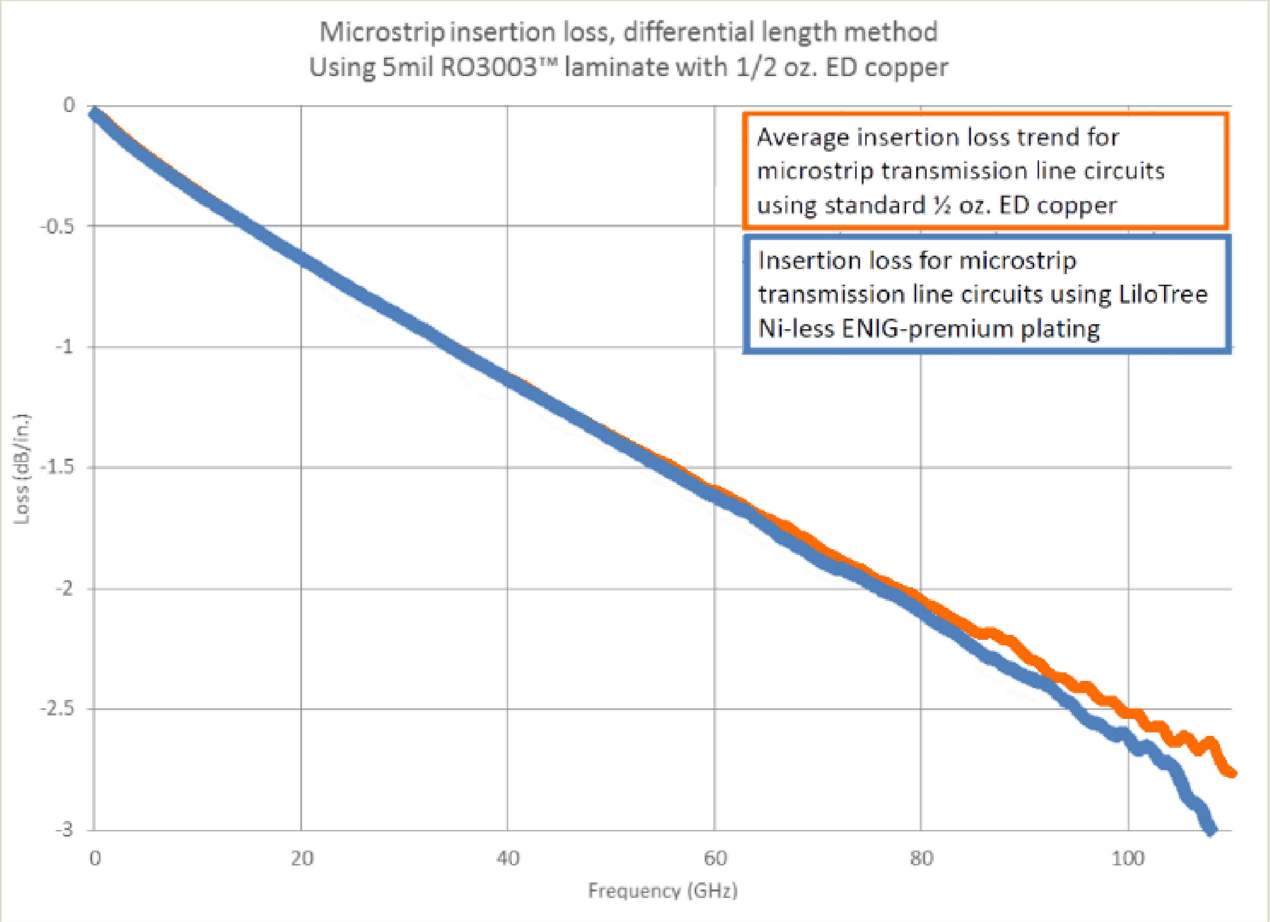
- DIG: Direct Immersion Gold: 150-200 nm of Au directly on Cu
- EPIG: Electroless Palladium Immersion Gold: 100 nm of Pd +100 nm of Au on Cu
- EPAG: Electroless Palladium Autocatalytic Gold: 100 nm of Pd + 100 nm of Au on Cu

Current solutions show reliability concerns in terms of brittle solder joints and resort to higher thickness of precious metals (not cost-effective)

Novel Ni-free Surface Finish

- Novel Ni-free surface finish: 50 nm of Au on nano-engineered (barrier layer treated) Cu
- Robust solder joints (thin & distinct intermetallics)
- Cost effective: Significantly lower thickness of Au (50 nm vs. 150-200 nm of Au or Pd+Au)

Insertion Loss of Novel Surface Finish

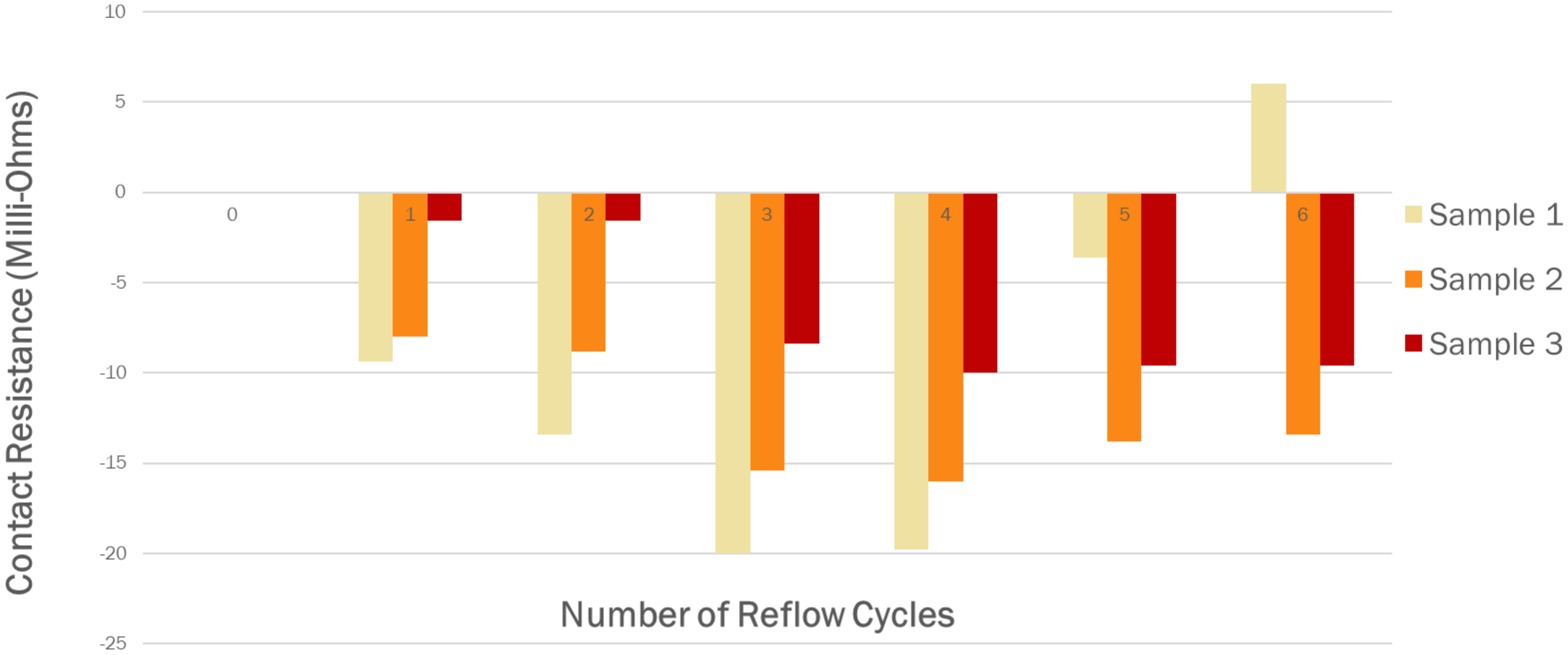


Insertion loss of the Ni-less surface finish (blue) compared to bare standard ½ oz. ED copper (orange) from 0 – 100 GHz on microstrip transmission circuits

- The insertion loss of the Ni-less surface finish almost exactly identical to the insertion loss of bare copper over the 0 – 100 GHz frequency range

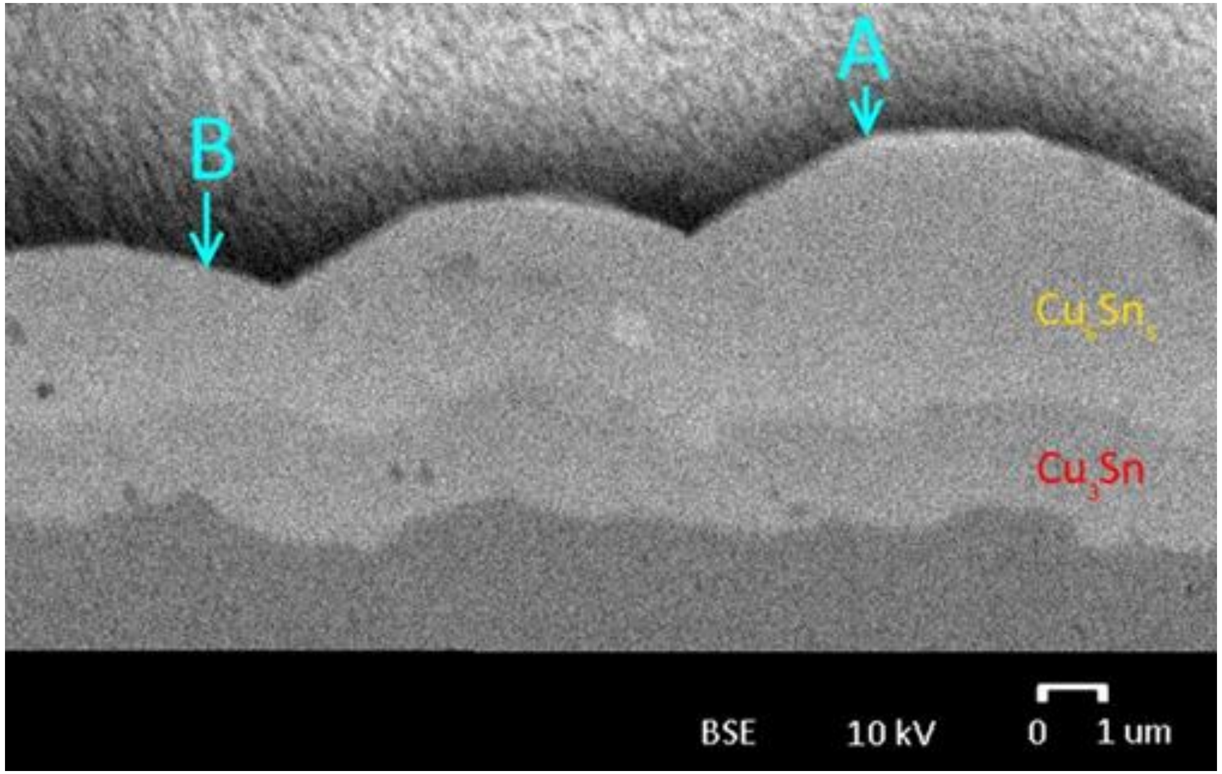
- Ni-free surface finish is able to be used in high-frequency applications with hardly any insertion loss increase compared to bare copper

Contact/Sheet Resistance



- Change in contact resistance after every reflow cycle for each sample is negligible
- Nano-engineered barrier layer on copper surface prevents diffusion of copper into gold surface leaving the surface corrosion free even after 6 reflow cycles

Intermetallics: Ni-free surface finish vs. DIG

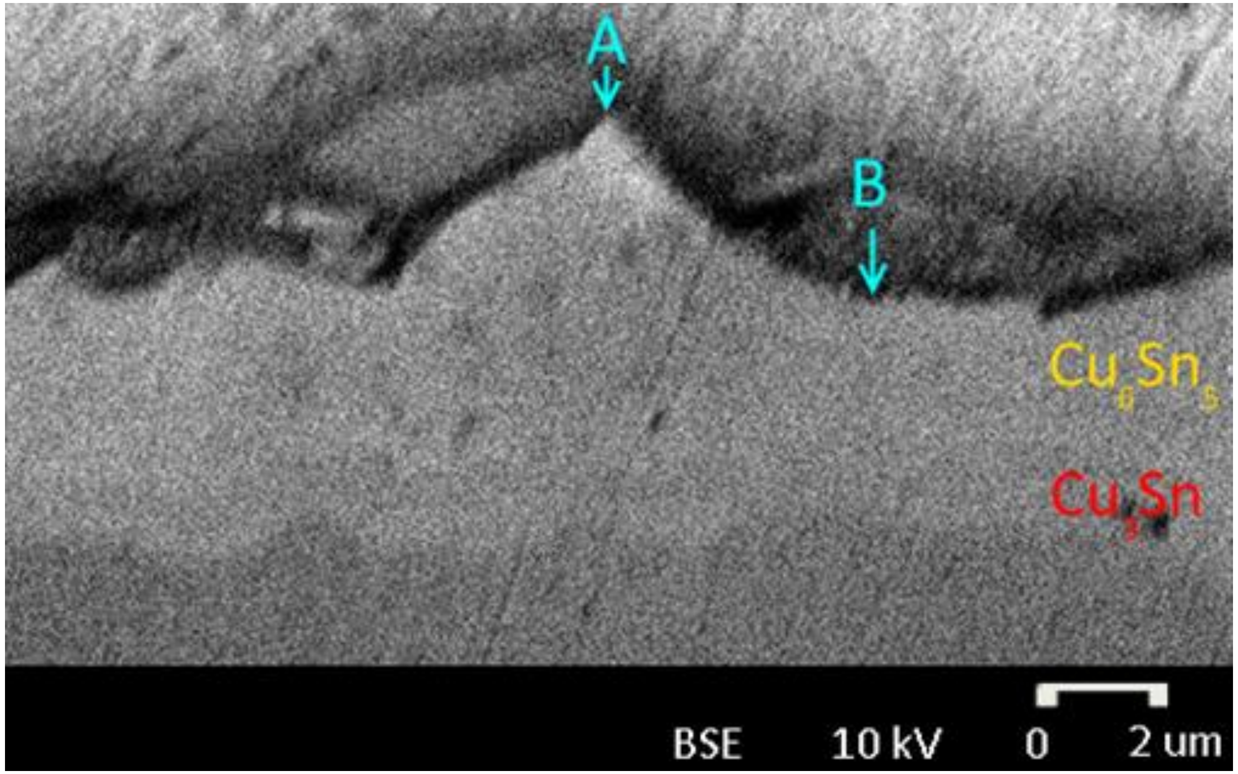


SEM image of Ni-less surface finish intermetallics after 6 reflow cycles and 1000 hours of aging

	Direct Immersion Gold	Ni-less surface finish
Surface Finish Contents	Gold (150-200nm)	Barrier Layer, Gold (50 nm)
Total IMC Thickness Range	~6 – ~11 µm	3.8 (B) – 6.5 (A) µm

- Ni-less surface finish shows superior intermetallic (lower thickness) and requires lower gold thickness (50 nm vs. 150-200 nm) compared to DIG

Intermetallics: Ni-free surface finish vs. EPIG/EPAG

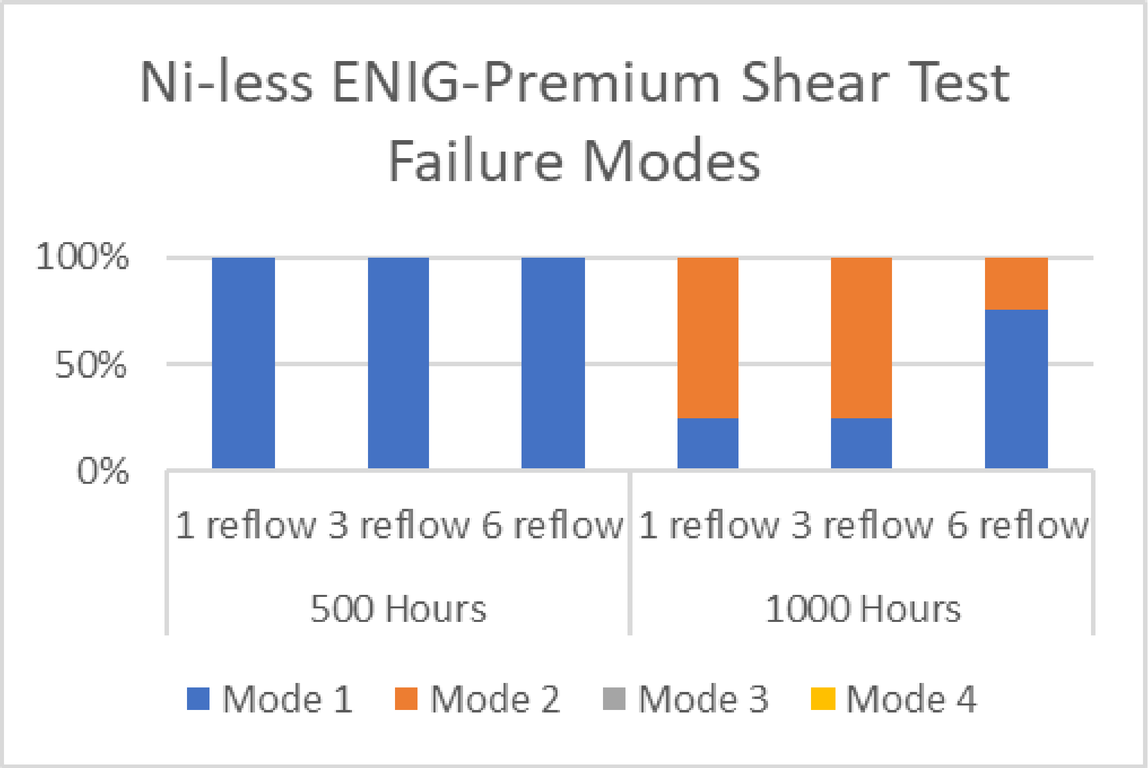


SEM image of Ni-less surface finish intermetallics after 6 reflow cycles and 500 hours of aging

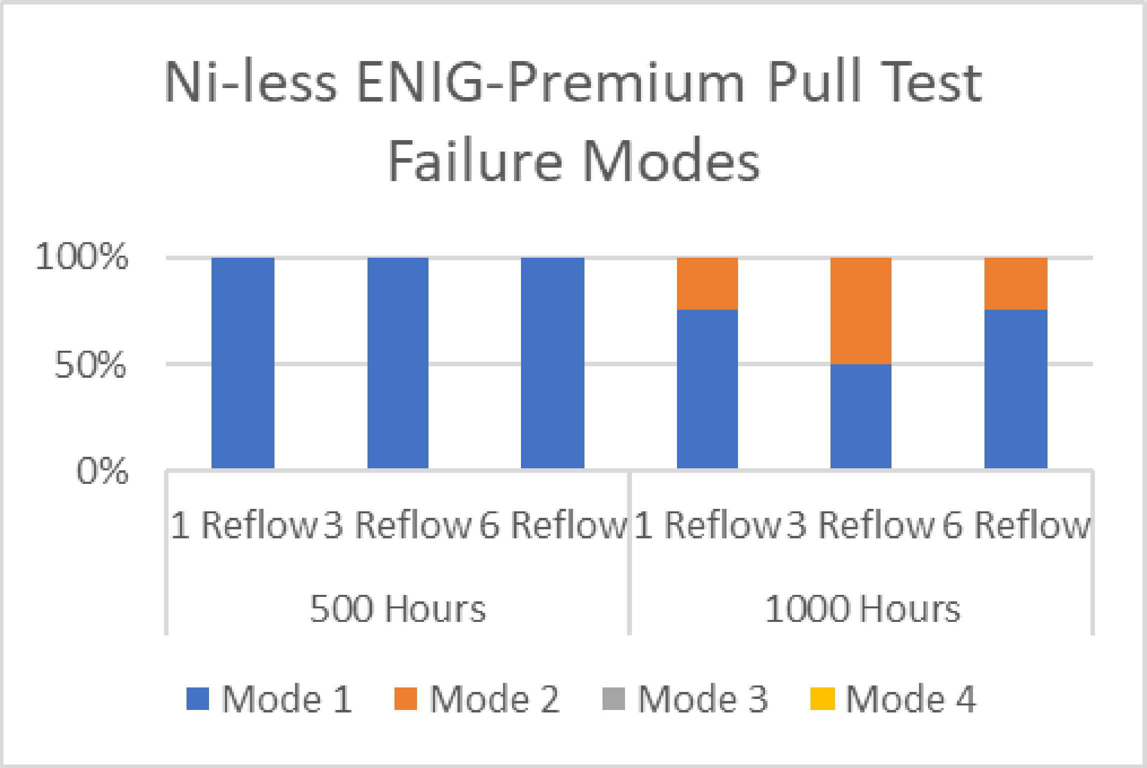
Parameter	EPIG/EPAG	Nickel-less surface finish
Surface Finish Contents	Palladium (100 nm), Gold (100nm)	Barrier Layer, Gold (50 nm)
Total IMC Thickness Range	~3 – ~10 µm	1.7 (B) – 3.2 (A) µm

- Ni-less surface finish shows superior intermetallic (lower thickness) and requires lower gold thickness (50 nm (Au) vs. 200 nm (Au +Pd)) compared to EPIG/EPAG

Solder Ball Shear/Pull Tests



Failure modes during shear tests (JESD22-B117) on solder balls on the Ni-less surface finish for 1, 3, and 6 reflow cycles and 500 and 1000 hours of aging



Failure modes during pull tests (JESD22-B115) on solder balls on the Ni-less surface finish for 1, 3, and 6 reflow cycles and 500 and 1000 hours of aging

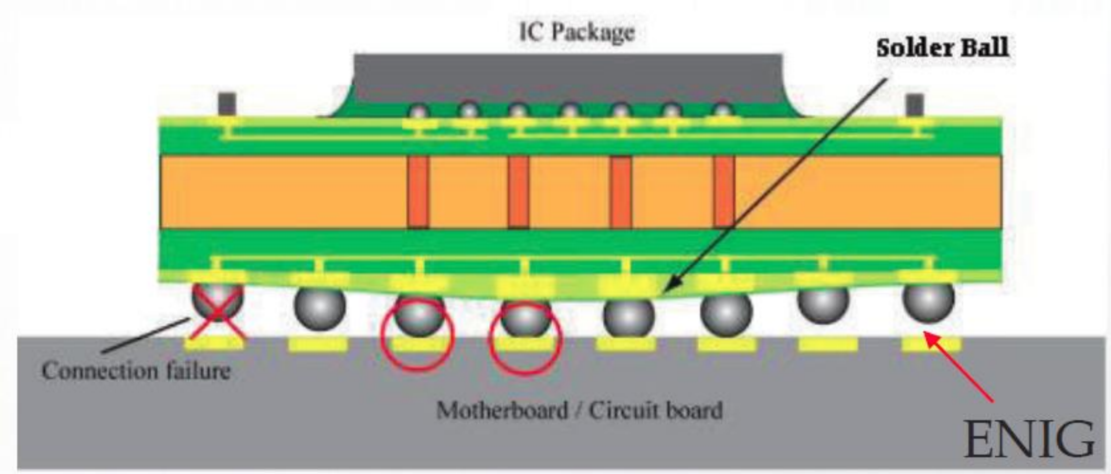
- No brittle intermetallic solder joint failures (Mode 4) observed

Novel Ni-free Surface Finish: Nano-Engineering

Nano-engineering (inclusion of barrier layer) has helped improve the reliability of electronic assemblies

- ✓ *Ni-less solution: Low insertion loss- equivalent to bare Cu*
- ✓ *Long shelf life: Au based surface finish*
- ✓ *Cost-effective: Lower gold thickness (50 nm vs. 150-200 nm)*
- ✓ *High reliability: No brittle failures at solder joints (including Lead-free)*

Key Takeaways



- Connection (Solder Joints) between PCB & surface mount components are prone to high number of failures
    - *Especially with lead-free solder assemblies*

- Innovative technologies are essential to improve intermetallics (solder joints) for better reliability and optimum performance of electronic assemblies

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Thank You!

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Questions?