IPC Wisdom Wednesday

January 8, 2020

Semi Additive Process

High-Performance, High Density Printed Circuit Boards

Averatek

Spun Out of SRI International

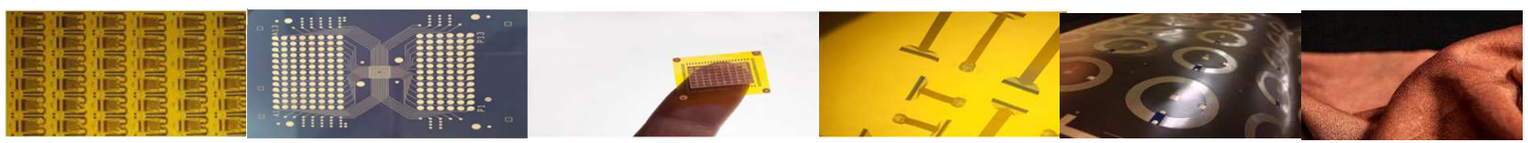
15 Employees

8000 Square Foot Facility

Located in Silicon Valley

Averatek's R&D Role in Electronics

- **Invent new manufacturing technology for the next generation of:**
  - High-Density PCBs
  - High Performance PCBs
  - Package Substrates and Interposers
- **Develop and market new enabling chemistry**
- **Cooperative development with plating and material suppliers**
- **License IP and sell chemistry to PCB manufacturers**
  - Includes extensive training and technical support
  - Assistance with application and market development



Product: LMI™

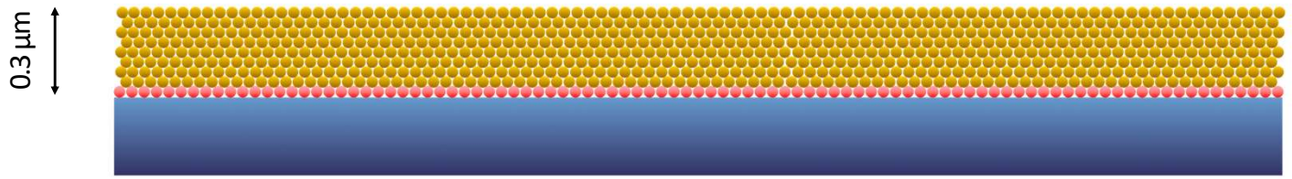
LMI™ -- Liquid Metal Ink

- Ultra thin – a few nanometers thick
- Ultra dense – fully packed atomic film
- Ultra conformal – conforms to any 3D surface
- Non-aqueous – enables low cost manufacturing
- Works for many different pure metals and alloys

LMI™ Technology Enables:
Thin, Uniform and Dense and Electroless Deposition

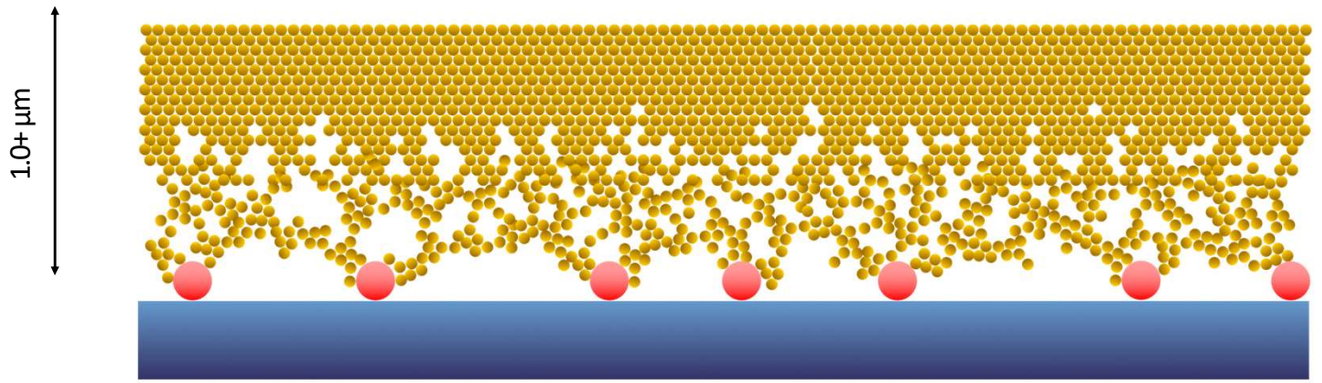
Averatek process: With ALD (Atomic Layer Deposition) palladium catalyst

Averatek LMI™ requires only 0.3 µm electroless Cu to get bulk conductivity
Uniformly spaced nano-layer of palladium produces a uniform and dense Cu layer.

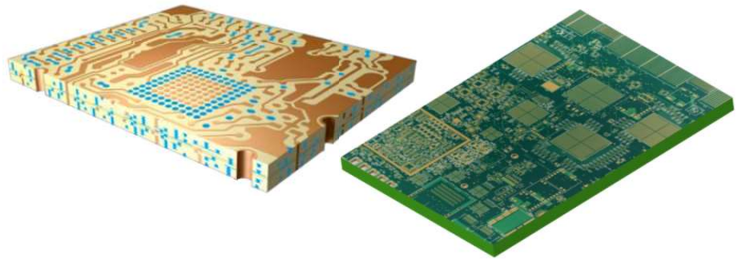
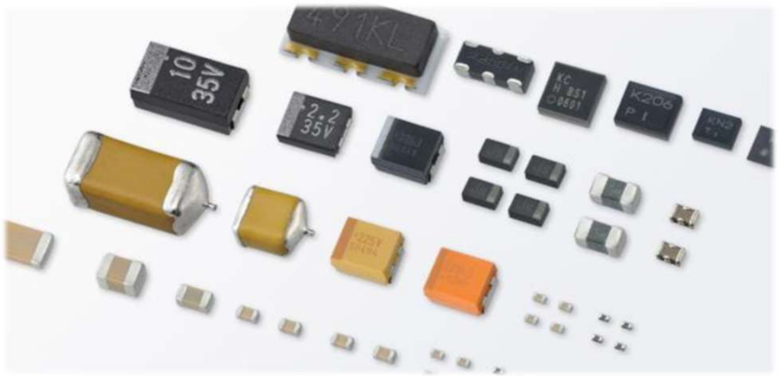


Conventional process: With colloidal or ionic palladium catalyst

Colloidal or ionic palladium requires about 1µm electroless Cu to get bulk conductivity.
The large palladium particles and spacing provides sporadic initial deposition.



Averatek Technology Dramatically Reduces Size and Cost, as well as Improving Functionality, of Key Components in Electronic Assemblies

	**Printed Circuit Boards** Dramatically shrinks size and weight / reduces cost with superior electronic connectivity.
	**Semiconductor Packaging** Eliminates the need for packaging chips and/or makes chip packages much lighter and less expensive.
	**Passive Components** Size and weight reduction permits closer and better integration of passive components within circuit boards and allows higher performance for wireless applications

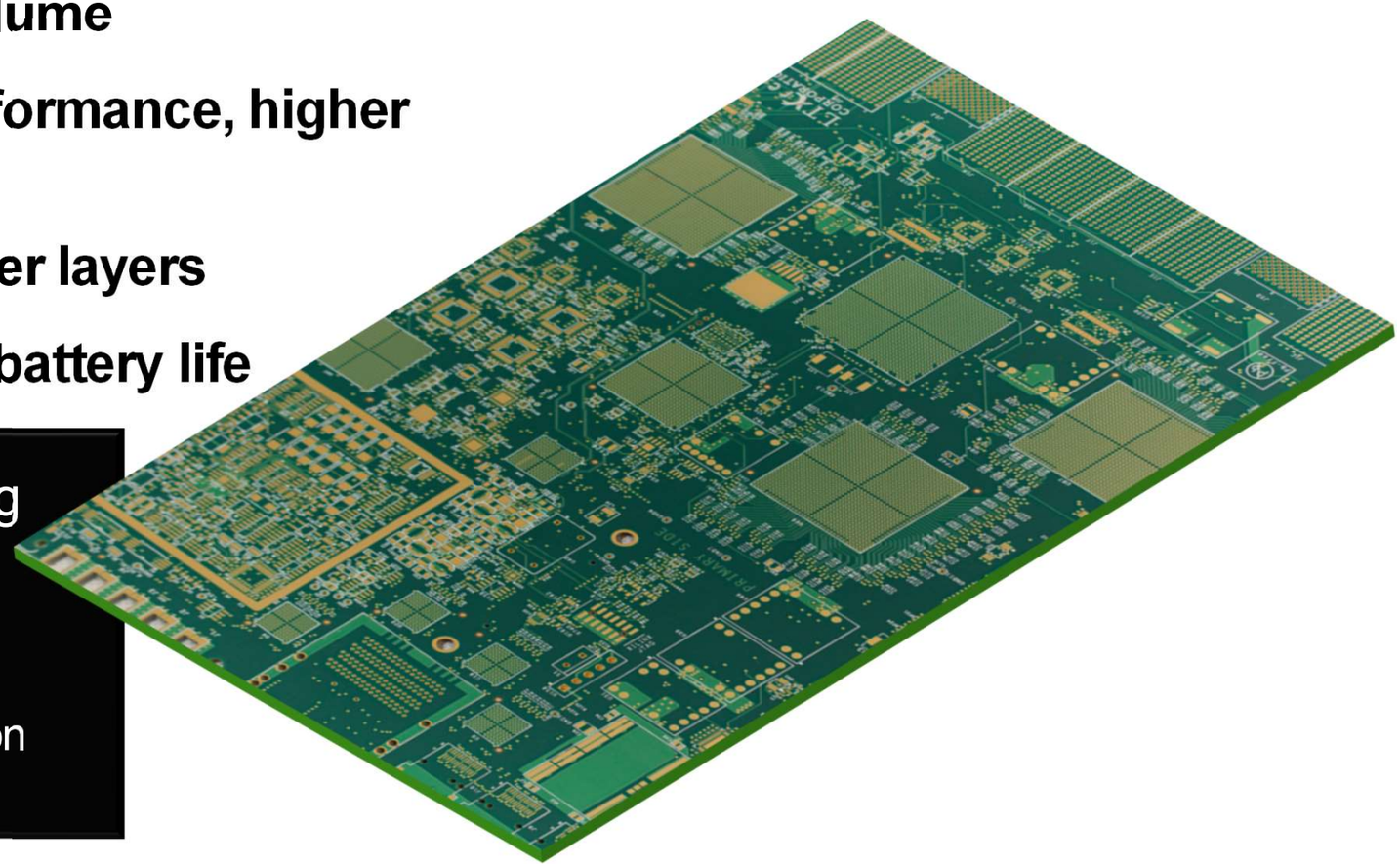
High Density PCBs

- **PCBs are one of the primary obstacles to electronics shrinking in both weight and volume**
- **Smaller often means higher performance, higher frequency operation**
- **Improved reliability through fewer layers**
- **More room for batteries, longer battery life**

Many conventional shops are lagging severely behind*

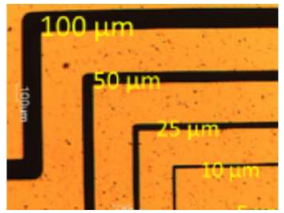
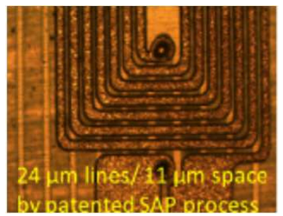
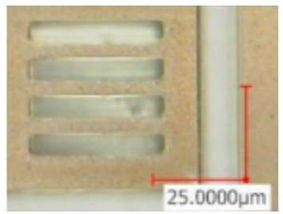
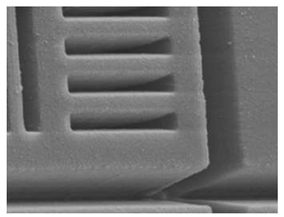
- Difficult to catch-up with competitors
- Easier to leapfrog past them with innovation

* 2018 DoD / Commerce Department 284 page analysis.



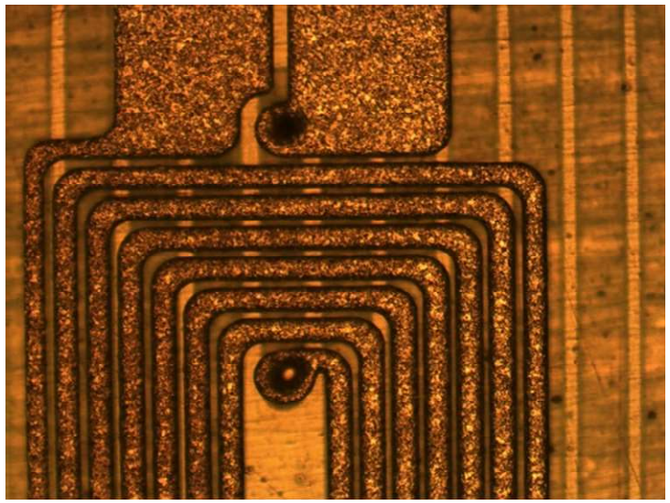
Roadmap for Averatek's Manufacturing Processes

To Maintain the Leading Edge into the Foreseeable Future

	Averatek **Full Additive** Line/Space 5/5 µm Thickness 1 µm	**Ideal for medical and some military applications.** **Current usage in next generation heart catheters.**
	Averatek **A-SAP™** Semi-Additive Process Line/Space 15/15 µm Thickness: Aspect ratio 1:1	**Licensed to commercial manufacturers.** **Designed for easy adoption at existing electronic assembly facilities.**
	Averatek **LIP-C™** Line/Space 5/5 µm Thickness 5 to 15 µm	**Ideal for very high frequency applications.** **In development with U.S. Air Force.** **Expected commercial launch in 2 years.**
	Averatek **ELCAT™** Line/Space 5/5 µm Thickness 5 to 15 µm with embedded die	**Maximum density – In development with U.S. Navy.** **Expected commercial launch in 3 years.**

Example Circuit Board Applications

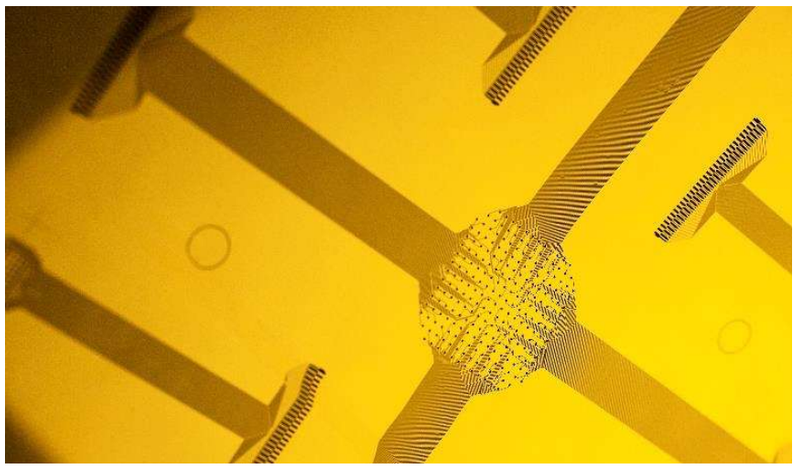
25 µm line & space
by full additive process



24 µm line/ 11 µm space
by patented A-SAP™ process

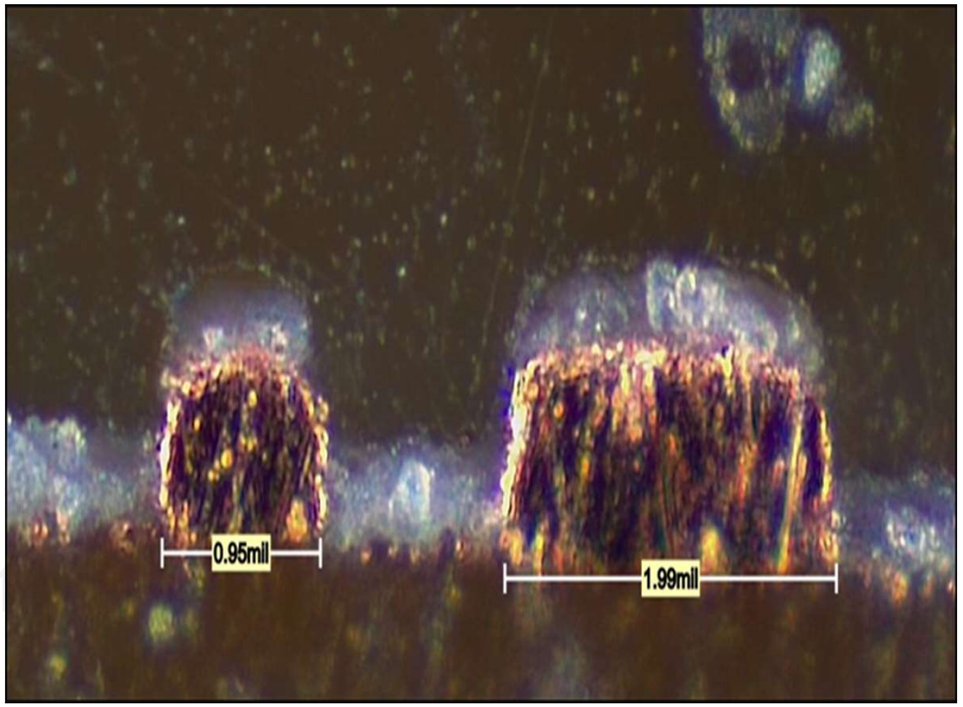
25µm gold circuit neural probe

- **Neural probes designed for brain stimulation**
- **Unique gold on polyimide without any tie layer - ideal for In Situ applications**
- **25 um leads**
- **64 leads per side**

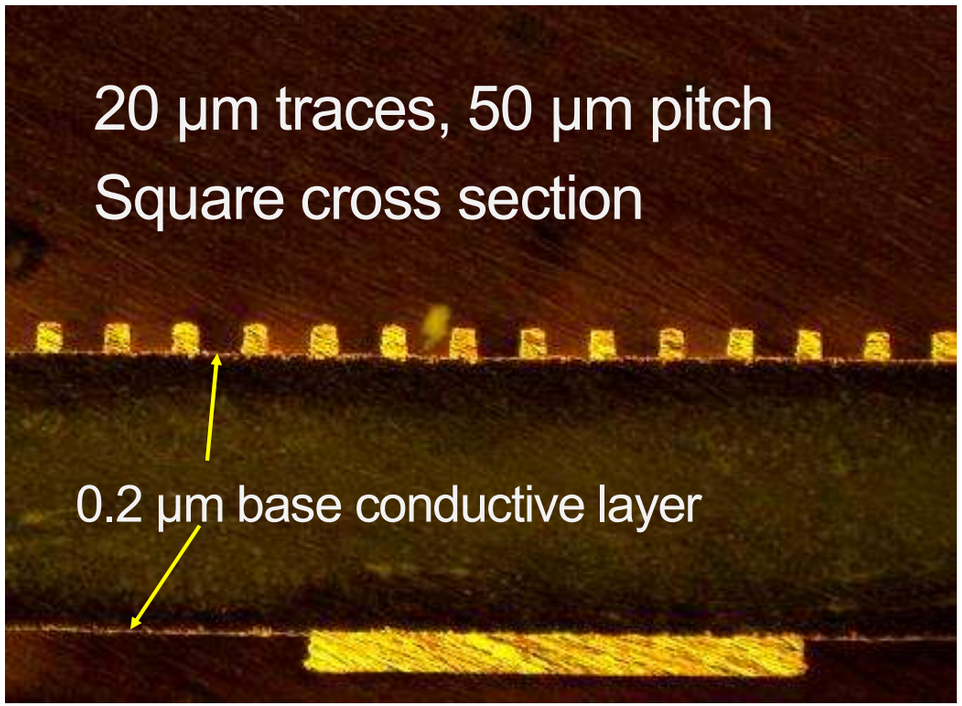


Averatek

Example of Averatek Semi-Additive Process (A-SAP™)



25 micron technology realized at Calumet Electronics. Sidewalls are straight due to ASAP



Rigid substrate cross section
Thin A-SAP™ base conductor film

Design Benefits

To Name a Few:

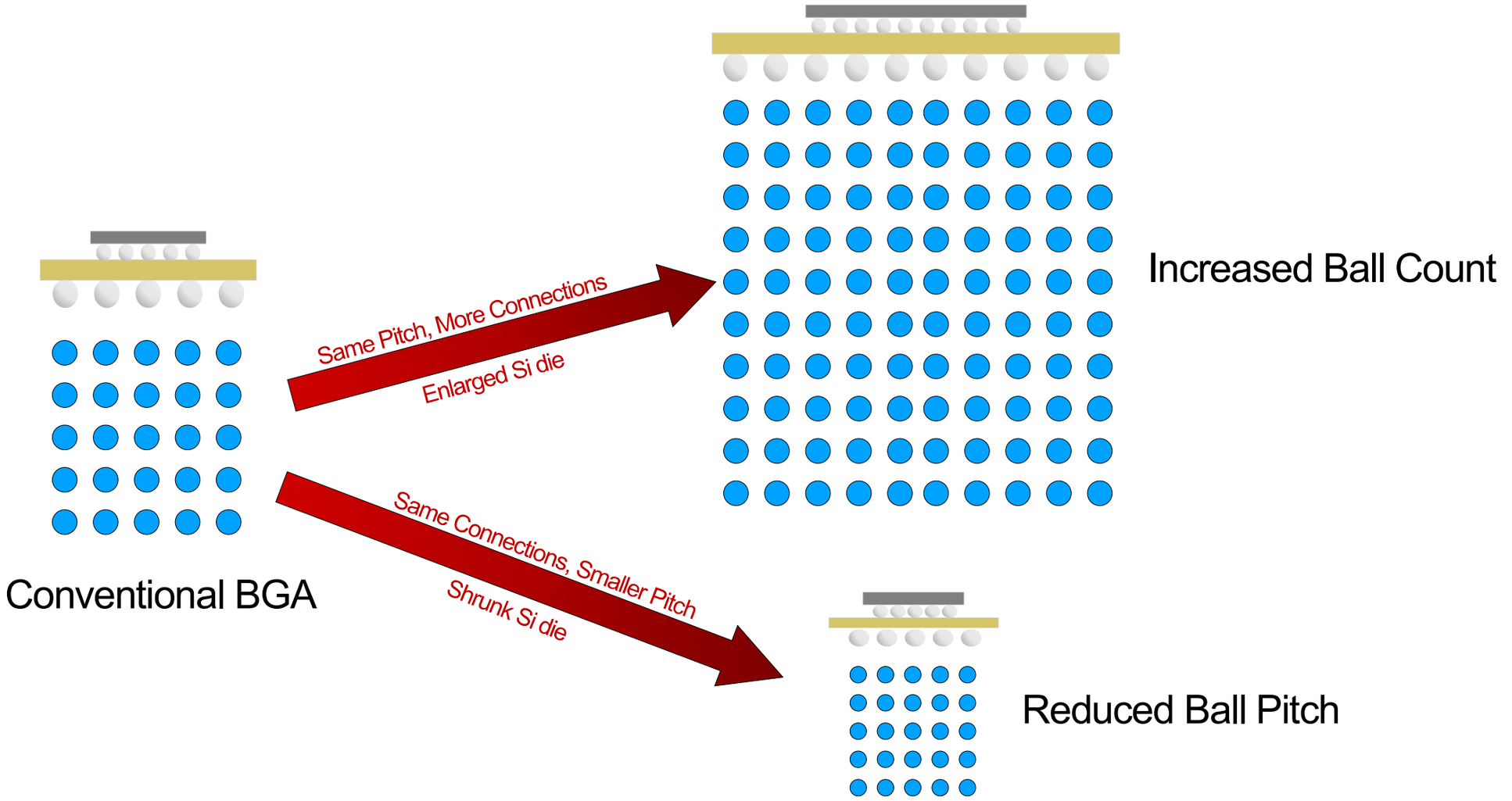
- Reduced Size and Weight (10X to 100X)
- Reduce required sequential lamination cycles
- Reduce layer count
- Reduce overall size of PCB
- Reduce use of microvias, particularly stacked
- Increase electronics in existing structure

Improved RF Performance

- Narrower transmission lines with much lower impedance available
- High quality embedded RF components
- Much smaller parasitics and interconnect loading

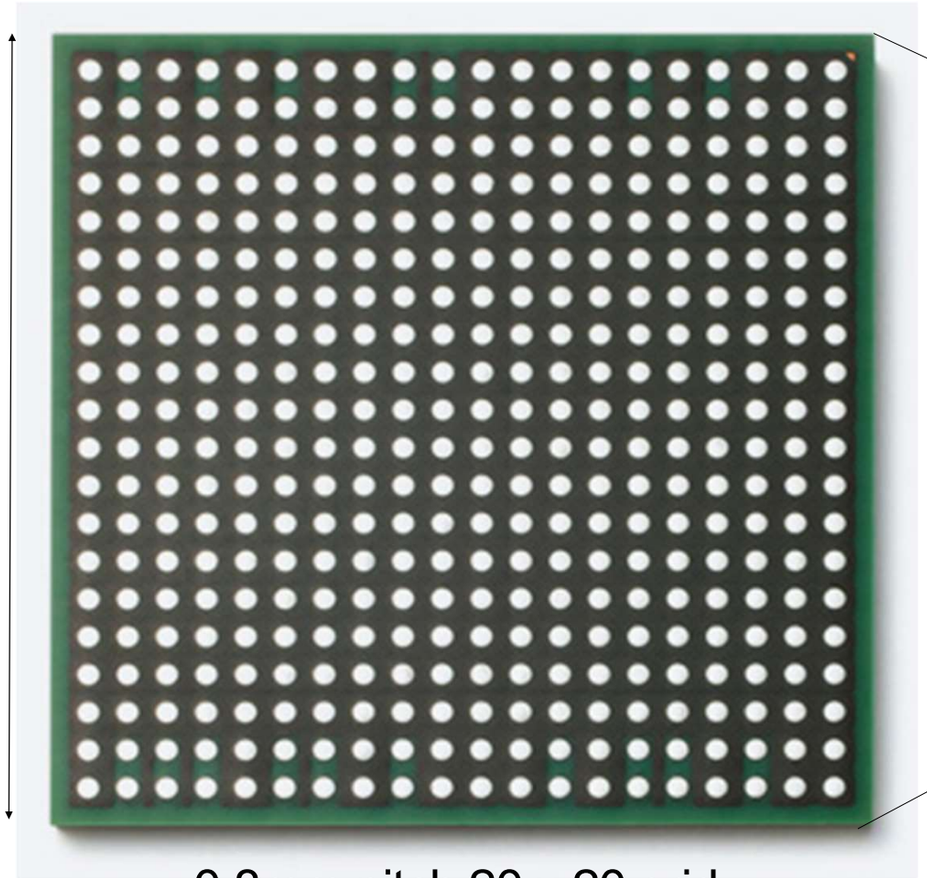
A highly collaborative approach to PCB design and fabrication is encouraged. Work with your fabricator early in the process.

Emerging BGA Designs Push Narrower Trace/Space Requirements



Averatek A-SAP™ Allows Use of Much Smaller Packages

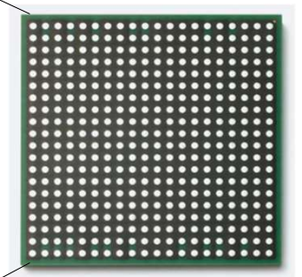
Immediate Benefit of Using A-SAP™ for Domestic Vendors



0.8mm pitch 20 x 20 grid

3 routing layers using

Standard PCB with L/S 3mil/3mil



10X Area Reduction

0.3mm pitch 20 x 20 grid

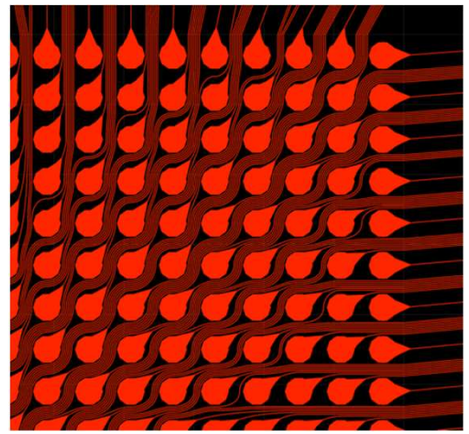
3 routing layers using

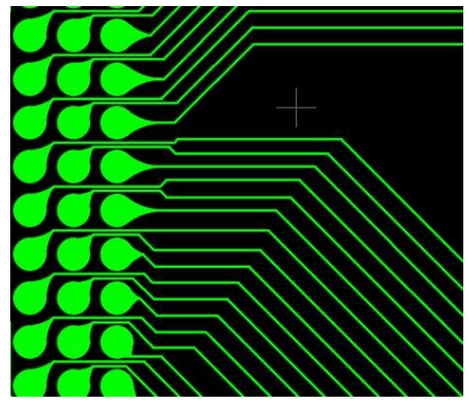
A-SAP™ PCB with L/S 1mil/1mil

Effect of Increased BGA Grid Size and Reduced Ball Pitch

Layer Count versus Minimum Feature Size

BGA* grid	Ball Pitch	Pad Size or Spacing	Routing Layers Required	# of Traces between pads	Trace & Space (Min Feature Size)
15 x 15	0.5mm	250µm	**1**	4	**27µm** (1.1mil)
	0.8mm	400µm	**1**	4	**44µm** (1.7mil)
20 x 20	0.5mm	250µm	**3**	2	**50µm** (1.9mil)
	0.5mm	250µm	**2**	3	**35µm** (1.4mil)
	0.8mm	400µm	**2**	3	**57µm** (2.2mil)
	0.8mm	400µm	**1**	6	**30µm** (1.2mil)
50 x 50	0.5mm	250µm	**6**	2	**50µm** (1.9mil)
	0.5mm	250µm	**4**	3	**35µm** (1.4mil)
	0.5mm	250µm	**3**	4	**28µm** (1.1mil)
	0.5mm	250µm	**2**	6	**19µm** (0.8mil)
	0.5mm	250µm	**1**	12	**10µm** (0.4mil)

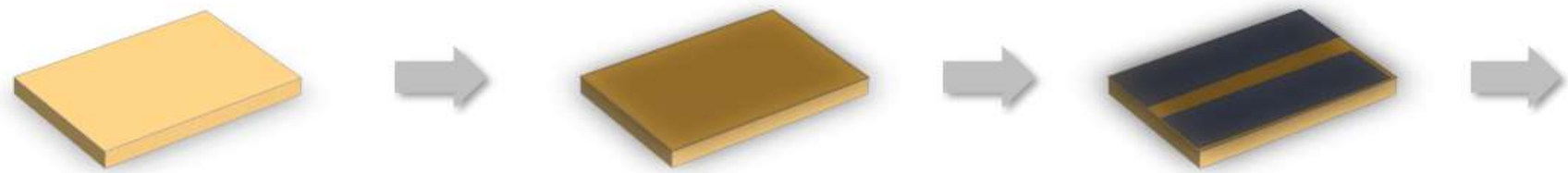




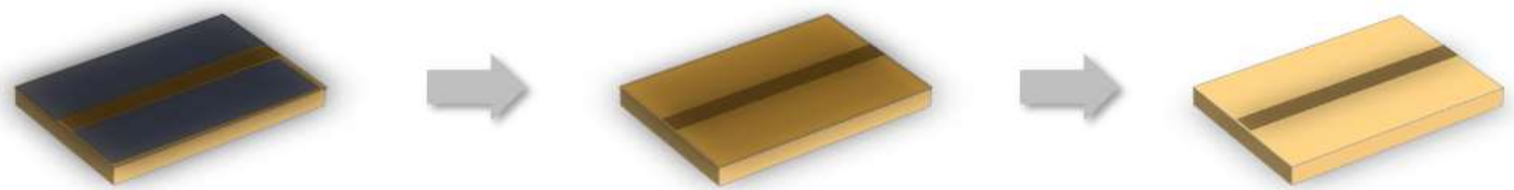
* For simplicity of analysis we assume all pads are signal pads.

Averatek Semi-Additive Process (A-SAP™)

Easily Implemented in Traditional PCB Shops



1. Bare laminate without metal and blanket coated with LMI™
2. Electroless Cu coated laminate
3. Dry film resist (DFR) imaging



4. Electrolytic Cu plating
5. Dry film resist strip
6. Flash etch

Collaboration Today

Technology is licensed to US based PCB Fabricators

Integrating with traditional PCB fabrication process

Direct DoD Engagement

Technology development for the *next-generation warfighter*

Direct OEM Engagement

Educating, engaging and continuous learning of application potential

Meet us at IPC APEX 2020

- Technical Conference Sessions
- Panel Discussion
- Community of Interest Meeting

Thank you

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