IPC-2221B APPENDIX A Version 4.0 April 2022

A.1 INTRODUCTION This appendix was developed by the IPC 1-10c Test Coupon and Artwork Generation Task Group and is included in this current document revision as a resource for the design of conformance and qualification coupons. The intent of this document is to provide an overview of the coupon designs, limitations and intended uses. However, this Appendix is not intended to provide a complete set of rules for the design of these coupons. The IPC 1-10c committee recommends that this Appendix be used in conjunction with the IPC-2221B Gerber Coupon Generator (https://www.ipc.org/ipc-standards-related-resources), which uses product board design driven user inputs and outputs Gerber files that are intended to be placed on the fabrication panel. This website also provides the latest version of this Appendix. If conflicts arise or the information provided is incomplete, the design of the coupon features should be in accordance with the associated product board design requirements. Note that etch and solder mask fabrication compensation **shall** be applied uniformly to both the coupons and product board.

Due to the general proliferation of designs that require the use of multiple complex via structures where specific design attributes such as diameter, pitch, offset and layer flooding have a direct impact on the long-term reliability of the product board, the task group recommends that the propagated B and D coupons described in A.3 and A.7.1, respectively, be designed by or reviewed by the OEM to insure the best possible representation of the product board.

It is the task group's recommendation that all other coupons be designed by the printed board fabricator in order to ensure that the correct drill sizes and feature sizes after etch compensation are used.

Solder mask layers are documented for each of the coupons; however, they are only to be used if the associated product board design requires solder mask.

Table A.1-1 provides a summary of coupon designs that are described within this appendix.

A.1 Version Changes Changes that were incorporated in this version of Appendix A to IPC-2221B are indicated in gray shading of the relevant subsection(s). Changes to a figure or table are indicated by gray shading of the figure or table header.

Table A.1-1 IPC Coupons

Section	Coupon	Description	Purpose
A.2	AB/R	General purpose AB coupon for through features	Plated hole/via evaluation, feature size and spacing, registration, thermal stress and rework simulation
A.3	Propagated B	B coupon propagated (blind, buried or filled through) via features	Via evaluation, feature size and spacing, registration, thermal stress and rework simulation
A.4	E	Moisture and insulation resistance coupon	Moisture and insulation resistance
A.5	S	Hole solderability coupon	Hole solderability
A.6	W	Surface mount solderability coupon	Surface mount solderability
A.7	D	General purpose AB daisy-chain via coupon	Plated hole/via thermal stress
A.7.1	Propagated D	Daisy-chain via coupon for propagated structures	Plated hole/via thermal stress
A.8	G	Solder mask coupon	Solder mask adhesion
A.9	H	Surface insulation resistance coupon	Surface insulation resistance

A.10	P	Peel strength coupon	Peel strength and plating adhesion
A.11	Z	Controlled impedance coupon	Controlled impedance
A.12	K	Registration (internal spacing)	Verification of internal spacing between plated holes and copper on internal layers

A.2 AB/R COUPON Coupon AB/R combines the heritage A, B and R coupon design features along with a C feature which represents the smallest via or component hole which has the smallest annular ring. In order to better represent the product board, the B1 feature contains internal lands only on layers 2 and n-1, the B2 feature contains internal lands only on internal signal layers and the B3 feature contains internal lands only on internal plane layers. The design also includes features to allow the assessment of minimum conductor and space widths from the product board. To accomplish this, the B4 lands are square and the minimum conductor for each layer is located adjacent to the B4 lands at the minimum spacing for each layer.

Even when there are no B features, the AB/R coupon can still be used, there will just not be any B sized drills. Until the coupon generator has been updated to accept designs without B features, the following is suggested to be used for the B: Land size: 1.02 [0.040] and Via size: 0.51 [0.020]. Once the coupon has been generated, the manufacturer should remove the B drills from the drill file.

The R feature provides a method to electrically assess 360° registration without the need for microsectioning. Due to the contribution of etch variation with heavier innerlayer foils use of the R features is recommended for design with foil weights of 1 oz. or less. The design parameters for coupon AB/R are shown in Table A.2-1.

Table A.2-1 AB/R Coupon Parameters, mm [in][1,3,4,5]

Feature	Description	Design Requirements
A	Largest component hole with its smallest associated D+ Round lands on all layers	Drill size **shall** be ≤ 1.07 [0.042] Land size **shall** be ≤ 1.65 [0.065]
B1	Smallest via with its smallest associated D+ Round lands on layers 2 and n-1	Land size **shall** be ≤ 1.02 [0.040] Grid size: 1.27 [0.050]
B2	Smallest via with its smallest associated D+ Round lands on signal layers	
B3	Smallest via with its smallest associated D+ Round lands on plane layers	
C	Smallest D+ with its smallest associated via or component hole Round lands on all layers	Drill size **shall** be ≤ 1.07 [0.042] Land size **shall** be ≤ 1.65 [0.065]
RA[2]	Registration based on the A feature	Anti-land calculation (minimum of): (Land diameter + 0.0127 [0.0005]) - (2 x annular ring requirement)
RB[2]	Registration based on the B feature	
RC[2]	Registration based on the C feature	
RB1[2]	Registration based on the B feature with a 0.0254 [0.001] allowance	Anti-land calculation: RB anti-land calculation + 0.0508 [0.002]
G	Common connection for “R” measurements	Maximum drill size is 0.51 [0.020] (Square) Land size is 1.02 [0.040]
L	Minimum conductor width (in line with B4 lands)	Minimum conductor for each layer
S	Minimum space width (in line with B4 lands)	Minimum space for each layer
T	Tooling hole	Drill size is 2.00 [0.0787]

Note 1. Thieving may be added to the coupon provided it is in accordance with the associated product board design.
Note 2. The “R” measurements should be used with caution for copper weights greater than 1 oz. or when positive etchback greater than 0.0127 [0.005] is present.
Note 3. For direct plane layer connections B3 and B4 pad size are 1.02 [0.040].

Note 4. B1, B2 and B3 **shall** have lands on every layer for designs using non-functional lands.
Note 5. When the smallest B land exceeds 1.02 [0.040], a modified AB/R coupon with a unique designation (e.g., AB/R-1) **shall** be used to assess the via feature by using the B land size in the A land location.

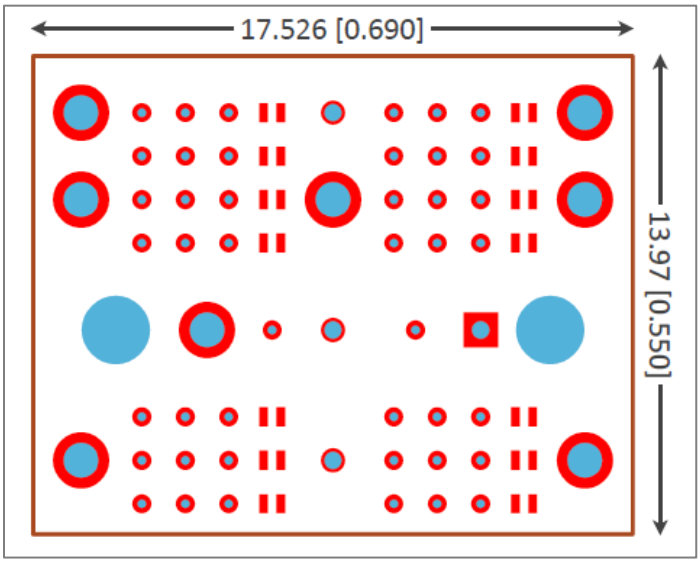


Figure A.2-1 AB/R Coupon Layout, mm [in]

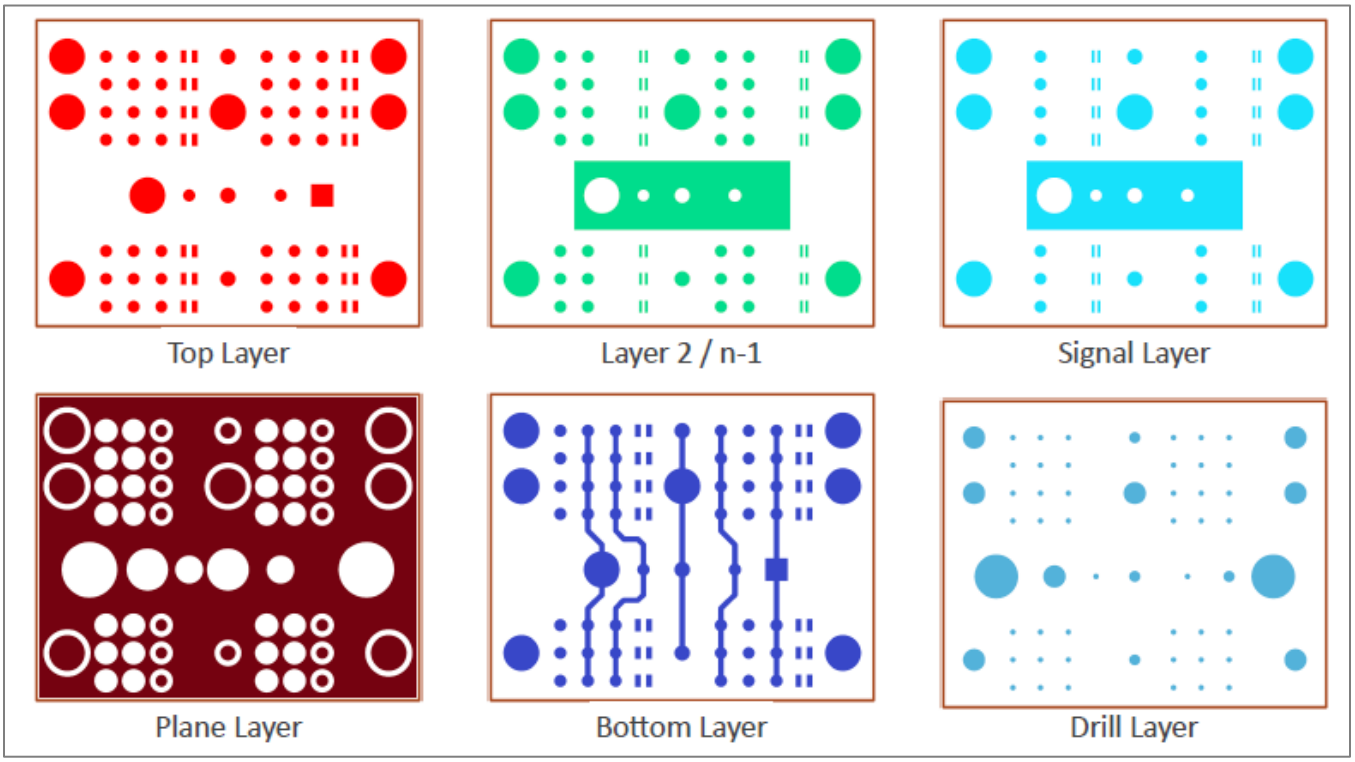


Figure A.2-2 AB/R Coupon Example Layers

A.3 Propagated B Coupon Propagated B coupons are defined by the following:

- Simple structures are composed of a single via
- Complex structures are formed by combining two or more unique vias
- Offset between vias is the distance between their centers
  Nets are formed by replicating vias or structures into a daisy-chain
  Independent vias are vias with pad-to-pad spacings > 0.006 in.
- Overlapping vias consist of two independent vias with overlapping spans (i.e., a via that spans layers 2 to 3 followed by a second via that spans layers 2 to 9, the latter of which overlaps layers 2 and 3)

Rules for propagated B coupons include the following:

- All vias from a design **shall** be included in at least one net
  Unique vias with pad-to-pad spacings of ≤ 0.006 in. **shall** be represented within a complex structure
- The pitch of a structure **shall** match the smallest associated design pitch
  Complex structures **shall** involve as many layers as possible
- The most complex structures **shall** be used
  - Smaller vias with their associated smallest land are more complex than larger vias
  - Stacked vias are more complex than staggered vias
  - Smaller offsets between vias are more complex than larger offsets
- Overlapping vias are not allowed.

Propagated B coupons are used to evaluate other board structures (blind, buried, filled, etc.) that don't meet the criteria for the AB/R coupons. Coupon B follows the same design intent as the AB/R except that it is based on the **structures** used for the propagated D coupon and does not include the R feature. As such, a maximum of two (2) via structures can exist in a B coupon, although these may represent many drilling and plating steps. (See A.7, D Coupon and A.7.1, Structures, below.)

The first via structure (left half) is referred to as Bx and the second via structure (right half) is referred to as By. Each via structure can be either; through holes (filled or not), blind (stacked or staggered), buried or some combination of blind and buried. Each via structure is then separated into lower and upper sections. The lower section for each via structure is built with the structures that match the D coupon and is intended to be used to evaluate structural integrity of the structures.

The upper section is modified so that it can be used to evaluate registration. This requires any traces used for staggered interconnects be removed and any lands on a single layer be separated by 0.005 in (edge to edge). A round 0.030 in land in the lower left of the coupon denotes the Structural Integrity section. The layer spans of each of the structures is also marked on layer 1.

When structures are stacked, both sections will be the same and only a single microsection is needed. But when staggered structures exist, two microsections need to be evaluated, one from each, upper and lower, of the sections.

The grid is defined as a function of the specified grid from the D coupon. If it is 0.025 in or less, then the X grid is 0.0375 in and the Y grid is 0.025 in. If the D coupon grid is greater than 0.025 in, then the X and Y grids are 0.075 in. The exact X axis positioning of the features in the coupon will vary depending on the pitch. The Y axis (microsection planes) are fixed.

When the grid and feature sizes are small enough (e.g., single or stacked microvias), the design provides seven holes in each of the three microsection planes, each offset in alignment by 0.00846 mm [0.00033 in] to improve the probability of meeting the 10% via diameter requirement during microsectioning.

When spacing allows, additional holes are placed within the arrays to improve coupon copper density, to improve the representability of the coupon from a plating perspective. These holes are located between the microsection planes and are not intended to be evaluated. With the smaller (microvias) pitch, there are an additional two rows of vias between the primary microsection planes. With the larger pitch, an additional set of vias is placed in the center of the area between the holes to be evaluated.

Propagated B coupons are required for each via structure. If multiple vias are included in a via structure, individual B coupons are not needed for each individual via, since they are included in the structure. All drilling and plating operations required by the design shall be represented.

The design parameters for coupon B are shown in Table A.3-1. An example of a B coupon is shown in Figure A.3-1, which depicts stacked and staggered microvia structures.

Table A.3-1 Propagated B Coupon Parameters, mm [in]

Feature	Description	Design Requirements
BX	Smallest via of type "X" with its smallest associated D+ Round lands on representative layers[2]	Drill size **shall** be < 1.02 [0.040] Land size **shall** be ≤ 1.65 [0.065] Grid size: X and Y: 1.91 [0.075] or Grid size X: 0.95 [0.0375] and Y: 0.63 [0.025] Y offset: 0.00846 [0.00033] (Depending on structure)
BY	Smallest via of type "Y" with its smallest associated D+ Round lands on representative layers[2]	
T	Tooling hole	Drill size is 2.00 [0.0787]

Note 1. Internal or external thieving may be added to the coupon provided it is in accordance with the associated product board design.
Note 2. BX and BY have lands on every layer for designs using non-functional lands in the registration section.

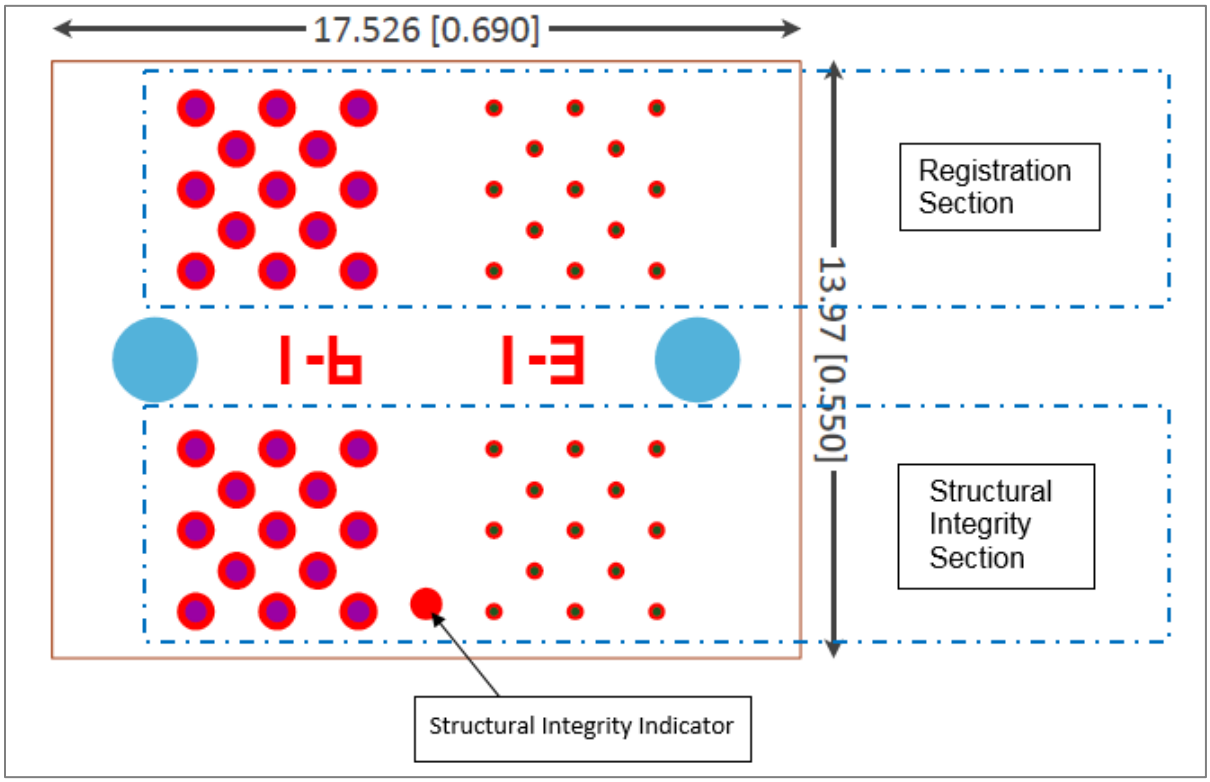


Figure A.3-1 Propagated B Coupon Layout

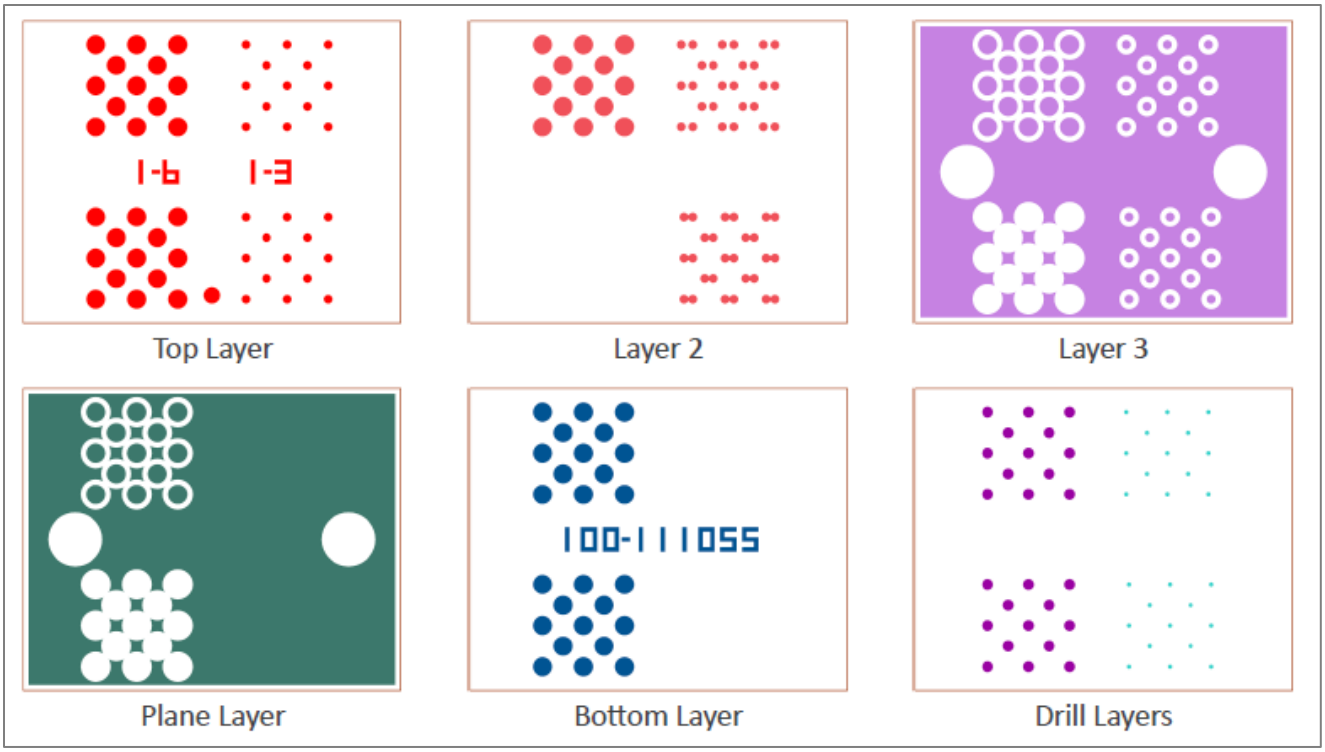


Figure A.3-2 Propagated B Coupon Example Layers

A.4 E COUPON Coupon E is used to evaluate moisture and insulation resistance of laminated base materials. The coupon is designed to test a maximum of ten layers. For designs with more than 10 layers additional coupons are required and each shall contain the last layer of the preceding coupon (e.g., L1 - 10, L10 - 19, L19 - 28, etc.). The design parameters for coupon E are shown in Table A.4-1.

Table A.4-1 E Coupon Parameters, mm [in]

Feature	Description	Design Requirements
1 - 10	Plated-through test points	Recommended drill size: 1.02 [0.040] Recommended land size: 1.52 [0.060] Grid: 2.54 [0.100]
Electrodes	Parallel electrodes	Width: 0.635 [0.025] Length: 25.40 [1.000] Gap width: 0.635 [0.025] Plane clearance: 0.635 [0.025]

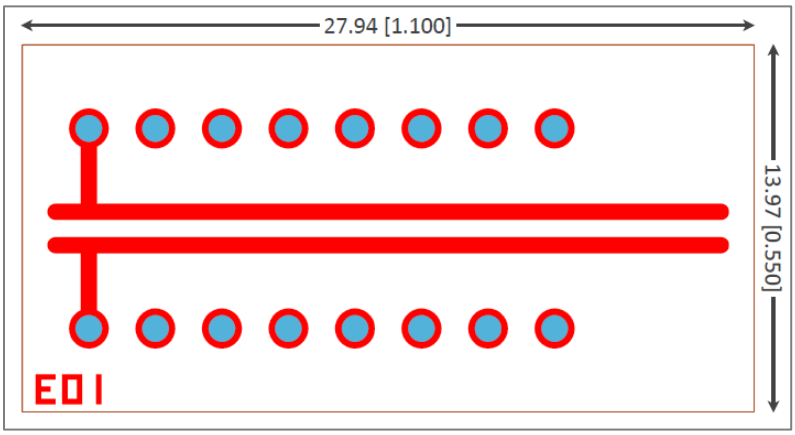


Figure A.4-1 E Coupon Layout, mm [in]

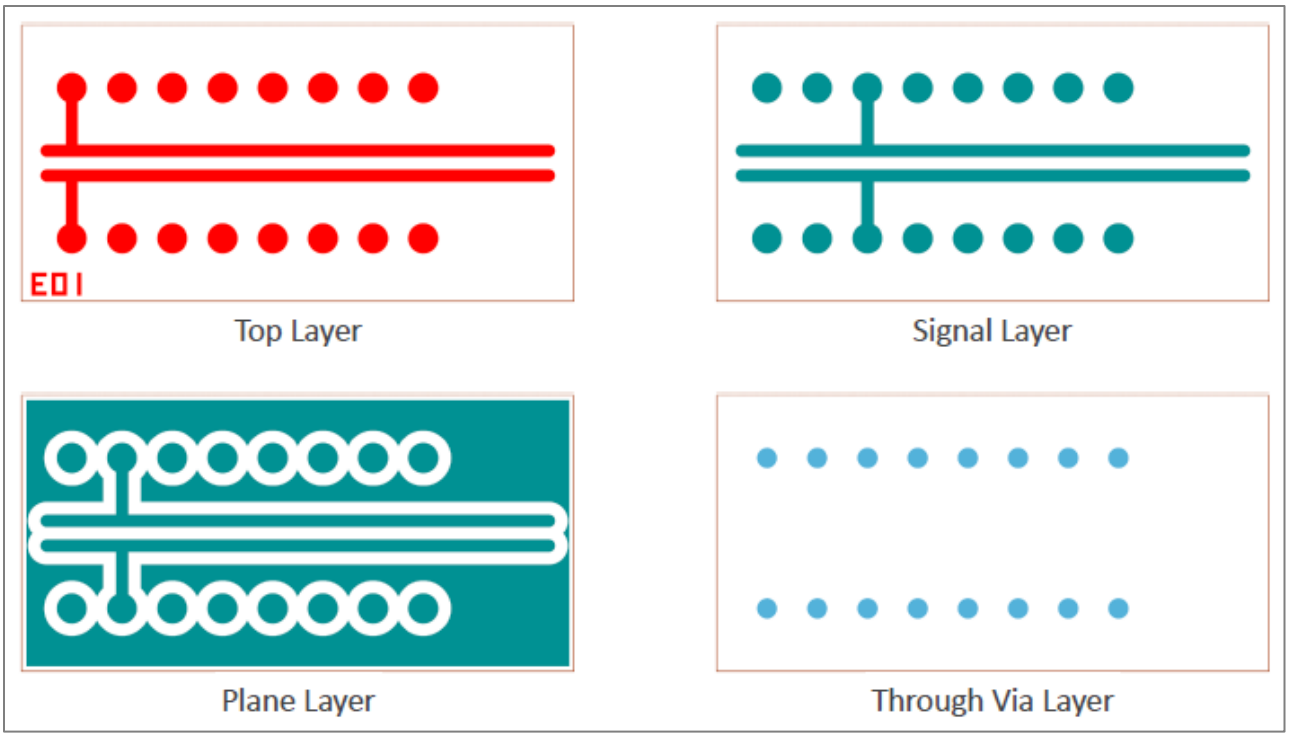


Figure A.4-2 E Coupon Example Layers

Note that the patterns above are shown with all lands present. For designs with non-functional (NF) lands removed, the NF lands should be removed on layers where the design has NF lands removed.

A.5 S COUPON Coupon S is used to evaluate through hole solderability. Representative copper patterns may be placed on internal layers, however, no innerlayer lands are to be included in the design coupon. The design parameters for coupon S are shown in Table A.5-1.

Table A.5-1 S Coupon Parameters, mm [in]

Feature	Description	Design Requirements
S	Plated-through holes (32 each)	Drill size: 0.81 [0.032] Recommended land size: 1.52 [0.060] Grid: Staggered (see Figure A.5-1)

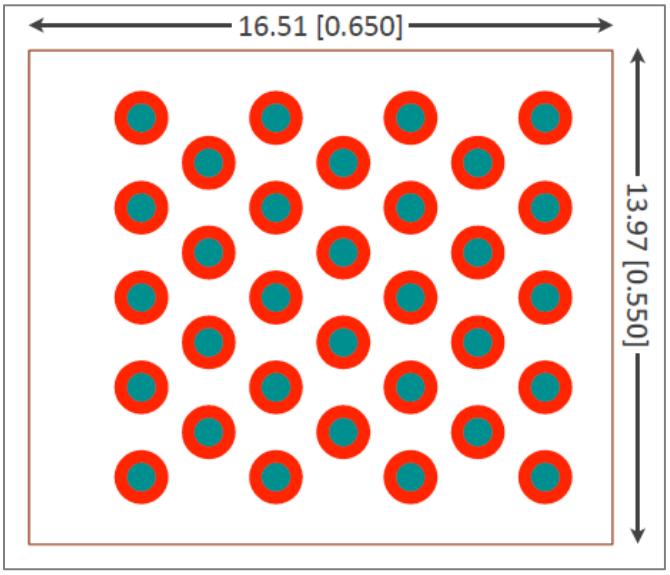


Figure A.5-1 S Coupon Layout, mm [in]

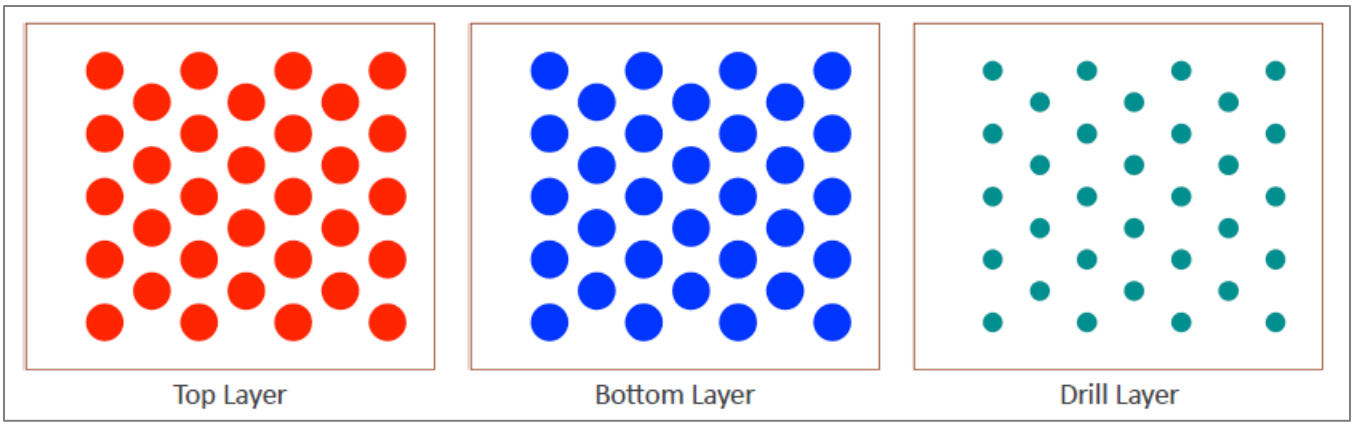


Figure A.5-2 S Coupon Example Layers

A.6 W COUPON Coupon W is a double-sided pattern used to evaluate surface mount land solderability. By intent, no inner layers patterns are included and no solder mask is to be applied to this coupon. Manufacturers should add copper to inner layers as necessary to allow the coupon thickness to match that of the design. The artwork pattern extends outside the rout line by intent to purposely cut through the pattern to facilitate wetting balance testing. The design parameters for coupon W are shown in Table A.6-1.

Table A.6-1 W Coupon Parameters, mm [in]

Feature	Description	Design Requirements
1	Round lands (12 each)	Land size: 1.52 [0.060] Optional Drill Size: 1.15 [0.0453] Pitch: 1.91 [0.075] No solder mask on this coupon
2	Rectangular surface mount lands (12 each)	Land size: 10.16 x 1.52 [0.400 x 0.060] 2 clipped to dimension shown (.64 [0.025] overhang) Pitch: 1.91 [0.075] No solder mask on this coupon
3	Square surface mount lands (4 each)	Land size: 1.52 x 1.52 [0.060 x 0.060] Pitch: 1.91 [0.075]] No solder mask on this coupon
4	Alignment features for solder dip	Land size: 0.635 x 0.254 [0.025 x 0.010] Pitch: 0.508 [0.020] No solder mask on this coupon

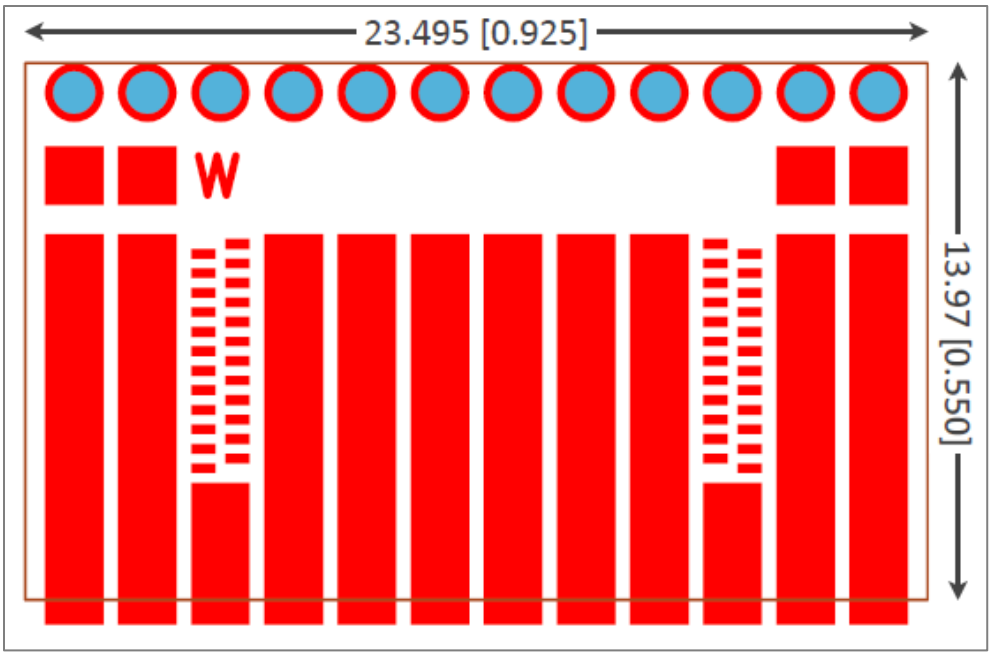


Figure A.6-1 W Coupon Layout, mm [in]

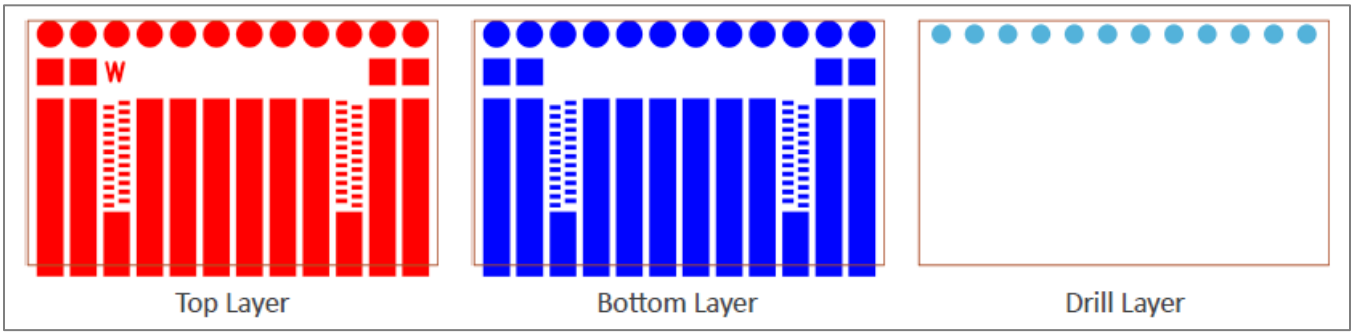


Figure A.6-2 W Coupon Example Layers

A.7 D COUPON Coupon D is used to evaluate plated hole and via reliability by thermal stress. The coupon is designed to have a sufficient number of plated holes or vias in a chain to obtain a precise resistance measurement. D coupons contain two (2) nets representing component holes or via structures.

D coupons may be created with A and B features or with propagated (blind vias, buried vias, or filled through holes) structures. The propagated structures used in D coupon nets are intended to contain the most complex **structures** used in the board design. See the definitions and rules for propagated structures below in A.7.1.

D coupon nets may represent a single hole size or via structure (e.g., A or B features) or may contain many drilling and plating steps representing multiple vias (e.g., a structure with vias from 1-2, 2-3, 3-14, 14-15, and 15-16).

For designs with less than 2 features that meet the design requirements for A or B, a propagated structure may be used for one of the nets. For example, in a design with both component holes (A feature) and filled vias (or other propagated structures), the A feature could be used in Net1 and one of the propagated structures could be used in Net2. In general, Net1 and Net 2 may be either both propagated, both unpropagated, or one of each.

The daisy chain patterns that are used to connect the vias are placed on Layers 2 and n-1 for unfilled through holes (A and B features). They are placed on the outermost layers for propagated structures. The interconnecting conductors to the connector mounting locations are located on the lowest numbered layer where daisy chain circuits exist.

The design parameters for coupon D are shown in Table A.7-1. Independent grids are used for each net and vary based on the pitch and feature sizes. When the nets have no layers in common, the D coupon may be

constructed with each net utilizing the entire coupon width (extended area). Using the extended area is preferred to increase the via sample size to better represent the number of vias on the manufacturing panel.

Table A.7-1 D Coupon Parameters, mm [in]

Feature	Description	Design Requirements
A	Largest component hole with its smallest associated D+ Round lands on layers 2 and n-1	Drill size **shall** be ≤ 1.07 [0.042] Land size **shall** be ≤ 1.65 [0.065] Maximum grid size: 1.91 [0.075] Interconnect conductors: Layer design minimum not to exceed 0.20 [0.008] Interconnect sequence: Layer 2 to n-1
B	Smallest unfilled via or component hole with its smallest associated D+ Round lands on layers 2 and n-1	Drill size **shall** be ≤ 1.02 [0.040] Land size **shall** be ≤ 1.65 [0.065] Maximum grid size: 1.91 [0.075] Interconnect conductors: Layer design minimum not to exceed 0.20 [0.008] Interconnect sequence: Layer 2 to n-1
Propagated Structures Net 1 & Net 2	Smallest via used for each portion of the intended structure, with its smallest associated land. Round lands on all start and stop layers for all drills in the structure.	Drill size **shall** be ≤ 1.07 [0.042] Land size **shall** be ≤ 1.65 [0.065] Grid: Variable (≤ 1.91 [0.075]) Interconnect conductors: Layer design minimum not to exceed 0.20 [0.008] Interconnect sequence: Layers at the extremes of the structure
Connector	VH: Four-wire resistance high voltage input IH: Four-wire resistance current source VL: Four-wire resistance low voltage input IL: Four-wire resistance current sink	Finished hole size: 1.02 ± 0.076 [0.040 ± 0.003] Land size: 1.91 [0.075] Grid size: 2.54 [0.100] Interconnect conductors: on the lowest layer number where the daisy chain conductors exist

Note 1. Each of the chains **shall** contain only one unique via structure.
Note 2. When there is only a single component hole size and no unfilled vias, the B feature in this coupon may be a propagated structure.

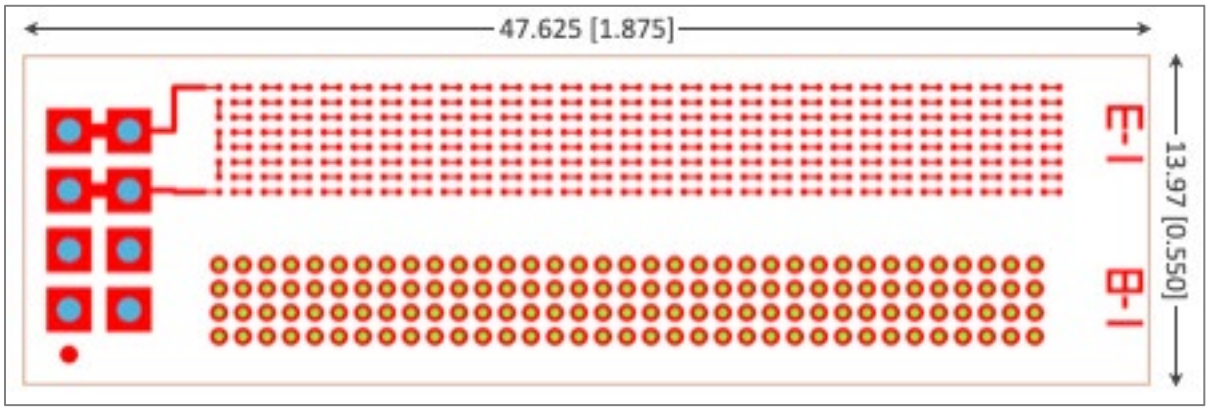


Figure A.7-1 D Coupon Layout with A and Propagated Features, mm [in]

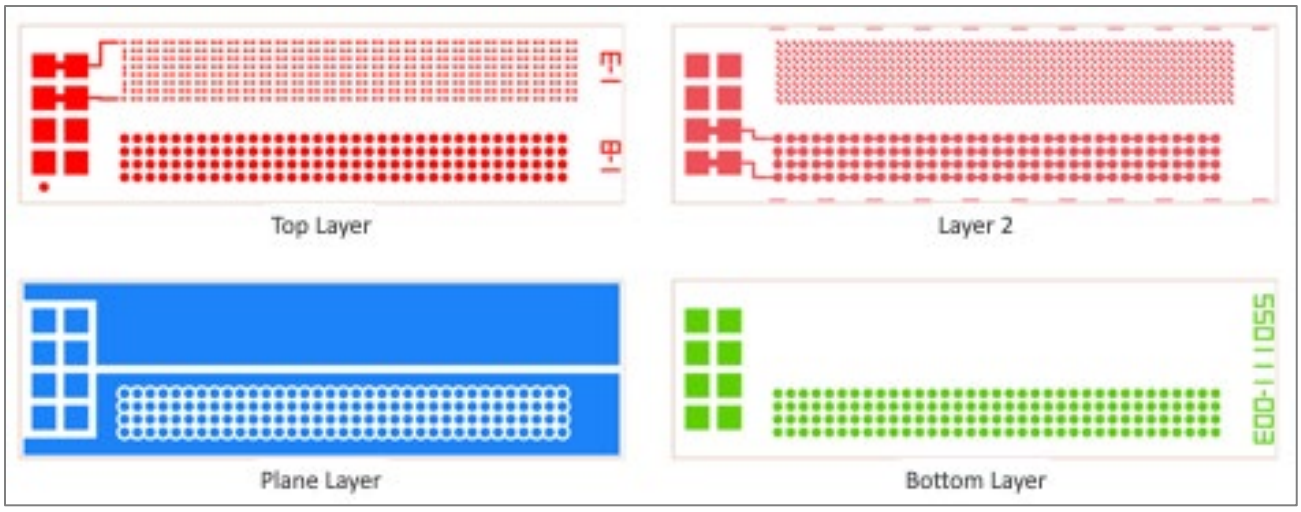


Figure A.7-2 D Coupon Example Layers

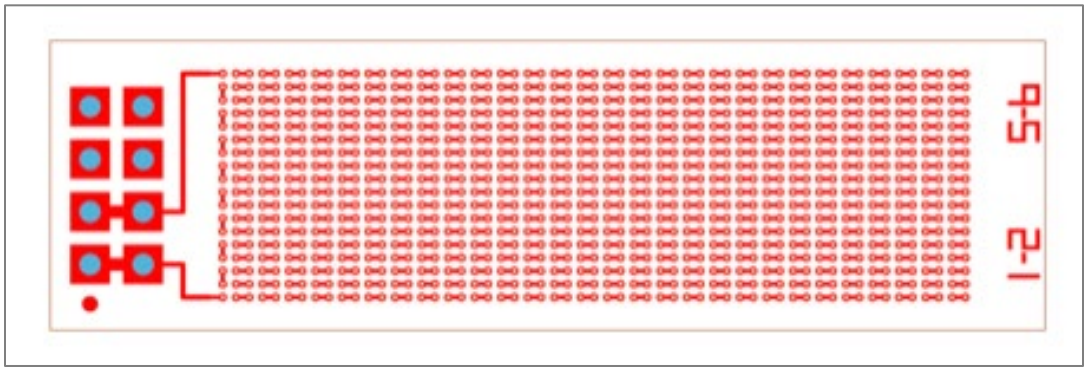


Figure A.7-3 D Coupon Layout with extended area

A.7.1 Structures Any individual drilling/plating sequence was previously considered to be a structure. In many of today's designs, a single net may utilize many different, closely spaced propagated vias. To address this, structures are now defined to include holes drilled and plated at different times when they are closely spaced and used together in the design. Vias **shall** have a single intermediate layer in common in order to be combined together to form a structure. Figure A.7-4 illustrates several examples of via structures.

The following definitions are associated with propagated structures:

- Simple structures are composed of a single via
- Complex structures are formed by combining two or more unique vias
- Offset between vias is the distance between their centers
  Nets are formed by replicating vias or structures into a daisy-chain
  Independent vias are vias with pad-to-pad spacings > 0.006 in.
- Overlapping vias consist of two independent vias with overlapping spans (i.e., a via that spans layers 2 to 3 followed by a second via that spans layers 2 to 9, the latter of which overlaps layers 2 and 3).

Rules for propagated D coupons include the following:

- All vias from a design **shall** be included in at least one net
  Unique vias with pad-to-pad spacings of ≤ 0.006 in. **shall** be represented within a complex structure
- The pitch of a structure **shall** match the smallest associated design pitch
  Complex structures **shall** involve as many layers as possible
- The most complex structures **shall** be used
  - Smaller vias with their associated smallest land are more complex than larger vias
  - Stacked vias are more complex than staggered vias
  - Smaller offsets between vias are more complex than larger offsets
- Overlapping vias are not allowed.

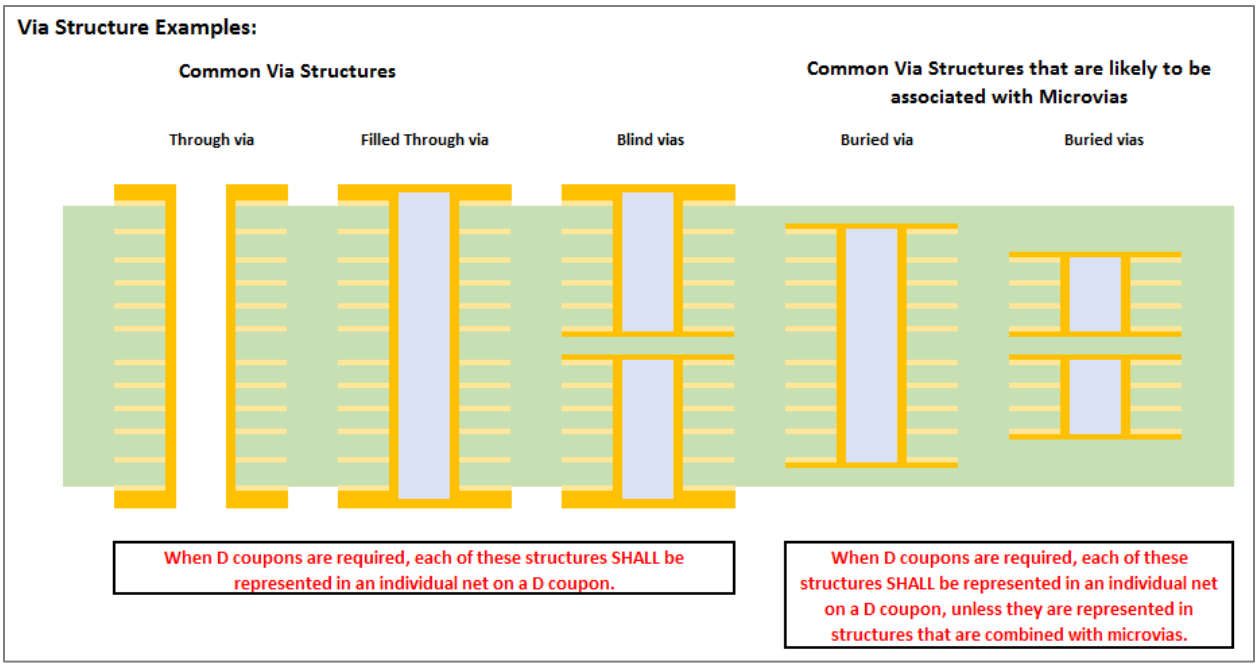


Figure A.7-4 D Common Via Structures

Figures A.7-5 through A.7-7 illustrate structures in several example designs and identify the structures to be represented when testing the design.

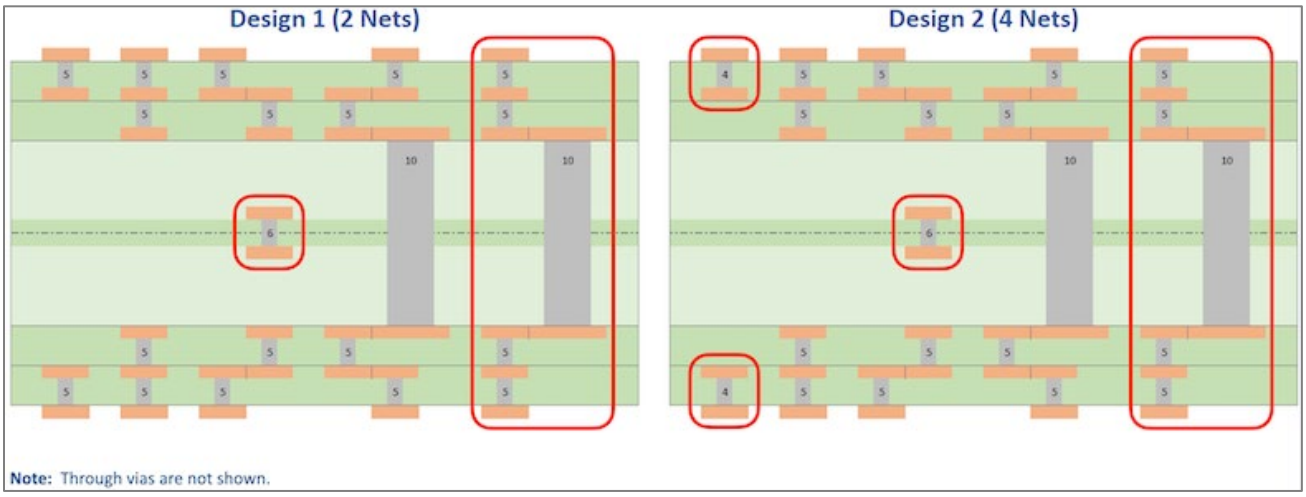


Figure A.7-5 Nets for D Coupon Testing

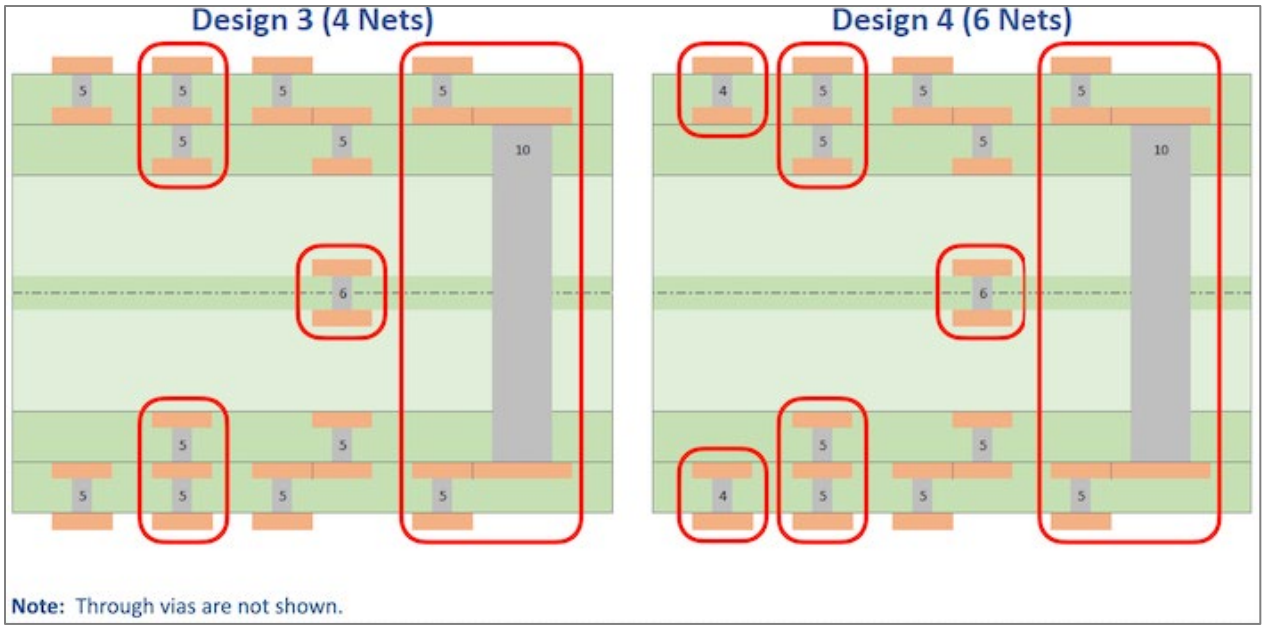


Figure A.7-6 Nets for D Coupon Testing

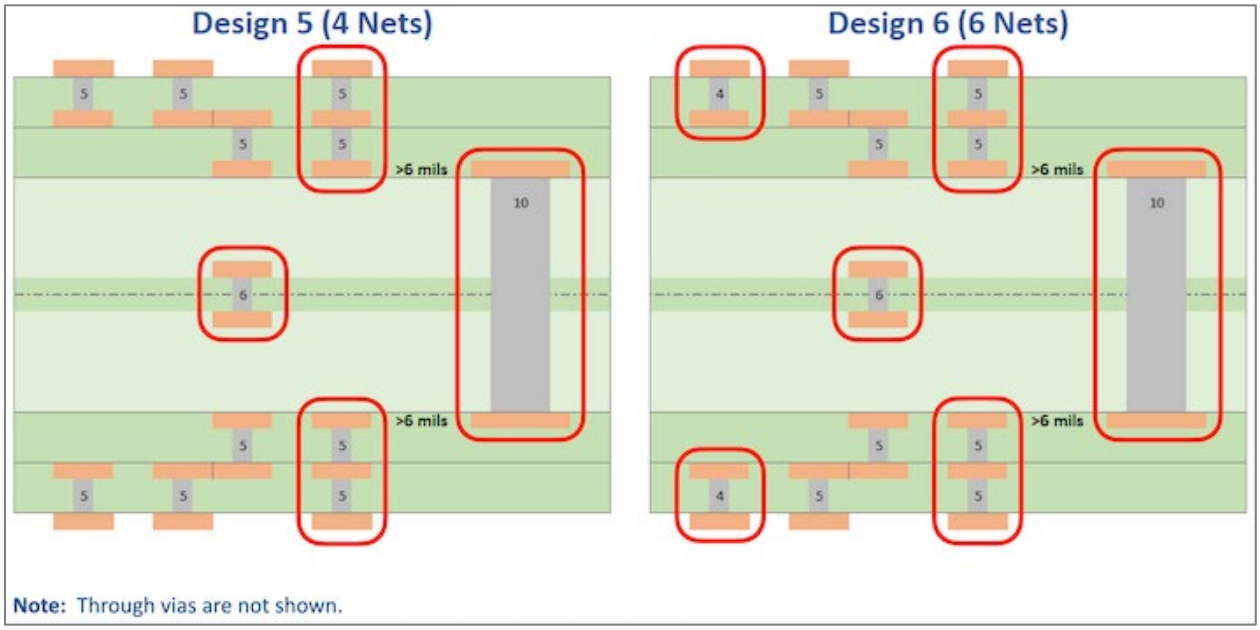


Figure A.7-7 Nets for D Coupon Testing

A.8 G COUPON Coupon G is used to evaluate solder mask adhesion and is divided into three regions 1) solder mask over copper or surface finish, 2) solder mask over laminate and 3) minimum solder mask web and minimum interconnect conductor width. The surface finish shall represent the product board design and the minimum web spacing and minimum conductor are per the product board. The design parameters for coupon G are shown in Table A.8-1.

Table A.8-1 G Coupon Parameters, mm [in]

Feature	Description	Design Requirements
1	Rectangular lands	Grid size: 1.27 [0.050] Solder mask anti-land calculation: 1.27 [0.050] - minimum solder mask web Land calculation: Solder mask anti-land - (2 x minimum solder mask clip back)
2	Round lands	

C	Minimum conductor	Minimum interconnect conductor associated with the solder mask web features
SMOC	Solder mask over copper or surface finish	Solder mask anti-land size: 0.61 [0.024] Grid size: 0.64 [0.025]
SMOL	Solder mask over laminate	Solder mask anti-land size: 0.61 [0.024] Grid size: 0.64 [0.025]

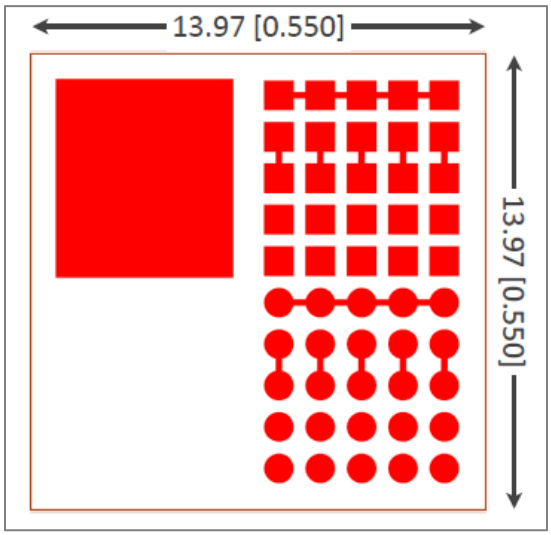


Figure A.8-1 G Coupon Layout, mm [in]

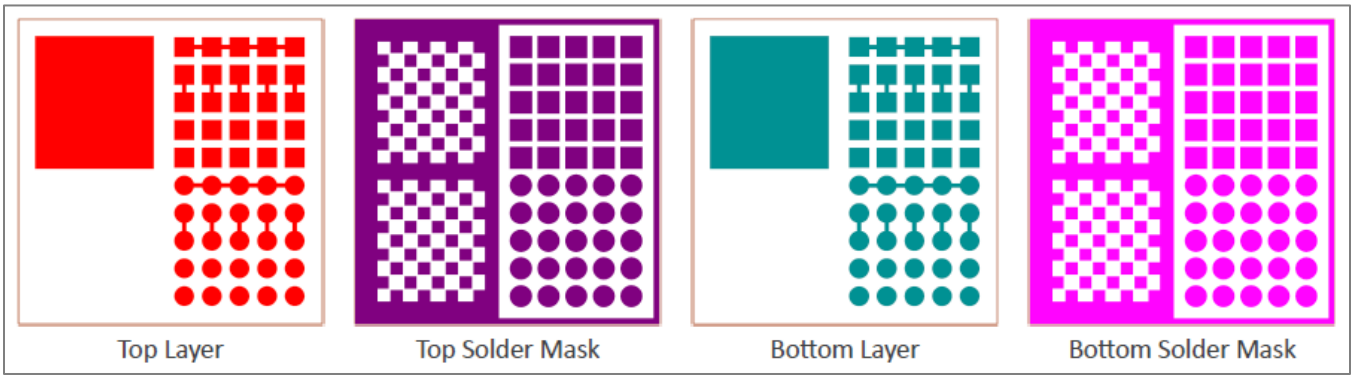


Figure A.8-2 G Coupon Example Layers

A.9 H COUPON Coupon H is used to quantify the effects of process and/or handling residues on surface insulation resistance. The coupon consists of an interstitial comb pattern per panel side. Representative copper patterns may be placed on internal layers. While a solder mask image is documented, the pertinent performance specification may preclude the use of solder mask on the coupon. The design parameters for coupon H are shown in Table A.9-1.

Table A.9-1 H Coupon Parameters, mm [in]

Feature	Description	Design Requirements
1	Plated-through test points	Recommended drill size: 1.02 [0.040] Recommended land size: 1.52 [0.060]
Electrodes	Parallel electrodes	Width: 0.40 [0.016] Pitch: 0.60 [0.024]

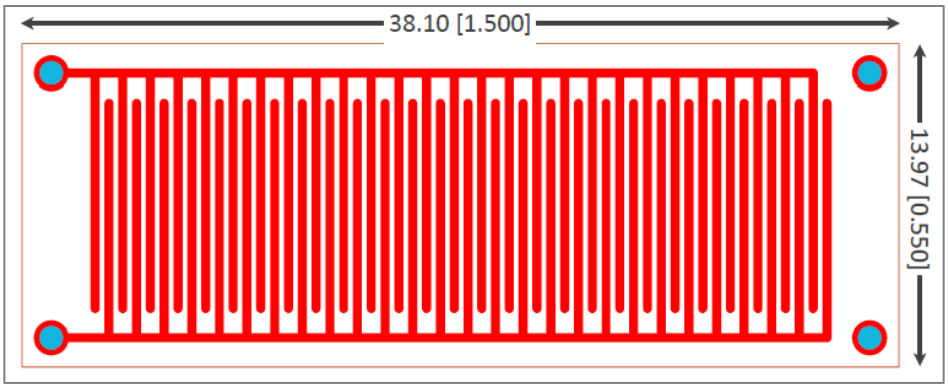


Figure A.9-1 H Coupon Layout, mm [in]

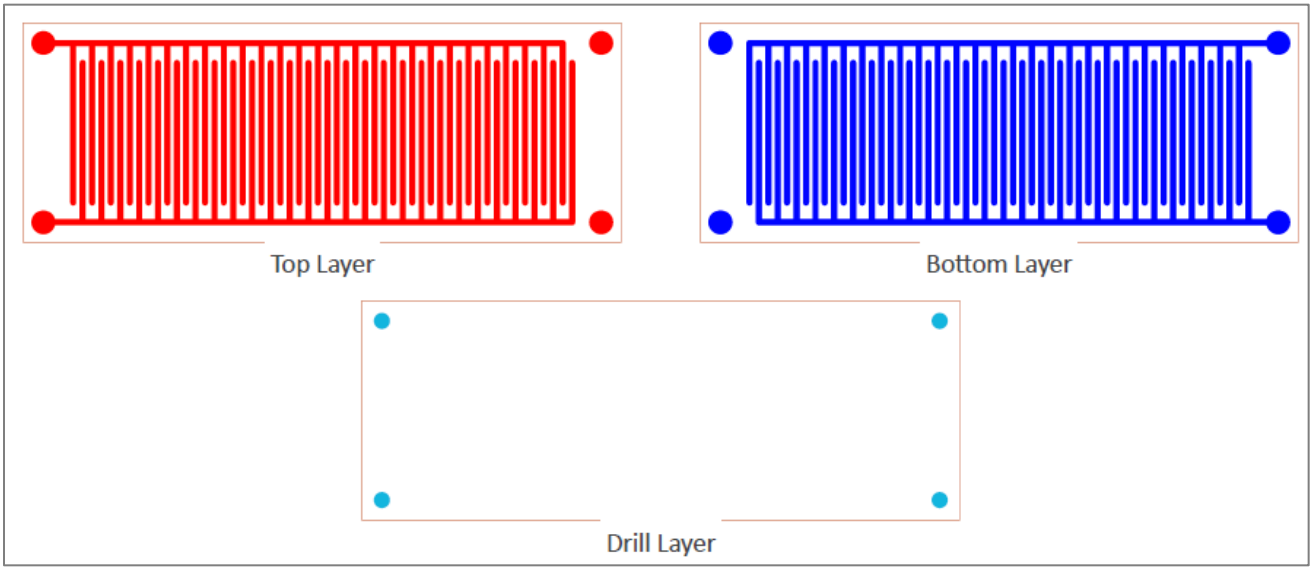


Figure A.9-2 H Coupon Example Layers

A.10 P COUPON Coupon P is used to evaluate the peel strength of metallic foils laminated to the outer layers of a printed board during the foil lamination process and to evaluate plating adhesion. The coupon consists of a conductor pair per panel side that provides a minimum test length of 25.40 [1.00]. Representative copper patterns may be placed on internal layers. The design parameters for coupon P are shown in Table A.10-1.

Table A.10-1 P Coupon Parameters, mm [in]

Feature	Description	Design Requirements
Peel	Peel conductor	Width: 3.18 [0.125] Minimum length: 25.4 [1.000]
Tab	Peel tab	Width: 5.72 [0.225] Length: 6.99 [0.275]

Note 1. Performance specifications preclude the use of surface finish on the coupon.

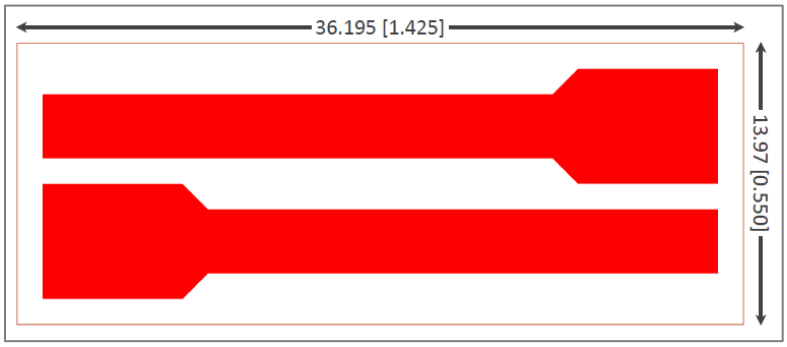


Figure A.10-1 P Coupon Layout, mm [in]

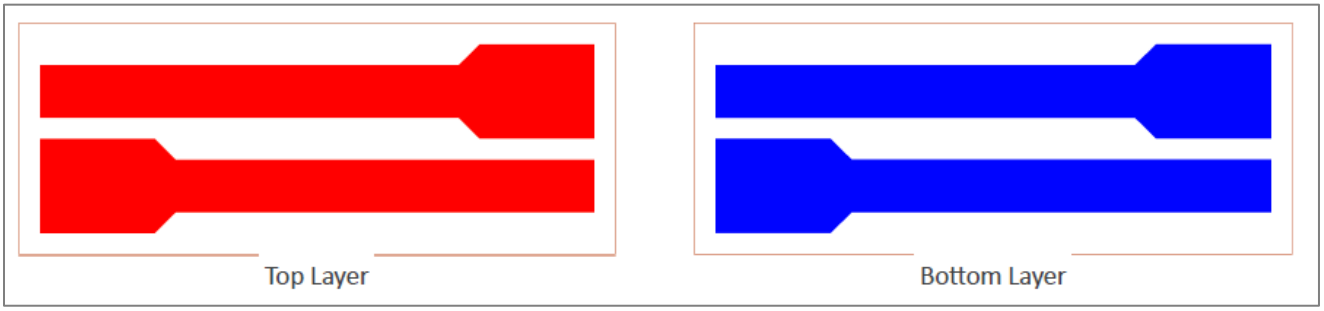
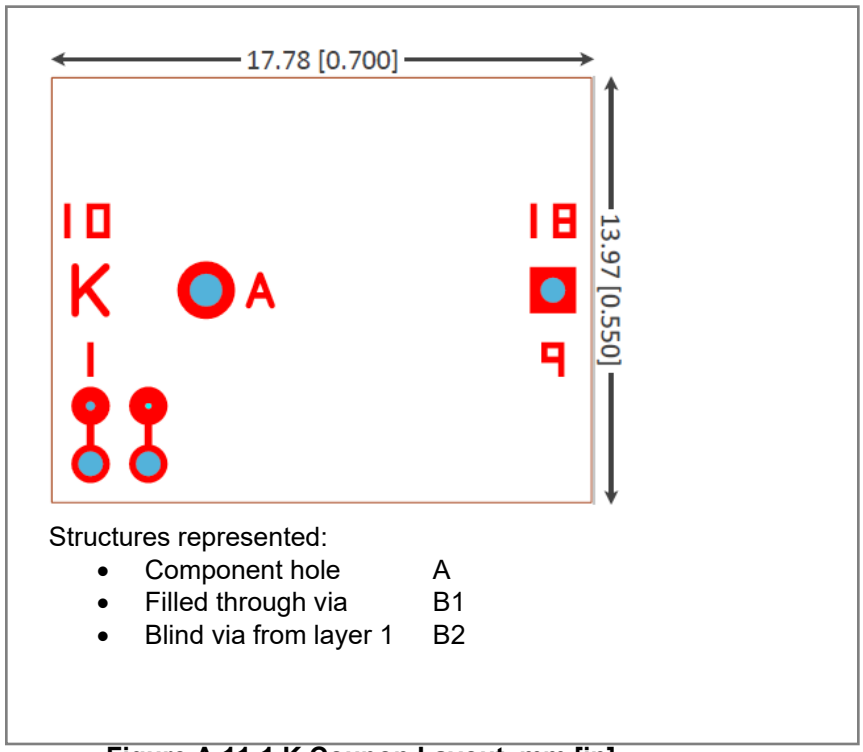


Figure A.10-2 P Coupon Layout, mm [in]

A.11 K COUPON Coupon K is used to verify that minimum spacing requirements exist between plated holes and copper on internal layers. The coupon is tested electrically using an ohm meter. A short between any of the round via test points and the square common test point indicates a failure. Coupon generator inputs, which include feature sizes and spacing requirements, **shall** match the same minimum feature sizes in the printed board.



Structures represented:

- Component hole A
- Filled through via B1
- Blind via from layer 1 B2

Figure A.11-1 K Coupon Layout, mm [in]

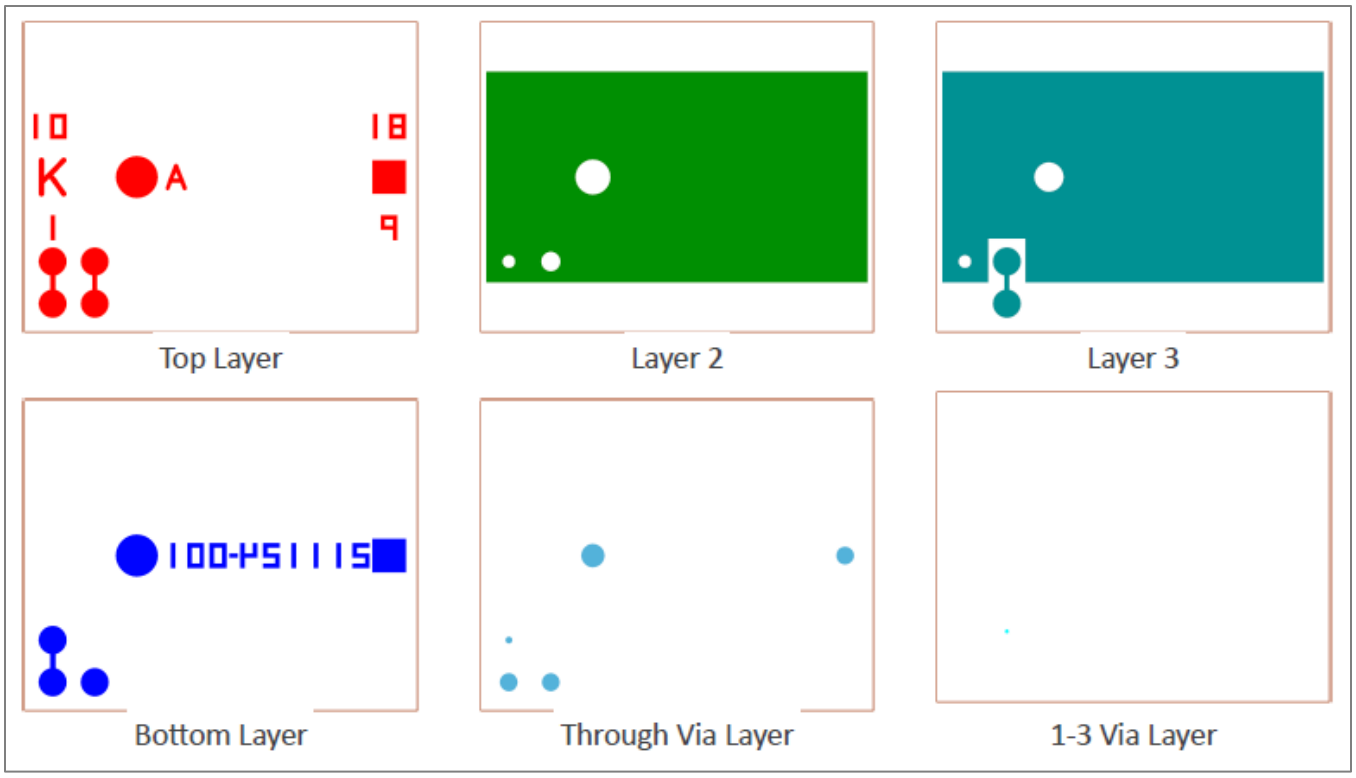


Figure A.11-2 K Coupon layer Examples