Technical Overview of the Semiconductor Chip Industry
SYLLABUS

INSTRUCTOR INFORMATION:

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Best time to call: Usually available between 6 p.m. and 9 p.m., Pacific Standard Time. You may leave a message anytime through WhatsApp.

PROGRAM DESCRIPTION

The semiconductor chip industry is deep and comprehensive. This course provides a technical overview of the industry from design and manufacturing to assembly and testing. All are welcome, including those with little or no knowledge of the subject, as the content is presented in an easy and approachable manner.

The instructor, Cheah Soo Lan, is an engineering manager with more than 30 years of experience in the electronics and semiconductor industry. She's proficient with both PCB CAD and custom IC design layout tools and is a certified Master IPC Trainer for PCB Design CID and CID+ under IPC Asia. Cheah Soo Lan spent the last 15 years as a manager in technical and vocational education for Malaysia. Prior to teaching, she worked 15 years as an engineer in support of network and television, research, and development of electronic and semiconductors at the national research centers and defense industry of Singapore.

LEARNING AND PERFORMANCE OBJECTIVES

Upon completion, participants will be able to understand:

- The basic semiconductor components at the microelectronics level
- Terminologies and technologies in the semiconductor industry
- The semiconductor ecosystem (supply chain) relationship
- The basic flow to develop and deliver the semiconductor chip
- The general flow and processes in semiconductor chip fabrication, assembly, and testing
- Basic concepts in failure analysis of semiconductor chips

COURSE STRUCTURE

This course provides engaging videos, handouts, and quizzes designed to help you grasp an overview of the semiconductor chip industry.

- Instructor and participants meet online twice per week from the comfort of their own home.
- Participants can view recorded online sessions to review course content and class discussions.
- Participants apply key concepts to create a real-world design from concept to completion.
- All required materials are included in the course. Participants may utilize a PCB design authoring software program of their choice. If participants do not have access to PCB design authoring software, IPC will provide complimentary access to Altium.
- Course materials are accessible 24/7 on the IPC Edge learning management system.
- The course can be accessed on virtually any device with an Internet connection and major web browsers, including Chrome, Firefox, Safari, Edge, and Internet Explorer.

IPC EDGE LEARNING MANAGEMENT SYSTEM

Take a moment to update your personal profile when accessing the course for the first time. IPC Edge supports the most recent versions of Google Chrome, Firefox, Safari, Internet Explorer, and Microsoft Edge. Courses can be accessed on desktops, laptops, tablets, and mobile phones. Please refer to Browser Settings under the Start Here! tab on your dashboard to make sure your browser functions seamlessly with the IPC Edge learning management system. If you need further technical assistance, please send an email to certification@ipc.org or call IPC Member Support at +1 847-597-2862.

SUPPLEMENTAL MATERIALS

- *Modern semiconductor devices for integrated circuits* (Chenming Hu) https://www.chu.berkeley.edu/modern-semiconductor-devices-for-integrated-circuits-chenming-calvin-hu-2010/
- *LM311 Datasheet* (Texas Instruments)
- *The Semiconductor Ecosystem* (Steve Blank) https://gordianknot.stanford.edu/publications/semiconductor-ecosystem

IPC STANDARDS COVERED (PROVIDED WITH COURSE)

- IPC-T-50: *Terms and Definitions for Interconnecting and Packaging Electronic Circuits*

COURSE SCHEDULE

WEEK 1

Lecture #1:

- **Introduction to Semiconductor Basics (Microelectronics)**
  - Semiconductor materials, P-N Junctions
  - Bipolar Junction Transistor, CMOS transistor technologies
  - VMOS, DMOS, BCD, FinFET, and GAA Technologies
  - IC packaging types and evolution
- **Semiconductor Supply Chain and Global Relationships**
  - Integrated device manufacturer (IDM), fabless, design house, outsourced assembly, and testing (OSAT) and IP (blocks or cell library)
  - Semiconductor cycle
  - International Roadmap for Devices and Systems (IRDS)
  - Semiconductor Industry Association (SIA)
  - Challenges in the industry

Lecture #2:

- **IC Design Process 1 (Front-end)**
  - The general flow of IC design
  - Specifications of a chip
  - Electronic design automation (EDA or CAD)
  - Basic digital design flow
  - Process development kit (PDK)
  - Design entry: HDL or Verilog language
- **IC Design Process 2 (Front-end)**
  - Basic analog IC design flow
  - Specification of a chip
  - Schematic entry & simulation
  - Floor plan concepts
  - Primitive cells (PCells, with examples)
  - Cross-sectional view (with examples)
  - Layout (mask) design

ASSIGNMENT:

- Revision of terminologies and concepts (Puzzle 1)

WEEK 2

Lecture #3:

- **Facilities and Raw Material**
  - Cleanroom classification
  - General safety

    - Electrostatic Discharge (ESD)
    - Wafer preparation (raw material – ingot)
    - Wafer size
- **Wafer Fabrication Processes (Basic) Part 1**
    - Process flow chart (simplified)
    - Oxidation:
        - Dry
        - Wet
    - Lithography:
        - Imaging
        - Mask, reticle
        - Photoresist (PR)
    - Etching:
        - Dry
        - Wet

Lecture #4:

- **Wafer Fabrication Processes (Basic) Part 2**
    - Ion implantation
    - Diffusion
    - Annealing (rapid thermal process [RTP])
    - Deposition:
        - Chemical vapor deposition (CVD)
        - Physical vapor deposition (PVD) (Sputtering)
        - Low Pressure (LPVD)
        - Plasma Enhanced (PECVD)
- **Wafer Fabrication Processes (Basic) Part 3**
    - Chemical mechanical polishing (CMP)
    - Metallization
    - Passivation
    - Metrology (Measurement)
    - Wafer sort (Mapping)
    - Yield

ASSIGNMENT:

- Revision of terminologies and concepts (Puzzle 2)

WEEK 3

Lecture #5:

- **Backend Semiconductor Assembly and Test 1**
    - Review of outsource assembly and testing (OSAT) operations
    - IC packaging and evolution
    - Dicing (Sawing)

    - Die attach
    - Wire bond or flip chip
    - Encapsulation (molding)
    - Marking
- **Backend Semiconductor Assembly and Test 2**
    - General flow of IC testing
    - IC test equipment and setup
    - Wafer test and IC package test
    - Types of tests
    - Review of electrical test
    - DC, AC, functional test
    - Build-in-self-test (BIST)
    - JTAG Boundary Scan
    - Burn-in test

Lecture #6:

- **Introduction to Chip Package Failure Analysis**
    - Bathtub curve (reliability)
    - What and why failure analysis
    - Failure modes
    - Investigation flow
    - Non-destructive / destructive
    - Visual inspection example
    - Example of a full flow (open circuit)
- **Final Exam Review**

ASSIGNMENT:

- Final Exam

You must achieve a final exam score of 70% or higher to earn a certificate of completion. You are allowed two attempts, and the highest grade is recorded.