Improving SMT Yield with AOI and AXI Test Results Analysis

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ABSTRACT
As printed circuit board assembly (PCBA) becomes more complex, Automatic Optical Inspection (AOI) and Automatic X-ray Inspection (AXI) systems are becoming more widely used in electronics manufacturing. AXI has good defect detection capabilities, but its TaKT time becomes a concern when compared to other machines (screen printer, pick-and-place, reflow, and wave soldering) on the SMT line. How can these two testing machines be used effectively to test production? This translates into: (1) how can we reduce AXI test time by supplementing it with AOI? And (2) how can we use the AOI and AXI test results to improve the overall manufacturing process and thereby increase production yields? Some studies were reported in the past with only AXI[1-3]. We have been doing this project with AOI and AXI test data analysis to improve assembly test yields.

With the Flextronics Manufacturing System (FMS) approach, we focus on Lean Manufacturing. Lean is a manufacturing philosophy that recognizes WASTE as the primary driver of cycle time, and employs techniques to continually drive out waste in the various processes. Waste elimination is the most effective means to achieve cycle time reduction. We develop new processes to deal with three types of waste: (1) Over process (2) Defect waste, & (3) Inventory accumulation. We used the key elements of Six Sigma DMAIC (Define, Measure, Analyze, Improve, & Control) and statistical tools for the project. In this study we first started with one customer's product, which previously had 100% components covered with AOI and >95% covered by AXI. We studied AOI, AXI, ICT, and Functional Test data for six months, and reduced AXI test coverage for some non-critical components. As a result of the reduction of AXI coverage, we were able to reduce AXI test time from above 4 minutes to below 3 minutes. In the meantime we also focused on process issues and improvements using daily AOI and AXI test results.

Test and process engineers worked together on this project and used the AOI/AXI test results to adjust the machine settings for solder paste printing, pick and place, and wave soldering machines; solving the process and material issues and making very good progress. An example of one product: We reduced AXI test time by only testing BGA, Fine Pitch ICs, RNs, and some "Critical to Function" parts. Therefore AXI component and pin coverage changed from 98.4%, and 98.9% to 13.6%, 50.1% respectively. AXI test time was reduced from 4.1 minutes to 2 minutes. Meanwhile, the yields of AOI (top), AOI (bottom), AXI, ICT, and FT increased from 98.9%, 97.3%, 88.4%, 98.9%, and 100% to 99.6%, 99.0%, 96.2%, 98.9%, and 100% respectively. The cost saving results will be discussed in the paper.

Key words: AOI, AXI, TaKT time, Lean Manufacturing, Six Sigma, and process control.

Introduction
The average density of PCBs is increasing rapidly, and electrical access is shrinking for In-Circuits Test (ICT). With the increase in component count and solder joint count, Automatic Optical Inspection (AOI) and Automatic X-ray Inspection (AXI) systems are being considered to "add" to manufacturing by reducing downstream electrical testing costs[4]. AOI is relatively low cost and easy to use and to set up. AOI is also capable of finding certain defects, especially wrong parts. AXI is able to detect over 95% of total defects including Ball Grid Array (BGA) voids, solder joint quality defects, plated through-hole (PTH) insufficient solder, press fit missing pins, SMT connector opens or insufficient solder, and defects associated with "hidden" joints. Using AXI in combination with conventional test techniques helps to ensure all defects are caught before products are delivered to customers. However for high-density assemblies, AXI cannot keep up with the assembly process speed because its test time is much longer than other SMT machines, thus a build up of inventory occurs in front of AXI, extending the manufacturing lead time of the assembly. Therefore balancing the SMT line can be a challenge.

Lead time reduction is crucial to become lean. Waste elimination is the most effective means of achieving lead time reduction. There are seven main types of waste: transportation, inventory, motion, waiting, over production, over-processing, and defects. For this project, we focused on the following three wastes: over-processing, defects, & inventory. There are currently fourteen Agilent AOI machines and three 5DXs at the Flextronics Shanghai site**.** We decided to keep the AOI test with 100% coverage, and reduce AXI coverage for this revolutionary network product. The PCB layer varies from 6 to 24 for its assemblies. Our purpose was to improve SMT yields with AOI and AXI test results analysis. There are two phases of this project. Phase I is the reduction of AXI test time with 100% AOI test. We reviewed the AOI, AXI, ICT, and FT historical data, to understand and optimize the various aspects of the process and defect types. We then modified the AXI program by reducing components coverage. Phase II focused on the improvement of SMT yields with the help of the process engineers.

We had to first ensure that the AOI and AXI programs were in good shape. We wanted to have AXI and AOI defect feedback immediately so that the root cause of process issues could be identified and resolved before much "waste" was created. The process details will be described in the section of methodology. In the conclusion section, we will also list the savings for this project.

Methodology

Lean is about system improvement. We have to think of AOI and AXI not as machines or tools, but as systems. Lean goes beyond the tools and provides a methodology for system thinking, cultural change and sustainable improvement. Both test engineers and process engineers have been working together on this project to improve SMT yields with AOI and AXI test results analysis.

Table 1 - The historical test yields without AXI test reduction

Assembly #	Month	Test Yield				
		AOI (top)	AOI (bottom)	5DX	ICT (process)	FCT (process)
	5-Oct	99.40%	98.70%	98.60%	99.40%	100.00%
	5-Dec	97.60%	100.00%	83.70%	100.00%	100.00%
	6-Jan	98.00%	100.00%	88.60%	100.00%	100.00%
	6-Feb	98.70%	99.30%	94.60%	99.10%	100.00%
Assembly-A	6-Mar	98.00%	98.70%	93.80%	97.30%	100.00%
	5-Nov	98.70%	97.20%	92.90%	98.70%	100.00%
	5-Dec	98.50%	98.80%	94.70%	99.60%	100.00%
	6-Jan	98.90%	97.30%	88.40%	98.90%	100.00%
	6-Feb	98.40%	96.50%	95.40%	99.20%	100.00%
Assembly-B	6-Mar	98.80%	97.80%	95.20%	98.00%	100.00%
	5-Oct	95.20%	96.80%	96.80%	99.20%	100.00%
	5-Nov	95.90%	96.60%	90.50%	100.00%	100.00%
	5-Dec	96.20%	98.00%	84.80%	97.40%	100.00%
	6-Jan	100.00%	100.00%	75.00%	97.00%	100.00%
	6-Feb	96.90%	93.30%	89.30%	97.80%	100.00%
Assembly-C	6-Mar	95.70%	92.20%	92.80%	98.50%	99.90%
	6-Jan	100.00%	100.00%	72.10%	100.00%	NA
	6-Feb	100.00%	99.00%	93.10%	97.10%	100.00%
	6-Mar	97.70%	96.30%	95.50%	99.70%	100.00%
Assembly-D	5-Dec	98.80%	97.70%	85.00%	98.80%	100.00%
	6-Jan	100.00%	100.00%	88.30%	96.20%	NA
	6-Feb	96.20%	93.80%	90.80%	100.00%	99.40%
Assembly-E	6-Mar	98.80%	88.80%	91.00%	98.50%	100.00%

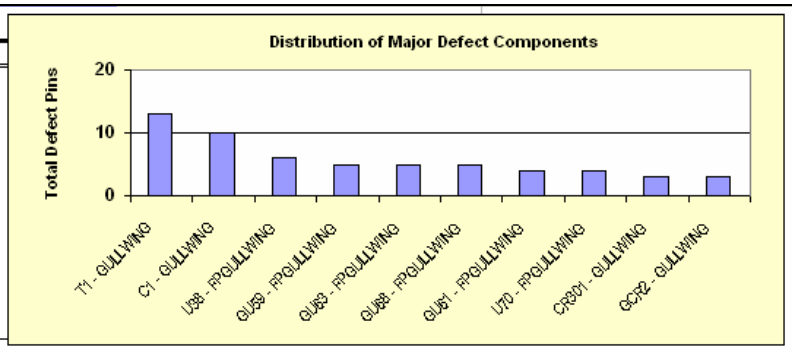
1. Reduction of AXI Test Time

How to reduce AXI test coverage? We used the key elements of Six Sigma DMAIC (Define, Measure, Analyze, Improve, & Control) and statistical tools for the project. First we reviewed test yields (AOI, AXI, ICT, and FT) for chosen assemblies for the previous 3-6 months. At the beginning, we only chose the products with stable processes and satisfying test yields (AOI>95%, AXI>80%, ICT>95%, and FT>99%) and with two digits DPMO (<30). Table 1 lists previous test yields for the first 5 assemblies we studied for this project.

What historical defects have been caught by 5DX? Which components have these defects? Figure 1(a) lists top ten defect component locations and Figure 1(b) shows the defect types for one assembly. This assembly has 0402 parts, 19.7 mils pitch size FPGullwing, 24 mils BGA ball on 14 layers PCB. Table 2 lists the top ten defects for seven assemblies for previous three to six months' data. Based on the analysis of this historical data, we learned that the main defects are from Fine Pitch Gullwing and Resistor Networks.

*** 5DX TEST SUMMARY ***

Panel Name	Assembly-C
Date from	02/01/06
Date to	02/28/06
Total boards tested	527
Boards with defects	66
Board Yield (%)	87.48
Total Defect Pins	145
Primary Components	1774
Secondary Components	716
Total Tested Pins	10070
DPMO	22
Comment	



Component	DefectTotal	Serial No.	Total	Open	Short	Void	Excess	Misalign	Insuff	Multiple	Miss	KnockOff
Sub Total	145	All	145	62	27	0	0	0	37	13	6	0
T1 - GULLWING	13	80602090098	8	4	0	0	0	0	4	0	0	0
		80602090227	5	0	0	0	0	0	5	0	0	0
C1 - GULLWING	10	80601090021	1	0	0	0	0	0	0	1	0	0
		80602090045	3	0	0	0	0	0	3	0	0	0
		80602090200	2	0	0	0	0	0	2	0	0	0
		80602090337	4	3	0	0	0	0	1	0	0	0

Figure 1a - Main top ten defect locations for Assembly-C assembly

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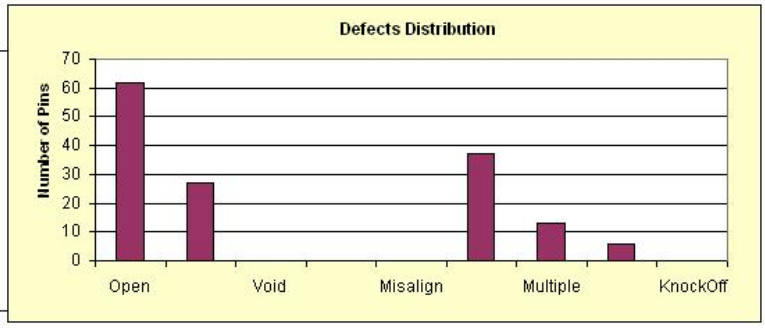


Serial No.	DefectTotal	Component	Total	Open	Short	Void	Excess	Misalign	Insuff	Multiple	Miss	KnockOff
Sub Total	145	All	145	62	27	0	0	0	37	13	6	0
80601090023	10	GR534 - RES	2	2	0	0	0	0	0	0	0	0
		GU61 - FPGULLWI	4	3	0	0	0	0	1	0	0	0
		U38 - FPGULLWIN	4	0	0	0	0	0	0	4	0	0
80602090098	8	T1 - GULLWING	8	4	0	0	0	0	4	0	0	0
80602090227	7	T1 - GULLWING	5	0	0	0	0	0	5	0	0	0
		U36 - FPGULLWIN	2	0	2	0	0	0	0	0	0	0

Figure 1b - Main defect type for Assembly-C assembly

Last year, we used 100% AOI and 100 AXI test inspection coverage for all assemblies for this customer. What is the definition for over-processing? It is the processing above and beyond the customer's (internal and external) requirement. It is nice to have AXI with 100% coverage because of its proven capabilities of catching solder joint defects. However AXI test time is much longer than other SMT machines, and therefore, if we test 100% we are not able to improve SMT process with "real time" AXI defect feedback. We consider this as being an example of over-processing: 100% AXI inspection after wave machines with the intent to catch and prevent "escaping defects." Here, 100% testing is used as a substitute to improving upstream processes. To reduce "over-processing" we modified the AXI programs (i.e. reduced test coverage) for these assemblies. AOI test coverage remained at 100%. We based our changes to the AXI programs on the historical data we collected. We removed from the AXI test those components which did not have defects for the last six months; the exception being BGAs. Table 3 lists AXI test coverage and test times with previous and current programs for the assemblies chosen. The AXI test programs were modified to only test BGAs, Fine Pitch, Gullwing, PTH, and the "Critical to Function" components that were found defective over the last six months. Therefore the AXI components coverage and pin test coverage was reduced to <20%, and about 55% respectively. The AXI testing time was reduced to about 55% of previous time as shown on Table 3. This not only created a savings in test time, but also added to a much better balanced SMT TaKT time. It also enabled "real time" AXI defect feedback for SMT line.

Table 2 - Top ten component locations which have the most defects

Assembly-F	GU25	GRN137	U30	GRN138	P1	L2	C11	GU27	U307	GY1
	BGA	RN	QFN	RN	Connector	Inductor	Chip	SOT	TSOP	gullwing
Assembly-G	U503	GU2	U506	U12	GY1	U11	GU3	U5	U37_A	U37
	TQFP	TSSOP	TQFP	PSOP	OSC	PSOP	TSSOP	PSOP	pth	pth
Assembly-C	U319	U50	U72	GP3	U70	C1	GU8	T1	GU1	DL3
	TSOP	QFP	QFP	Connector	TQFP	Chip	TSSOP	gullwing	gullwing	pth
Assembly-A	RN46	RN44	U16	U53	RN36	U60	U56	P14_A	Y3	P10
	RN	RN	PLCC	QFP	RN	SO16	PSOP	pth	gullwing	pth
Assembly-B	GU101	PS2	U17	C9	U19	U522	SCT3	U519	GRN137	GP1
	TSOP	gullwing	TQFP	Chip	TQFP	TQFP	SOT	TQFP	RN	Connector
Assembly-D	P9	U623	U604	P20	U507	U1	RN559	U531	RN511	C502
	Connector	PSOP	PSOP	Connector	PSOP	PSOP	RN	TSOP	RN	Chip
Assembly-E	Y5	P23	U588	U38	U512	L24	U531	U594	U612	U500
	OSC	Connector	SOT	TSSOP	TQFP	Inductor	TSOP	PSOP	PSOP5	PSOP5

Table 3 - AXI test coverage and test time with previous and current programs for some assemblies

Item	**AXI Component coverage %**		**AXI Pin coverage %**		**AXI Test time (s)**	
Assembly #	**Previous**	**Current**	**Previous**	**Current**	**Previous**	**Current**
Assembly-A	94.4	14.7	94.07	56.2	184	85
Assembly-B	99.47	13.6	99.15	50.1	226	90
Assembly-C	95.9	13.5	98.37	54.2	305	80
Assembly-D	98.52	18.3	95.33	51.4	410	206
Assembly-E	98.52	18.2	95.19	51.4	410	206

2. SMT Improvement

We all believe that prevention is better than detection. Per the key elements of Six Sigma DMAIC (Define, Measure, Analyze, Improve, & Control), here is the list for main items that we focus on:

a. Maintaining effective AOI and AXI programs
b. Ensuring machines are in good working condition
c. Elimination of defect by identifying the root cause
d. Maintaining real-time test result feedback to upstream processes

2a. Effective AXI and AOI Testing

First, we ensured that AOI and AXI programs in good working condition, i.e. able to detect real defects. We then establish two feedback loops: AXI "to" AOI; ICT and FT "to" AXI. If AXI found a defect which escaped from AOI, then the AXI team would "feedback" this information to the AOI team. ICT and FT teams also provide "feedback" to the AXI team if a solder escape was detected at ICT or FT. Figure 2 is an example: Assembly 415-149 location GRN6 (10 pins components with pitch size 25 mils) was found as solder insufficient at ICT. (NOTE: This defect was detected by "visual" inspection as ICT testing does not detect "insufficient" solder.) It is a very obvious defect on this particular part as visually you cannot see a heel. Why didn't AXI detect it? The original AXI setting was focused on the heel only, and it is shown on Figure 3(a), the "blue" bar. We adjusted the Gullwing Algorithm for different orientation for testing the heel, center and toe location as shown in Figure 3(b). With the new setting, AXI was able to detect the insufficient defect effectively even those insufficient joints which are not very obviously from the image. Having stable and effective AOI and AXI programs is the main requirement for defect detection. We have been monitoring and modifying AOI and AXI programs on a regular basis, especially with the help of downstream defect information feedback.

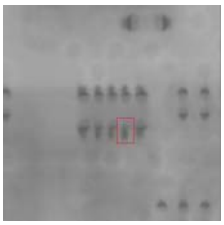
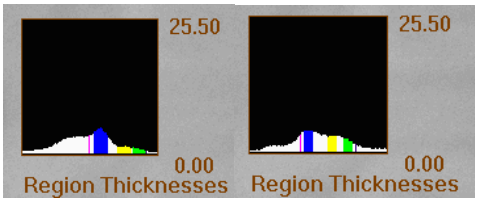


Figure 2 - Solder insufficient defect on component GRN6



(a) **(b)**

Figure 3 - (a) Previous and (b) modified algorithm setting for component GRN6

2b. Machine Calibration

Second, in order to ensure all AXI machines are operating under good test conditions, we perform tests daily on a "baseline" board. (NOTE: A "baseline" board is a board with known solder defects/locations. If this "baseline" board is tested under constant conditions including system "health," the AXI test will always identify the same solder defects). In our case, our "baseline" board has 12 known defects. If the machine is in good condition, the AXI testing of this board on a daily basis should always identify the 12 solder defects. If there is variation in the defects detected, it is likely that the machine needs to be calibrated (i.e. Confirmation and Adjustment performed) —which should be done immediately. As a rule, we must perform machine calibrations per the recommendations of the AXI vendor. We also regularly check Cp/Cpk for SMT machines (DEK printer, Panasonic pick and place, and Heller oven machines).

2c. Defect Data Analysis

Third, we provide a Defect Data Analysis (defect distribution) brief report to the process team, focusing on the main defects for each assembly for the next run. Here are examples for solving the defect at the root cause.

Example 1: Many PS2 (RPOTS) locations had insufficient or open defects detected on production boards (Figure 4). The root cause was "in-coming" material with a lifted leads. This resulted in insufficient or open solder as shown in Figure 5. That was why some boards had defects on PS2, and some boards didn't have defects at this location. Our customer allowed for the component vendor to have 9 mils tolerance of lead lift. However the PCBA has fine pitch components with a stencil thickness requirement of <= 6 mils. Therefore we manufactured step-up stencil to give PS2 10 mils height solder paste without any impact on other locations. The figure 6 shows the current stencil with step-up for location SP2. The failure rate for this location was reduced from 1.5% to 0% is because we resolved the root cause of this problem.

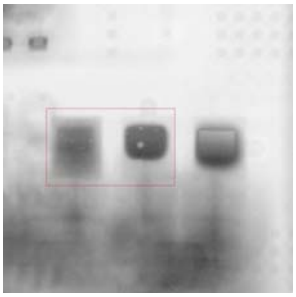


Figure 4 - Insufficient defect on component RPOTS-24, top side PS2, power supply

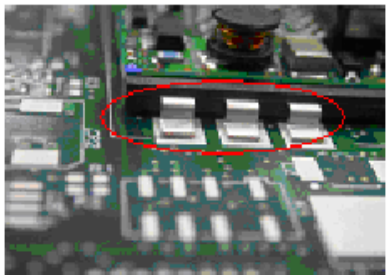


Figure 5 - Raw material lifted leads on component RPOTS-24, top side PS2, power supply

Figure 6 - Step-up stencil on component RPOTS-24, top side PS2, power supply

Example 2: AOI found many chip capacitors with de-wetting: There were a total of 38 parts with solder joint defects on 1581 boards from August 29 to September 21. We were able to identify the root cause: These two parts are lead-free components, and the original oven profile didn't meet the lead-free solder requirements. Therefore we modified the oven temperature of Zone 1, Zone 7, and Zone 8, so that the peak temperature was higher than before (increased about 10 ^{o}C), and the reflow time (above 183 ^{o}C) was reduced about 5 seconds. Meanwhile, we also regularly checked the Heller oven's Cp/Cpk, and kept Cpk > 1.5 or higher. From September 22 to October 12, after the profiles were changed, there was only 1 defective joint detected on 651 boards tested.

2d. Real Time Defects Data Feedback

With the reduction of the AXI test time, we were able to obtain "real time" AXI defect data feedback. We created some in-house software to analyze the AXI data. We placed the resulting AXI yield and defect information on a common folder for everyone to review and utilize. We wanted to eliminate the random defect as soon as possible.

Table 4 - AOI, AXI, ICT and FT test yield for the assembly-C before reducing AXI coverage

Month	Volume	AOI (top)	AOI (bottom)	5DX	ICT (process)	FCT (process)
Oct-05	62	95.3%	96.8%	96.8%	99.2%	100.0%
Nov-05	158	95.9%	96.6%	90.5%	100.0%	100.0%
Dec-05	236	96.2%	98.0%	84.8%	98.5%	100.0%
Jan-06	12	100.0%	100.0%	75.0%	97.0%	100.0%
Feb-06	527	96.9%	93.3%	87.5%	97.8%	100.0%
Mar-06	264	95.7%	92.2%	92.8%	98.5%	99.9%
Before	1259	96.3%	94.6%	89.6%	98.4%	100.0%

Table 5 - AOI, AXI, ICT and FT test yield for the assembly-C after reducing AXI coverage

Month	Volume	AOI (top)	AOI (bottom)	5DX	ICT (process)	FCT (process)
Apr-06	191	96.0%	94.5%	99.0%	98.3%	100.0%
May-06	207	99.5%	97.6%	96.1%	98.3%	100.0%
Jun-06	364	98.3%	99.1%	93.7%	98.0%	100.0%
Jul-06	516	99.3%	99.6%	96.0%	99.3%	100.0%
Aug-06	0	0.0%	0.0%	0.0%	0.0%	0.0%
Sep-06	205	98.5%	97.5%	98.1%	95.6%	100.0%
After	1483	98.5%	98.3%	96.1%	98.2%	100.0%

Table 6 - Cost saving for AXI machine with eleven assemblies for six months

Monthly Saving $	April	May	Jun	Jul	Aug	Sep	Sum
Assembly-A	**200.72**	**93.31**	**156.01**	**65.61**	**212.38**	**164.27**	**892.3**
Assembly-B	**1241.14**	**608.33**	**479.2**	**315.79**	**611.39**	**692.17**	**3948.01**
Assembly-C	**162.45**	**176.05**	**309.58**	**438.86**	**0**	**174.35**	**1261.29**
Assembly-D	**249.21**	**7.02**	**491.4**	**215.28**	**623.61**	**410.67**	**1997.19**
Assembly-E	**249.21**	**72.54**	**0**	**249.21**	**336.96**	**341.64**	**1249.56**
Assembly-H	**40.34**	**8.1**	**14.58**	**13.12**	**7.94**	**12.64**	**96.71**
Assembly-I	**145.5**	**242.81**	**126.68**	**207.93**	**22.03**	**591.19**	**1336.15**
Assembly-J	**12.78**	**129.26**	**48.1**	**96.19**	**0**	**48.85**	**335.17**
Assembly-F	**1043.08**	**727.79**	**789.75**	**394.88**	**566.8**	**481.14**	**4003.43**
Assembly-K	**531.63**	**223.05**	**332.94**	**172.26**	**487.67**	**667.95**	**2415.5**
Assembly-L	**1019.7**	**272.7**	**630.9**	**301.5**	**747**	**947.7**	**3919.5**
Sum	**4895.76**	**2560.96**	**3379.14**	**2470.63**	**3615.78**	**4532.57**	**21454.84**

A lean system is a philosophy and an orientation for people. Our test and process engineers work as a team to create value for our customers. With everyone's help and effort in identifying and resolving problems in the production process we have been seeing good progress. Table 4 and 5 lists the yields for "before" and "after" for AOI, AXI, ICT, and FT yields. After reducing AXI coverage for one assembly, AOI (top), AOI (bottom), AXI and ICT yields changed from 96.6%, 94.6%, 89.6%, and 98.4% to 98.5%, 98.3%, 96.1%, and 98.2% respectively, and FT test yields still remained at 100%. Our standard procedure is that we will use the original AXI program (i.e. high component coverage) if the ICT or FT yields drop several percentage points for any assembly. So far we have not had to return back to the original program as yields have remained consistent.

Conclusion

1. AOI & AXI are more efficient when used to complement each other. Together, they will identify virtually all defects before electronic test.
2. AOI & AXI are test tools, and they can also be used as SMT process improvement tools if their test results are properly analyzed and fed back to upstream processes.
3. By balancing the coverage between AOI & AXI, the AXI cycle time can be noticeably reduced eliminating AXI as a bottle-neck. This will also reduce the "waste" to achieve FMS (lean) concept.
4. With AXI coverage reduction, there is a significant cost savings. Table 6 lists the savings for AXI machines with eleven assemblies for a period of six months. Here we considered AXI machines as 5 years depreciation, 28 days/month, 22 hours/day, and 85% machine testing time efficient rate.
5. We suggest using 100% AXI coverage for new products especially when new package types are used. It is necessary to review all test yields and data to confirm a stable SMT process before reducing AXI test coverage.

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Acknowledgements

Wei Bing Qian, Jack Shen, Winde Wang, Wendy Zhang, Angery Lee, Allen Wei, Andrew Ho, EB Yeoh, David Geiger, Jane Phan, Gary Liu, Sam-TS Wong, Barbara Koczera, Heidi Hanson and Flextronics Shanghai engineering and production teams.

Improving SMT Yield with AOI and AXI Test Results Analysis

FLEXTRONICS

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February 2007

FLEXTRONICS

Agenda

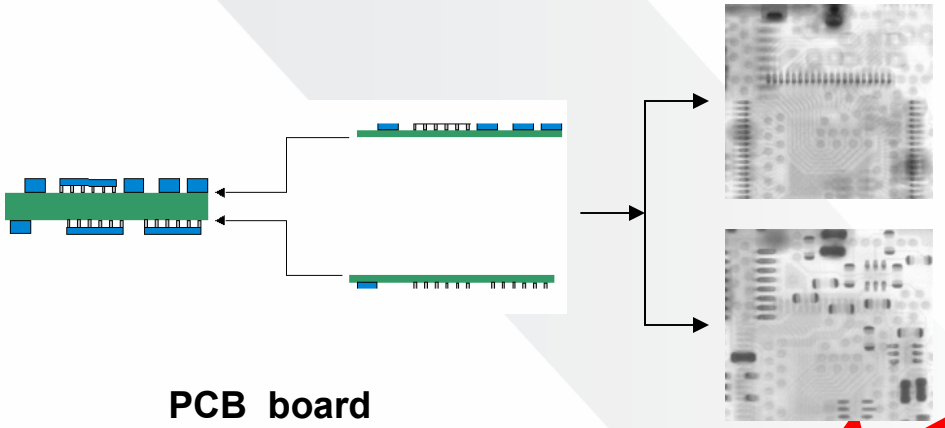
Introduction

Reduce 5DX Test Time (AOI & 5DX)

Conclusion

Introduction - Background

As PCBAs become more complex – parts are getting much smaller in size with more "hidden" joints -- Automatic X-ray Inspection (AXI-5DX) is becoming more widely used in electronics manufacturing.



PCB board

SMT line

AXI – 5DX

Ways to eliminate the bottleneck

- Option #1: Purchase a "second" 5DX to support each line --- VERY COSTLY!!!
- Option #2: Reduce 5DX test time by decreasing test coverage

Introduction - 3 strategy in Flextronics International

Currently in Flextronics International, we have 3 strategies to reduce 5DX test time efficiently:

Strategy # 1

When properly implemented, 5DX test time can be reduced by removing parts that are known to be reliably tested at ICT or by implementing 5DX board sampling testing. Testing for this strategy was performed at Flextronics -San Jose.

Strategy # 2

The 5DX test time reduction can be achieved by reducing component coverage at 5DX by including AOI in the Test Strategy. Testing was performed at Flextronics -Shanghai.

Strategy # 3

We have found there is good correlation between SPI and 5DX and will combine SPI, 2D Xray,5DX to reduce test time. The "initial" phase of this evaluation was performed at Flextronics -Plano.

Hypothesis

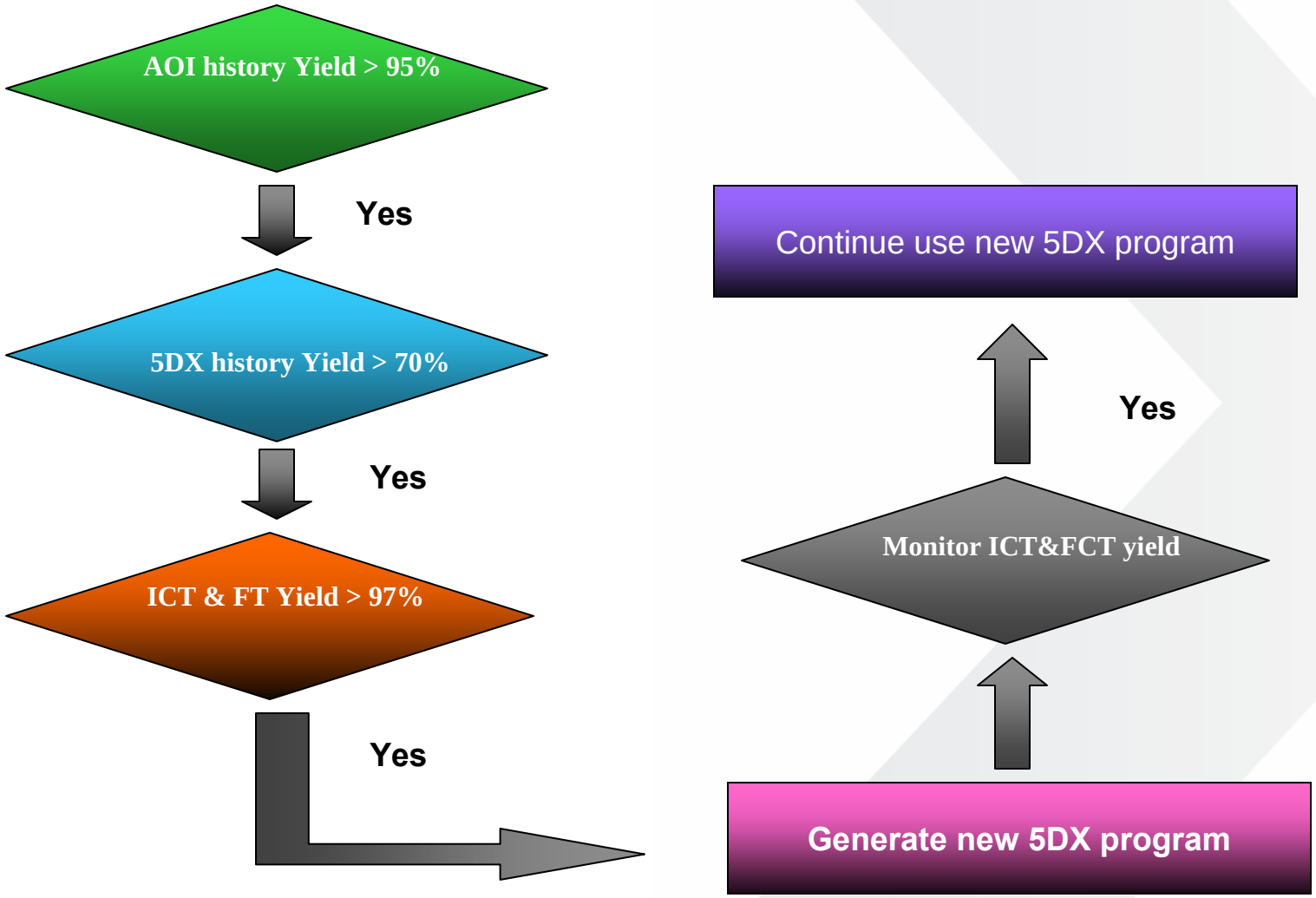
Scenario	Complex board	5DX Sampling size	5DX test component coverage	5DX Capacity
1	Medium to High	↑ (100%)	↑ (100%)	↓ (5DX can become bottleneck)
2	Medium to High	↑ (100%)	↓ (50-80%)*	↑(reduce about 20% test time)
3	Low to Medium	↓(20-50% test)*	↑ (100%)	↑ (reduce about 20-70% test time)
4	Low to Medium	↓(20-50% test)*	↓ (50-80%)*	↑↑ (no bottleneck at all)

Reduction of 5DX time = Increase of 5DX capacity (No bottleneck)
educed coverage tests must be constantly monitored to ensure good quality
Use 100% coverage for the first 5 boards for each build to ensure stable processes.

- High complex : BGA and FPGullwing size < 20 mils, solder joints > 20,000.

- Low complex : BGA and FPGullwing size > 25 mils, solder joints < 10,000.

Strategy # 2 Flow Chart: 5DX & AOI Method



Strategy # 2: 5DX and AOI

Shanghai Malu Manufacturing

Goal & Method & Key steps

Goal

1. Reduce 5DX test inspection times by removing from the 5DX test those parts that have no failure history, are inspected AOI, are not “Critical to Function.”
2. Improve Production Yields with “Real Time” Process Defect Feedback.

method

Reduce 5DX test time by analyzing 5DX data for 3-6 months to determine which components had NO HISTORY of failure as candidates for removal from 5DX test. Test boards 100% with AOI, and Revise the 5DX program to test only hidden joints (BGA, QFN, PTH, etc…) and all Fine Pitch Gullwing devices.

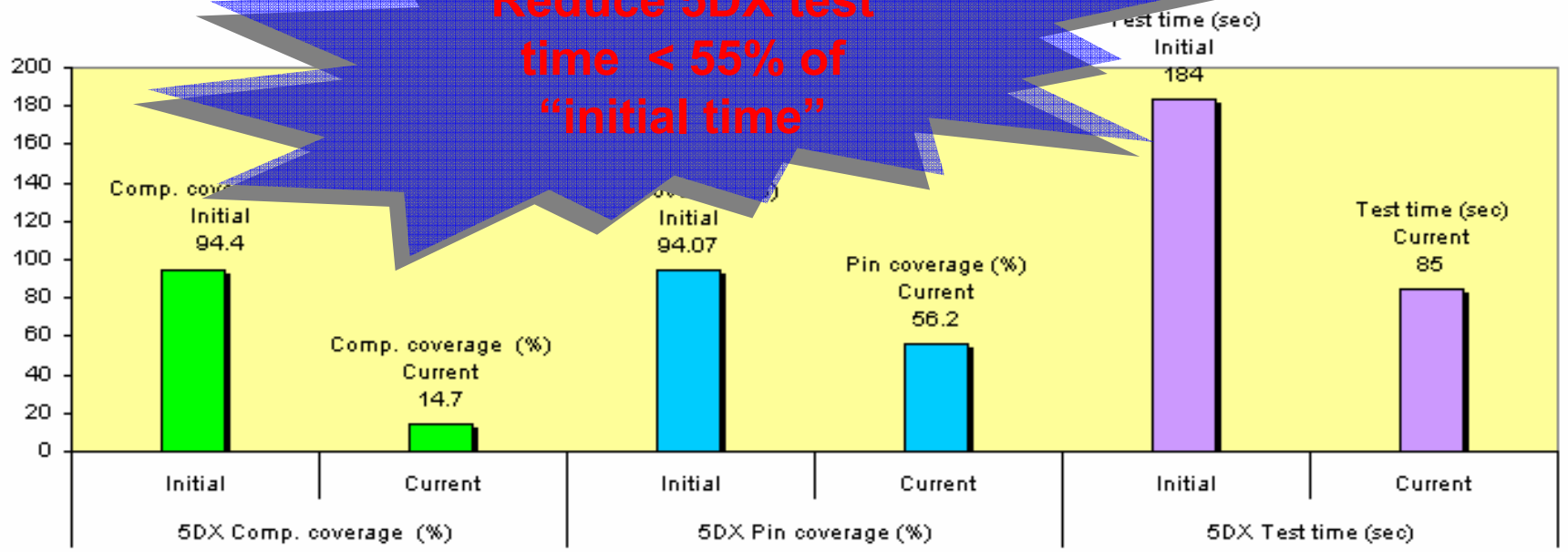
Key steps

1. Review the 5DX, ICT and FT history data.
2. 5DX Tests revised to include critical parts
3. Keep AOI 100% board & components for the Production Line
4. Establish a 5DX “Real Time” feedback system.
5. Monitor process to ensure that “REAL TIME” defect feedback

Test Time Reduction Results:

Model "Calix"	5DX Comp. coverage (%)		5DX Pin coverage (%)		5DX Test time (sec)	
	Initial	Current	Initial	Current	Initial	Current
Assembly-A	94.4	14.7	94.07	56.2	184	85
Assembly-B	99.47	13.6	99.15	50.1	226	90
Assembly-C	95.9	13.5	98.37	54.2	305	80
Assembly-D	98.52	18.3	95	51.4	410	206

Reduce 5DX test time < 55% of "initial time"



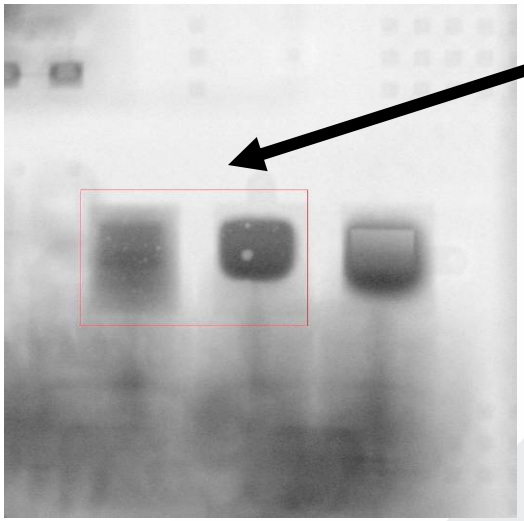
Examples of “Real Time” Process Defect Feedback

Example: 5DX feedback to SMT process

- Top Side, Package: **RPOTS-24,** Ref.Des**: PS2,** Defect: **Insufficient Solder/Open**

5DX's finding:

Many production boards have "Insufficient" solder on the PS2 devices. The defects are not "continuous" , i.e. from board to board, but it is believed to be related to the process. .



Action:

Working with PE to determine the root cause.

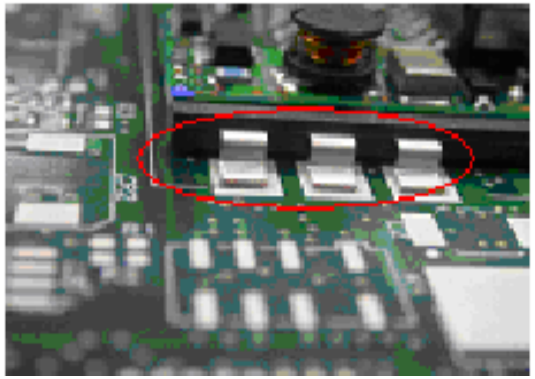
Example: 5DX feedback to SMT process

- Top Side, Package: **RPOTS-24,** Ref.Des**: PS2,** Defect: **Insufficient Solder/Open**

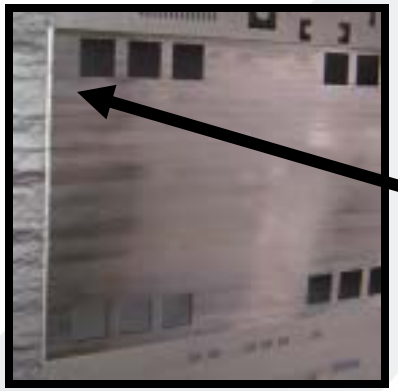
Root Cause Analysis : In-coming Material with “Lifted Lead” results in Insufficient Solder and Open joints.

Action: Customer permits Component Vendor 9mil tolerance of lead lift, but the PCBA has fine pitch components requiring that the stencil thickness be within 6 mil. So Flextronics manufactured a **step-up stencil** to give PS2 a 10 mil height solder paste without any impact on other locations.

Result: The failure rate reduced from 1.5% to zero.



Raw Material
lead lift



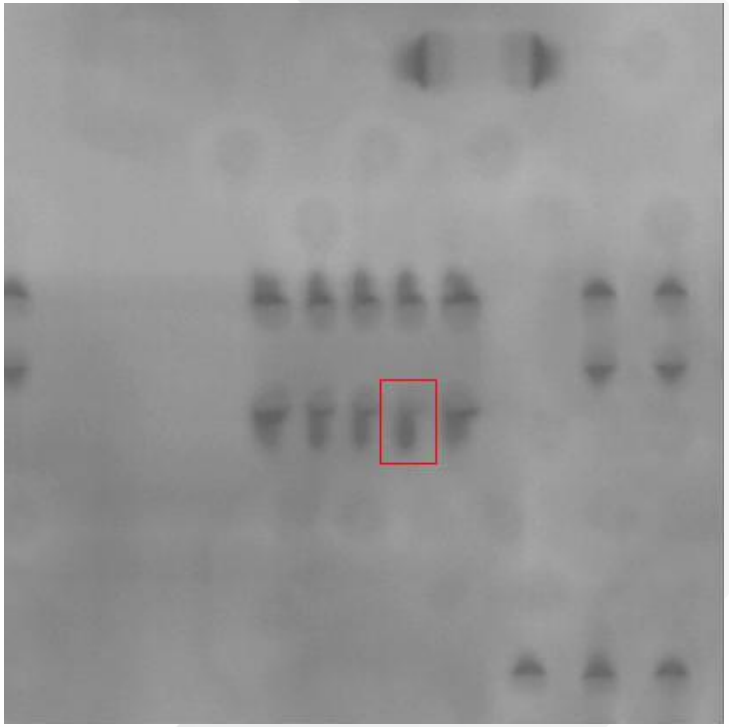
Step-up
Stencil

Example: ICT feedback to 5DX

ICT caught the defect due to escape from 5DX, we have real time feedback loop to make sure 5DX program with good shape.

Defect Location: **GRN6**
(SN:080608390725)

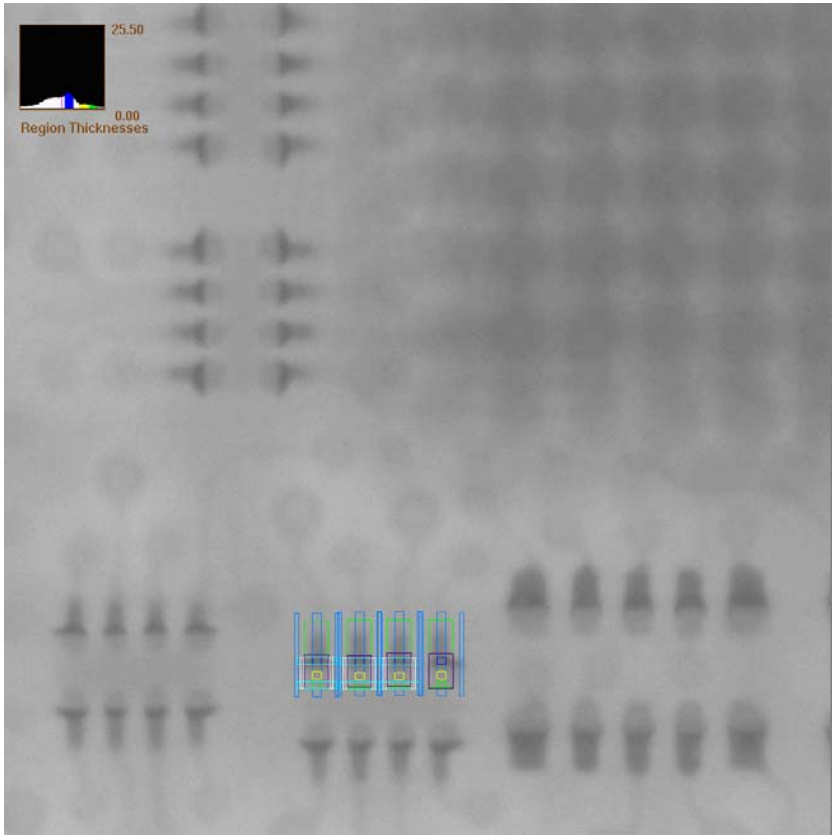
ICT found defects. We retested the component, and 5DX image as shown:



From this photo, we can find that the defect not very obvious and the pin heel is not clear.

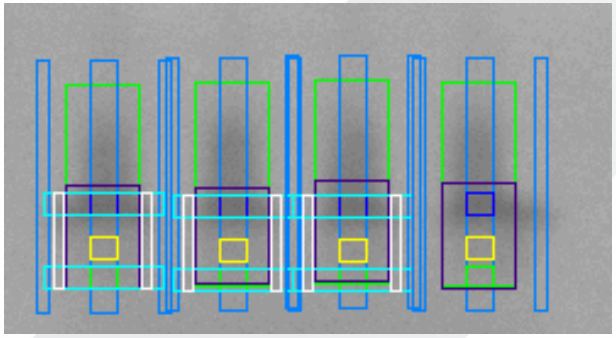
Example: ICT feedback to 5DX

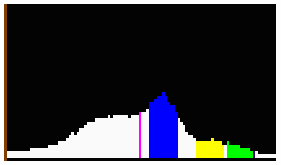
The components were tested with Gullwing Algorithm as this orientation: heel, center, toe location as shown:



Heel line (Blue) is on the real heel location. Center line (Yellow) and toe line (Green) are under the component.

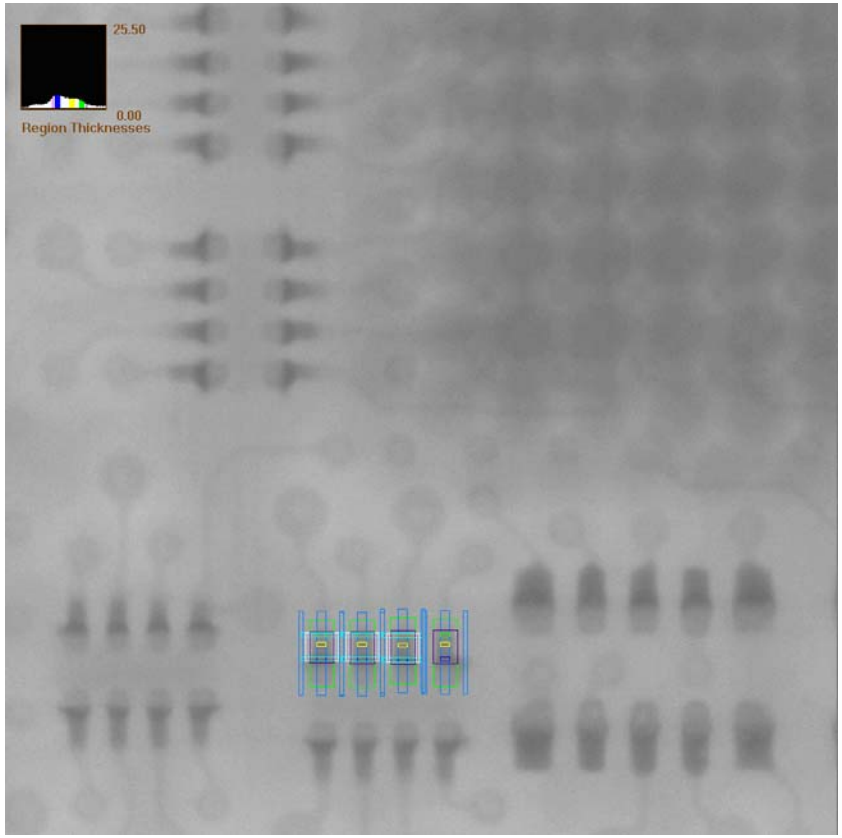
This set is focused on the heel only. The open signal can be very high, however it is easy to miss insufficient defect as shown on previous slide.





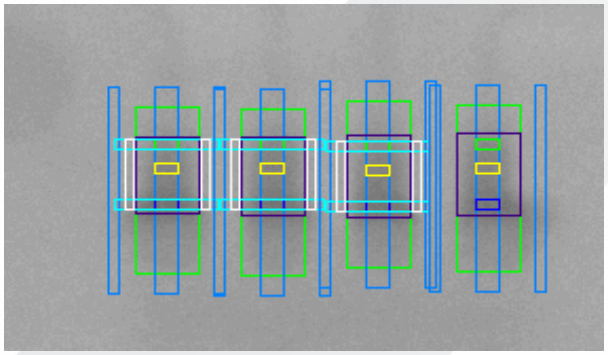
Example: ICT feedback to 5DX

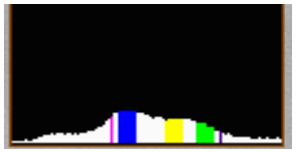
After 5DX team analyzed this kind of defects, we adjusted Gullwing Algorithm on this kind of components.



We set the heel, center, toe line from the different direction (The line location follow the pin's feature).

With this setting, we have very good graphic for heel, center and toe area. Now, we can catch insufficient defects which are not very obviously.

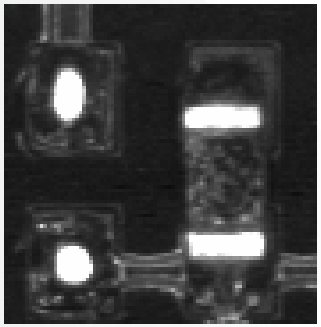




Example: 5DX feedback to AOI

5DX's finding: Assembly-B Location: GR194

Resistor 's Insufficient defects happened some times. But they are not covered by AOI station

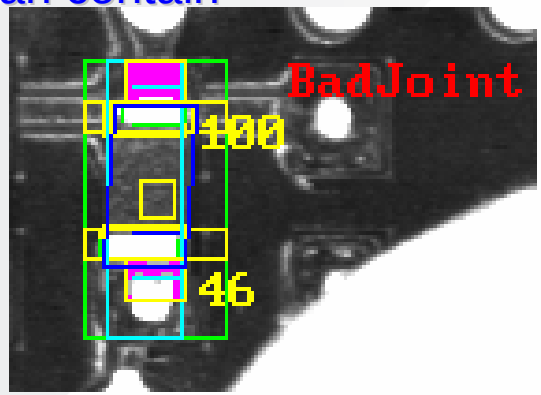


Root Cause Analyze :

1. The image of Resistor's NS is special, bright spot will not spread over the Pad, but is an ellipse in Pad Center
2. AOI program set Joint Check Window as usual, size:200x400um ,not include all the bright spot.

Action:

Resize the Joint Check Window to 250x400um,which can contain most of bright spot when No Solder



Result:

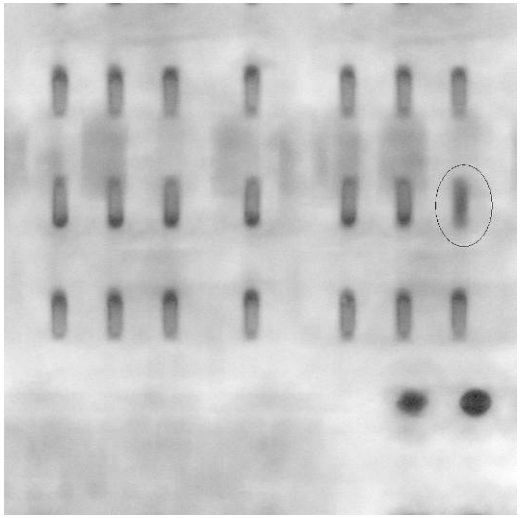
AOI can catch Most Resistor NS without False Call

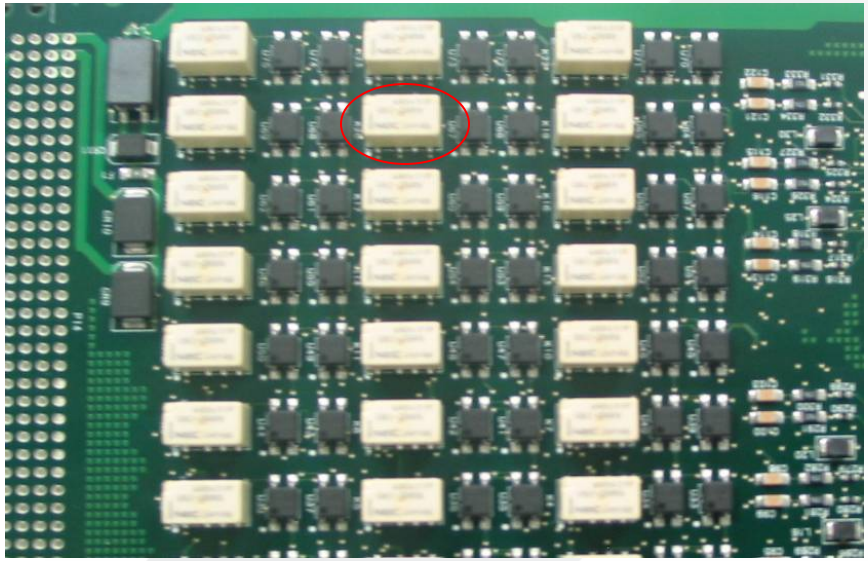
Example: 5DX feedback to material

5DX's finding:

Model : Assembly-B/ Assembly-F
Location: Kxx , Part Number:609-00005/609-00002…

Relay (Kxxx) 's Lift Lead is detected seriously in product.





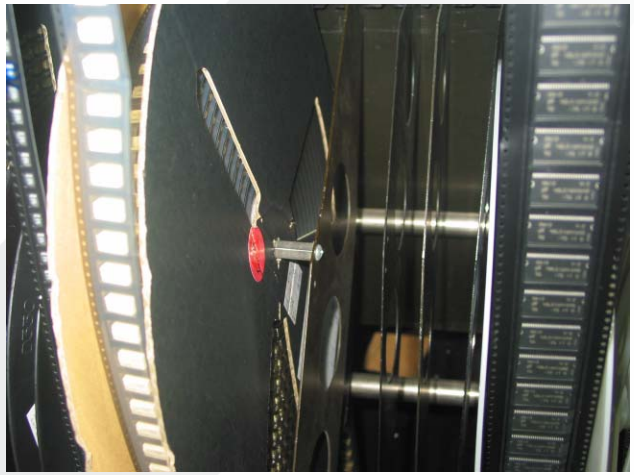
Example: 5DX feedback to material

Root Cause Analyze :

1. The package of this part is paper-reel, which is easy to be distorted due to paper's low intension when turnover
2. Operator's incautious action

Action:

1. QD is pushing forward vendor to replace package from paper to plastic which has high strength in protecting material
2. Also Kaizan in Feeder Table ,
   add stick to hold weigh of reel

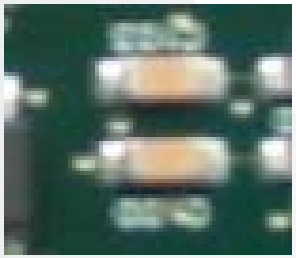


Remark:

Keep on observe any defect of Kxxx after modification in feeder table;

Example: AOI feedback to SMT process

AOI ’s finding:



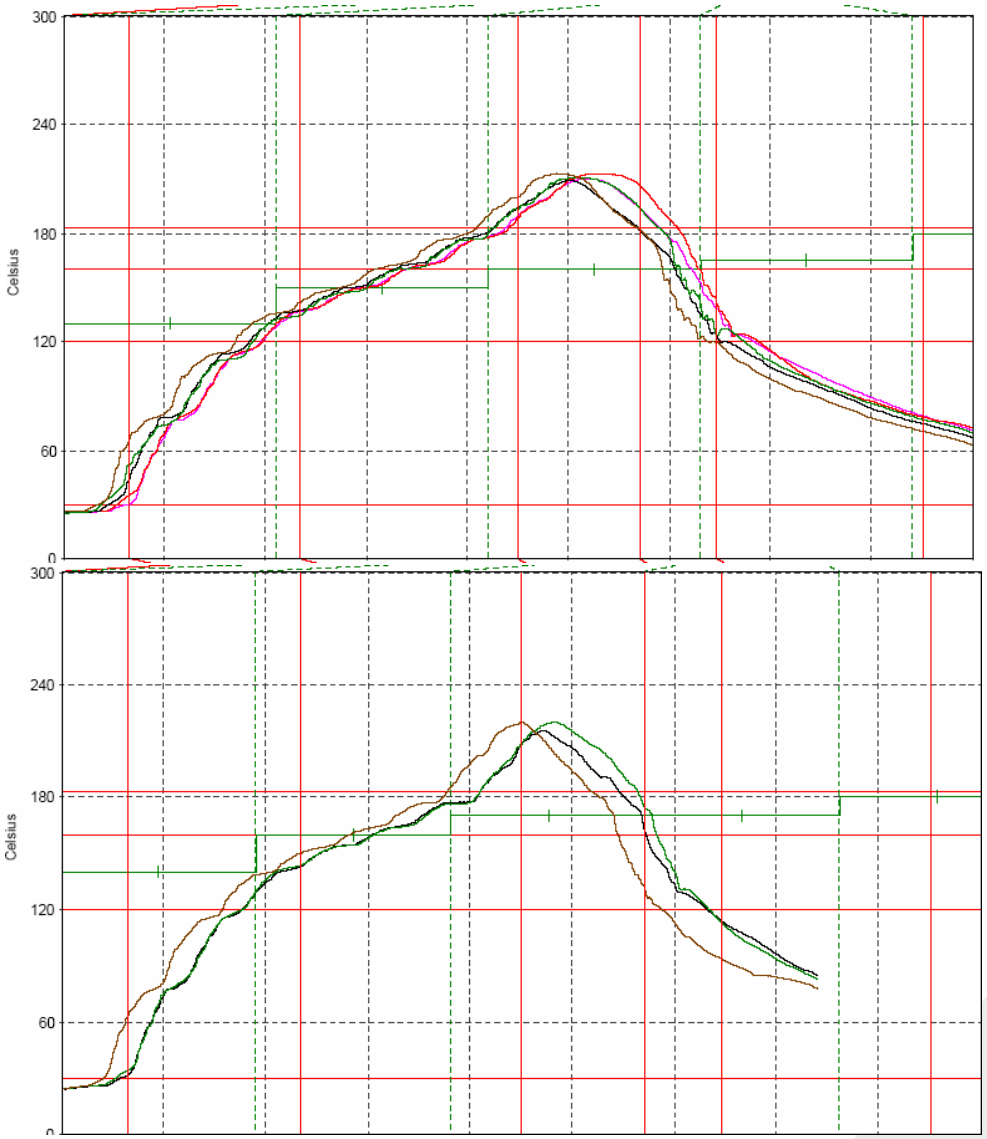
Part Number:720-00388;720-00440
Location: Cxx

Many Chip Capacitor is de-wetting
From Aug 29 to Sep 21,total 38 parts with joints defect on 1581 boards.

Root Cause Analyze :

These two parts are lead free component, original oven profile can not meet lead free requirement.

Example: AOI feedback to SMT process



Original Over Profile

	Peak	Max Rising Slope	Max Falling slope	Rising time betwe en 30/120	Rising time betwe en 120/16 0	Total time above
CB27B	210.6	1.04	-0.97	64.38	68.92	73.38
CB49B	213.1	1.03	-1.05	69.06	67.86	80.17
CR570 B	213.3	1.03	-1.04	65.78	67.32	76.2
Point4	215.5	1.17	-1.09	58.03	60.9	65.37
Point5	220.1	1.16	-1.2	60.14	61.77	74.18
Point6	220.1	1.17	-1.24	55.92	59.54	67.93

Updated Over Profile

Example: AOI feedback to SMT process

Actions : Enhance the temperature of Zone 1,Zone 7, Zone 8, so that the Temperature of the Peak is higher than before, and reflow time (above 183 c) is reduced.

Result: From Sep 22 to Oct 12, only 1 joints defect happened on 651 boards

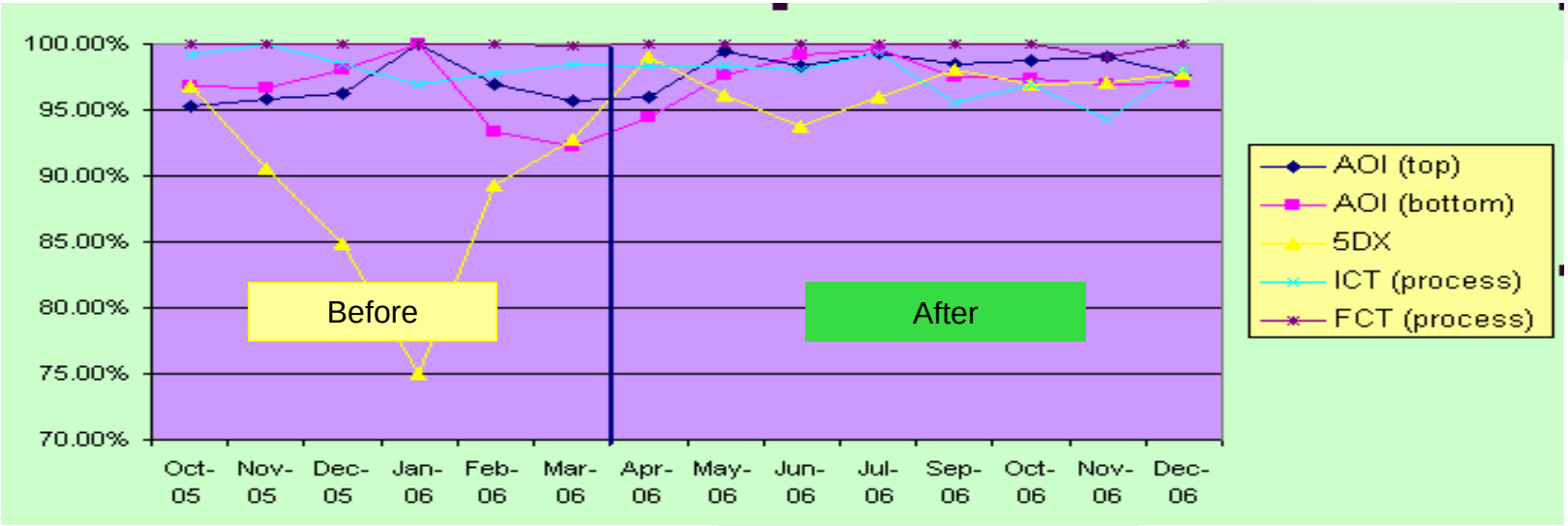
Real-Time Process Defect Feedback Yield Improvements

Example:Resulting Change in Yield at each tester(overall Yield Improvement)

Example: Assembly -C

Month	Volume	AOI (top)	AOI (bottom)	5DX	ICT (process)	FCT (process)
Oct-05	62	95.3%	96.8%	96.8%	99.2%	100%
Nov-05	158	95.9%	96.6%	90.5%	100%	100%
Dec-05	236	96.2%	98.0%	84.8%	98.5%	100%
Jan-06	12	100.0%	100.0%	75.0%	97.0%	100.0%
Feb-06	527	96.9%	93.3%	89.3%	97.8%	100.0%
Mar-06	264	95.7%	92.2%	92.8%	98.5%	99.9%
Initial (Average)	**1259**	**96.3%**	**94.6%**	**89.6%**	**98.4%**	**100.0%**

Month	Volume	AOI (top)	AOI (bottom)	5DX	ICT (process)	FCT (process)
Apr-06	191	96.0%	94.5%	99.0%	98.3%	100.0%
May-06	207	99.5%	97.6%	96.1%	98.3%	100.0%
Jun-06	364	98.3%	99.1%	93.7%	98.0%	100.0%
Jul-06	516	99.3%	99.6%	96.0%	99.3%	100.0%
Aug-06	0	0	0	0	0	0
Sep-06	205	98.5%	97.5%	98.1%	95.6%	100%
Oct-06	166	98.7%	97.4%	97.0%	96.9%	100%
Nov-06	523	99.0%	97.0%	97.1%	94.3%	99%
Dec-06	431	97.6%	97.1%	97.8%	98.1%	100%
After (Average)	**2603**	**98.5%**	**97.7%**	**96.7%**	**97.3%**	**99.8%**



Production Cost Savings due to Machine Usage Reductions

Progress - Machine cost Saving (US$)

Total saving is $**31,743.58** from April to December, 2006.

Monthly Saving $	April	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec	Sum
Assembly-A	200.72	93.31	156.01	65.61	212.38	164.27	209.95	196.34	243	1541.59
Assembly-B	1241.14			15.79	611.39	692.17	284.58	0	642.6	4875.2
Assembly-C				8.86	0	174.35	141.18	444.81	366.57	2213.85
Assembly-D	2			.28	623.61	410.67	345.15	246.78	281.97	2871.09
Assembly-E	24			21	336.96	341.64	54.44	878.67	530.01	2812.68
Assembly-H	40			13.12	7.94					138.84
Assembly-I	145.00	242.81	126.68	20						1585.84
Assembly-J	12.78								69.89	523.81
Assembly-F	1043.08						.13	0	0	4094.57
Assembly-K	531.63		332.9	2.2	57	667.95	151.17	1080.49	608.85	4256.01
Assembly-L	1019.70	272.70	630.90	301.50	47.00	947.70	279	1708.2	923.4	6830.1
Total	4895.76	2560.96	3379.14	2470.63	3615.78	4532.57	1786.74	4810.92	3691.08	**31743.58**

Save $31,743 within 9 months

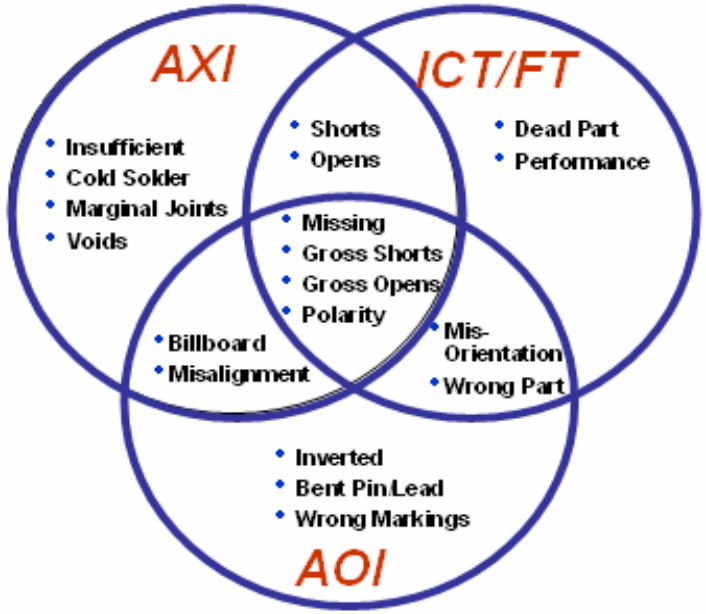
1. The 5DX will be considered as 5 years depreciation.
2. Use 28day*22hours*0.85 hours per month

Note: 85% is the efficiency rate of the 5DX; taking into account downtime due to machine calibration time, idleness due to shift-change, etc….

Conclusion

AOI & AXI are more efficient complementing each other, so as to can identify virtually all defects before electronic test. By balancing the coverage between AOI & AXI, the AXI cycle time can be noticeably reduced eliminating AXI as a bottle-neck. This will also reduce the “waste” to achieve FMS (lean) concept and there is a significant cost savings.

AOI & AXI are test tools, and they can also be used as SMT process improvement tools if their test results are properly analyzed and fed back to upstream processes.



We suggest using 100% AXI coverage for new products especially when new package types are used. It is necessary to review all test yields and data to confirm a stable SMT process before reducing AXI test coverage.

Acknowledgement

The Flextronics engineering and production teams at Shanghai, China

Wei Bing Qian
Allen Wei
Winde Wang
Angery Lee
Andrew Ho
Jane Phan
Sam-TS Wong
Heidi Hanson
Jack Shen
Wendy Zhang
Yuanyuan Peng
Teddy Zai
EB Yeoh
Gary Liu
Barbara Koczera

Thank you!