BGA Breakout Challenges

Charles Pfeil
Mentor Graphics

Abstract
The routing of large pin-count and dense BGAs has a significant impact on the cost of the PCB, primarily in terms of layer count and via technology. This paper is the result of considerable research done with the intent of providing a general flow solution to the BGA breakout problem. It explores the need for collaboration between chip, package and PCB designers - emphasizing the dependencies that need to be managed to reduce board costs. The number of variables confronted in large BGA routing is significant and this paper reveals solutions based on a logical analysis of ASIC and FPGA BGA pin density, array patterns, packaging requirements, pin swap constraints, layers, via technology, topology planning and routing methods.

Introduction
Using a BGA is the most common method today for packaging a high pin-count or very dense ASICs and FPGAs. BGAs have been proven to be a reliable, cost effective package while at the same time providing flexibility to address miniaturization and functional requirements. However, the increasing pin-count and decreasing pin-pitch creates a significant problem for PCB designers who must minimize layer count (to reduce fabrication costs) and fulfill signal integrity requirements (to meet the high performance goals). Most PCB designers who are using leading edge BGAs claim that the breakout of the device is the greatest contributor to the number of PCB layers. The term "BGA Breakout" means applying a fanout solution and routing traces from those fanouts to the perimeter of the device prior to general routing of the PCB. Low pin-count devices (less than 500 pins), even with a pin-pitch of less than .8mm, do not present a significant breakout problem and are usually routed without a "breakout" method.

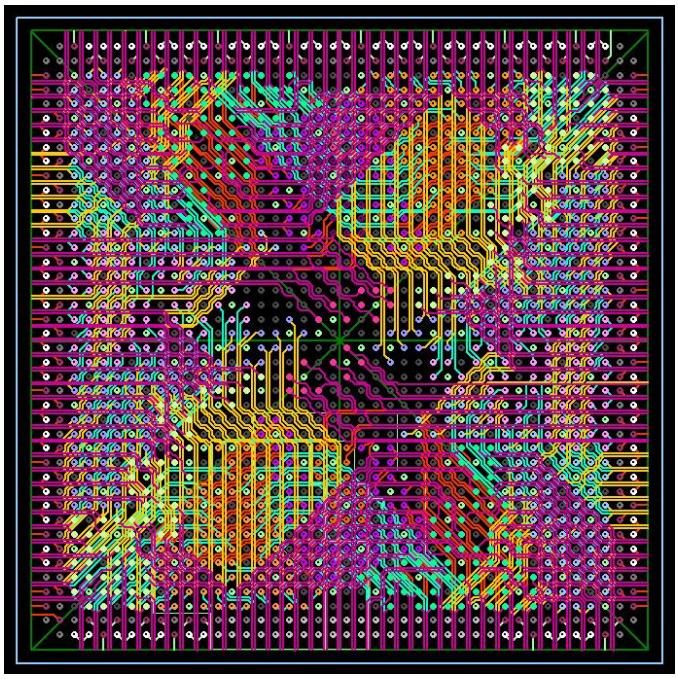


Figure 1 – Example of a BGA Breakout

The BGA breakout challenge starts with over 1000 pins and 1mm pin-pitch. The largest FPGA in production today is the Xilinx Virtex-4 and Virtex-5 FF1760 series with 1760 pins and a 1mm pin-pitch. The future will bring over 2000 pins and a 0.8mm pin-pitch.

During the past year, I have worked with a team at Mentor Graphics Corporation to research the existing methods for routing large BGAs with the intent of finding both interactive and automatic routing solutions for the short-term and long-term. The methods presented in this paper address the 1760 pin / 1mm pitch devices well and touch upon methods for the future devices.

Reality Strikes
My initial research on the subject of BGA breakouts took me into the realm of theoretical solutions. It wasn't long before it became apparent that most of the theory in this area breaks down when confronted with the reality of attaining reasonable manufacturing costs and fulfilling the signal integrity requirements.

There are numerous papers offering mathematical solutions to high pin-count devices in which the minimum number of layers can be calculated and various patterns for the traces are shown. Unfortunately, these proposals do not account for the impact of power and ground pins, the distribution FPGA banks in various arrangements (with the requirement that all signals in the bank need to have the same reference plane), reasonable design rules to reduce crosstalk, and nets that should be routed as differential pairs - or worse yet, nets that can be routed either as single-ended or differential pairs depending on the performance goals of the circuit.

Along with mathematical solutions, there are a plethora of proposals for spacing aligning fanout vias. While it is true that the fanout method is the key to a successful breakout; it is not true that any one method can be applied to all situations especially when the stackup and via models are usually chosen on a fabrication cost basis.

Compromise
The art of engineering is to appropriately compromise the myriad of variables and still have the project fulfill the time, cost and performance goals. In the context of BGA breakouts, there are indeed a myriad of variables; however, these are the ones that have the greatest impact on cost and performance:

- Layer Stackup
- Via Models
- Design Rules
- Signal Integrity

By making initial decisions in these areas, the task of finding a breakout solution becomes feasible as opposed to overwhelming. For purposes of this paper, I have chosen a specific set of values for these variables that work well together for large pin-count BGAs.

Stackup and Via Models
Your choice of stackup and via models will have the greatest impact on reducing layer count.

		1mm pin-pitch						
Stackup	**Via Model**	**0-300**	**300-500**	**500-1000**	**1000-1760**	**1760-2000**	**>2000**	**Pins**
Laminated	Thru	OK	OK	OK	marginal	unlikely	no way	
Laminated	Blind & Buried	OK	OK	OK	OK	marginal	unlikely	
Buildup	Thru	OK	OK	OK	marginal	unlikely	no way	
Buildup	Micro	OK	OK	OK	OK	OK	OK	
Buildup	Buried	OK	OK	OK	OK	OK	OK	
		< 1mm pin-pitch						
Stackup	**Via Model**	**0-300**	**300-500**	**500-1000**	**1000-1760**	**1760-2000**	**>2000**	**Pins**
Laminated	Thru	marginal	unlikely	no way	no way	no way	no way	
Laminated	Blind & Buried	marginal	marginal	unlikely	unlikely	no way	no way	
Buildup	Thru	marginal	marginal	unlikely	unlikely	no way	no way	
Buildup	Micro	OK	OK	OK	OK	OK	OK	
Buildup	Buried	OK	OK	OK	OK	OK	OK	

Figure 2 – Stackup and Via Model Use

Of course there will be exceptions to my recommendations in Figure 2 and the data in the chart should be considered as guidelines. What happens if you try to use a borderline via model and stackup? You will have to compromise design rules (smaller feature sizes and clearances) resulting in lower fabrication yields and potential crosstalk problems.

Laminated Versus Buildup – Buildup technology, also known as High Density Interconnect (HDI), has taken over the handheld industry and is the preferred stackup for all PCBs in the PAC Rim. However, it still lags behind FR-4 laminated in the US and Europe for computer, network and larger designs in general. High pin-count and <1mm pin-pitch BGA will force the adoption of HDI for all PCBs. The good news is that HDI is now low cost and for the same pin density actually lower cost than laminated. I highly recommend learning more about HDI and the significant benefit it brings to solving PCB density problems.

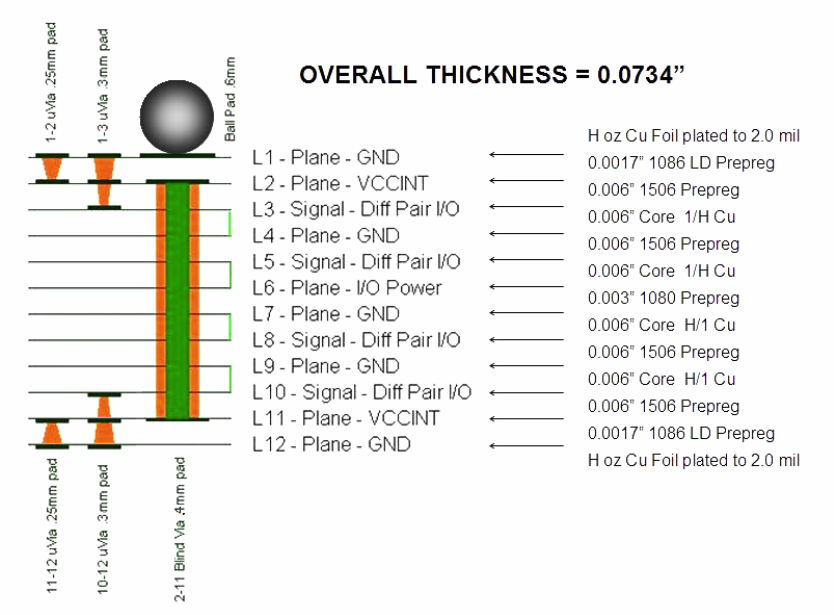


Figure 3 – HDI Stackup

The stackup in Figure 3 is one that worked best with my breakout attempts for the Virtex-4 and Virtex-5 series with 1760 pins. In the world of HDI, this stackup is common and cost effective.

- GND is on the outer layers and each signal layer has a good reference plane next to it. Having the GND on the outer layers also provides excellent control of EMI.
- There are 4 signal layers, which is enough for the breakout. If you want more signal layers, they can be added in the center of the stackup.
- The 11-12 and 10-12 vias are not used for the signal breakouts, but may be used for power and ground if bypass capacitors are needed. Some FPGAs like the Virtex-4 and Virtex-5 series have bypass capacitors in the BGA package, minimizing the need for them on the PCB under the device.
- The signal layers are not paired; rather they are separated by GND planes. The breakout traces on a large BGA usually result in layer-to-layer parallelism. Using GND planes between the layers eliminates the crosstalk potential.

Design Rules

Only two criteria drive design rules; obtaining high fabrication yields (cost) and fulfilling signal integrity requirements (performance). Of course a third could be “what we have done in the past” as a justification to ignore the first two; fortunately, the number of companies wrapped up in that praxis are few.

For signal integrity purposes, it is generally desirable to have 50 ohm traces for single-ended nets and 100 ohm traces for differential pairs. Using the HDI Stackup shown in Figure 3, this can be attained by using the following design rules: (values for English units are rounded off)

- Single-ended – width .13mm (5^{th}), clearance .13mm (5^{th})
- Differential pairs – width .1mm (4^{th}), clearance .15mm (6^{th}), pair to pair clearance .3mm (12^{th})
- Layer 1-2 micro-via pad .25mm (10^{th}) , hole .1mm (4^{th})
- Layer 1-3 micro-via pad .3mm (12^{h}), hole .15mm (6^{th})
- Layer 2-11 buried-via pad .4mm (16^{th}), hole .2mm (8^{th})
- Ball pad .6mm (24^{th})

These design rules are also quite good for low fabrication cost since most PCB fabricators routinely produce boards with .1mm width and clearance.

Depending on the fanout and routing method used, it may be necessary to compromise these design rules inside the BGA. For example, to enable routing from the fanout vias to the perimeter of the device, it may be necessary to for the single-ended routes to have a .1mm width and clearance. The consequence of this compromise is that you will have a small impedance

discontinuity when the trace changes to .13mm – this may or may not be a significant problem in the context of all the other signal integrity effects being managed in the design.

Signal Integrity
While creating the breakouts for the Xilinx Virtex-4 and Virtex-5 series FPGAs, the following signal integrity considerations were made:

- Reference Planes - Common reference plane for all signals in the same bank. This was addressed by routing all the signals in the same bank on the same layer and by providing a good reference plane for each layer.
- Differential Pairs - Routing the pairs as 100 ohm transmission lines, with similar length, appropriate compliment spacing, and sufficient clearance from other differential pairs to minimize crosstalk.
- Single-ended Nets - Routing these nets as 50 ohm transmission lines, and providing sufficient clearance to other traces to minimize crosstalk.
- Buried Via Crosstalk – Some concern has been expressed over the potential for crosstalk between the buried vias in the HDI stackup and that the clearance between them should be more than .1mm. My investigation on this has shown varied opinions and the question won't be resolved until the appropriate simulations are run. One version of the breakout includes increased clearances between the buried vias of different differential pairs. However, this method forces the number of signal layers to be 6 instead of 4 because the fanout vias need to be staggered as opposed to aligned.

Fanout Via Patterns
After setting up the design to properly minimize fabrication costs and manage signal integrity, the fanout via patterns have the most significant effect on the number of layers for the breakout.

Thru-vias - If thru-vias in a laminate structure must be used, then there really is only two options when the pin-pitch is .1mm. Either place the vias in the center between the ball pads or put the via in the pad (which increases the fabrication costs because the via must be filled and the ball pad smoothed prior to assembly).

Micro-vias - Using micro-vias in an HDI stackup is an essential part in reducing layer count. In the context of the Figure 3 stackup, you should maximize the number of breakouts created with the 1-3 via. By doing this, it opens up considerable routing space on the other 3 routing layers because the 1-3 via doesn't exist as shown in Figure 4

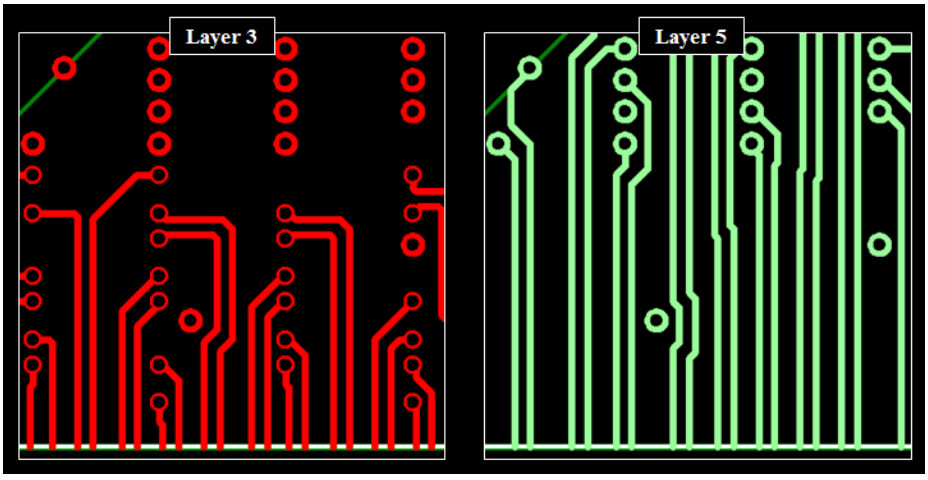


Figure 4 – Use of 1-3 Fanout Vias

If you align the 1-3 fanout vias in a pattern as shown in Figure 5, additional routing space is created compared to just having a matrix of vias on 1mm spacing.

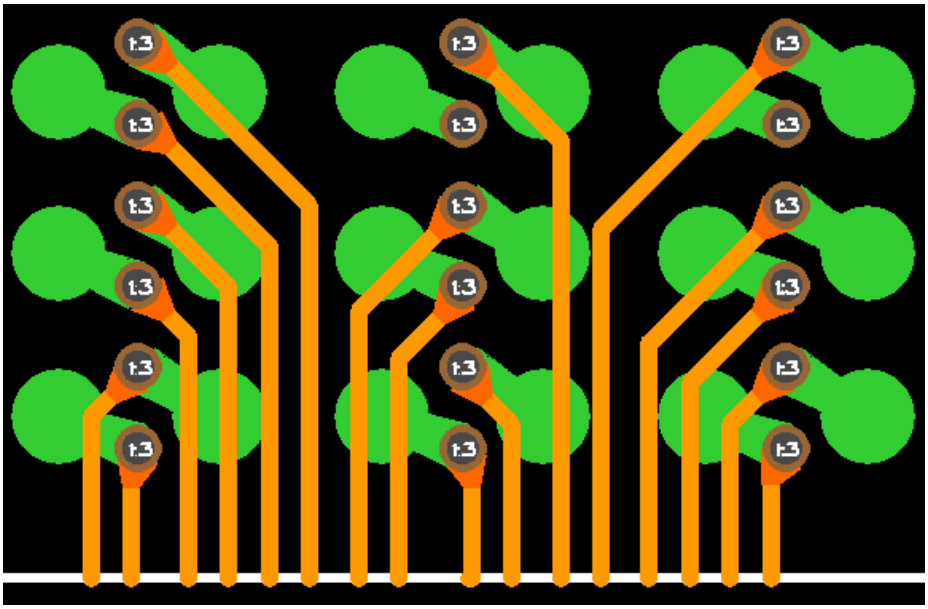


Figure 5 – Layer 3 with 1-3 Fanout Micro-vias Aligned

Micro-vias Plus Buried-vias – To get to the routing layers 5, 8 & 10 it requires the use of a 1-2 fanout micro-via and a layer 2-10 buried-via. Again, a good fanout pattern is needed to maximize the routing space. In Figure 6, an effective pattern is shown.

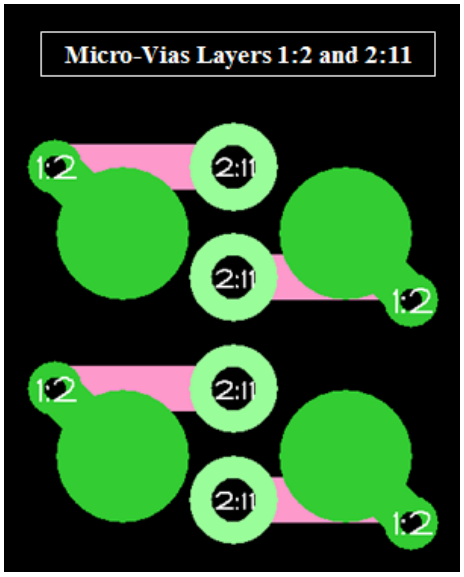


Figure 6 – Micro-vias and Buried-vias

If it is necessary to increase the clearance between the buried-vias to minimize crosstalk between differential pairs, then you can stagger the vias as shown in Figures 7 and 8.

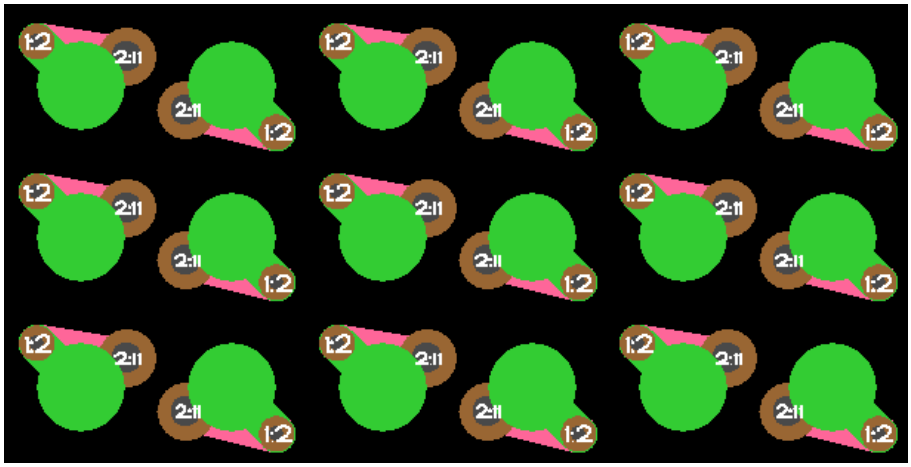


Figure 7 – Staggered Buried-vias

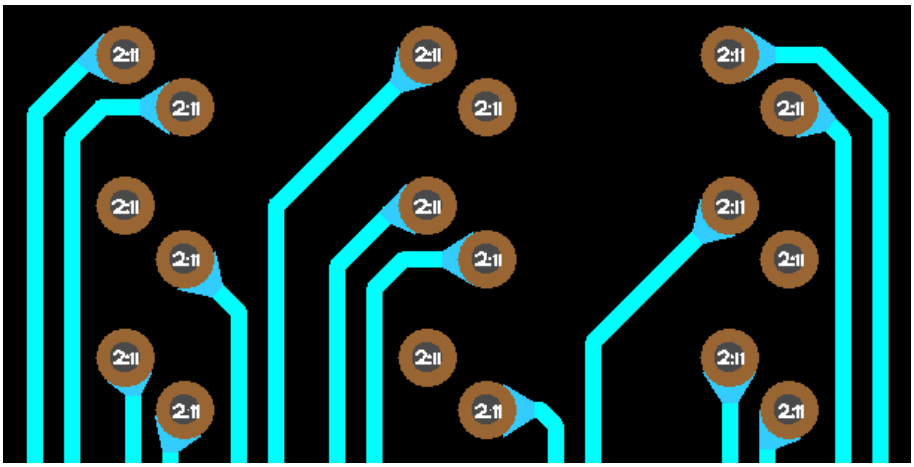


Figure 8 – Staggered Buried-vias Routed

Each large pin-count BGA presents different problems for fanout patterns and because of this, it is likely that a different fanout pattern will be required. The following factors and combinations of them may cause unique fanout patterns to be used:

- Arrangement of power and ground pins. Sometimes they are grouped in the center, other times sprinkled around the device in regular or irregular patterns that could interrupt the ability to use the same fanout pattern for the I/O pins.
- Arrangement of the banks on an FPGA. The banks may be grouped together nicely or sometimes split up. The arrangement of the pins in the bank may or may not be convenient for differential pair routing, especially since the use of aligned or staggered micro-vias and buried-vias tend to warp the nice symmetry that is often provided at the ball pad level as shown in Figure 9.

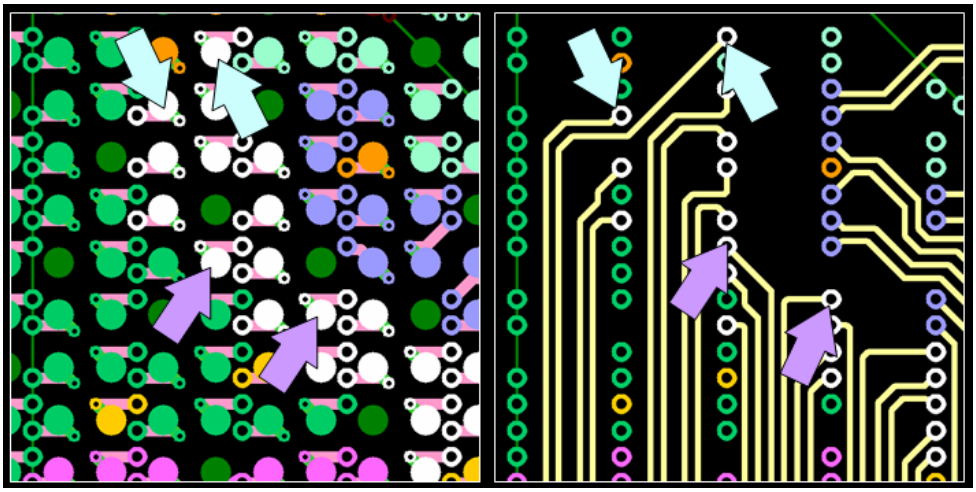


Figure 9 – Contortion of Differential Pairing

- Extremely dense BGAs. In Figure 10, you can see the areas that are easy to breakout (green) and the difficult areas (red). To breakout the red areas using minimum layers on a very dense BGA will require contortion of the fanout via patterns simply because there is so little available space and each area needs to be customized as is the case with any very dense PCB routing. This is illustrated in the alternating via patterns shown in Figures 11 thru 12.

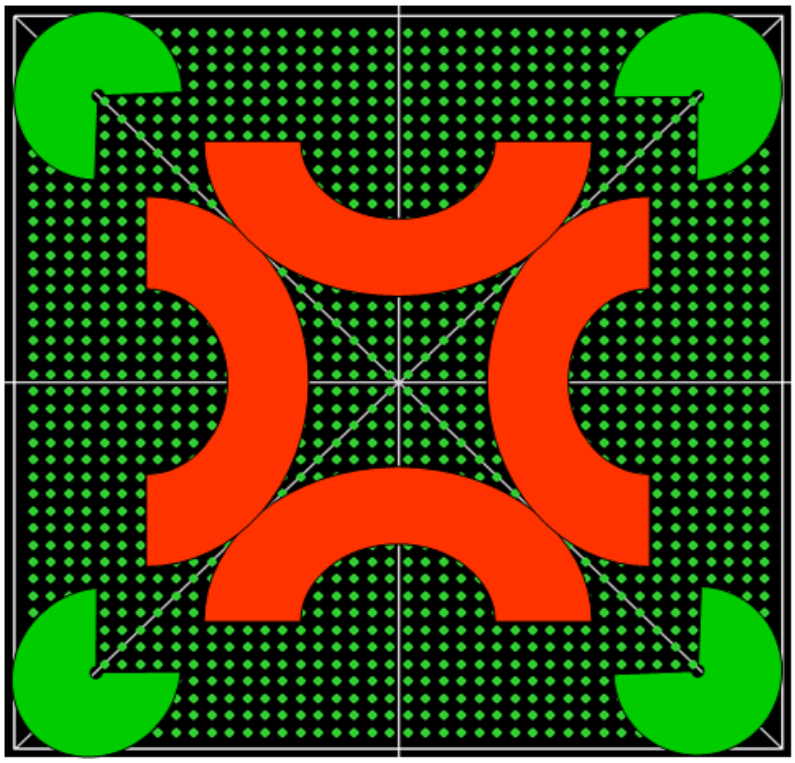


Figure 10 – Red = Difficult, Green = Easy

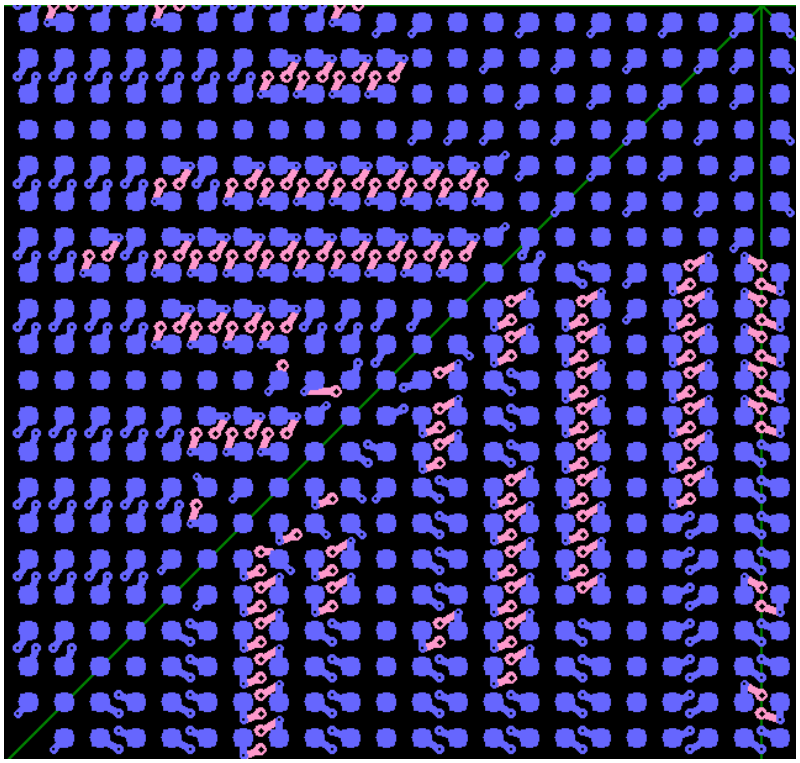


Figure 11 – Alternating Via Patterns, 1-3 versus 1-2 & 2-10

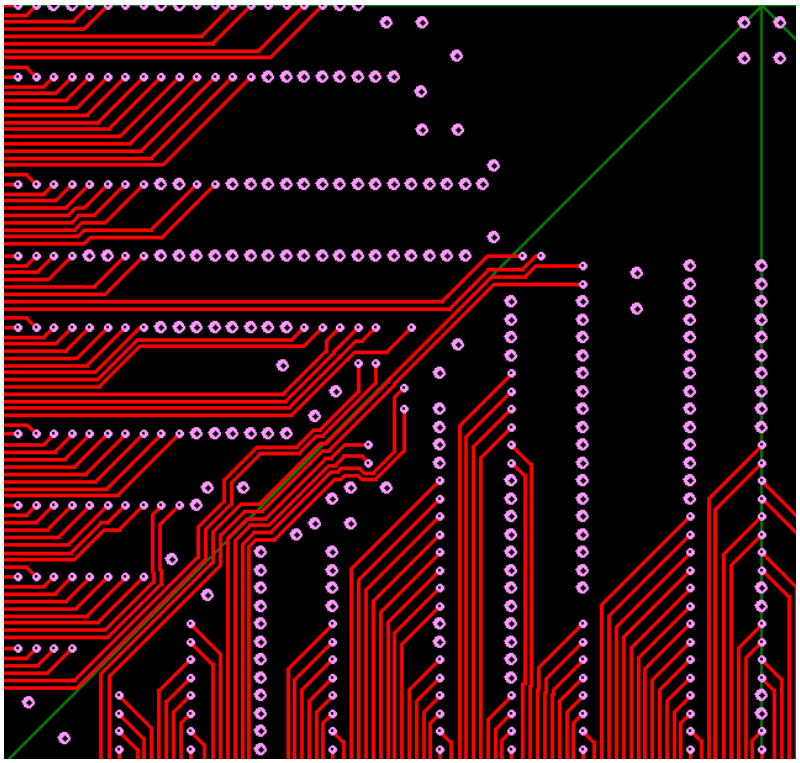


Figure 12 – Routing of First Signal Layer

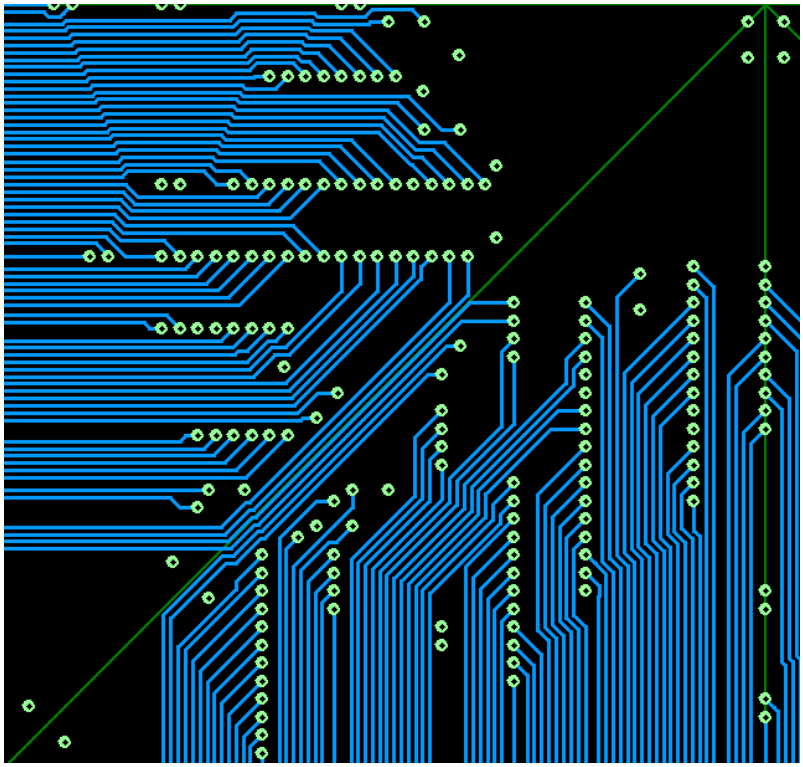


Figure 13 – Routing of Second Signal Layer

The Tipping Point

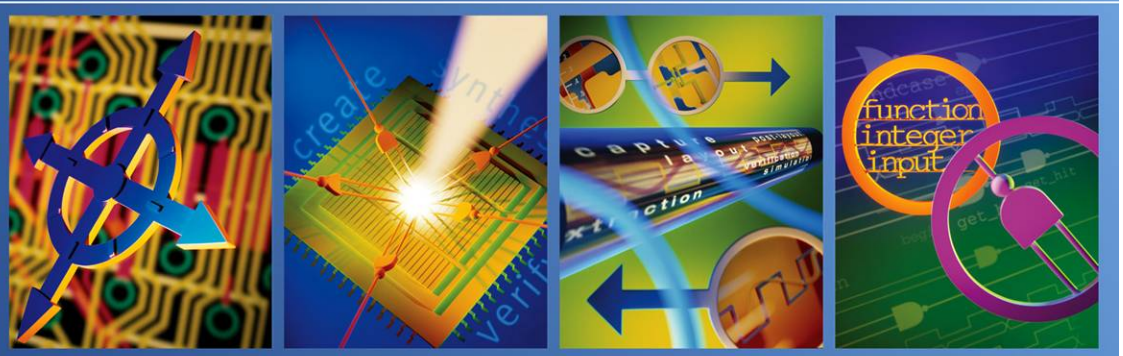
BGAs will continue to grow in pin-count and density. At 1mm pin-pitch it is still feasible to use laminated PCB technology with thru-vias and/or blind and buried vias. However, if you want to minimize layers, using HDI with micro-vias is the best method. Once the BGA packages have more than 2000 pins and a pin-pitch of .8mm, HDI will be required. Now is a good time to get ready for this change.

Conclusion

With the large number of variables involved in the BGA breakout process, for this paper I could only provide a few recommendations in the context of a very specific layer stackup. Yet the principles shown for fanout patterns and the guidance on board fabrication methods should be helpful for any company that has BGA breakout challenges. My research will continue in this area with the goal of driving Mentor Graphics software solutions and a book on the subject that will go into much greater detail to help our PCB design industry get ahead of this advancing technology.

BGA Breakout Challenges

Charles Pfeil
Product Marketing Director
Systems Design Division

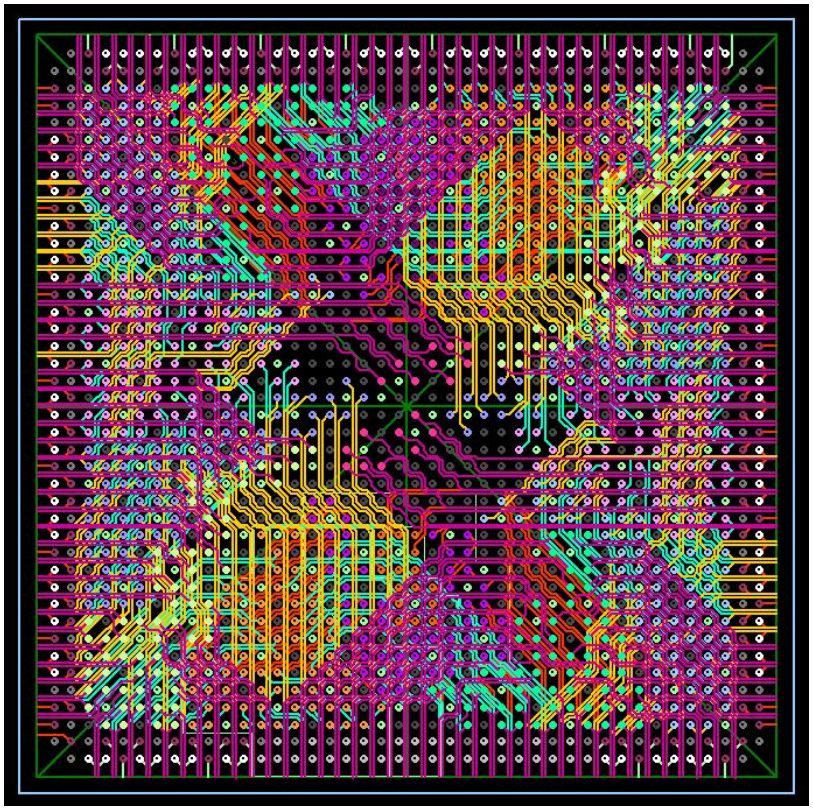


Mentor Graphics

IPC APEX 2007

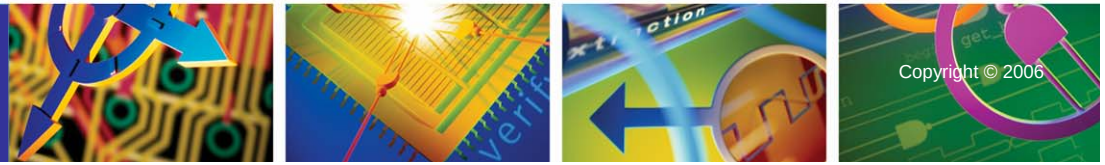
Introduction

- **Routing of BGAs > 1500 pins, 1mm pitch are the primary influence on layer count**
- **Future will bring > 2000 pins, .8mm pitch**
- **Theoretical solutions break down when signal integrity, fabrication cost and pin assignments are considered**

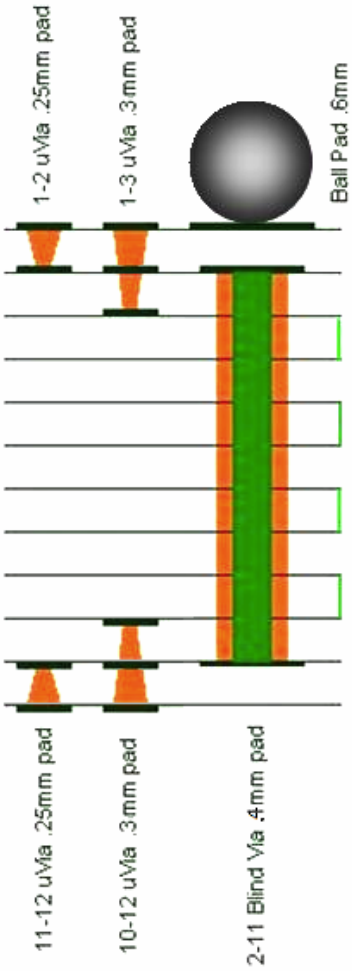


BGA Breakout Variables

- **The art of engineering is to appropriately compromise the myriad of variables and still have the project fulfill the time, cost and performance goals**
- **Many variables**
  - **Layer Stackup**
  - **Via Models**
  - **Design Rules**
  - **Signal Integrity**
- **Worked with Xilinx Virtex-4 & Virtex-5 series with 1760 pins, .1mm pin-pitch**

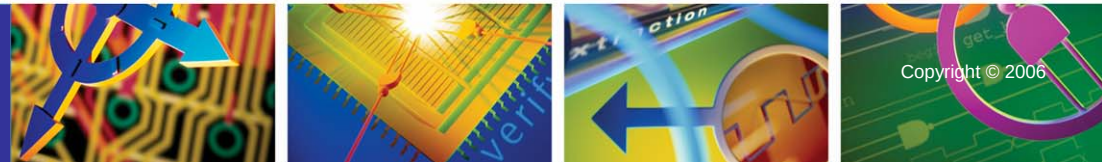


Layer Stackup & Via Models



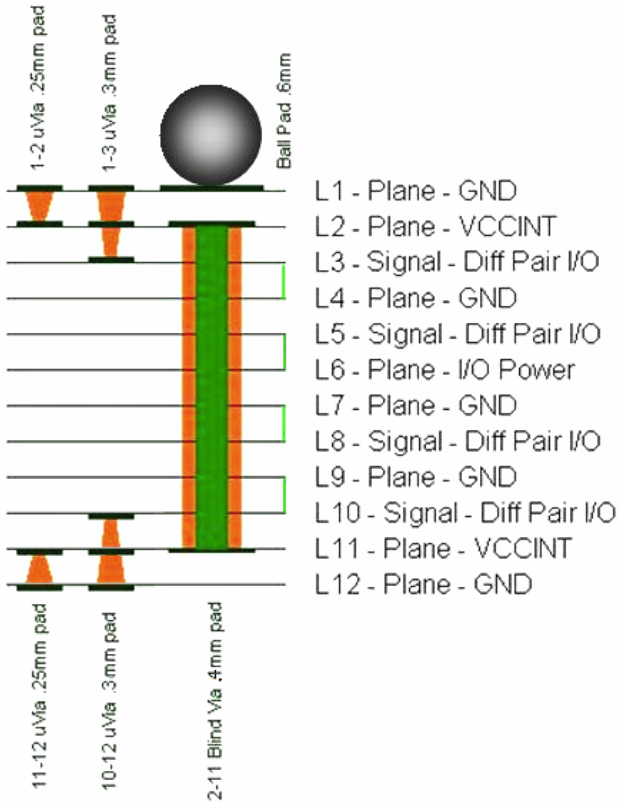
OVERALL THICKNESS = 0.0734”

	H oz Cu Foil plated to 2.0 mil
L1 - Plane - GND	0.0017” 1086 LD Prepreg
L2 - Plane - VCCINT	0.006” 1506 Prepreg
L3 - Signal - Diff Pair I/O	0.006” Core 1/H Cu
L4 - Plane - GND	0.006” 1506 Prepreg
L5 - Signal - Diff Pair I/O	0.006” Core 1/H Cu
L6 - Plane - I/O Power	0.003” 1080 Prepreg
L7 - Plane - GND	0.006” Core H/1 Cu
L8 - Signal - Diff Pair I/O	0.006” 1506 Prepreg
L9 - Plane - GND	0.006” Core H/1 Cu
L10 - Signal - Diff Pair I/O	0.006” 1506 Prepreg
L11 - Plane - VCCINT	0.0017” 1086 LD Prepreg
L12 - Plane - GND	H oz Cu Foil plated to 2.0 mil



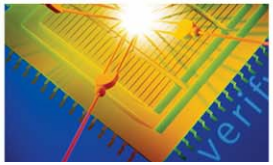
Design Rules

- **Single-ended – 50 ohm**
  - **Width .13mm (5th), space .13mm (5th)**
- **Differential pairs – 100 ohm**
  - **Width .1mm (4th), space .15mm (6th), pair to pair space .3mm (12th)**
- **Layer 1-2 micro-via**
  - **Pad .25mm (10th) , hole .1mm (4th)**
- **Layer 1-3 micro-via**
  - **Pad .3mm (12h), hole .15mm (6th)**
- **Layer 2-11 buried-via**
  - **Pad .4mm (16 th), hole .2mm (8th)**
- **Ball pad .6mm (24 th)**



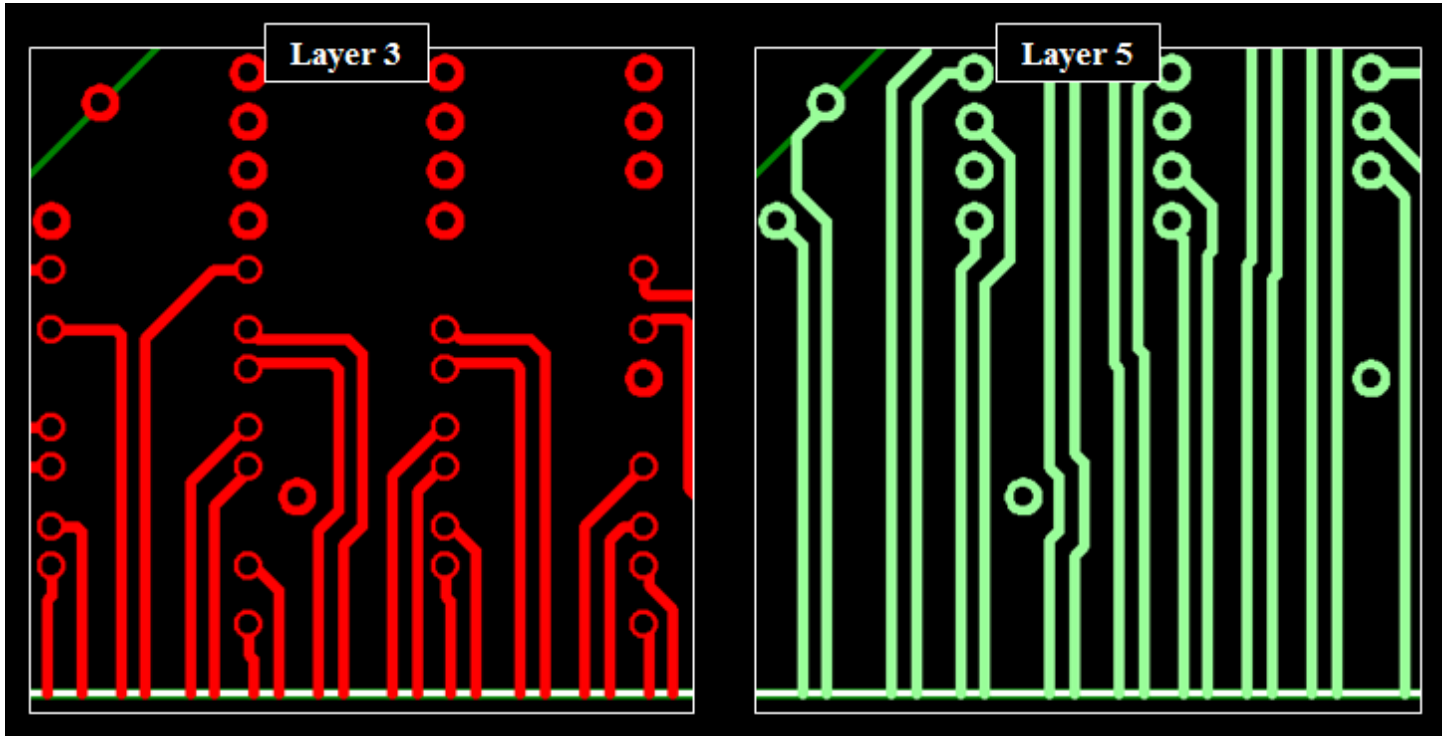
Signal Integrity

- **Reference Planes**
  - **All pins in same bank have same reference plane**
  - **Entire bank has breakouts on same layer**
- **Differential Pairs**
  - **Matched length**
  - **Same reference plane**
  - **Sufficient distance from other differential pairs to minimize crosstalk**
- **Buried Via Crosstalk**
  - **Potential for crosstalk problems**
  - **May require via fanout patterns that are staggered**

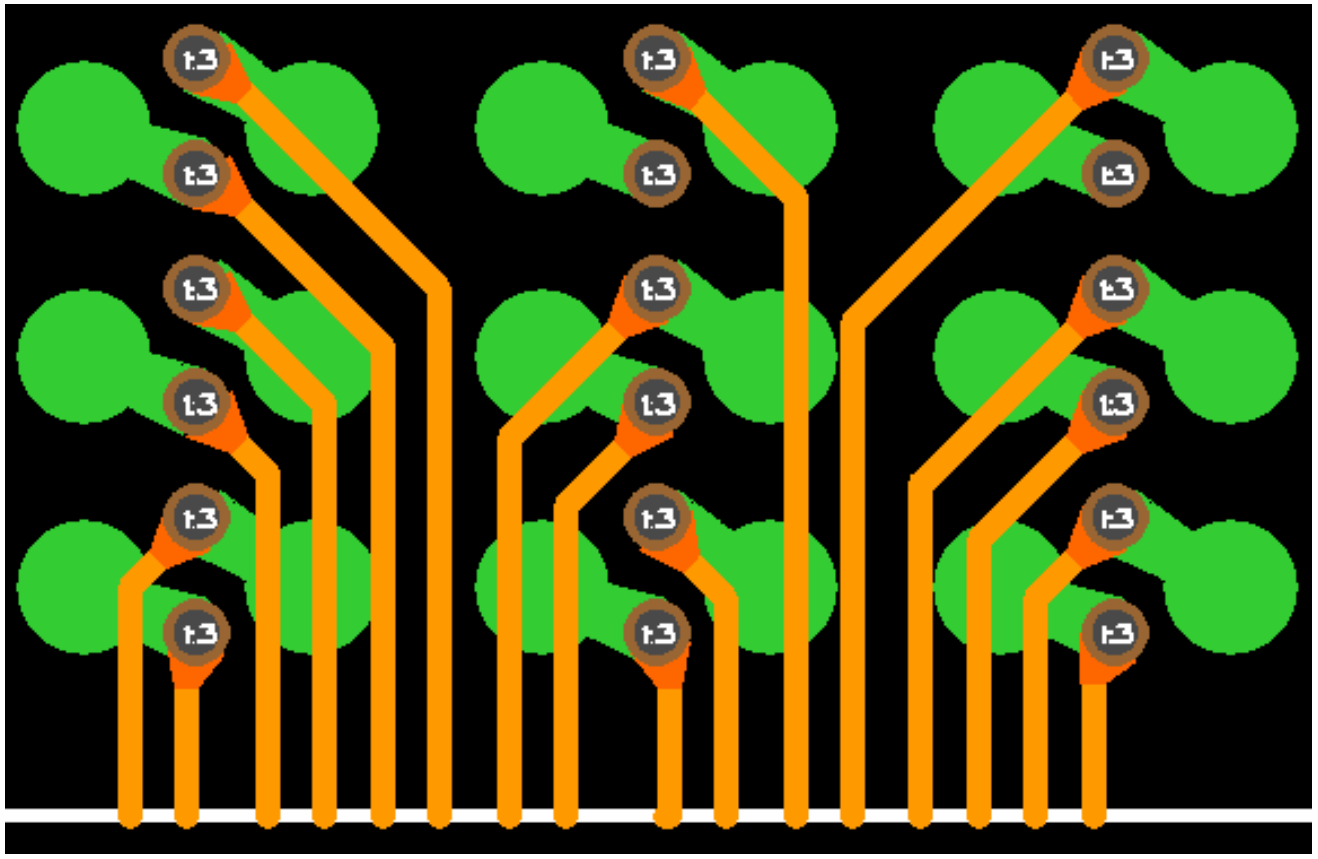
Fanout Via Patterns

- **Very important to minimize layers for breakout**
- **HDI with microvias opens considerable routing space on other layers**



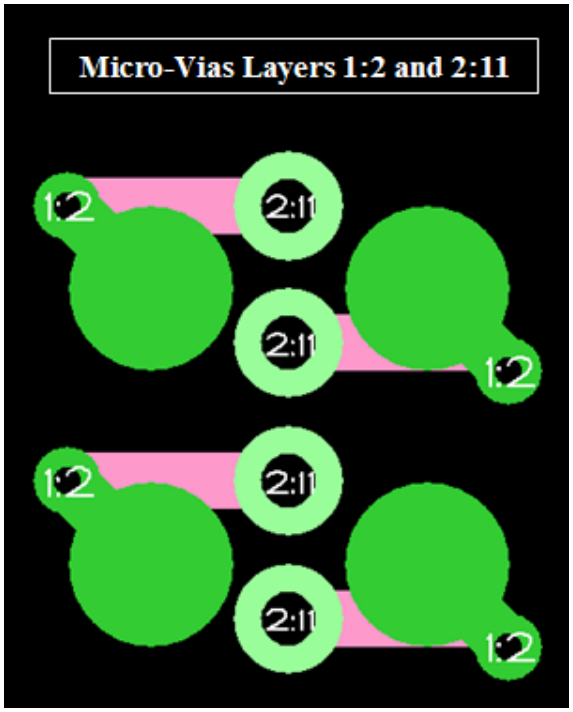
Fanout Via Patterns

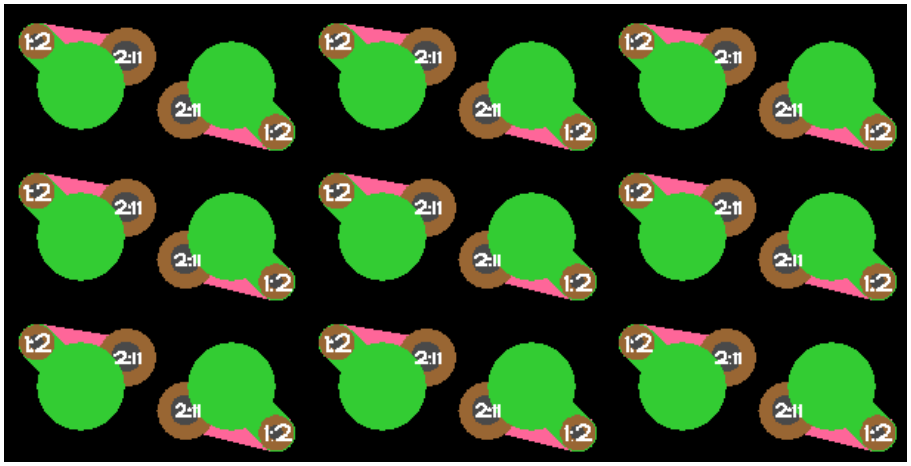
- **Alignment of vias increases space**

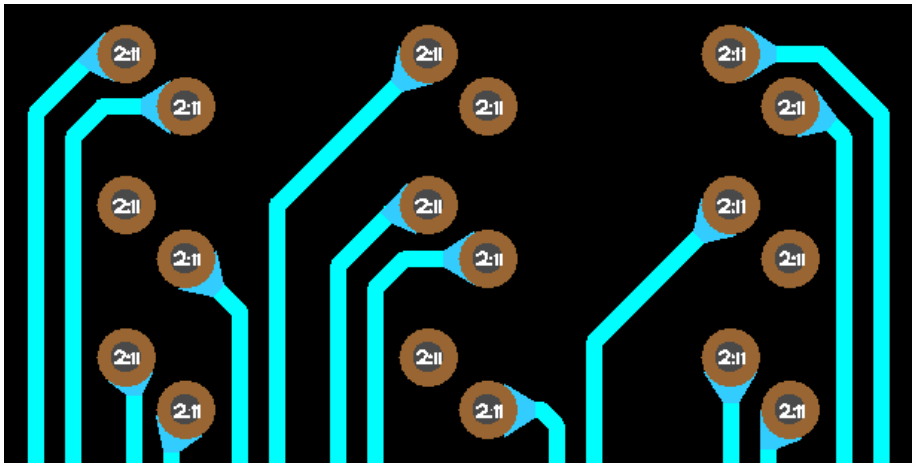


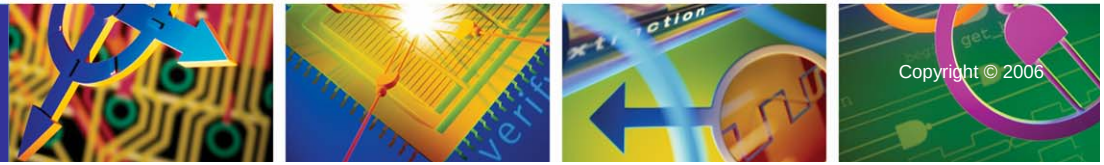
Fanout Via Patterns

- **Many possible via patterns**



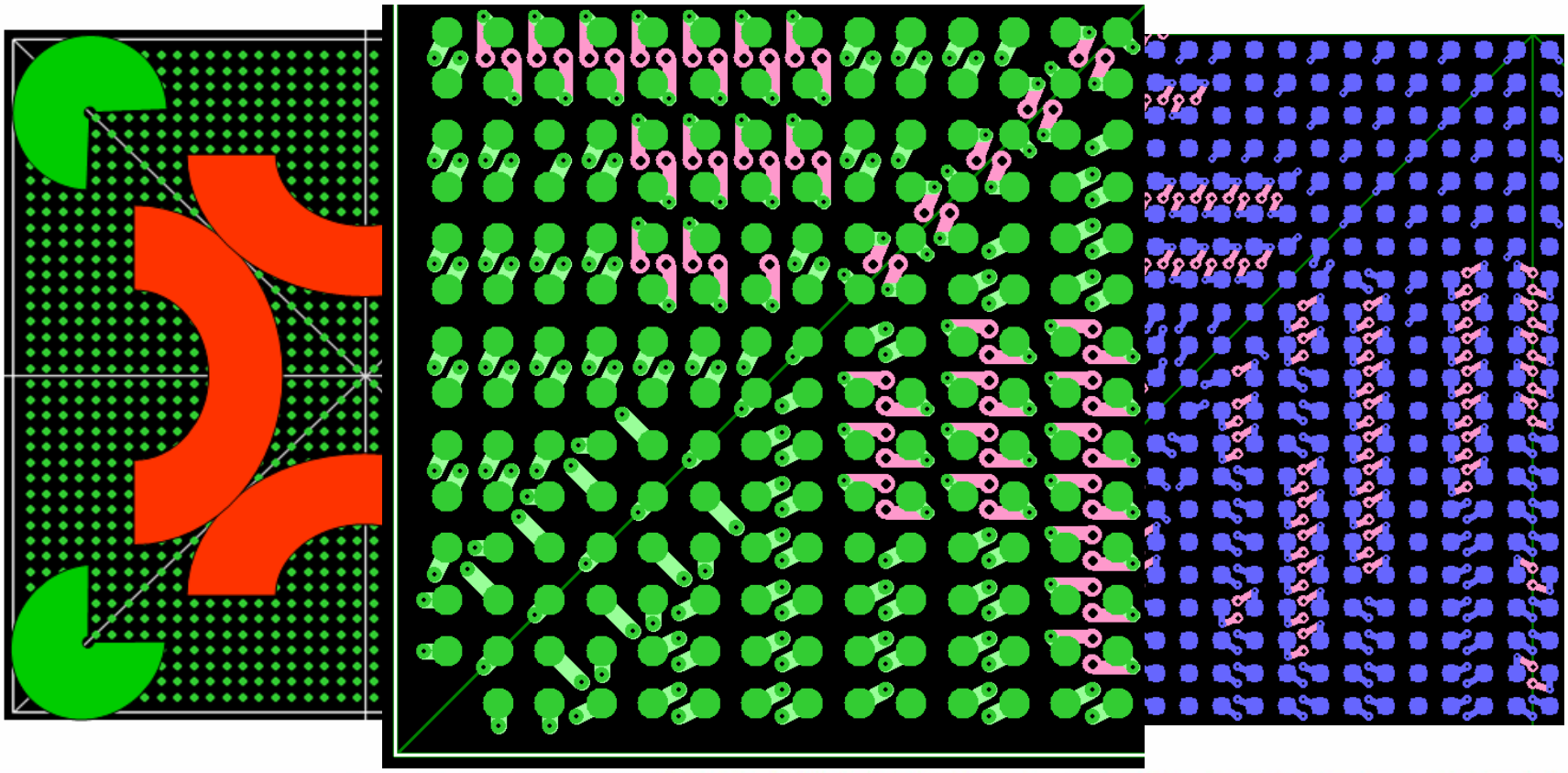






Very Dense BGAs

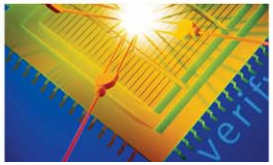
- **Red = Difficult, Green = Easy**
- **Alternating & varied via patterns may be required**



Conclusion

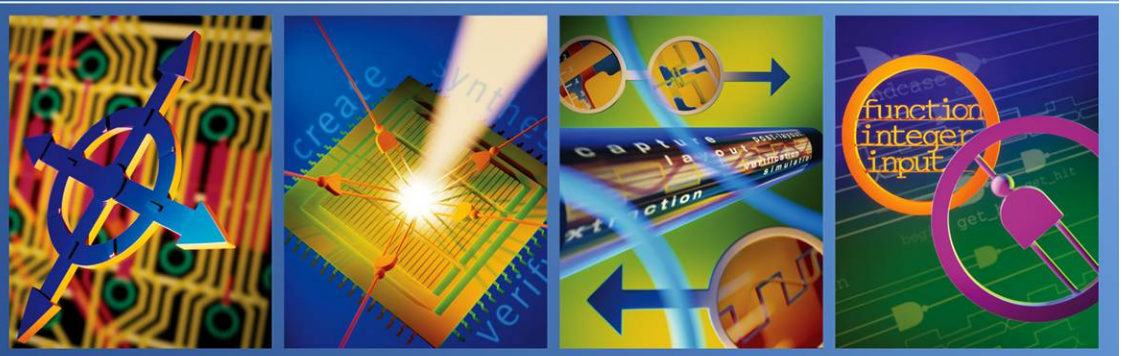
- **Should be able to breakout large dense BGAs in 4-6 layers while managing signal integrity and fabrication cost**
- **>2000 pin and .8mm pin-pitch presents a significant new challenge and will require HDI**
- **Specific methods in my IPC paper**
- **You can contact me for further discussions**

charles_pfeil@mentor.com

BGA Breakout Challenges

Charles Pfeil



Mentor Graphics

IPC APEX 2007