How to use Simulation Kits to Accelerate High-Speed, High-Density Design

Humair Mandavia, Amy Clements
Zuken

Introduction

With design requirements becoming more stringent as implementation of new technology standards evolve, designers are faced with the challenge of front-loading more effort in the design cycle than ever before. The need for simulation in all facets of the product design, whether the Engineer is in the middle of drawing his schematic or a layout designer is in the middle of routing his printed circuit board, has become common.

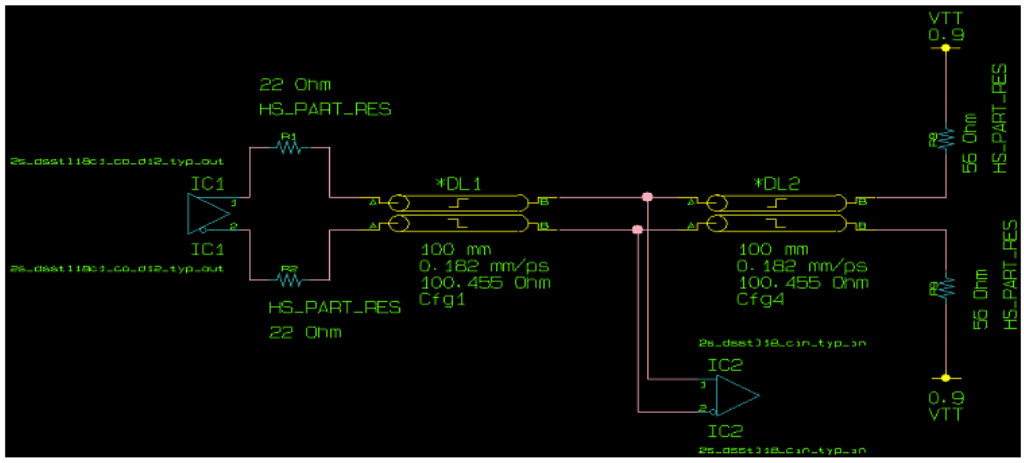
This introduces a new design task where an Engineer has to hunt for device models or does various what-if analyses to test out the termination scheme or to manage DDR2 functionality within their signal integrity tools. Setting up differential pair drivers and testing them versus multiple layer stack-ups based on a chip maker's requirements and takes time and effort, and we all know that in most cases, the "time" aspect is relatively scarce. To help in the effort to enhance predictability and turnaround time, a simulation kit can be used as part of the design process.

Contents of Simulation Kits

Today, a designer will go to a component vendor's website to search for datasheets, and application notes, using the information they have distilled from them to drive their designs. Next is the time-consuming and often trial-and-error process of implementing the recommendations from the datasheets. By using a simulation kit, the designer can design with ready made *scenarios* that represent the recommendations provided by the vendor for signal topology. A scenario is the simulation-ready equivalent circuit of a recommended signal topology. Scenarios make assumptions about proposed layer stack and route lengths that engineers can easily alter to refine their model – this process means the simulation results obtained even before design start become directly comparable with those from final verification of the routed design. For example, the scenario below (part of a Zuken simulation kit) represents a differential 1.8V SSTL signal from a large FPGA.

01_StratixII_DSSTL18_C1_Flyby_PtToPt

1.8V Differential SSTL Class I point-to-point with flyby termination
(12mA differential drivers modeled for simulation)



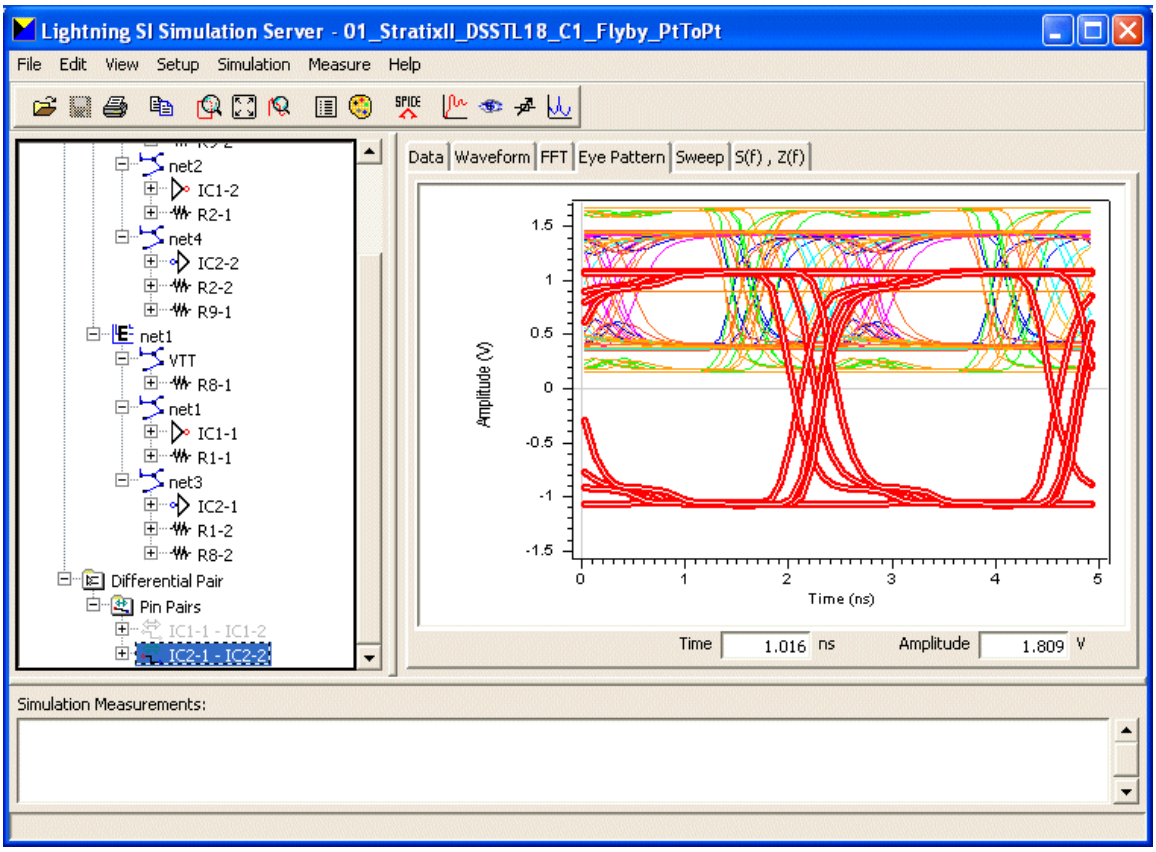
Points to Note:

1. Terminating resistors to VTT should match odd-mode characteristic impedance as closely as possible.
2. Connections between series terminating resistors and driver pins should be as short as possible.
3. Characteristic impedance displayed next to differential transmission lines is the differential-mode value (double the odd-mode value).

Scenario representing a Differential 1.8V SSTL Class I topology

Simulation kits also contain topology templates that can be applied to relevant signals within the design to ensure that tested connection orders are obeyed during physical design.

Vendors can also specify various stack-up strategies with trace characterization to compliment any termination components with regards to impedance control, and these can be defined in simulation kits. Commonly-needed stimulus patterns can be provided for the technology being implemented, allowing easy eye diagram generation such as that obtained for the differential 1.8V SSTL Class I scenario.



Eye diagram obtained for the 1.8V Differential Class I SSTL signal

All this is then linked with device models (ex: IBIS models) and then tested with simulation. Most of the information provided in Simulation Kits can be used right away for analysis, saving the time typically spent entering model libraries, scenarios (equivalent circuits), etc just to get started with the signal integrity aspect of the design flow.

How to Use Simulation Kits

After you download the simulation kit provided for the vendor device or signaling technology within the respective signal integrity tool, it is time to take advantage of all the pre-defined information.

Proposed topologies and layer stacks can be modeled even before design entry. For instance, the differential pair topology illustrated earlier can be edited to modify any assumptions that need to change. In the design being considered here, the main differential pair routing will be on an inner layer rather than the outer layer used in the scenario supplied with the kit.

In the crusade to reduce component count on a design, you can take the recommended termination components and simulate them to decide whether or not those components will be necessary to implement as part of the signal termination. In this case, we are staying with the recommended termination style for SSTL Class I.

The important factor to consider here is to make sure that the stack-up being applied are actually based on design rules that have been approved for manufacturing, and this results into greater accuracy when approaching impedance mismatches.

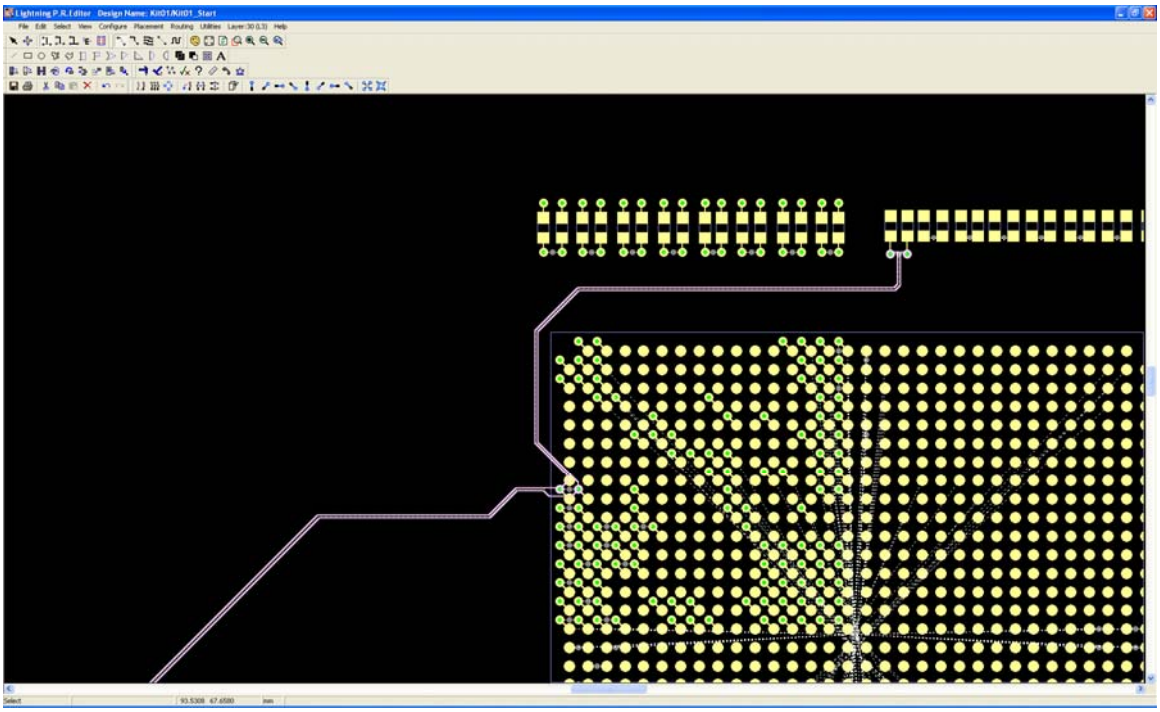
In the case of differential signals implemented to JEDEC standards, proper analysis can be made because the scenario will not only contain the proper termination and transmission line definition, but spacing requirements to insure that effective

coupling is realized. This type of analysis will also incorporate proper IBIS models for driver and receiver pin definition so correct V/I information is utilized against the calculated impedance on a signal so actual reflection can be determined. Once simulation is conducted, a designer can use proper stimuli to generate eye-patterns for differential signals and compare them to eye-mask properties defined in a datasheet.

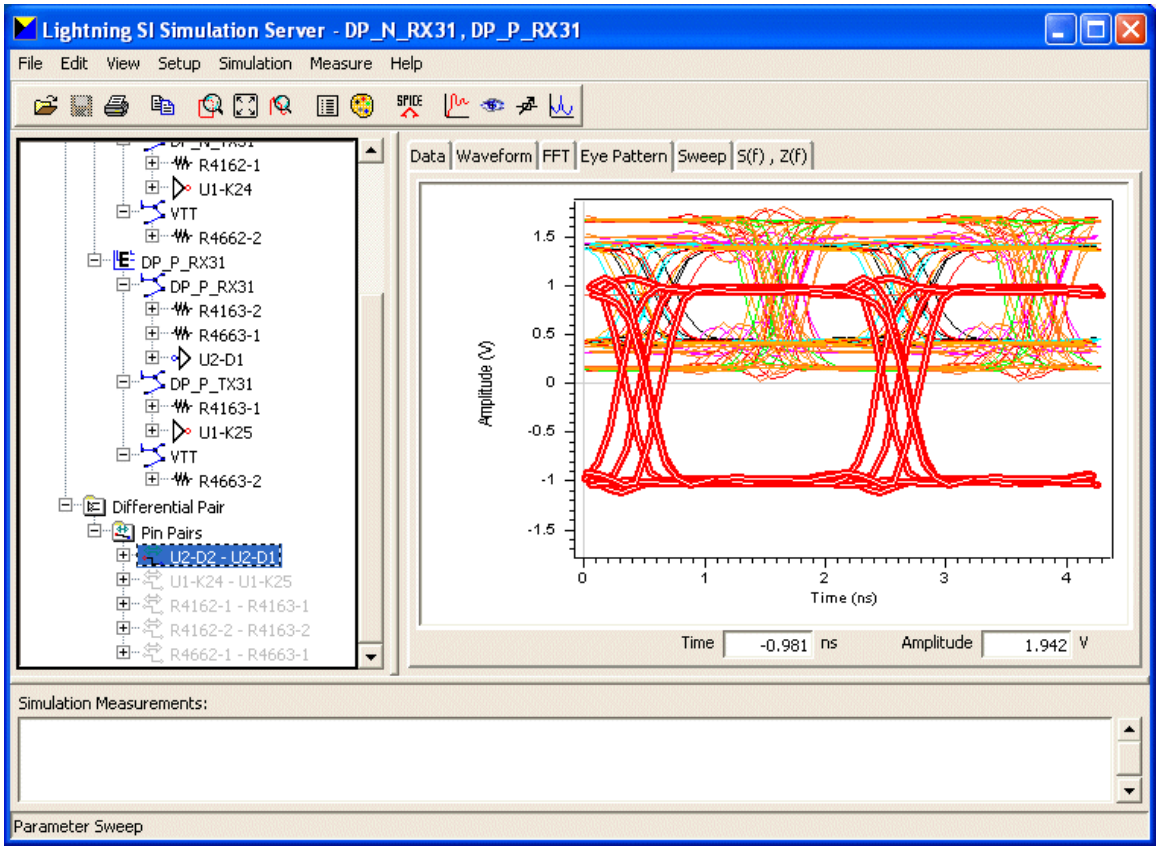
Once it has been determined what signal termination method to move forward with, the topology templates can be modified or used "as is". Topologies can then be simulated for a pre-route analysis or as post-route analysis for verification of implemented topologies. This allows designer to make modifications or adjustments to a design in a seamless manner.

To aid with the routing process, fan-out pattern templates of BGA (also knows as dog-boning or footprinting) can also be defined to ease the process of exit direction on signals. Defining an escape route can be very challenging on a high pin count device such as a BGA, and being able to implement a pattern template can save a great deal of time considering that it is tested to conform to the design requirements with your defined layer stack-up.

Finally, here is part of the routed differential pair and its simulated eye diagram.



The Differential Pair, Routed to SSTL Class I Topology Constraints



Eye diagram for the routed differential pair showing good comparison with the eye diagram simulated in the pre-design scenario

Conclusion

There is a tangible productivity and accuracy benefit in using simulation kits - there is no reason why engineers should need to re-invent pre-design plans and model setup when these can be standardized. The industry has already realized that investment in signal integrity tools pays for itself after just a few reductions in re-spin count of printed circuit boards. Turnaround time can be shortened even more by using simulation kits that include “ready to use” scenarios and templates for the latest signaling standards. Simulation kits also work in conjunction with constraints to manufacturing standards, ensuring that simulation results reflect actual signal behavior after product development.