LOWERING LAYERS w/HDI for RoHS ROBUSTNESS

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ABSTRACT: A perplexing challenge for RoHS compliance is adapting large, complex and thick, high-layer count multilayers to lead-free assembly. These are typically dense, complex assemblies with large BGAs and significant heat spreading features integrated into the design. Fine-pitch packages (QFPs and BGAs) and increasing pin count of packages further complicates the conversion to RoHS.

To provide RoHS robustness to an assembled multilayer that has a very high heat-sinking characteristic requires that the total layers be reduced, as well as its overall thickness. ***But how can this be accomplished?*** The answer is to increase signal routings per layer by 2X to 4X, and thus reduce overall signal layers and their referenced plane layers. The other new design feature is to change 'topology' so that a majority of vias are now 'blind vias', thus freeing up innerlayer space for this to be accomplished.

HDI is the interconnect technology that has been developed to respond to these needs. Microvias are the principal feature of HDI, along with thinner dielectrics and smaller traces and spaces. The important feature is the ***"Design For Lower Layers Using HDI"***. This paper covers the major design solutions from HDI that allows designers to implement fewer layers in a multilayer:

- Reduction in layer count for thickness control and RoHS compliance (Lead-Free Assembly)
- How to integrate high-I/O and fine-pitch devices without adding layers
- How to achieve higher component density and component I/Os without adding layers

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CHALLENGES OF LEAD-FREE

Environmental regulations are placing increased requirements upon printed circuits. The European Reduction of Hazardous Waste (RoHS) and Waste from Electrical and Electronic Equipment (WEEE) directives will significantly affect the requirements placed upon base materials. Among other elements, RoHS restricts the use of lead (Pb). Tin/lead (Sn/Pb) alloys have been used for many, many years in the assembly of printed circuits. Eutectic Sn/Pb has a melting point of 183ºC and temperatures during assembly commonly reach 230ºC. The primary alternatives to Sn/Pb are tin/silver/copper (Sn/Ag/Cu or "SAC") alloys. These alloys have melting points near 217ºC with typical peak assembly temperatures reaching 255-260ºC. This increase in assembly temperature coupled with the possibility of multiple exposures to these temperatures requires the base materials to have improved thermal stability. Recent technical papers have illustrated important data on the effect of Pb-free assembly on base materials [1,2]. While there are many important properties to consider, there are a few that deserve special attention in light of current trends and the resulting need for improved thermal performance. These include:

- The glass transition temperature (T_g),
- Coefficients of thermal expansion (CTEs),
- Decomposition temperature (T_d)

EFFECT ON LAMINATES

As the temperatures to which printed circuits are exposed to increase, as in Pb-free assembly processes, the decomposition temperature (T_d) of the material becomes a much more critical property to understand [4]. The decomposition temperature is a measure of actual chemical and physical degradation of the resin system. This test uses thermogravimetric analysis (TGA), which measures the mass of a sample versus temperature. The decomposition temperature is reported as the temperature at which 5% of the mass of the sample is lost to decomposition. Experience is showing that the decomposition temperature is a critical property, and appears to be at least as important, if not more important than the glass transition temperature when planning for Pb-free assembly conversion. While the definition of the decomposition temperature uses a weight loss value of 5%, it is very important to understand the point at which 2-3% weight loss occurs, or where the onset of decomposition

begins. In assembly processes that can reach peak temperatures of 255ºC to 270ºC, severe levels of degradation can result from multiple exposures to these temperatures.

CONSEQUENCES FOR MULTILAYERS

While the simplest steps to comply with lead-free assembly may be changing the base laminate and replacing the tin-lead finish, this may not be suffiecient for thick, complex, high-layer count multilayers, as seen in **Figure 1**. These multilayers have a much higher thermal mass as well as increased through-hole parts and copper planes. With the possible increased need for rework of complex parts and hand-soldering, the total thermal environment may exceed what any FR-4 is capable of. When this occurs, the remidy is to reduce the thermal mass by reducing the mulitlayer's layers. Five alternative that can be used are:

1. Laser drilled microvias to replace through-holes
2. Layer assignment changes (architectures)
3. Fewer signal layers with higher routing density
4. Thinner materials along with smaller traces
5. Routing BGA using channels

MOVING TO MICROVIAS

Microvias are nearly 25 years old now, having been used in high-volume by OEMs like Hewlett-Packard for their first 32 bit computer-the FOCUS chip- in their 9845 desktop computer starting in 1982. They employed laser drilling of blind vias in a 8-layer PTFE dielectric with copper used as the core layers for cooling., termed "Finstrate" for this feature. Other OEM like IBM and Siemens also developed microvias technologies for their computers but the technology did not really take off until the need for miniturization in portable products like cellular phones.

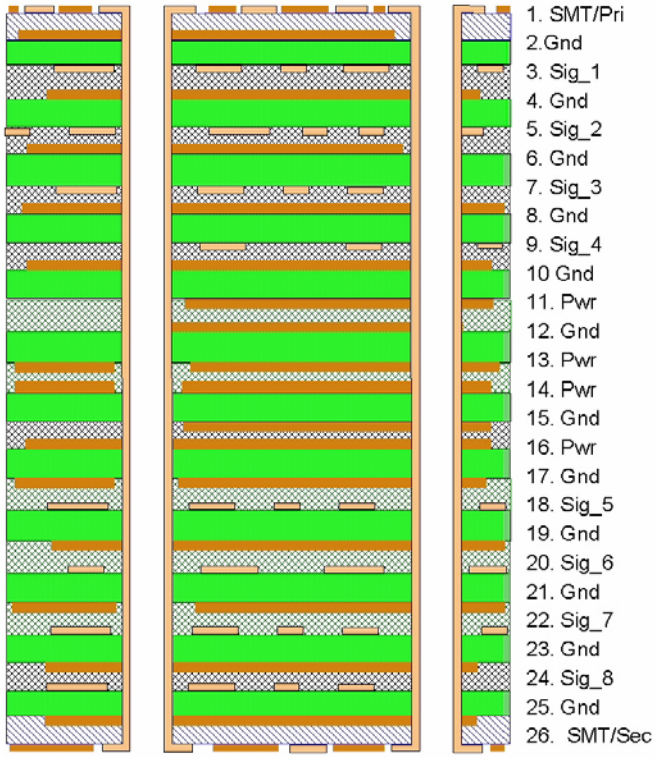


Figure 1 - Large complex, high-layer multilayers such as this used in telecom or computer applications make lead-free assembly very difficult.

Today it [HDI] is the fasting growing segment of interconnect packaging, used in portable products, IC and ASIC packaging and in large complex multilayers for telecom and servers, as seen in **Figure 2**. **Figure 3** shows the rapid growth of microvias for mobile phones during the late 90's, especially in the larger more complex base station boards in the middle 2000s. It is these complex multilayers that this paper is adressing.

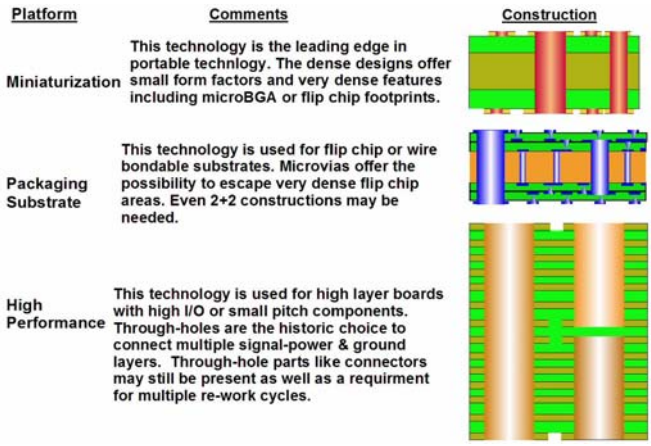


Figure 2 - The three main platforms for microvia applications: portable-miniturized products, IC/ASIC packaging and high-performance multilayers.

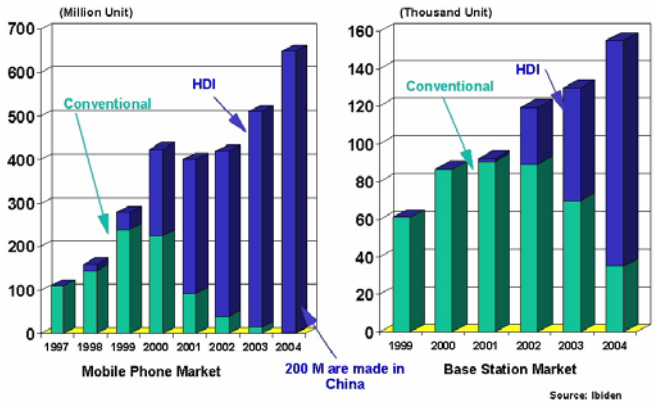


Figure 3: The rapid increased use of microvias has been fuelled by the popularity of cellular phones and the need to make them as small and as light as possible. Now all products are using microvias.

MULTILAYER LAYER ASSIGNMENT

Blind microvias are a surface feature. In order to help reduce the number of layers of a traditional multilayer with microvias, more work needs to be performed on the surface three layers of each side of the board. What this looks like is illustrated in **Figure 4**.

First priority is to reduce and elliminate through-vias. These block routing channels on the innerlayers. By eliminating 25% of the TH, 2X to 3X as many traces can be routed on the innerlayers. One way to do this is to move the ground-plane (that is usually on layer 2) to the surface and use the microvias as via-in-pad (VIP) or near-via-in-pad (NVIP). This eliminates the most abundant vias on the boards- the ones to ground. In none critical areas, this surface ground pour can be connected to other ground layers. The second most abundant vias are to power, so by moving this plane to layer 2, a blind via can connect SMT pads to this plane and not be very deep. Signals will start on layer 3, depending on line-width, these skip-vias will not be very deep and will have a conventional aspect ratio and land size.

If higher wiring density is required, then layer 2 and 3 should be signals. If fine lines are used (~3 mil), then skip vias will allow X-Y connections, otherwise, buried vias (Type II) or buried microvias (Type III) are required to connect the two signal layers.

The only way blind-vias can contribute to layer reduction is for them to replace through-holes (TH) vias. Since blind-vias exist only on the first three layers of a multilayer, these three layers have to assume a greater role in the multilayer archetecture. We must move from the traditional stackup (as seen in Figure 1) of 'SMT-GND-SIG' to one of the HDI structures seen in **Figure 4**. Whether or not the HDI is Type I, Type II or Type III, by moving GND up to the surface, the most numerous THs on the board are now not required, or at least not in critical routing areas. This can eliminate as many as 30% to 40% of the THs, while improving EMI / RFI emissions and sensitivity.

The second key change is to move the PWR planes from the interior of the board up to layer_2 (and layer_n-1). This allows the thinnest dielectric (for maximum capacitance) and replaces the THs with a shallow blind-via. This eliminates the second most used TH-vias.

Finally, with 40% to 60% fewer TH-vias, we now have the room to increase routing on fewer innerlayers. 2X to 3X increase in trace density is possible. With fewer signal layers, fewer reference planes are required for impedance control. This process is shown in **Figure 5**. The result of this, as in the example, is going from 18_Layers to 10_Layers!

HDI-Microvias provide the opportunity to reduce the number of layers of traditional through-hole boards. Microvias are typically, 5 to 6 mil with 10 to 12 mil pads while TH vias are 13 mils with 24 mil pads. This obvious increase in space is multiplied by the fact that a blind-vias only go from the surface to the second or third layer down. This opens up additional channels on the rest of the innerlayer to route additional traces. The other opportunity with HDI is the reduction of trace widths to go allong with the reduction in dielectric thicknesses. Three mil (0.003") are not uncommon as well as 3.5 mil lines and spaces. This provides the opportunity to route 80 to 100 traces per square inch.

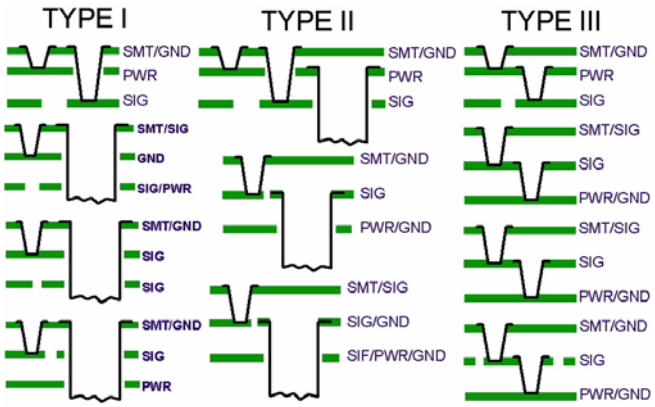
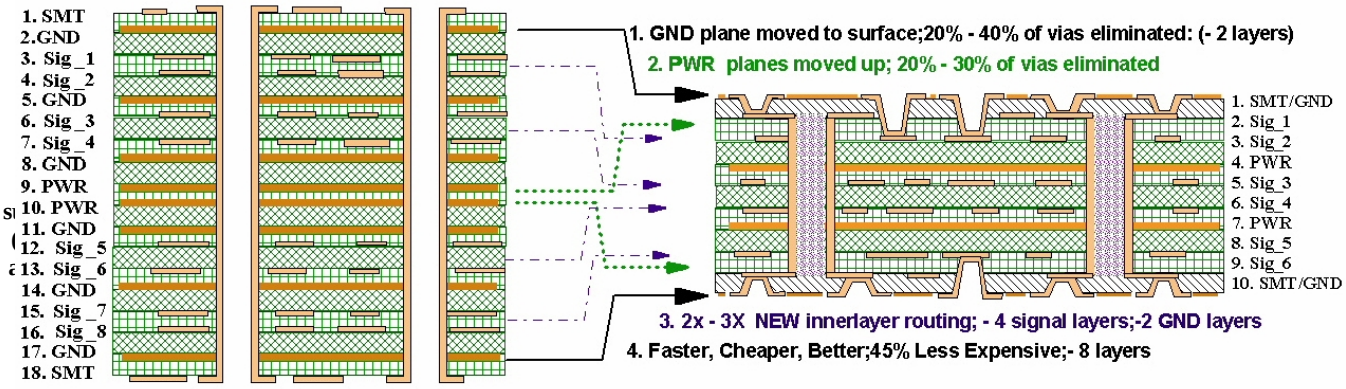


Figure 4 - Various layer assignments available when using HDI and microvias. The goal is to remove as many TH as possible to free up routing space on the innerlayers.

ROUTING BGAS USING CHANNELS

Noting the importance of using the blind microvias to eliminate TH, a second important function, especially on large boards that have high I/O BGAs, is ***where*** the microvias are placed. Historically, the blind-vias were placed around the perimeter of the BGA. This works well for BGAs with <400 pins, but for the new BGAs, like FPGAs, that contain 300 to over 1700 pins, the blind-vias are placed differently. **Figure 6** shows a typical 1153 pin ASIC (FPGA). In theory, this 1153 pin (34x34) BGA has 132 possible routing escapes per layer (1 trace between vias) plus 20 traces in the channel (5 traces). This means that 8 layers would be required (plus 5 plane layers) to connect this BGA to the rest of the circuit. The TH vias create



a 'fence' that makes routing very 'layer- intenesive'.

If we create more routing channels on the innerlayers by placing the blind-vias on the surface (**Figure 6:colored dogbones**), we connect more traces per layer and reduce the total layers. *Channel Routing* uses blind microvias to form 4 or more additional cross-shaped, L-shaped or diagonal channels in a BGA fanout pattern. These new channels allow up to 48 extra

connections per layers for this BGA (8x6 traces). Four routing layers and four plane layers can be eliminated in this example.

In some cases, the channel is not to escape the inner-pins of a BGA but to allow access to an adjacent BGA. The blind vias can be via-in-pad, near-via-in-pad or traditional dogbones. If working with a FPGA where pin swapping is possible, then the channels should be assigned to ground and power first.

THINNER MATERIALS

A logical alternative to make a multilayer thinner is to use thinner materials. Multilayers useing 4 or 5 mil traces need 5 or 6 mil thick dielectrics to maintain impedance. But, reducing to 3 or 4 mil cores and prepregs will not only allow thinner lines for the same impedances, but as seen in **Figure 7**, will lower crosstalk.

The figures shows that there is a benefitial effect to moving signals closer to their reference plane. The parameter, S/H will increase if H decreases, and the near-end crosstalk (V) will decrease with increasing S/H. For the same crosstalk (constant S/H), decreasing H permits shrinking S, or higher density.

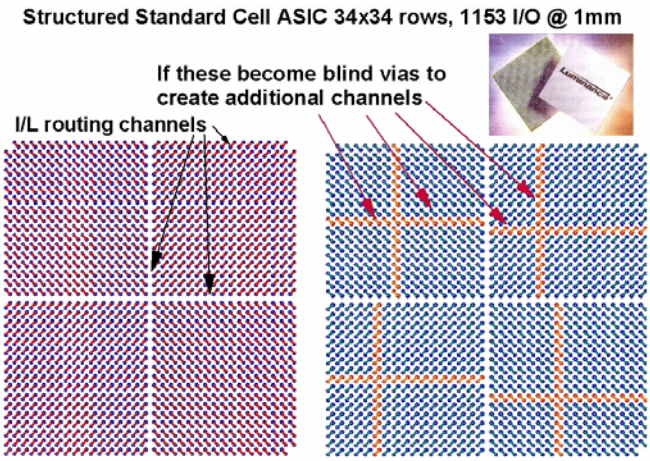


Figure 6 - Using blind vias to form cross, L-shaped or diagonal channels allows the innerlayer to route up to 3X the number of escapes from a large BGA.

MULTILAYER COST-DENSITY TRADEOFFS

The increase in density offered by HDI is illustrated in the COST-DENSITY TRADEOFF CHART (**Figure 8**).

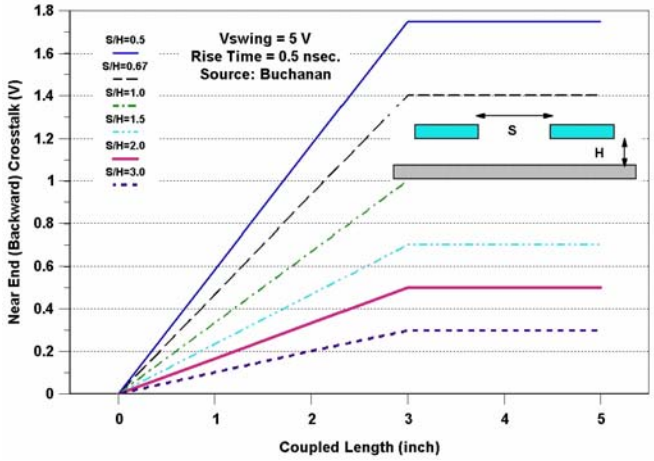
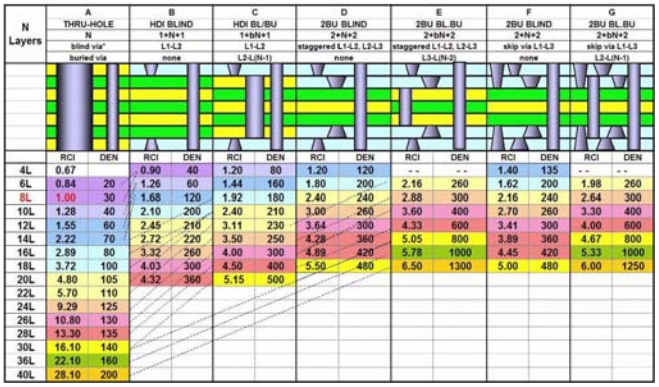


Figure 7 - As signals are closer to their reference plane (H), the distance between them (s) for the same crosstalk can be reduced.

The first column is traditional TH boards from 4 to 40 layers. The prices (RCI) have all been adjusted to a basis of the cost of an 8-layer board from China. The DEN is the average density of the stackup in pins per square inch. To find the equivalent of a particular TH board, you move diagonally, following the dashed lines.

For example, if you had the 26_Layer_TH multilayer (RCI=10.80), the HDI Type III would be a 16_Layer board (RCI=5.78); the Type II would be, RCI=4.0 . These all have approximately the equivalent **DEN**sity, but the HDI boards are less costly by 46.5% for the Type III and 63% for the Type II.



N Layers	A THRU-HOLE N blind via* buried via		B HDI BLIND 1+N+1 L1-L2 none		C HDI BL/BU 1+bN+1 L1-L2 L2-L(N-1)		D 2BU BLIND 2+N+2 staggered L1-L2, L2-L3 none		E 2BU BL/BU 2+bN+2 staggered L1-L2, L2-L3 L3-L(N-2)		F 2BU BLIND 2+N+2 skip via L1-L3 none		G 2BU BL/BU 2+bN+2 skip via L1-L3 L2-L(N-1)	
	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN
4L	0.67		0.90	40	1.20	80	1.20	120	--	--	1.40	135	--	--
6L	0.84	20	1.26	60	1.44	160	1.80	200	2.16	260	1.62	200	1.98	260
8L	1.00	30	1.68	120	1.92	180	2.40	240	2.88	300	2.16	240	2.64	300
10L	1.28	40	2.10	200	2.40	210	3.00	260	3.60	400	2.70	260	3.30	400
12L	1.55	60	2.45	210	3.11	230	3.64	300	4.33	600	3.41	300	4.00	600
14L	2.22	70	2.72	220	3.50	250	4.28	360	5.05	800	3.89	360	4.67	800
16L	2.89	80	3.32	260	4.00	300	4.89	420	5.78	1000	4.45	420	5.33	1000
18L	3.72	100	4.03	300	4.50	400	5.50	480	6.50	1300	5.00	480	6.00	1250
20L	4.80	105	4.32	360	5.15	500								
22L	5.70	110												
24L	9.29	125												
26L	10.80	130												
28L	13.30	135												
30L	16.10	140												
36L	22.10	160												
40L	28.10	200												

Figure 8 - The PRICE-DENSITY MATRIX compares the relative prices (RCI) of through-hole (TH) multilayer boards to their equivalent HDI-Microvia board, along with the average density (DEN) of pins per square inch. [4]

RESULTING SIMPLER MULTILAYERS

For out TH example in Figure 1, the *Layer Reduction Process* just described was applied. The resulting HDI structure is seen in **Figure 9.** In addition to being only 16_Layers, its total thickness is only 0.084". This is nearly one-half the original thickness of 0.152". In addition to the lower thermal mass, the aspect ratios of holes is now ½.

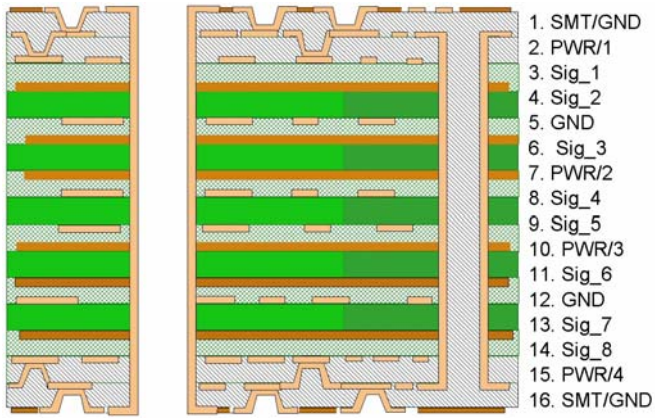


Figure 9 - The redesigned 26_Layer_TH board resulted in a 16_Layer_HDI board (Type III). This is the conservative design with the four PWR planes kept intact but now with only 8 signal layers instead of the original 10 signal layers.

Further design refinements resulted in simplification to a Type II HDI structure, as seen in **Figure 10**. This simpler 16_Layer_HDI structure is also 63% lower in cost than the original 26_Layer_TH board, but even more important, had a 700 IST cycle-life with 6X 270C LF preconditioning.

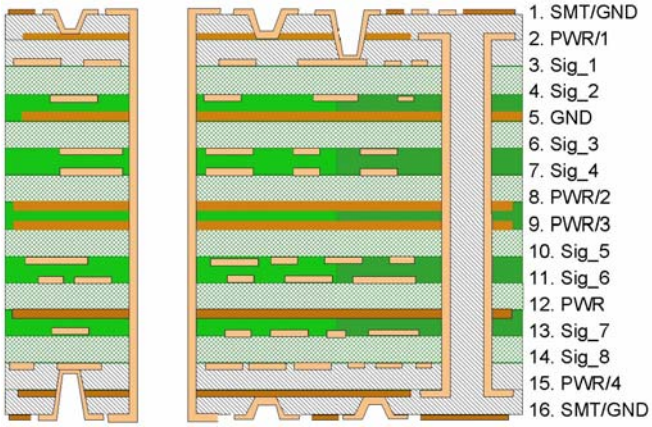


Figure 10 - The redesigned 26_Layer_TH board was further refined and simplified to a 16_Layer_HDI board (Type II). This is still a conservative design with the four PWR planes kept intact but now with only 8 signal layers instead of the original 10 signal layers.

CONCLUSION

One of the more difficult type of multilayer to get to accept a lead-free assembly process is the high-layer, thick multilayer with through-hole parts and multiple rework capability. This paper outline five techniques to help in the reduction of thickness and number of layers for these types of boards.

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