Stacked Array Packaging
A Flex Based IC Packaging Solution for Single and 3D Multiple Die Applications

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Abstract
The challenge manufactures face when competing in the world marketplace is to offer a product that will meet all performance and functionality expectations without increasing product size or cost. Increased electronic functionality can be achieved through the development of more complex silicon integration but that route generally requires a great deal of capital resources and an excessive amount of time. Multiple-die package concepts are often proving superior to the system-on-chip alternative because it minimizes risk and has the potential for economically integrating several different but complementary functions. The information presented in this paper will review several existing package-on-package configurations and introduce a new substrate fabrication process developed to improve IC package density and circuit routing efficiency. In addition, the basic package assembly methodology will be described and examples of high density stacked memory and mixed function variations shown. In keeping with IPC presentation guidelines it should be noted that a portion of the technical information presented focuses on unique fabrication processes developed for the substrate and are a licensed technology covered by several US and foreign patents.

Background
Hand-held communication and entertainment products will continue to dominate the consumer markets worldwide and, with each generation offering more and more features and/or capability, system level integration and miniaturization becomes more of a priority. And even though the actual applications and functionality of the new product offering expands, the customer is expecting each generation to be smaller and lighter that its predecessor. A number of single-die and stacked-die package innovations have been developed for this broad market but many supplier companies are not meeting acceptable manufacturing yields and the difficulty of simultaneous testing of multiple mixed-die technology is not always practical. Without implementing more innovative package methods, the functional capability of the newer generation of hand-held and portable products may never reach expectation or achieve manufacturing cost objectives.

The material developed for this IPC program will outline current expectations for multiple function packaging for hand-held and portable electronic applications and detail the development of a new and innovative vertically stacked MicroContact package methodology that offers a practical high-yield solution for a broad range of system-in-package applications. A key advantage of this polyimide film based substrate technology is that each layer of the package can be pre-tested before joining. This capability greatly improves the manufacturing yield and the functional reliability of the final package assembly is assured.

Evolving Multiple Die Package Applications
The motivation for developing higher density IC packaging continues to be the market and the consumers' expectation that each new generation of products furnish greater functionality. The miniature IC package evolution began with the development of chip-scale and die-size package technology. These flex-based package innovations (µBGA®, µStar™, µCSP™ for example) proved ideal for portable and hand-held electronic applications. To address the need for even more functionality without increasing their products size, a number of companies have adapted various forms of multiple-die 3D packaging. A 3D package is a component that incases multiple semiconductor devices within a single package outline. A number of these early multiple function devices relied on the sequential stacking of die elements onto a single substrate interposer. The die-to-substrate interface was generally made using a conventional wire-bond process. Because the wire-bonding of multiple tiers of uncased die is rather specialized and the die used may have had relatively poor wafer level yields or were not always available in a pre-tested condition, overall manufacturing yield of the stacked-die packaged devices have not always met acceptable levels. For one or more of these reasons, many suppliers are moving away from all but the most basic stacked-die processes. Basic stacked-die applications in the future will likely rely on only die that are very mature and will conceivably furnish the user with a more respectable finished product yield.

Many companies have already moved into a package assembly methodology that is more predictable and have adopted or plan to adopt the package-on-package methodology. The stacking of one package onto another is a process where sections of the package can be individually assembled and fully tested before joining into the final package configuration. The joining process is currently accomplished using mass reflow solder processes with in-line configured solder alloy ball contacts.

In preparation for package-on-package stacking, one or more die are assembled onto a substrate interposer to provide a single testable fine-pitch BGA (FBGA) unit typical of those shown in Figure 1.

Figure 1 - Package-on-package assembly process enables individually FBGA packaged sections to be thoroughly tested before joining together.

The flex based substrate interposer for the examples above has been designed to provide a vertically configured package-on-package (PoP) format. The stacked package with ball contacts has already found universal commercial success. Several major memory suppliers, for example, have recently adopted the ball stack process to enable a substantial increase in memory density to support high-end processors and routers.

Package Interface Methodology

Alloy spheres have proved to be an excellent interconnect method in regard to assembly compatibility and reliability and will continue to be used for a wide number of applications, however, the contact density (pitch) is somewhat limited, restricting circuit routing channels on both package substrate and board. The example shown in Figure 2 illustrates the potential restrictions hampering efficient circuit routing as the ball contact pitch shrinks below 0.65 mm.

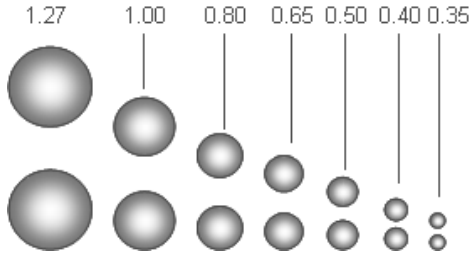

Figure 2 - As the ball contact pitch shrinks, circuit routing channels are severely restricted.

Addressing the limitations of circuit routing on the finer pitch package and to provide a more efficient methodology for package-to-board interface, a new concept for contact design has emerged, replacing the spherical contact with an integrated conical post-like contact or MicroContact (see Figure 3).

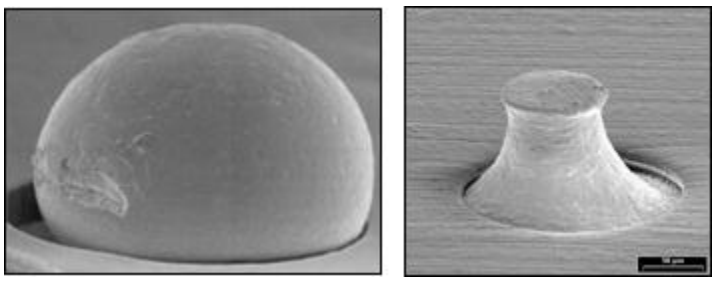

Figure 3 - Comparing the 300 micron diameter ball contact to a 180 micron diameter MicroContact

In keeping with the array contact format of the popular BGA and FBGA, the new contact can be provided with the established pitch variations already defined in JEDEC package design guidelines. The technology can furnish the same or smaller footprint as other FBGA packages but, because it is much smaller in diameter than the spherical contact, the land pattern provided on the PCB for solder attachment can be made smaller as well. A smaller land pattern provides a wider spacing between contact features thereby enabling higher density PCB circuit routing. For example, a very common contact pitch for the FBGA is 0.50 mm with a contact land of 300 microns, while the new system's land pattern having the same pitch can be as small as 200 microns allowing more surface area for circuit routing. Adapting 40 micron conductor width and a 40 micron space between conductors, it's possible to route only two conductors between 0.5 mm pitch ball contacts. Because the new system requires only 200 micron diameter lands, three 40 micron circuit conductors can be routed between lands as detailed in Figure 4.

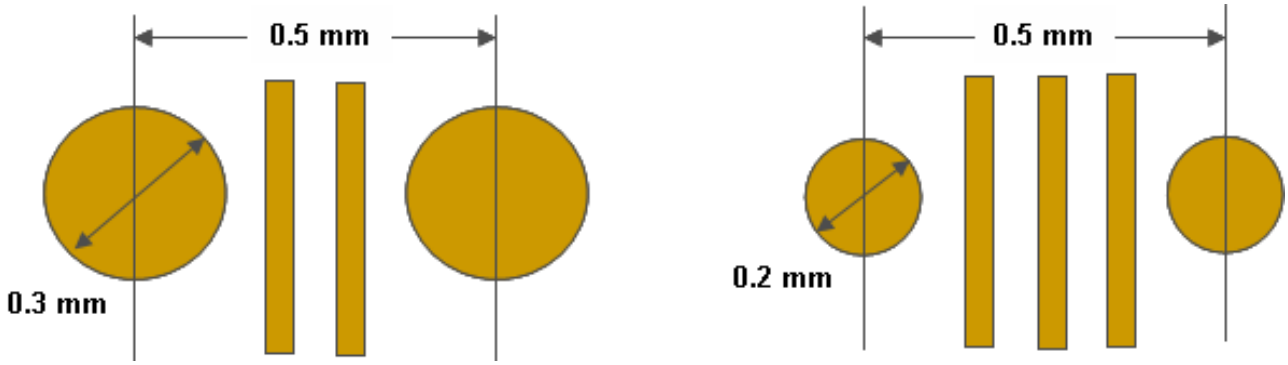

Figure 4 - Comparing FBGA and new land pattern and circuit routing capability.

In addition, the new profile is much lower than traditional CSP contact spheres, potentially improving electrical performance through reduced inductance and resistance.

Substrate Development for the New Interconnection

The material set selected for any multiple die substrates must furnish good dielectric characteristics and be able to withstand the relatively high assembly process temperatures needed for the newer generations of lead-free products. Although most dielectric materials (even those with glass or fiber reinforcement) are flexible in their basic sheet form, the non reinforced polyimide film dielectric has proved to be preferred for growing number of high-performance IC package applications. Polyimide films are often selected for products that must operate in more hazardous or high temperature environments as well. The in-package and package-to-PCB interface generally relies on one or two copper circuit conductor layers. For the single metal layer substrate, the copper is typically applied to the flexible base dielectric as a foil with adhesive. An alternative process casts a polymer dielectric directly onto the copper foil without adhesive. In both single metal material variations, holes and other features are drilled or punched through the composite structure; circuit features are imaged using photo resists and chemically etched to provide the finished circuit pattern.

Although metalized dielectrics are in wide use for IC packaging, the processes developed for fabricating the new package substrate is very different. The primary difference is, the dielectric is applied to the base metallization. The unique base metal is a tri-metal (three layer) copper-nickel-copper composite (see Figure 5).

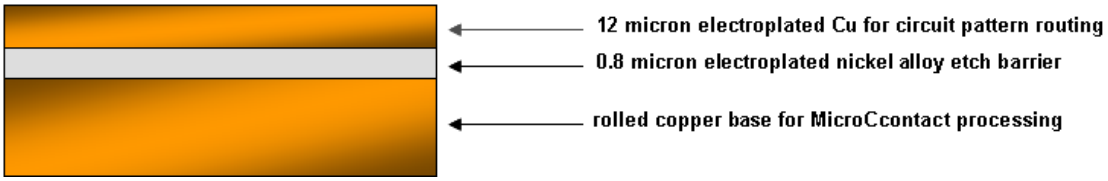

Figure 5 - The unique tri-metal composite is built up on a 80 to 180 micron thick rolled copper base.

The base alloy is a rolled copper foil that is furnished in thicknesses up to 180 microns. One side of the copper foil is electroplated with a thin (0.8 to 1.0 micron) nickel. The nickel plated surface is then electroplated with 9 to 18 microns of copper. The heavy layer of copper will provide the actual contact features while the thin layer of copper on the opposite side of the nickel will be reserved for in-package circuit routing. There are two alternative fabrication processes currently in use; one referred to as circuits-out and the other identified as circuits-in. Depending on the variation selected, the fine-line circuit

pattern is imaged and chemically etched on electroplated surface of the composite copper base before or after the contact features are processed.

Contacts-in process overview: The contacts-in fabrication process begins with resist application and imaging of the contact array pattern. Using a two stage chemical etch (subtractive) process, the contact features are formed. These features are first defined using a photo-imaged resist. All non-coated areas are initially etched using a *cupric chloride* process followed by a less aggressive fine etch process using an *alkali* based chemistry. The resulting contact features derived from this process are somewhat conical in shape. For example, when the resist is removed, the 125 micron high contact will taper from its 100 micron base diameter to just 80 microns at the tip. Because the rolled copper material thickness is very uniform, coplanarity of all contacts on the finished substrate are near perfect.

Following the contact forming process a 25 micron thick polyimide film dielectric is applied. The dielectric film is bonded onto the same surface as the contact so it must first be prepared with openings at each contact site using a die-punch process or laser ablation. In preparation for circuit features, a photo-resist material is applied to both sides of the tri-metallic structure. The resist applied to the thin copper layer opposite the contacts is a commercial photo-imageable composition to ultimately furnish the chemically etched circuit conductor features within the substrate. After chemically etching the circuit, the resist material is removed and the circuit pattern and dielectric are insulated with a thin dielectric cover-coat material. Areas reserved for die attachment and wire-bonding are free of the cover-coat material. Resist material applied to the contact side of the substrate is finally stripped and all exposed copper circuit and contact features are plated with a thin layer of gold over a nickel alloy barrier layer.

Contacts-out process overview: Using the Cu/Ni/Cu tri-metallic material as a base, the circuit features are first coated with photo-resist on the thin copper side. The circuit pattern is then imaged, developed and chemically etched. Following the resist removal, only the copper conductors remain on the surface of the nickel alloy core layer. Before further chemical etching processes are performed, a polyimide film is bonded over the circuit conductor surface. To expose features needed for die- attachment and/or wire-bonding, the polyimide film is selectively removed using a CO_2 laser ablation process. When completed, a second photo-imaged resist material is applied onto the heavier copper-clad side of the composite. After imaging and developing the resist, the new pattern array is chemically etched (as described above) to eliminate the heavy copper between contact features as well as the remaining thin nickel barrier layer. A photo-imaged cover-coat is applied over the now exposed circuit conductors leaving contacts and bond-sites open. All non-coated contact features are finally plated with a thin layer of gold over a nickel barrier layer to complete the substrate fabrication process as illustrated in Figure 6.

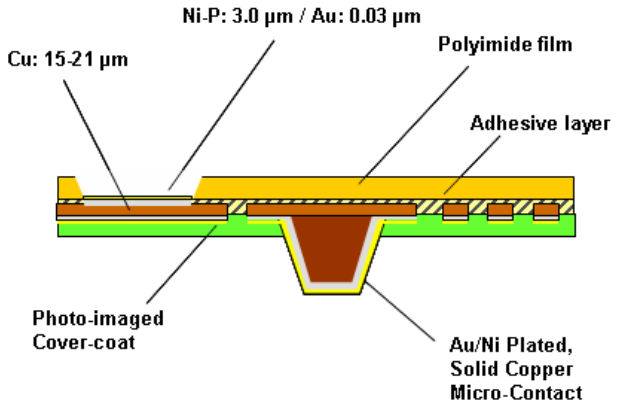

Figure 6 - The new substrate furnishes a solid copper contact for package-to-package and package-to-board interface

Package Assembly

The package assembly process is based on the already proven and mature technique developed for the micro BGA package technology. The individual package substrate is initially retained in an array strip format for efficient assembly processing. By utilizing very thin silicon die, a relatively thin substrate and a unique face-down wire-bond interface methodology, a number of practical, low risk solutions are available. Because the new system's features are outside the die perimeter the substrate is slightly larger than the die outline. The additional extension of the substrate material furnishes just enough space at its perimeter for both inter-package termination and the eventual interfacing with the PCB host structure.

Typical of the ball stack package technology, the individual package sites of our new system are prepared in a matrix pattern within a narrow rectangular strip format. Because the material is very thin it is necessary to mount the strip onto a rigid carrier frame for the package-level assembly processing. The test package substrate detailed in Figure 7 is a single package

section of the strip configured substrate that was initially developed for high performance memory die having center-bond pads. With the die mounted face-down onto the package substrate, a very short die-to-board interface is provided. This close coupling is a mandatory requirement for accommodating high-speed memory requirements.

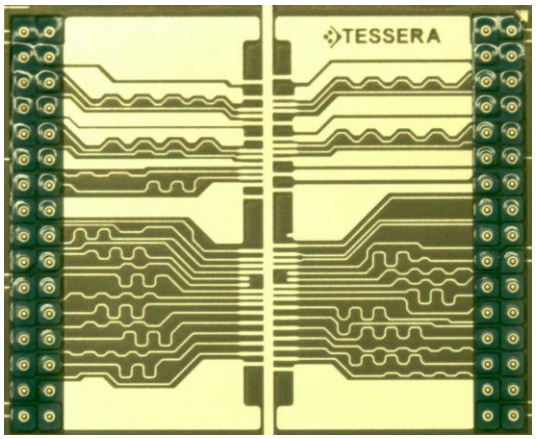

Figure 7 - New PoP substrate developed for packaging high-performance center-bond memory die.

In the package assembly process, each die are attached with the active face down onto a heat activated adhesive attachment site on the substrate base material. Electrically interconnect is accomplished using either a proprietary lead-bond bond process pioneered by Tessera or conventional wire-bond methodology. For the center-bond memory application, the etched copper pattern includes a wire-bond site near the edge of a narrow slot (or window) located in the center area of the substrate. The slot provides access for wire-bonding down to the die during package assembly. The conductors are individually routed from the wire-bond sites to a pre-designated interconnect site (see Figure 8).

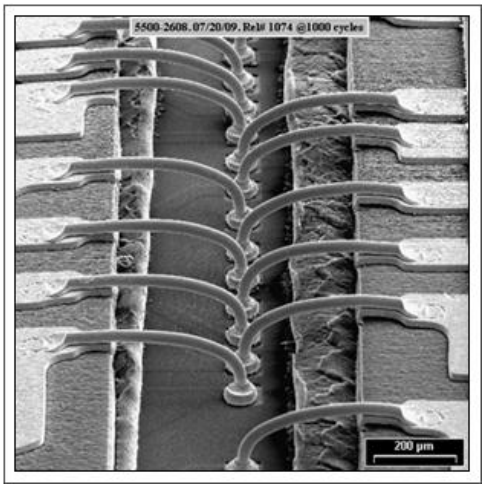

Figure 8 - Center bond die-to-substrate interface is made with conventional wire-bond technology

Following wire-bonding, the bond cavity is encapsulated to seal-off the exposed bond window, package units are singulated from the matrix and made ready for electrical test and, when required, burn-in. Because the contacts are an integral part of the substrate, the individual packaged devices are ready for electrical testing.

PoP Joining Process

Because of the relatively thin composite of elements within each section of the package, the overall height of the finished package is minimized, ultimately determined by the number of packages joined in the stack. The contact pattern base furnished on the lower side of the "circuits-in" substrate also serve as the attachment sites for the next package layer. The substrate furnished with "circuits-out" have a slightly larger hole ablated in the substrate dielectric on the opposite (top) side of the substrate to provide the attachment site for joining additional packages. This provision for vertical interconnect between package layers ensures the efficient transfer of electrical signals between each package layer, ultimately terminating at the PCB or module surface. In preparation for the stacking process, a specially formulated high temperature (Pb-free) solder paste is deposited at each interface contact land then transferred to a multiple site alignment fixture. The actual

stacking process begins with the transfer of the second layer package sequentially placed atop the base packages. The joining (stacking) process is repeated for each package layer and, when completed, the stacked units are transferred to a forced air/gas convection oven for mass reflow to finish the interlayer solder joining of all package layers as illustrated in Figure 9.

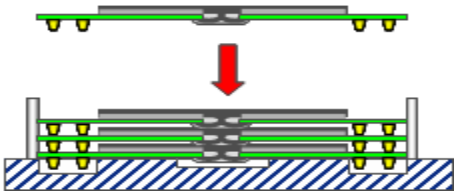

Figure 9 - Package stack process uses a RoHS compliant solder alloy composition and mass reflow for joining

Following cleaning and a final continuity test of the multiple package assembly, the stacked packages undergo a final physical inspection before transfer to partitioned trays designed for shipping to customer sites. In regard to board level assembly, the solid copper contacts are furnished with a thin Ni/Au alloy plating so they are compatible with either eutectic or lead-free alloy solder processes.

System-in-Package Development

The expanding functionality expectation for portable and hand-held electronic products has opened up a whole new category of IC package technology. This factor has increasingly become an issue and is evidenced by the physical restriction on the number of ICs that can be designed onto the circuit board. Package performance is also an issue. Until recently, the component packaging industry did not directly concern itself about system level performance, but, as multiple die are configured into a single package outline, the whole system performance issue must be kept in view. Any comparison should be done at the equivalent system level; one composed of single device packages and the other with multiple die packages and their interface methodology. As noted above, the perimeter located contact pattern of the package is designed to allow one package to sequentially mount on the top of one another. The package illustrated in Figure 10 is an example of a memory and logic package-on-package combination designed and developed by us for a prominent OEM.

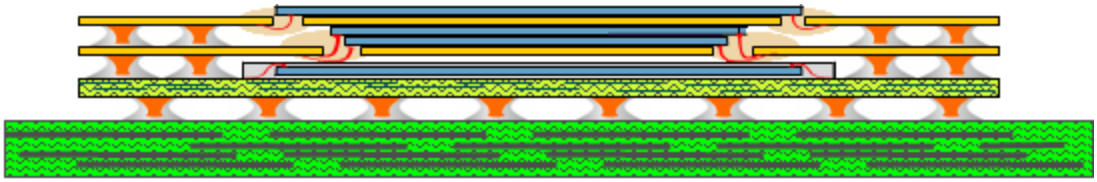

Figure 10 - The four die PoP package stack includes both logic and memory functions in a package profile no greater than 1.2 mm.

Both performance and yield of the finished multiple-die package is of significant concern. Because the package-on-package stacking interconnection pathways leading down to the host circuit board are very close, resistance and inductance are minimized so data can travel faster, thereby increasing the overall memory system performance. To achieve ultimate system level integration and miniaturization goals, companies adapting the new process are able combine any combination die within a single package outline. For mixed function applications, sections can even be sourced separately and joined at the board or module level assembly. The advantage OEM companies have when using the package-on-package configuration is that each IC package section or layer becomes a fully tested subsystem that can be certified by each supplier before joining. Of course, to ultimately support the theory that stacking of the individual package elements into a single module would meet performance expectations, a computational analysis of the stacked package must be conducted comparing the affects of different functional elements and the number of component layers in the stack.

In regard to package reliability, the packaging has demonstrated excellent board-level durability meeting industry recognized thermal cycling requirements for both eutectic and lead-free soldering as well as passing the drop and vibration test defined by handset OEMs. The primary factor contributing to the overall positive results from thermal cycle stress testing is the role the package structure itself plays. The substrate design, the location of the contact features (in relation to the die), the die-attach material and assembly process all contribute to reducing the potential stresses introduced through radically different coefficient of thermal expansion (CTE) between die and printed wiring board. The combination of materials utilized for the substrate, die attach absorbs a significant portion of the physical stress within the package by compensating for the CTE mismatch between the silicon die (3 ppm / ºC) and the laminate based circuit board structure (15-17 ppm / ºC).

Summary and Conclusion

When companies began to develop multiple-die (die-stack) packaging, in-package circuit routing and package-to-PCB interface efficiency and package assembly yield suffered. Many suppliers reverted to using larger substrates to provide additional circuit routing capability. Package stacking, on the other hand, has resolved both issues. Because each section (or layer) can be pretested before joining, the package assures a higher finished package yield and a lower risk solution for memory as well as mixed function. In regard to testing, separate testing of logic functions is preferred because the memory devices generally require unique testing, grading, sorting and burn-in before package level integration. And, the handling of packaged (encased) parts through all of these test related processes is far more efficient than attempting to test bare die, or to assume that all die within a multiple die single package are functioning within expectation.

A key factor when considering adopting this package methodology is that the infrastructure for high-volume manufacturing is already in place. Several of our worldwide network of licensed suppliers are currently ramping up a number of products and able to furnish this new packaging or packaging services for high-performance memory or other package stacking applications. Although prototypes and test models were initially developed within the company, it's acknowledged that production volume capability from a broad supplier infrastructure for any new technology must be established before wide acceptance would be possible. Addressing the need to provide a strong supplier infrastructure for the substrate, we have organized a select group of flexible circuit developers and fabricators to jointly develop a production process for the material. The development program for the circuits-in process began in late 2003. Joint development of a production process began in mid 2004 with parallel development of the circuits-out process a little later that same year. By 2005, licensing agreements and joint licensing agreements were in place and suppliers ready to go forward with providing both circuits-in and circuits-out substrates for the package.

Because the package assembly process utilizes the mature micro BGA manufacturing infrastructure the technology is transferable to a multiple source of supply. The new package technology is a 100% lead-free and bromide free process and the compliant package attributes will further assure high-reliability. Several concerns still remain for multiple die, mixed function SiP technologies. The management of multiple IC vendors and establishing reliable sources for bare die and/or wafers is a primary issue. Other issues include estimating compound yield of less mature ICs, controlling overall product quality and reliability, how to accommodate incompatible die shrinks and, most significant, how to qualify and maintain a reliable high volume substrate supply infrastructure. Of course, most of these issues are now being resolved to move the MicroContact package technology into the mainstream.

Biography for Vern Solberg

Vern Solberg currently represents Tessera as a special consultant within several industry organizations including IPC, SMTA, IMAPS and he is a US delegate to the JISSO International Council (JIC). Vern has served the industry for more than twenty-five years in areas related to design and manufacturing for both commercial and aerospace electronic products and was associated with Tessera for ten years as their Senior Applications Engineer. Vern is active as an educator and holds several patents for IC packaging innovations including the folded-flex 3D package technology and is the author of *Design Guidelines for Surface Mount and Fine-Pitch Technology* a McGraw-Hill publication.

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IPC APEX
Los Angeles, California – 20 February 2007

TESSERA®

Stacked 'MicroContact' Array Packaging

A Flex Based IC Packaging Solution for Single and 3D Multiple Die Applications

Vern Solberg
Tessera, San Jose, California USA

Agenda

- Review Flex Substrate Evolution for CSP
- Evolving Miniature IC Package Applications
- MicroContact Array Package Development
- Fab Process Details for MicroContact Substrates [1]
- High Density 3D Stacked SiP Assembly Variations

[1] The MicroContact application and unique fabrication processes are a licensed technology covered by several US and foreign patents.

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Background

- **Tessera was founded in 1992 as a multi-chip module (MCM) company to address the Known Good Die (KGD) problem (a problem still facing the semiconductor industry).**
  - **To solve this problem, Tessera developed a small and testable chip carrier that also dramatically reduced package size, improved package performance as well as reliability.**

This chip carrier, Tessera's micro Ball Grid Array (µBGA®) package, is today's solution-of-choice for many of the world's most influential semiconductor companies.

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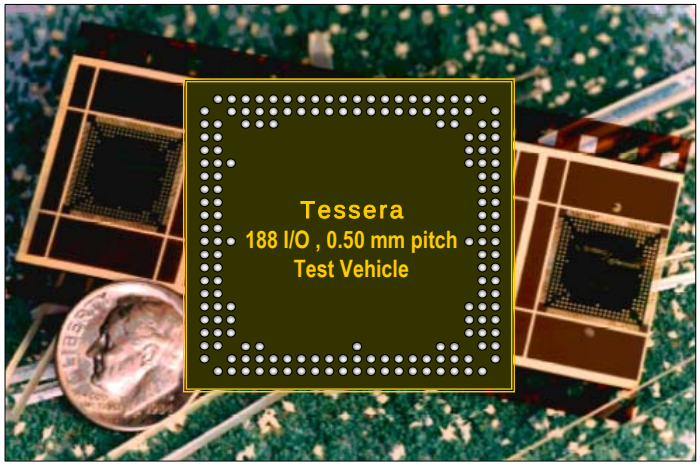
TV-188, 0.5mm pitch µBGA® Tessera's First Test Vehicle



Circa 1994-Single metal layer, polyimide tape based substrate

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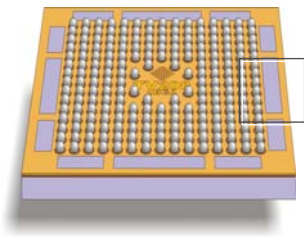
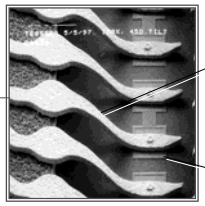
µBGA® (Lead-Bond) Package

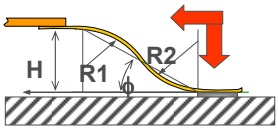




Gold plated Copper lead

Standard Aluminum bond pad

The 'S' shaped lead profile absorbs the stresses typically produced when materials with significantly different thermal coefficient of expansion ratios are exposed to wide variations of high and low temperatures.



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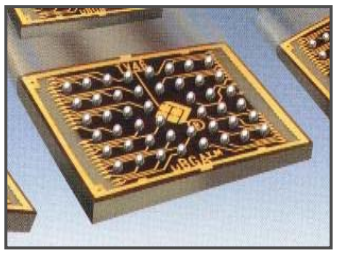
First large scale commercial application for µBGA®

- **Selected for Intel Flash**
  - Intel Corporation announced the adoption of Tessera's flex based µBGA® package in 1996 as part of its packaging portfolio for Flash memory devices used in wireless handsets and other mobile products.



5.5 mm x 7.5 mm Die
46 I/O, 0.75 mm Pitch
0.35 mm Ball Diameter

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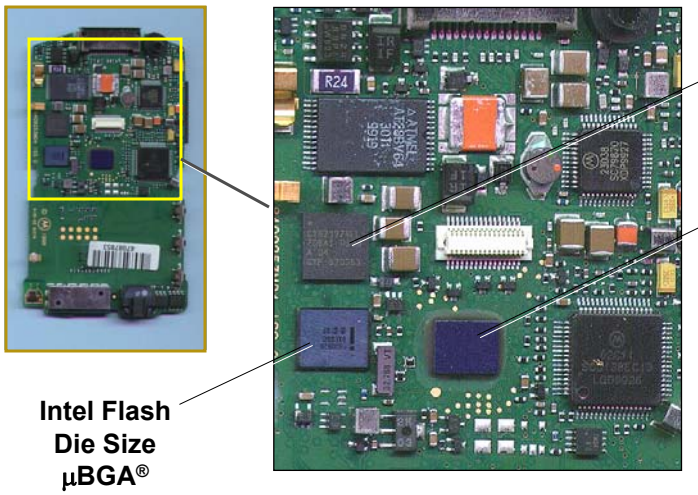
µBGA® Selected for Motorola StarTAC GSM



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IC Package Solution for Miniature Medical Electronic Applications

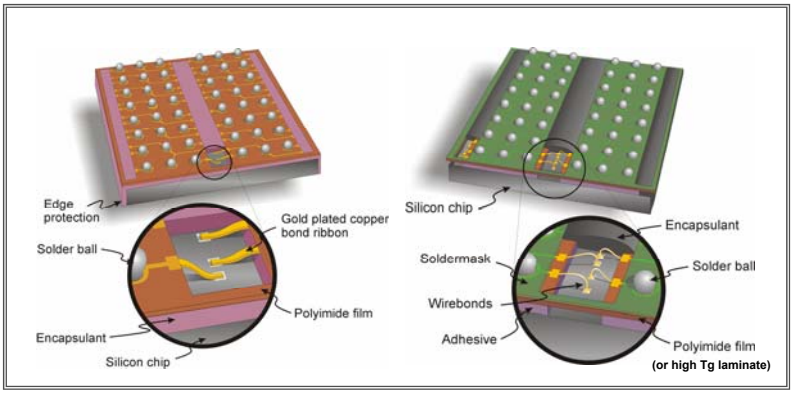
8 mm x 7 mm, 56 I/O single die µBGA® logic package using polyimide film substrate base

Single die package developed for Cochlear

8

µBGA® Flex Based Package for High Performance Memory

Lead-Bond µBGA **Wire-Bond µBGA**



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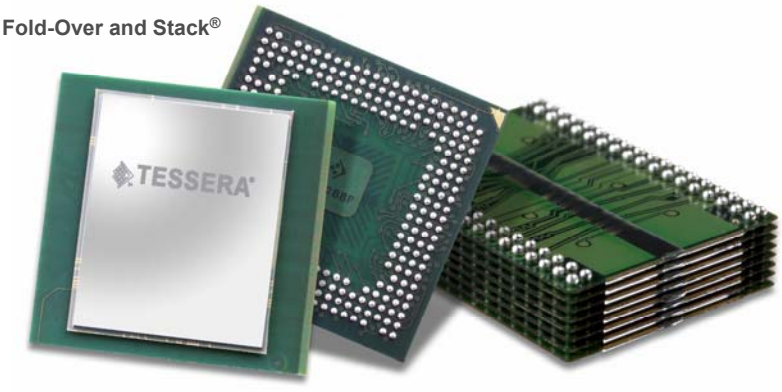
3D FBGA Package Innovations

µZ Fold-Over and Stack®



µZ Ball Stack®

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Multiple Die 3D Package Challenge

Multiple die packaging must solve key logistics issues:

- Accommodate incompatible die shrinks
- Simplify management of multiple IC vendors
- Enable package level test and burn-in
- Allow the combining of high and low yield devices
- Contribute to product quality and reliability
- Maximize configuration flexibility

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Limiting Factors of BGA Package Technology

- **Ball contacts have proved ideal for package stacking, however, the size (diameter) of the ball contact tends to limit inner-package routing density.**
- **As I/O increase:**
  - **Increased difficulty in routing and/or increased package size**
  - **Increased complexity in test and burn-in sockets (higher cost)**
  - **Potential limitation in high speed performance**
  - **RoHS requirements aggravate situation**

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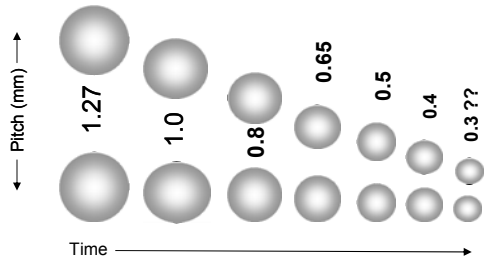
BGA Packaging Limitations



- **To address these issues and furnish a viable solution for increasing package density, new methodologies needed to be developed.**

Accordingly, Tessera has developed an IC package technology that replaces the solder balls on the package by employing an array of coplanar MicroContacts…

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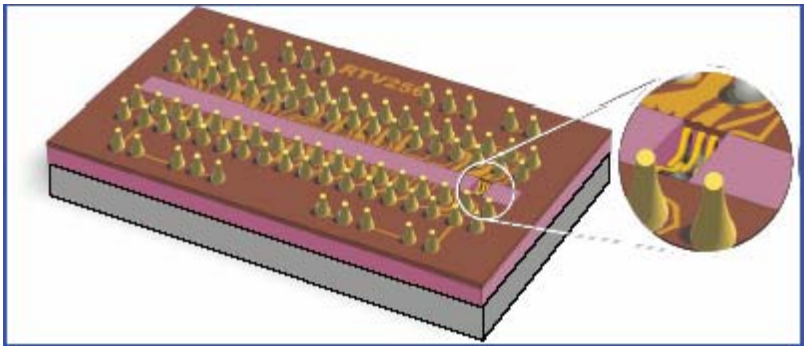
Solution: MicroContact Array for Higher Density IC Packaging



Tessera Lead Bond µBGA® with MicroContact Technology provides wider in-package circuit routing channels and enables a reduced overall package profile

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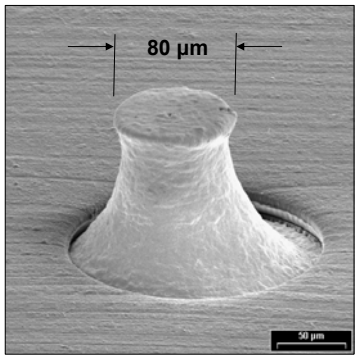
MicroContact anatomy:

Array of coplanar MicroContacts are provided on a compliant flex based substrate

- **Nickel/gold plated copper core**
  - **80 µm tips (typical)**
  - **180 µm base (typical)**
  - **125 µm height (typical)**
- **Same or smaller footprint as other FBGA packages**
- **Enables higher density I/O PCB routing**
- **Lower profile than traditional CSP**



SEM of MicroContact

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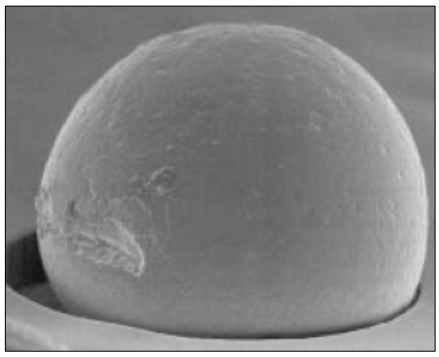
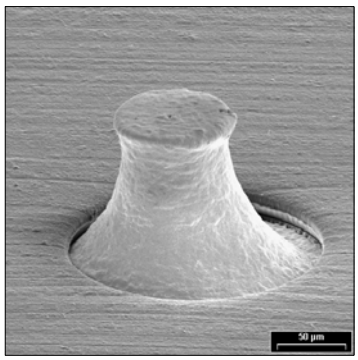
Comparing the Ball Contact to the MicroContact



300 micron diameter ball contact



180 micron diameter MicroContact

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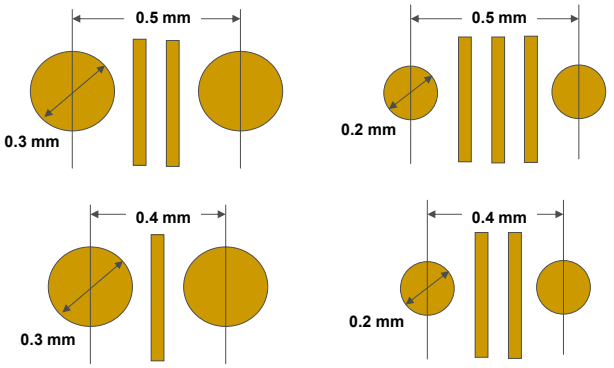
Comparing FBGA to MicroContact PCB Layout for Enhanced Circuit Routing



Solder Ball Land **MicroContact Land**

Trace width = 40 μm / Space width = 40 μm

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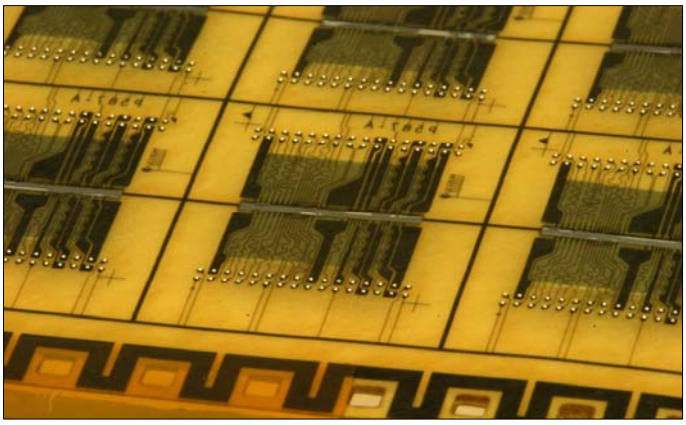
Circuit-in MicroContact Substrate (Sprocket Tape Format)



Substrate developed for a stackable, center-bond DDR-2 memory application

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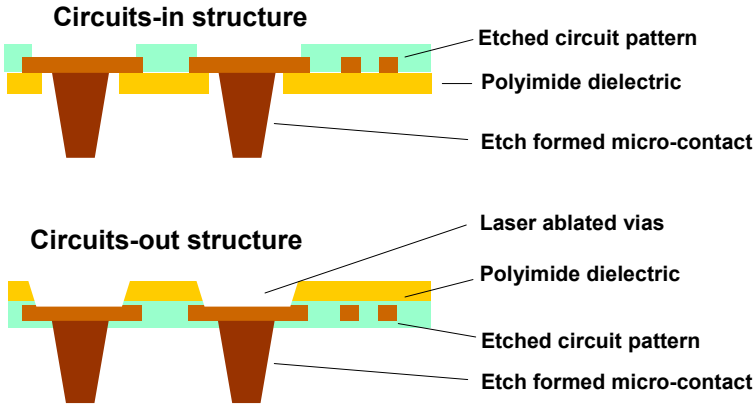
MicroContact Substrate Fabrication Variations



Note: the MicroContact application and unique fabrication processes are a licensed technology covered by several US and foreign patents.

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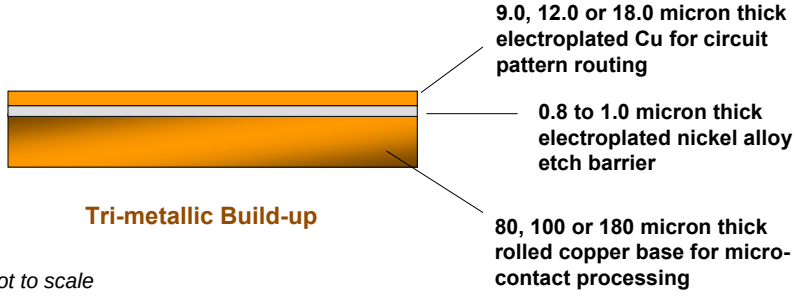
MicroContact Substrate Material

- **Material Set**
  - **Dielectric:** **Polyimide: UPILEX-VT**
  - **Dielectric Thickness:** **25 microns (1 mil)**
  - **Contact and Conductor:** **Tri-metallic *(Cu-Ni-Cu)* composite**



Tri-metallic Build-up

Not to scale

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Standard Variation of Tri-metallic Base Material

	Cu (for Bump)	Ni (for Etching Barrier)	Cu (for Circuit)
Type1	125 um (5 mils)	0.8um	15 um (12 um)
Type2			21 um (18 um)
Type3	100 um (4 mils)		15 um (12 um)
Type4			21 um (18 um)
Type5	80 um (3 mils)		15 um (12 um)

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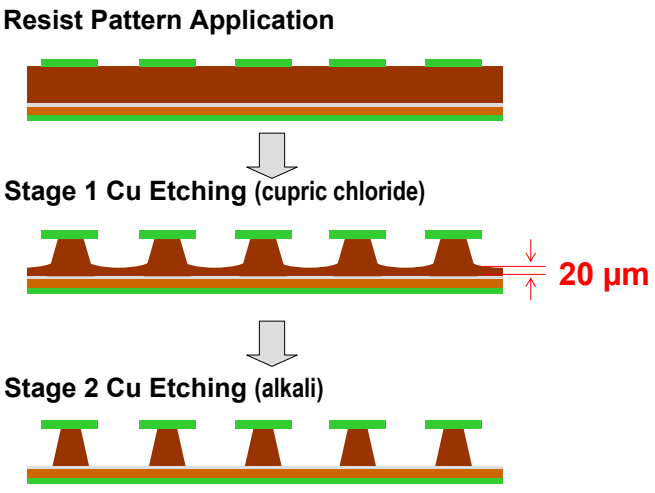
Process flow for Circuit-In Substrate Fabrication



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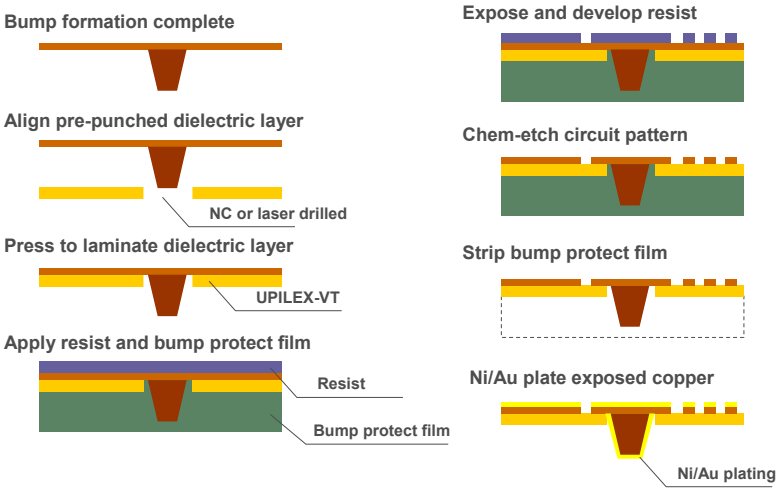
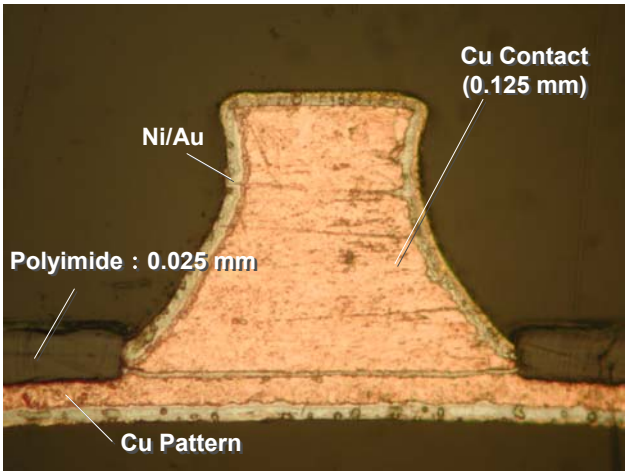
Process flow for Circuit-In Substrate Fabrication cont.



Circuits-in MicroContact Cross Section



Process Flow of Circuits-Out Substrate Fabrication

1. Apply and develop resist

2. Chem-etch, remove resist

3. Apply polyimide film

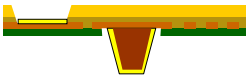
4. Laser ablate bond-site features

5. Apply resist and chem-etch contacts

6. Add electroless Ni/Au plating

7. Apply solder mask over copper features

8. Expose and develop solder mask



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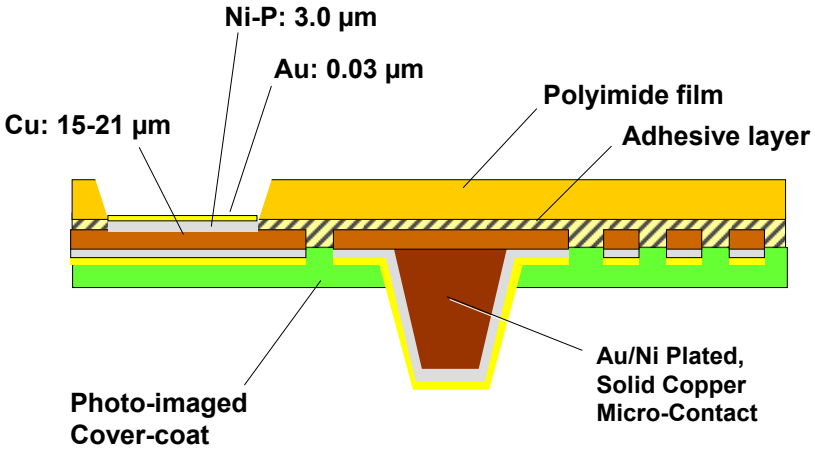
Final Form of Circuits-Out MicroContact substrate



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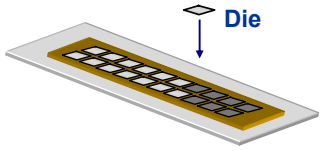
4 Layer Memory Stack Package Assembly Process



Attach Die [1]

Wire-Bond

Encapsulate / Cure

Singulate

Electrical Test

Mark and Grade

[1] dry die attach pad

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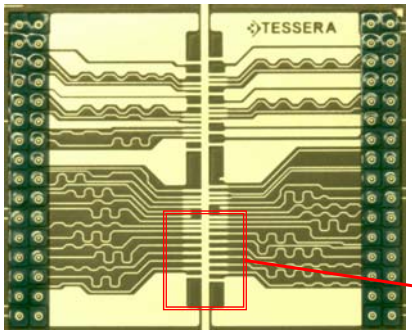
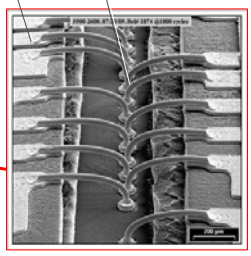
Memory Package Wire-Bond Process



MicroContact Substrate

Gold plated contact on substrate

Gold wire-bond on die



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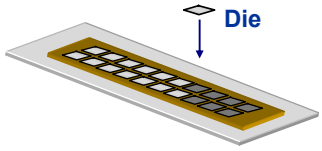
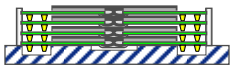
4 Layer Memory Stack Package Assembly Process





Attach Die [1]
Wire-Bond
Encapsulate / Cure
Singulate
Electrical Test
Mark and Grade
Print Solder Paste
Place Base Pkg
Add Upper Sections
Mass Reflow
Clean
Final Test / Ship

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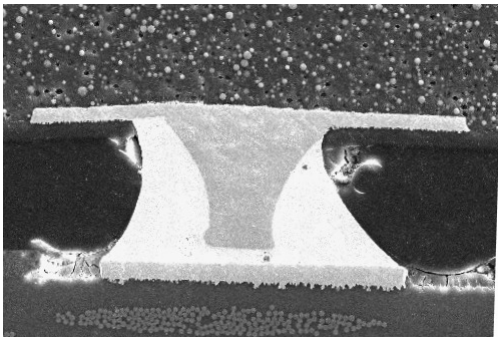
Soldered MicroContact Profile



This interconnection technology can reduce the package contact pitch, reduce package profile, and is completely compatible with established lead-free SMT manufacturing processes.

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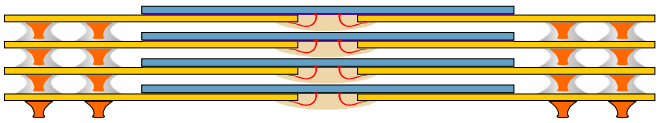
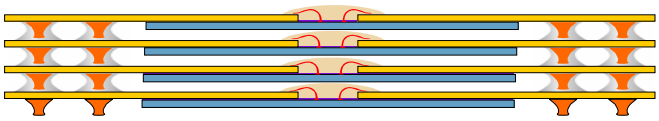
Wire-Bond Stacked Memory MicroContact Array Package



Die face-down µBGA® with Circuit-out MicroContact



Die face-up µBGA® with Circuit-in MicroContact

Die with center bond pads mounted for through-window wire-bond assembly

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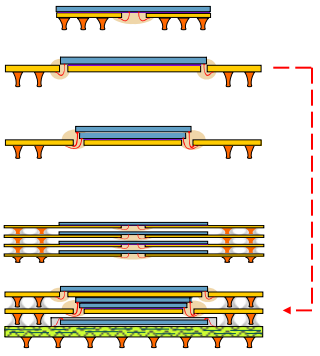
MicroContact Array Package Assembly Variations

- **Single Die Package**
- **Multiple Die Package**
- **Stacked Memory Package**
- **Stacked SiP Concept**



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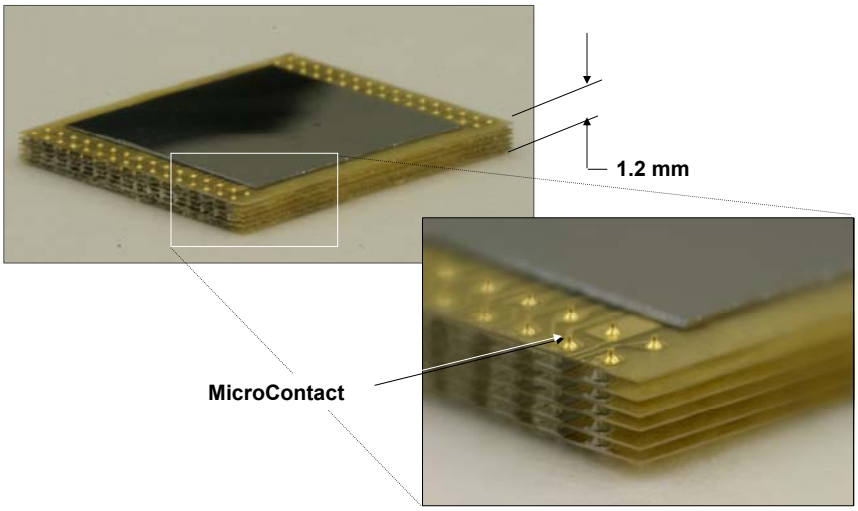
High-Density MicroContact 6 Layer Stacked Memory Package



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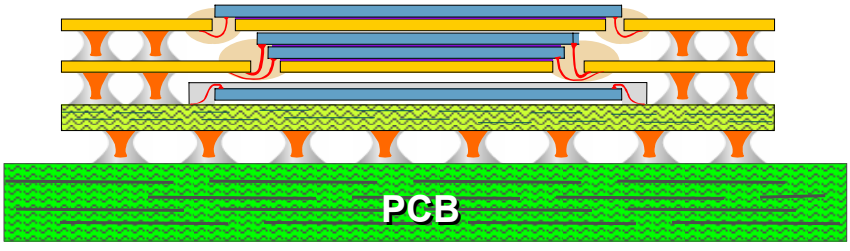
Wire-Bond Stacked SiP with MicroContact-Array Technology

Memory + Logic



1.2 mm max total package thickness (mounted)

Not to scale

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Potential for Enhanced Electrical Performance

- MicroContact allows finer geometries
  - Reduced contact-to-PCB stacking length results in lower impedance discontinuity
  - For I/O-limited packages- smaller footprint, less interconnect delay
  - Finer contact pitch enables increased power and ground I/O
- More space between MicroContacts for circuit routing
  - Increased conductor width can lower impedance
  - Increased conductor spacing can reduce coupling

Note: performance benefits are design dependent

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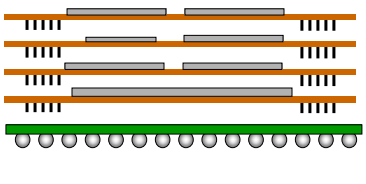
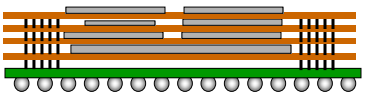
Package Stacking can Overcome Most SiP Challenges…

- Differing die outlines
- Incompatible die functions
- Multiple die sources
- Multiple source same function die
- Different testing and burn-in requirements

SiP Example



Stacked Package Assembly



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Current MicroContact Projects...

- Stacked MRAM devices for government agency
- NAND flash stack for a 4-substrate, 8-die 8GB product
- Evaluation project with leading burn-in board manufacturer
- 2-die stack (RF + baseband) design for mobile handsets

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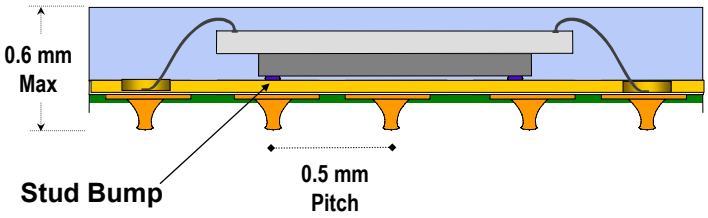
Wire Bond + Flip Chip MicroContact Array Package

- Baseband + RF to support GPS or wireless LAN module
  - Wire-bonded face up die for baseband
  - Stud-bumped flip-chip for RF die



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Benefits of MicroContact Array 3D Package Stacking:

- Enables smallest and thinnest 3D package outline.
- Sequential assembly allows separate burn-in and test.
- Technology transferable to multiple assemblers.
- Utilizes mature µBGA® manufacturing infrastructure.
- 100% lead-free and bromide free process.
- Compliant package technology assures high-reliability.

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Issues and Concerns

- Managing multiple IC vendors
- Known good die, test and burn-in
- Die and wafer availability
- Compound yield of less mature ICs
- Overall product quality and reliability
- Accommodating incompatible die shrinks

These issues are now being resolved to move MicroContact package technology into the mainstream!

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Substrate Supply Infrastructure

- **Licensed Suppliers of MicroContact Substrates**
  - **Maruwa:** small to medium volume, specialty products
  - **Unimicron:** high volume (process optimization underway)
  - **Sony Chemical:** high volume supplier (in start-up mode)

Tessera is currently pursuing additional high volume suppliers!

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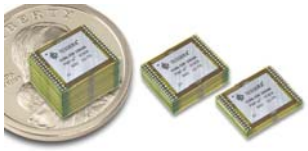

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