VERIFYING MICROVOID ELIMINATION AND PREVENTION VIA AN OPTIMIZED IMMERSION SILVER PROCESS

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Abstract

The Pb-free transition in the electronics industry has seen immersion silver emerge as a leading circuit board finish for RoHS compliant processes and products. It is utilized in a wide cross-section of end-use applications, both simple and technically sophisticated. The strengths of immersion silver are numerous; process simplicity at the fabrication level, contact functionality, and durability to multiple reflow cycles are some of the most noteworthy. Recently, the subject of solderjoint microvoiding has been linked to immersion silver processing, and studies of this phenomena have found microvoiding to present unacceptable risk to the reliability of electronic goods. This work is a continuation of previous publications which explained key root causes of microvoids, along with effective steps at preventing them. The work below presents a review of past findings, additional data confirming the proposed microvoid mechanism, and a substantial volume of production verification data. A direct comparison of this optimized process to alternative immersion silver chemistry is also given.

Introduction

Environmental legislation and directives, most notably the RoHS and WEEE directives, have had significant effect on the materials and processes employed within the electronics industry in recent years. Corporate, governmental, and industry-based initiatives have been underway to move electronics products and processes into compliance with these standards, many of which became "official and active" in 2006.

Printed circuit board finishing and subsequent component assembly are key segments within the broader electronics manufacturing chain. In these areas, new finishes and soldering materials have replaced their tin/lead counterparts. Silver, applied via an immersion silver plating process, has emerged as one of the most technically attractive and most-used Pb-free surface finishes. In 2001, the Pb-free movement was primarily in an "idea and evaluation" phase; utilization of silver as a board finish was less than 5% of total production. Today, estimates place immersion silver between 20 and 30% of total printed circuit board production worldwide[1].

Microvoiding Definition

The topic of microvoiding as it relates to immersion silver plating and subsequent component assembly has been active for two to three years. Despite this, a clear definition of microvoiding and the risk it poses is in order.

Microvoiding is a phenomena which has been given many names, the most common alternatives are: champagne voids/bubbles, planar microvoiding, microbubbles, or simply "voids". Microvoiding can be viewed as a sub-category within a broader classification of solder joint voiding defects. Confusion between microvoiding and other forms of voiding can be eliminated by considering two key and defining characteristics of microvoids: First, microvoids are extremely small, normally between 5 and 40 microns in size. This contrasts with more common and traditional solder process voids, which are typically much larger. Secondly, microvoids always occur at the interface of the bulk solder and the copper substrate. The mechanism of the void formation will be discussed later, but the key point at this time is that the microvoids form in the molten soldering process. At this critical time, the thin silver coating is dissolved into the bulk solder and a thin layer of tin/copper intermetallic is formed. When microvoiding is observed, it is always in the same area as the intermetallic.

Our initial microvoid findings, published in 2005, linked microvoiding with excessively thick silver deposits and reflow conditions[2]. While informative and important to later work, these findings did not offer a thorough explanation to the phenomena. Since that time, others have proposed links to organic codeposition from the silver plating, oxidation of the plated pad, surface finishing variation, and flux effects among others[3, 4, 5.]

Techniques for Identification and Measurement

There are at least three basic techniques for identifying and measuring microvoids. Each has their own strengths and weaknesses. One technique involves the physical "prying" of components from an assembly, with subsequent visual inspection of the pad after prying. This technique has obvious shortcomings, one of which involves poor reproducibility associated with variability in prying. Another technique involves the use of X-ray inspection. Figure 1 shows an example of voiding as observed in soldered pads joint via X-ray equipment. With this technique, an assembled solderjoint can be non-destructively observed. On a negative side, there may be doubt as to whether a void exists within the bulk solder or at the

copper interface. Additionally, X-ray equipment is costly and not present in many fabrication and assembly facilities. The second technique for identifying microvoids involves relatively simple cross sectioning. Figure 2 shows voiding observed in a BGA pad via cross-sectioning. It will be obvious to most that this technique is destructive, but also relatively simple and commonly employed. Lastly, it should be noted that the X-ray technique allows inspection of an entire pad surface, whereas the cross-section observations are limited to a "slice" of a given pad.
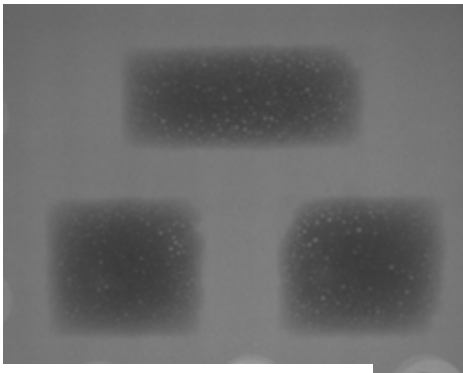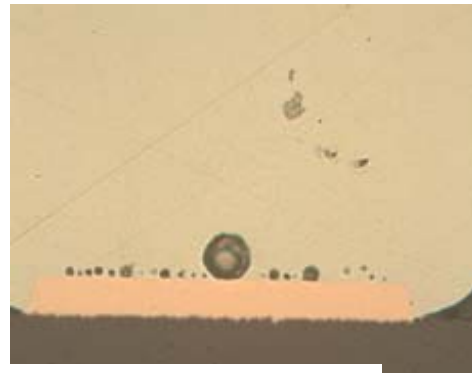

Figure 1
X-ray View of Microvoiding in

Figure 2
Cross-section View of BGA
Microvoiding

Regarding Reliability Risk
Recent studies and publications have shown that high densities of microvoids in solder joints do not affect assembly yields, but do present significant reliability risk. The key mechanism by which this risk is manifested is illustrated in figure 3. When subjected to the rigors of temperature cycling, assemblies exhibiting significant voiding failed via excessive crack propagation whereas those with little to no voiding did not. They key issue here is that the presence of microvoids enables the more rapid travel of cracks through the joint interface, resulting in electrical failure[6, 7].
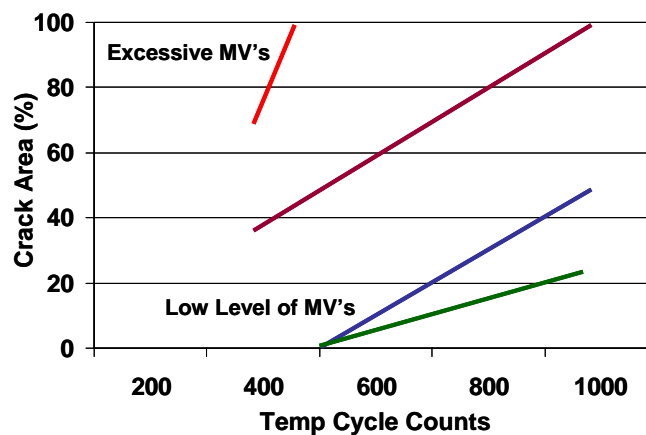

Figure 3 - Effect of Microvoid Density on Temp Cycle Performance[6, 7]

Discussion of Investigations Identifying Microvoid Mechanism

A Review of Metrology, Methods, and Metrics

The microvoid identification and quantification work conveyed below was arrived at via conventional cross sectioning techniques. This method was chosen due to its availability to the investigators as well as its reliability in delivering unambiguous results concerning the location of voids within the solder joint.

Throughout most of this work, a standard test vehicle was utilized to study microvoid phenomena. This vehicle could be conveniently used in both laboratory and production settings, and included a standard BGA component pattern with a squared configuration of pads (see figure 4). Cross sectioning and inspection for microvoiding was conducted across a row of these pads. Our standard procedure called for 16 pads to be analyzed across a cross-sectioned row.
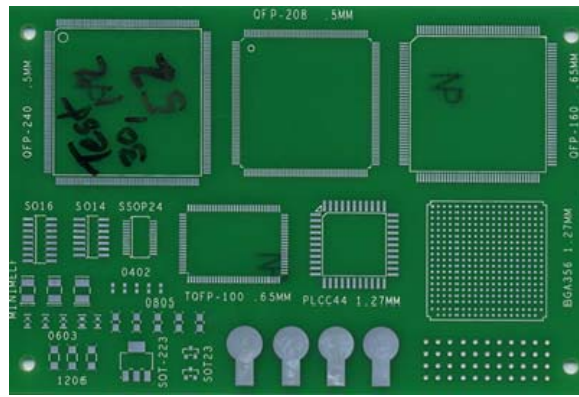
Figure 4 - Standard Test Vehicle with BGA Feature

Microvoid levels were then quantified and plotted utilizing the illustrative scale shown below in figure 5. This ranking system was scaled from zero to nine, where zero indicated an essentially void-free interface and 9 equated to near complete coverage of the pad.
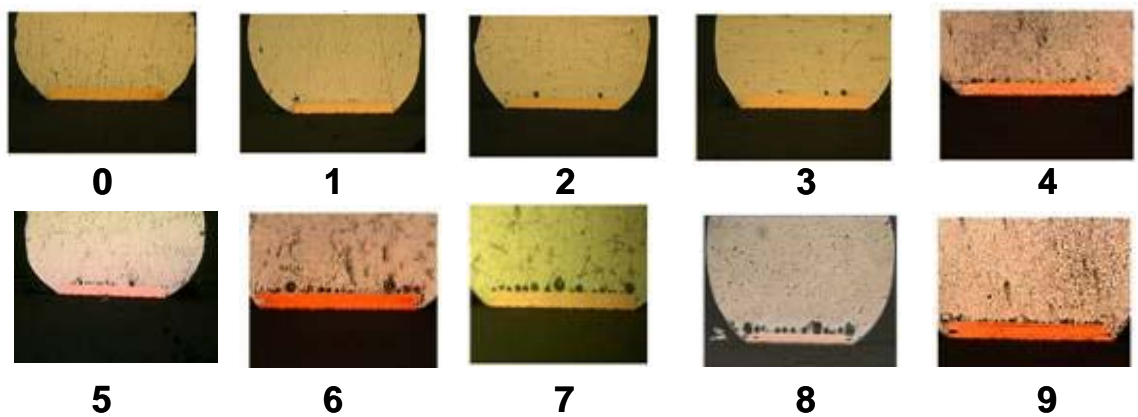

Figure 5 - Scale Used to Rank Microvoid Severity

A Review of Key Microvoid Enablers

In 2005 and 2006, following a significant investigation aimed at identifying factors which influence microvoid formation, MacDermid published the results of their work[2, 8, and 9]. This work identified two key process variables as being influential in enabling microvoid formation in a subsequent assembly operation. From this, corrective actions in the form of simple process modifications were incorporated into the "best practice" operating conditions for the MacDermid Immersion Silver plating chemistry. These key process modifications are addressed individually below.

1. Choosing the Appropriate Microetch

Figure 6 shows the results of a key study which involved the manipulation of several process variables, including microetch type. For this work, we prepared samples utilizing two commonly used microetches: an acidic peroxide based chemistry known to produce a more rough topography and a proprietary acidic persulfate based chemistry which delivers a smoother topography. Silver thickness was maintained at 0.25 microns. As figure 6 shows, samples processed through the persulfate based etch exhibited negligible microvoid levels; whereas those processed through the peroxide chemistry consistently produced significant voiding. This plot simply displays a sorted view of microvoid intensity, with microetch type highlighted; other influential factors are discussed later.
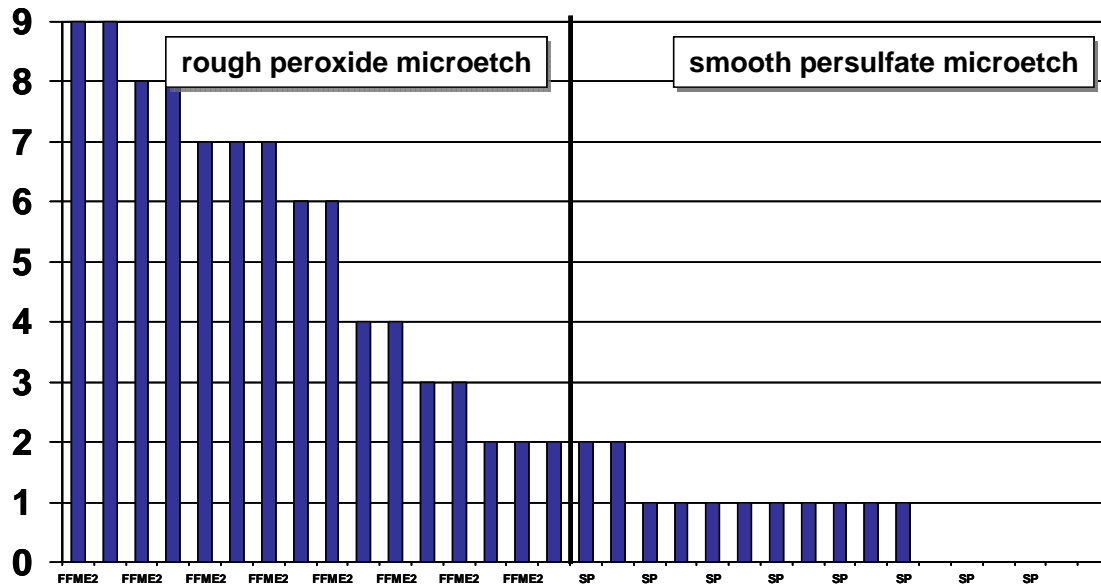
Figure 6 - Microvoid Results from One Study, Sorted by Severity and Microetch Type

In an effort to further validate this important effect, we chose to investigate the role of the rough topography microetch on a silver coating deposited from an alternative immersion silver chemistry claimed to be intrinsically resistant to microvoid formation, referred to as "Process A"[10]. Figure 7 below illustrates typical void levels from deposits processed through peroxide and modified persulfate based etches respectively. Again, all silver thicknesses were maintained at 0.25 microns. These results clearly support the claim that basic peroxide microetches commonly used in PCB fabrication sites (these etches do not typically contain additives which impart a polished surface) strongly induce and enable microvoid formation, independent of the silver plating chemistry employed.
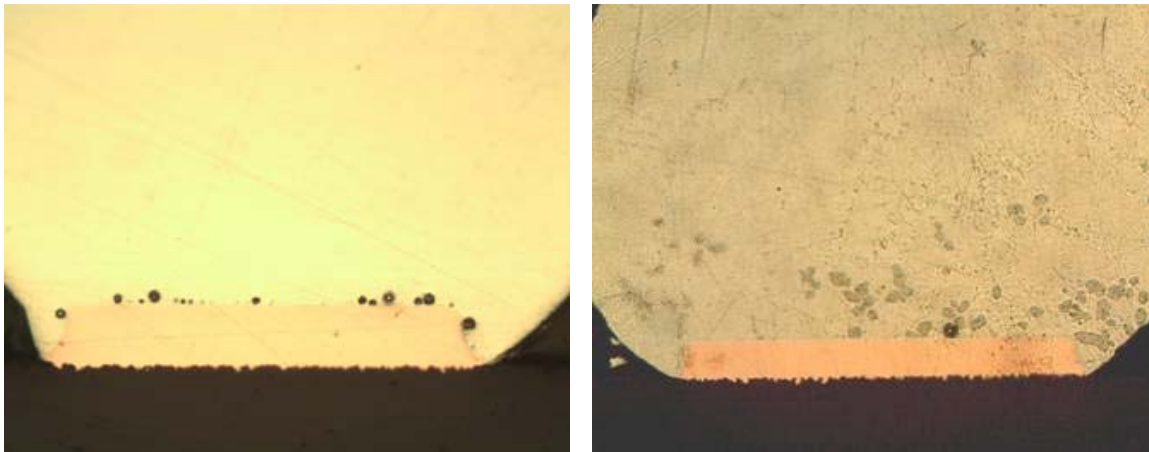

Figure 7 - Microvoids produced from "Process A" utilizing peroxide and persulfate etches

The strong effect observed via microetch naturally led to a question of what may be the cause of the phenomena. A close look at the surface topography of copper provided some clues. Figures 8 and 9 show SEM and Atomic Force Microscope (AFM) images of copper surfaces processed through each respective etch. A clear difference in structure is observed. One explanation offers that structural features produced by widely used peroxide treatments may result in highly active sites and localized non-uniform silver deposition in this area.
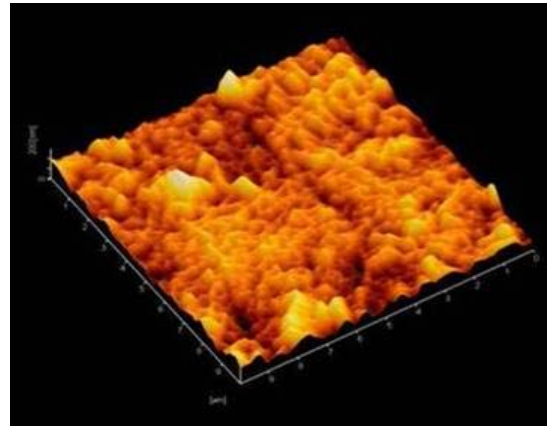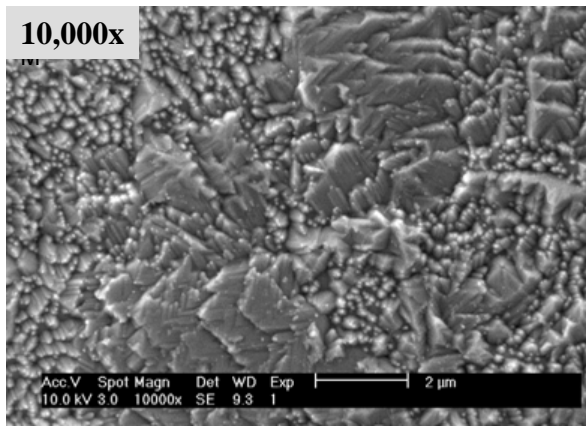
10,000x

Figure 8 - Structure of Peroxide Etched Copper by SEM and AFM
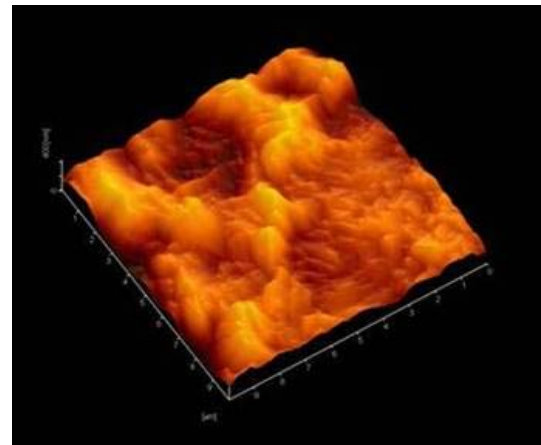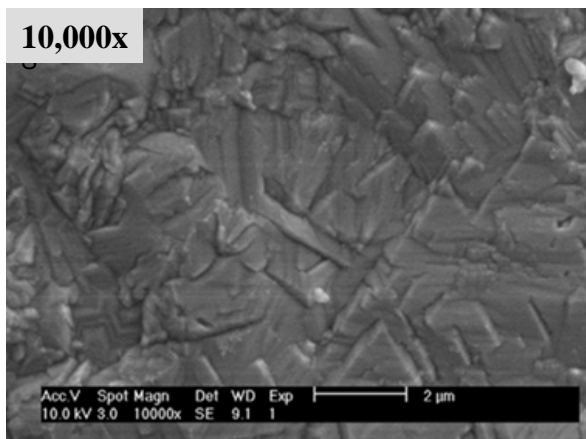

10,000x

Figure 9 - Structure of Persulfate Based Etched Copper by SEM and AFM

2. Controlling the Kinetics of Silver Deposition Through Reduced Silver Concentration.

Additional studies identified the rate of the immersion silver plating reaction to also be influential on the formation of microvoids. Figure 10 below shows output from a full factorial DOE which included silver concentration as a factor in the formation of microvoids. In this testing, two silver thicknesses were examined, 0.37 and 1.5 microns. Though not as dramatic as the microetch effect, the result is clear and statistically valid.
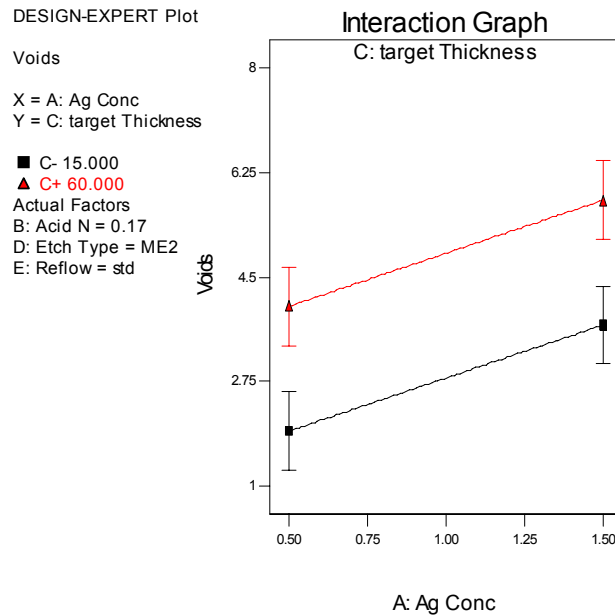
Interaction Graph
C: target Thickness

Figure 10 - Effect of Silver Content and Silver Thickness on Microvoiding

Mechanism for Microvoid Formation

A combination of internal work and discussion/cooperation with others studying the microvoid phenomena led us to more detailed investigation aimed at better defining a mechanism for microvoid formation[7]. The enabling effects of peroxide etch and higher silver concentrations were repeatable in a lab environment, but these results did not offer a mechanism for void formation. A very important finding involved the identification of "caves" underneath the plated silver surface in samples which subsequently exhibited void formation. Figures 11 and 12 exhibit images of cross-sectioned, silver plated test vehicles. Images shown in figure 11 were processed through conditions which promote microvoid formation (peroxide microetch and higher silver concentration). The cavities/vacancies observed underneath the plated silver have come to be commonly referred to as "caves"; they could be consistently produced by processing materials through the "enabling" conditions discussed above. Figure 12 shows few to no caves; these images were processed under conditions which promote a microvoid-free assembly (persulfate etch and lower silver concentration). These samples consistently yielded microvoid-free solderjoints/assemblies.
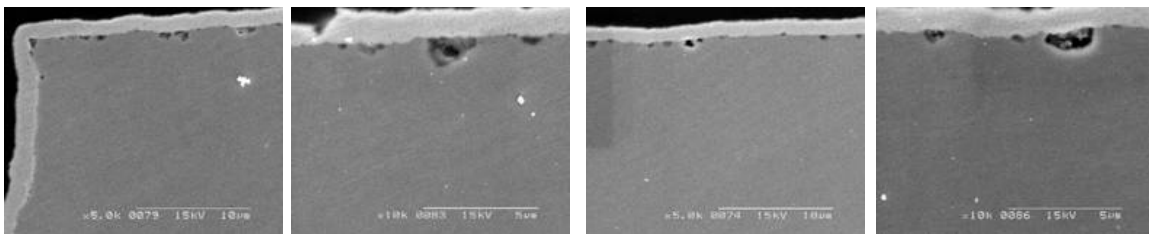

Figure 11 - Caves Produced Under Silver Coating Processed Through Peroxide Microetch
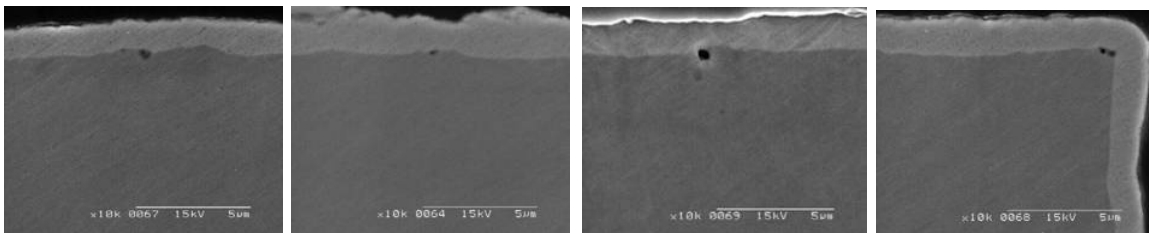

Figure 12 - Caves Produced Under Silver Coating Processed Through Persulfate Microetch

With the identification of the caving phenomena, a better mechanistic explanation for microvoiding is feasible. Images of caving are best seen via advanced tools such as Focused Ion Beam (FIB), but adequate analysis can also be obtained through careful and skilled traditional metallographic techniques (polishing).

Summarizing the work above, we propose the following as an explanation of the microvoid mechanism: The surface condition and topography of the copper as it enters into the silver plating step plays a critical role in the potential formation of caves, which eventually manifest as microvoids in the assembly/reflow operation. The topography created by the peroxide etch provides sites that are susceptible to cave formation in the plating step. This "susceptibility" to cave and microvoid formation may be enhanced if the copper is not effectively cleaned. Soldermask residues and scums may provide a seeding site for localized cave formation (copper corrosion) in the plating step. Furthermore, the driving force of the immersion silver reaction, when excessive, can result in hyper-corrosion at active sites on the copper surface, resulting in cave formation and silver bridging across the cave. An illustration of our proposed microvoid mechanism is shown in figure 13.
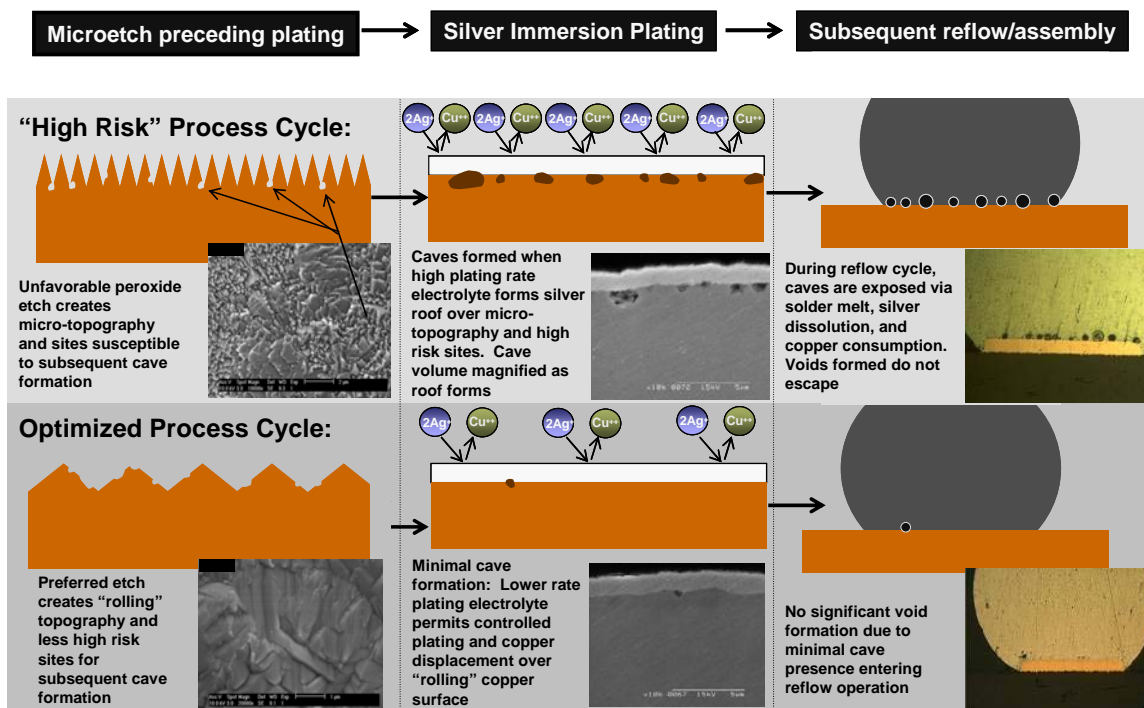

Figure 13 - Illustration of Proposed Microvoid Mechanism

Supplementing the mechanism proposed above, a key proposal is that the cave itself is leads to the formation of a microvoid. This may occur due the inability of entrapped air/gas to escape the molten solder. It may also be linked to the formation of water vapor through the reaction of hot solder flux with copper oxides on the walls of the cave.

Initial Production Verification

A next logical step in our problem solving effort involved testing the effectiveness of our microvoid "enablers" and corrective actions in a real-world production setting. Validating the effectiveness of our process modifications would be challenging since history clearly showed that very large volumes of product could be produced under "enabling" conditions without producing harmful microvoiding (it has been well documented that the microvoiding phenomena occurred very rarely and unpredictably). In part, our proposed mechanism suggests that the preferred conditions in the plating process offer a more robust process which forgives pre-existing conditions in the underlying copper which may encourage cave/microvoid formation.

Our initial field verification involved producing our standard test vehicle described in Figure 4 earlier at a high volume fabricator utilizing a peroxide based etch and old operating conditions (higher silver levels and lower temperature). This particular fabricator was also chosen because it utilized a second immersion silver chemistry from a process claimed to be intrinsically resistant to microvoid formation (referred to as "Process A" earlier in this paper)[10]. For this work, we started by running test boards with our control process. We then progressively altered three key variables (etch type, silver concentration, and plating temperature to assure deposit quality), sampling test boards as each process modification was made. Finally, we produced boards from immersion silver "process A" per standard operating practice for inclusion in our

evaluation. The silver thickness was held constant at approximately 0.25 microns throughout this testing (accomplished by altering immersion plating time) and subsequent microvoid analysis was conducted via cross-section technique as described earlier. A total of 5 test boards were run per condition, giving 80 individual void observations per condition (5 x 16 pads per board). The results from this work are displayed below in figure 14. While all microvoid results were relatively low and acceptable by most standards, it can clearly be seen that our key process modifications produced a statistically significant improvement in microvoid performance. This important result cleared the way for a modification of our best practice process recommendations for our customers.
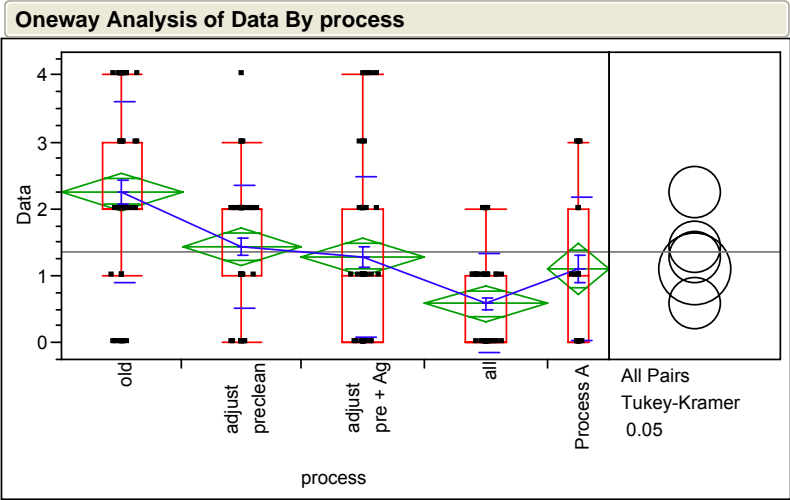

Figure 14 - Microvoid Results and Statistical Analysis of Production Implementation of New MacDermid Operating Parameters and Comparison to "Process A"

Best Practices for Assuring Microvoid-free Processing
Based on the work described above, the recommended operating parameters for our immersion silver chemistry was shifted to give processing conditions that minimized cave and microvoid risk. These changes were implemented throughout our customer base beginning in early 2006. The key modifications are summarized below in Figure 15 (though temperature changes were not highly influential on microvoid risk, higher temperatures assured a smooth and coherent silver deposit at reduced silver concentrations).

Key Variable	New Process	Old Process
Pretreatment Cycle	Final Finish Spray Cleaner + Sterling Surface Prep Microetch	Final Finish Spray Cleaner + Surface Prep Microetch or Microetch 2 (peroxide)
Silver Concentration	0.6-0.9 g/l Silver	1.0-2.0 g/l Silver
Plating Temperature	50-54 ºC	43-54 ºC

Figure 15 - Summary of New Best Practice Operating Conditions along with old practice

Production Experience
One of the large challenges historically plaguing the entire microvoid issue was the fact that they occurred extremely infrequently. Since millions of good immersion silver PCB's were produced under pre-2006 conditions without microvoid observations, it became clear that other factors were contributing to microvoiding. A basic premise underlying our mechanism proposal is that the microetch and plating kinetics are key variables in assuring that caves and microvoids are avoided, even if incoming copper is susceptible to cave formation; a logical hypothesis is the contribution from tenaciously adherent soldermask residues.

One strong example of this point is illustrated by an occurrence of microvoiding that we encountered early in 2006. This incident involved a fabrication site which suddenly experienced significant microvoiding; they had not yet converted to best practice operating conditions, but had been running problem free for an extended time. Upon converting to best practice conditions, the microvoiding disappeared permanently. Images of cave formation (via FIB) and microvoiding from past operating practices and new best practice conditions are shown below in Figures 16 and 17.
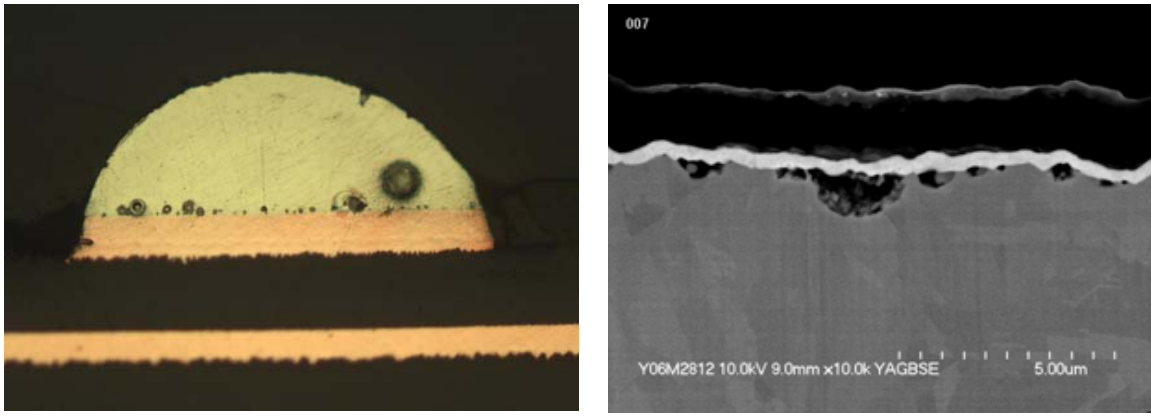
Figure 16 - Microvoids and Caves (FIB analysis) Produced Under Old Operating Conditions
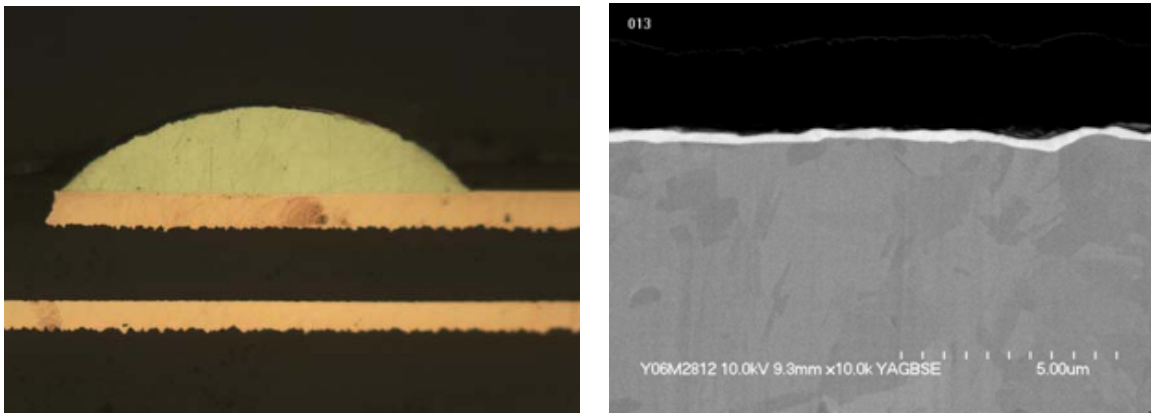

Figure 17 - Microvoid-free and Cave-free Samples Produced With New Best Practice Conditions

Controlled Production Verification

Despite the significant body of evidence supporting the effectiveness and validity of our process modifications, we conducted additional testing and data gathering aimed at further verifying our work. We had two basic objectives in this work. First, we wanted to confirm that our best practice operating conditions consistently produced boards with minimal to no microvoid occurrence throughout the useful life of our plating chemistry. Second, we wanted to critically compare the microvoid propensity of our process against self described intrinsically resistant "Process A"[10] described above. Given these two objectives, we selected two high volume fabrication sites that regularly used each chemistry. For each site and each plating chemistry, 10 boards were processed at standard conditions at 5 separate times spaced throughout the useful life of each electrolyte (starting with testing at bath make-up and ending at the time of bath disposal). This provided 800 data points for each chemistry at each fabricator (10 x 5 x 16 pads per board). For this work, we modified the metrics by which we quantified microvoid occurrence; this is discussed below.

The metrics employed for quantifying voiding were arrived at via discussion with others studying the microvoid phenomena. Initially, we employed a semi-quantitative grading scale which allowed analysts to approximate microvoid levels in any given analysis (referenced above). For this work, we implemented a more rigorous and quantitative technique for reporting microvoiding. This technique essentially amounts to measuring void size and counting individual voids for each joint analyzed. The specifics of our reporting methods are summarized below:

- Microvoids are classified as "type 1" and "type 2" as denoted by void size. "Type 1" voids are smaller than 15 microns in diameter. "Type 2" voids are larger than 15 microns (see Figure 18). All voids which are observed at the copper interface are considered to be microvoids.
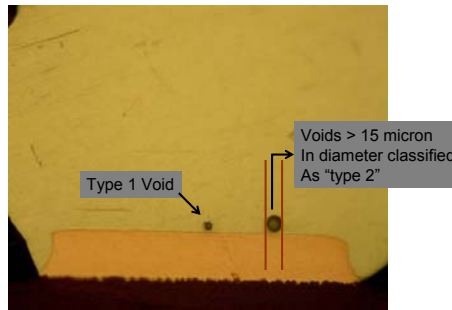
Figure 18 - Illustration of Type 1 and Type 2 Microvoids

- Microvoid responses are graphed in two ways: First, the distribution of type 1 void observations per pad is plotted. This allows even a single outlying bad joint to be identified. It also allows for trends in void propensity to be more easily seen. The second method for plotting microvoids involves plotting void occurrence for a set of pads on a given board. We report results which normalize the void data to an eight pad set (1/2 of the pads analyzed on our test vehicle). This provides an analysis which is capable of identifying individual board samples with moderate to high "pockets" of microvoids. These plots include references to upper limits for void occurrence (the limits represent the opinion of assembly experts with which we have worked).

The results of the work conducted at the two fabrication sites are presented in figures 19 through 21 below. This rigorous pad by pad analysis at multiple fabrication sites clearly indicates that our Sterling ™ Silver Best Practice consistently delivers a silver coating with minimal microvoid risk. This data also indicates that the two chemistries evaluated exhibit no significant difference in microvoid propensity.
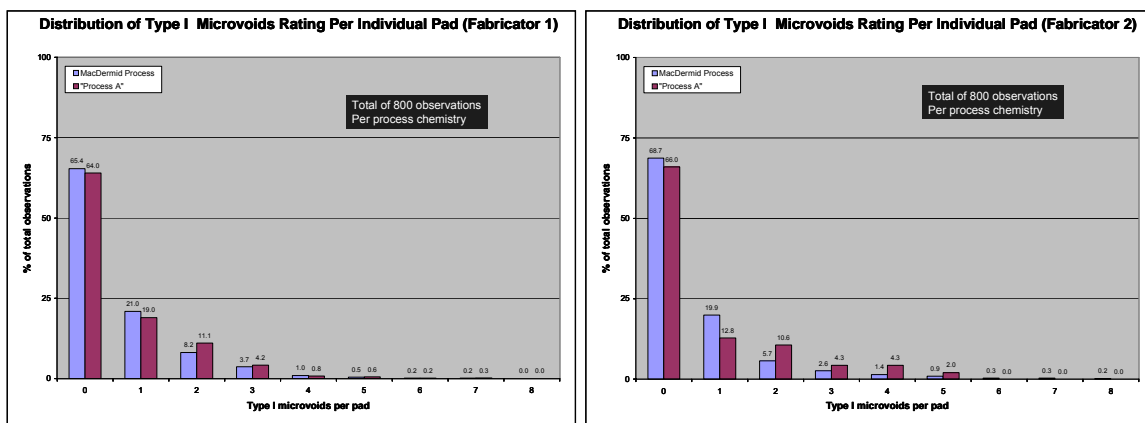

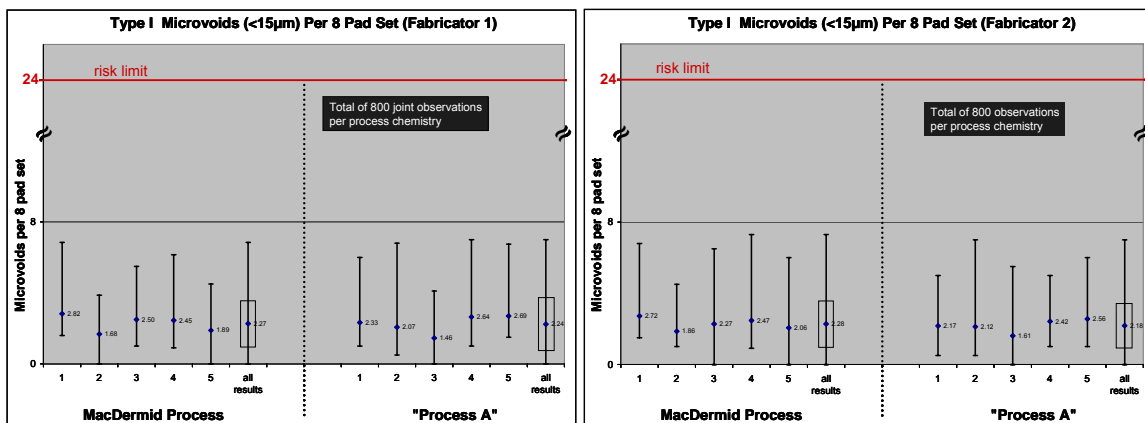**Figure 21 - Type 1 Void Distribution From 2 Process Chemistries at 2 Fabricators**

Figure 19 - Type 1 Microvoid Occurrence From 2 Process Chemistries at 2 Fabricators
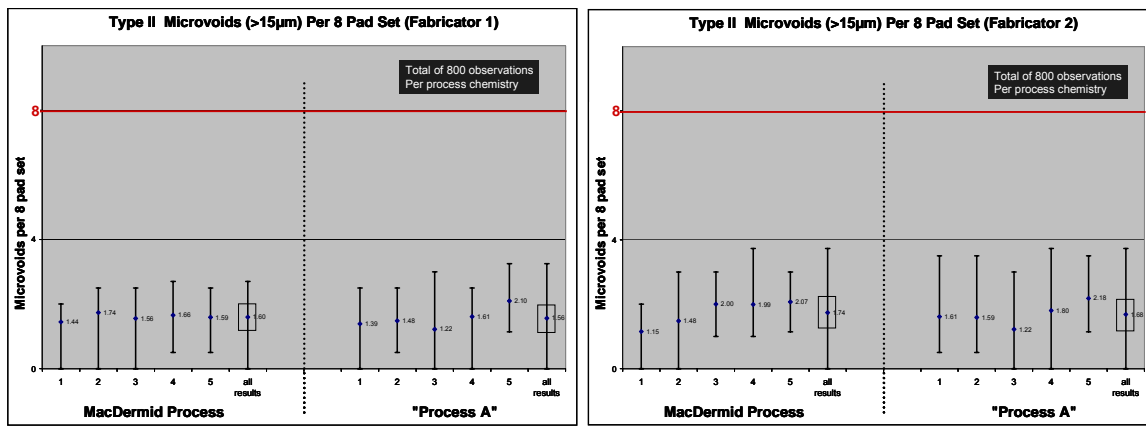
Figure 20 - Type 2 Microvoid Occurrence From 2 Process Chemistries at 2 Fabricators

Conclusions

- Theories linking cave formation to subsequent microvoiding have been verified through this work. Multiple observations, both in a laboratory and production setting, have confirmed that microvoid occurrences are necessarily linked to cave formation under silver plating.

- The silver pretreatment process, most notably the microetch, is a critical element involved in microvoid/cave prevention. It has been shown that a common peroxide microetch can induce microvoid formation with multiple plating chemistries. A propriety, modified persulfate etch has been demonstrated to be effective in preventing microvoid and cave formation.

- Further to the above point, an optimized MacDermid plating process has been identified which minimizes microvoid/cave risk. The critical elements of this process involve: appropriate microetch chemistry, reduced and controlled silver concentration, and operation at proper plating temperature to assure deposit quality.

- Sustained high volume production of quality circuit boards and assemblies via the above process throughout 2006 further verify the observations and conclusions above.

References

[1] IPC Executive Market and Technology Forum 2006 Estimates

[2] Cullen, D, "Characterization, Reproduction, and Resolution of Solder Joint Microvoiding", APEX 2005, Anaheim, February 2005

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[9] J. Swanson, "Planar Microvoiding", Intel Lead-free Technology Symposium, Scottsdale AZ, March 2006

[10] Y. Yau et al, "A Study of Planar Microvoiding in Pb-free Solder Joints", TPCA Forum, Taipei, October 2006