A STUDY OF PLANAR MICROVOIDING IN Pb-FREE SOLDER JOINTS

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Abstract

Planar microvoids have been observed on second level interconnections between solder metallizations and copper lands on PCB boards with immersion silver surface finish. These planar microvoids differ in size and density from the more common process voids that are found in solder joints. However, unlike the process voids, these planar microvoids reduce the reliability margin by accelerating crack propagation during thermal cycling. Therefore, desired target limits on the density of microvoids of different sizes are established. Monitoring of microvoids observed during PCB assembly production correlates the occurrence of microvoids to "caves" found in the copper land underneath the immersion silver coating on the bare PCBs of the same production lots. A mechanism is proposed to explain how the caves lead to microvoids during the reflow process. While a thick silver coating and a rough copper substrate were attributed as probable causes for microvoids in a previous study, a DOE is conducted in this study using a commercial immersion silver process, to evaluate these two factors together with silver bath chemistry and PCB substrate. There are no caves found in any of the conditions in the DOE, even for an extremely thick silver coating (more than 3 microns). Although the thick silver tends to have a slightly higher microvoid density, it is still well below the desired target limits, indicating the occurrence of microvoids is also chemistry dependent.

Introduction

Planar microvoids, also referred to as "champagne voids," are smaller than two mils (50 μm) in diameter [1]. They are found above the intermetallic compound (IMC) layer at the interface between the solder joint and the copper land on the PCB. Planar microvoids differ in size and density from the more common process voids, also called macrovoids, that can be found anywhere in a solder joint. Because they are actually a group of "empty bubbles" within the solder joint in a plane, they have a devastating effect on solder joint strength by accelerating solder cracking during thermal cycling as well as mechanical shock and drop. Reliability of the solder joint is further impacted when dealing with advanced fine pitch technology, such as BGA applications, as the chance of cracking increases.

Arrigotti [2] has shown that excessive microvoids lower the solder fatigue margin in an accelerated temperature cycle test. As shown in Figure 1, for PCBs with excessive microvoid densities such as lots 3, 5 and 6, cracks in the solder joints initiated early and propagated at a very fast rate, i.e., reaching 75% after 400 cycles and 100% after 500 cycles for lot 3. On the contrary, for lots with low microvoid densities such as lots 1 and 2, cracks initiated at a much later stage of the temperature cycling test. No crack area was detected after 500 cycles for both of them.

From lots that showed microvoids after assembly, the retained, pre-SMT assembled PCBs were examined by using focused ion beam (FIB) and scanning electron microscope. These cross sectional and surface analyses revealed "caves" in the center of copper lands on the pre-assembly PCBs [1, 2]. As shown in Figure 2, the "cave" under the immersion silver coating is approximately 1 μm in size and covered with oxide. It's suspected that this cave was caused by

contaminants of sub-micron organic particles or inorganic residues on the copper surface entering the immersion silver process. If these surface contaminants dislodge in the middle of the deposition process, the freshly exposed copper becomes a localized anode that preferentially oxidizes to provide electrons for the reduction reaction of silver ions taking place on the silver coating, resulting in a "cave". The presence of "caves" has also been found underneath the solder mask in solder mask defined pads. This is the well-know phenomenon of "galvanic attack" induced by the crevice between the solder mask and copper trace [3].

During the SMT reflow process, after the silver coating dissolves into the solder, the flux from the solder paste reaches into the caves, reducing the oxides and producing gaseous bubbles. If these small bubbles adhere to the intermetallic layer formed between the solder and copper, and don't have enough time to coalesce and rise, they will form a plane of microvoids on top of the IMC when the solder freezes.

Because of the reduced reliability in the thermal cycling test, PCB pre-production lots were screen tested for planar microvoids prior to full motherboard assembly at electronics manufacturing services (EMS) supplier sites. In this EMS monitor program, six boards were sampled from each lot of five hundred boards from each immersion silver production line of the PCB suppliers. After planting solder balls on BGA pads by mimicking the SMT assembly processes, the solder joints were cross sectioned and examined for microvoids. To better describe the size variations among these microvoids, they were separated into two groups; "small" microvoids for those with diameters less than the thickness of the IMC layer (about 5 μm), and "large" microvoids for those with diameters greater than the thickness of the IMC layer but less than 25 μm. As shown in Figure 3, the screening test results indicate that there is a wide spread in the propensity of planar microvoid formation. A "mean" number of "large" microvoids per solder joint less than 1, and a "mean" number of "small" microvoids per solder joint less than 3 were arbitrarily chosen as the "target" limits. Only lots that passed the screening test were used in production.

Based on these "target" criteria, the failure rate over a period of time from 17 production lines using four immersion silver chemistries at eleven PCB fabricators was analyzed. Considerable variability was found among the immersion silver chemistries as well as among the PCB suppliers who plated the immersion silver on the boards. As an example, boards from one particular PCB supplier using a particular immersion silver chemistry had a failure rate as high as 40%, but boards from the same PCB supplier using a different immersion silver chemistry had a 0% failure rate. This suggests immersion silver chemistry is one critical factor for the generation of planar microvoids.

Nevertheless, no consistent, definitive root cause has yet been found responsible for planar microvoid formation. Cullen [4] reported that microvoids are most prevalent in cases where the underlying PCB copper has a very rough topography and an excessive immersion silver plating thickness. Yu et. al [5] and Lee [6] indicated that microvoid occurrence seems to be related to the extent and composition of organic matter co-deposited in the silver deposit. In this study, a DOE was conducted to verify that the use of a specific immersion silver chemistry is a critical factor in preventing microvoid formation.

Design of Experiment

A two-level, full factorial DOE was conducted to determine if the immersion silver process AlphaSTAR® would generate

microvoids under extreme process conditions, utilizing different microetches, variable plating times and different PCB fabrication suppliers. The silver bath chemistry was adjusted from the normal condition to increase the deposition rate by lowering the pH from 2.0 to 0.8 and increasing the silver ion concentration from 0.5 to 1.5 g/l. The fast deposition rate was expected to produce a more porous silver deposit and increase galvanic corrosion and thereby "caves" in the copper substrate. The etch type was expected to have an impact on cave formation from prior studies using the other silver chemistry [4]. A hydrogen peroxide-sulfuric acid etch (AL-1000) was used to produce a semi-polished surface, while a persulfate-sulfuric acid etch (PC-7077) was used for a matte surface. The dwell time in the silver plating bath was increased to simulate the re-work process occasionally required and to exacerbate the microvoiding tendency by increasing the chance for galvanic corrosion and cave formation. The dwell time was set for 2.5 and 7.5 minutes for the normal deposition rate, and 1.5 and 4.5 minutes for the fast deposition rate. Finally, two PCB suppliers representing suppliers that had generated low and high levels of microvoids historically in the EMS monitor program were used to determine the impact of copper surface and/or copper plating.

Test coupons (3.25" x 3.25") were cut out from full size motherboards so that they could be processed in beakers. Four test coupons were plated under each condition following the standard procedures; i.e., cleaning, rinsing, microetching, rinsing, pre-dipping, silver plating, rinsing and drying [7]. The silver thickness on 0.5 mm diameter BGA pads was measured by x-ray fluorescence (XRF).

The propensity for microvoid formation was evaluated by planting SAC405 solder balls (24 mils diameter) using SAC405 solder paste through the SMT reflow process. Cross-sections of 31 or 33 solder joints from each test coupon were examined for the presence of "small" and "large" microvoids. The numbers of microvoids for each group were counted to calculate the microvoid densities, i.e., mean number of microvoids per solder joint.

Results of DOE

Three measurables, including mean number of small microvoids, mean number of large microvoids, and percent solder joints with at least one microvoid, were analyzed against the four independent variables of plating condition, microetch type, plating time and PCB supplier. As shown by the "main effect" charts in Figure 4, only plating condition causes a significant effect on all three measurables. With a fast deposition rate from the low pH and high silver ion concentration, the propensity for microvoiding is doubled. The mean of the mean number of small microvoid per solder joint increases from 0.015 to 0.05, the mean of the mean number of large microvoid per solder joint increases from 0.05 to 0.09, and the percent solder joint with at least one microvoid increases from 8 to 16%. The matte finish from PC7077 is slightly better than the semi-polished finish from AL-1000. The plating time has little effect. The effect of PCB supplier, however, is somewhat mixed. The "Bad" PCB supplier has more small microvoids, but less large microvoids and a lower percentage of solder joints with microvoids.

In addition to the four explicit independent variables in the DOE, the propensity for microvoiding is also examined against the implicit variable of silver thickness, which is a controlled parameter by customer specifications in PCB manufacturing. As shown in Figure 5, there is only a slight increase in both the small and large microvoid densities as the silver thickness increases from 0.12 to 3.8 µm (5 to 150 micro inches). This result indicates that silver thickness is not a contributing factor for AlphaSTAR®, as it is for the immersion silver chemistry described in [4].

No caves were found in the copper land in any of the test coupons, but galvanic attack is noticeable underneath the solder mask, especially at extremely high silver thickness. As shown in Figure 6, at 3.8 µm silver which is twenty times of the normal thickness, a groove of 8.5 µm deep and 37 µm wide is observed underneath the solder mask. Air and possibly flux entrapped in the groove lead to "process" voids, as shown in Figure 7. This ring of bubbles along the edge of solder mask is less than 9% of the total cross section for Class III requirement per IPC 7095 specifications for process voids.

Compared to the EMS monitor results, Figure 8, the microvoid densities from the DOE are extremely low and tightly distributed. Even under the extreme plating conditions, the propensity for microvoiding is well below the target limits, suggesting that our immersion silver chemistry is inherently resistant to microvoiding, and that the process is robust to accommodate the variations in surface topography of copper substrate often expected from electroplating copper and making solder mask.

"Normal" Conditions

Since the condition of low pH and high silver concentration is not realistically going to happen in a production line using our chemistry described above, the results from normal bath and short plating time, i.e., typical production condition, are further analyzed even though the numbers of microvoids are very small. As shown by the main effect charts in Figure 9, the matte finish from PC-7077 produced better results than the semi-polished finish from AL-1000 for all three measureables. There was a difference between PCB suppliers. However, since the numbers are very small, the difference could be caused by missing one microvoid in the cross section examined, i.e., one out of 33 solder joints or 3%. It's also noticed that the silver thickness (or the deposition rate) is much higher on the matte surface than the semi-polished surface, Figure 10. Finally, as expected, no galvanic attack is found underneath the solder mask, Figure 11.

Conclusions

(1) Our process for immersion silver process is intrinsically resistant to cave and microvoid formation and capable of overcoming copper surface variations.

(2) The fast deposition rate from the low pH/high silver concentration bath results in higher microvoid densities, however, these densities are well within the desired limits.

(3) The type of microetch has no significant effect on microvoid densities, but the matte microetch results in a higher silver thickness.

Acknowledgement

The authors would like to thank Raiyo Aspandiar and Vasu Vasudevan of Intel for their collaboration in preparing samples through SMT assembly process, evaluating the microvoiding propensity, as well as analyzing the reliability impact of planar microvoids on BGA solder joints.

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[6] N-C. Lee, “How to Control Voiding in Reflow Soldering”, Chip Scale Review, August-September 2005

[7] Y-H. Yau et al., “The Chemistry and Properties of a Newly Developed Immersion Silver Coating for PWB”, IPC/APEX, Anaheim, CA, 2004

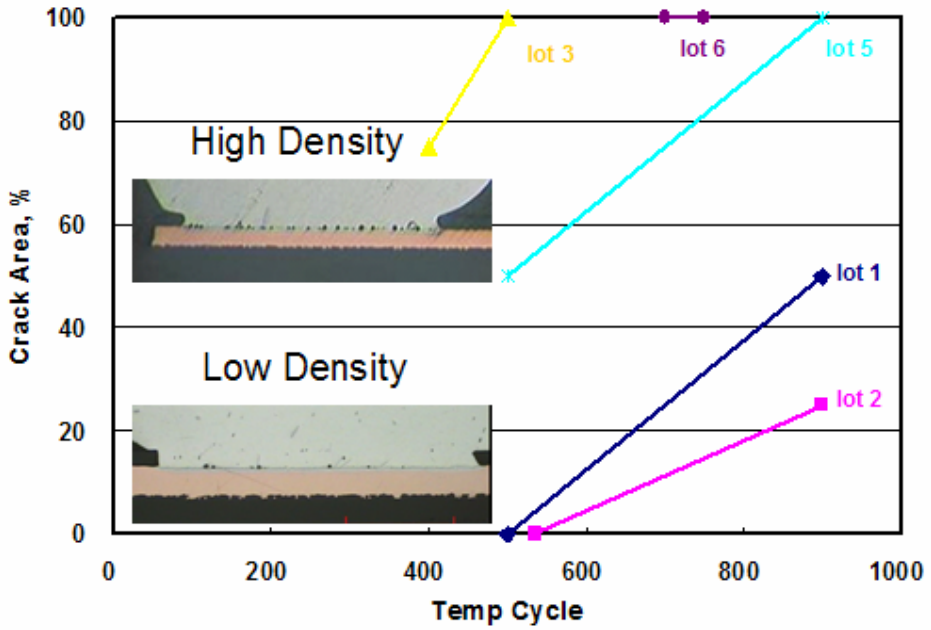

Figure 1 - Effect of Microvoids on Solder Fatigue Cracking within SAC405 Solder Joints [2]

(Source: Intel Corporation approaches, experiments & tests are in pre-production environment. Intel makes no guarantee of the same or similar results in your pre-production or manufacturing environment.)

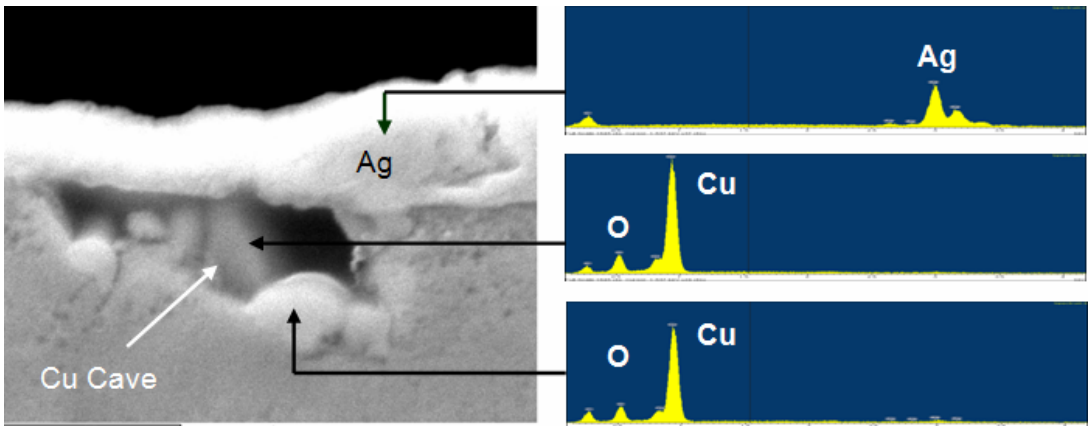

Figure 2 - Cross-Section and Chemical Analysis of a PCB Cu Cave Using Scanning Electron Microscope [1].

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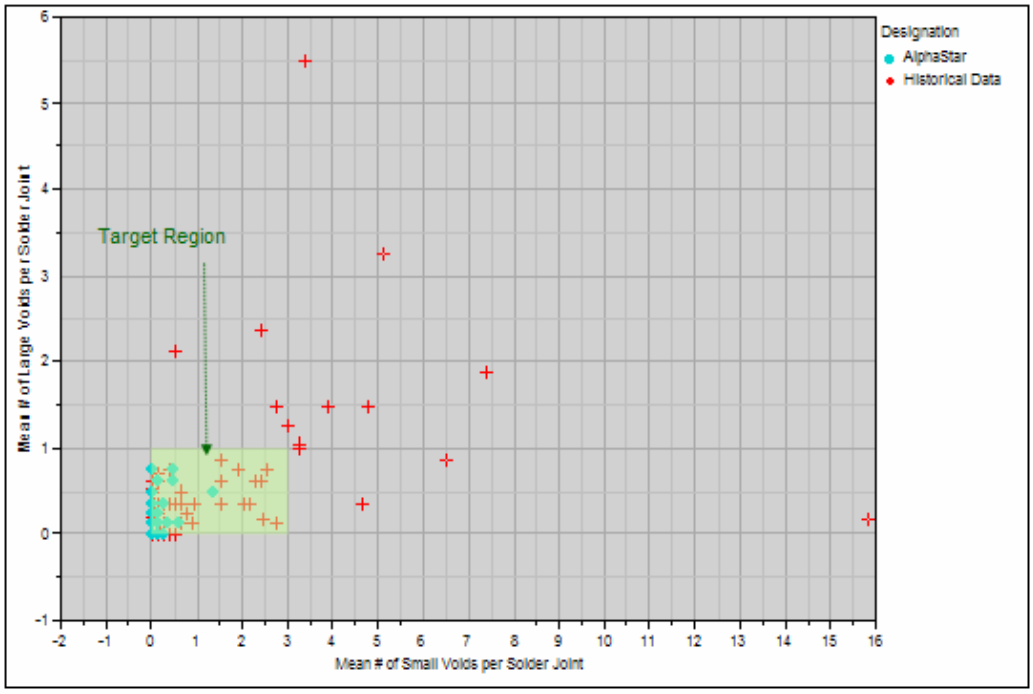
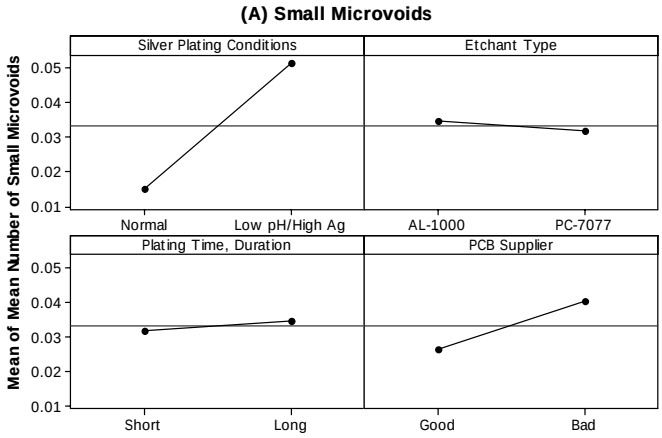
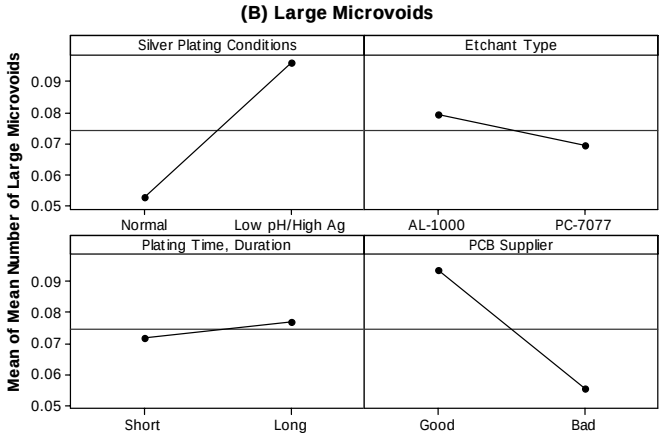


Figure 3 - Planar Microvoid Density Distribution for Historical Data vs. Our Silver Surface Finish

(Source: Intel Corporation approaches, experiments & tests are in pre-production environment. Intel makes no guarantee of the same or similar results in your pre-production or manufacturing environment.)





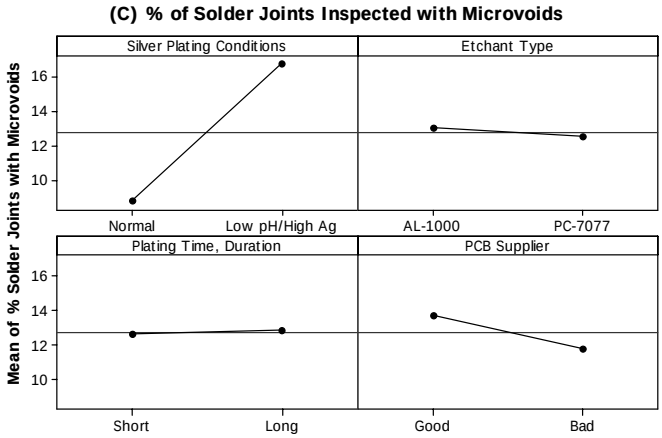


Figure 4 - Main Effects Plots for (A) Small Microvoids, (B) Large Microvoids, (C) % Solder Joints Inspected with At Least One Microvoid

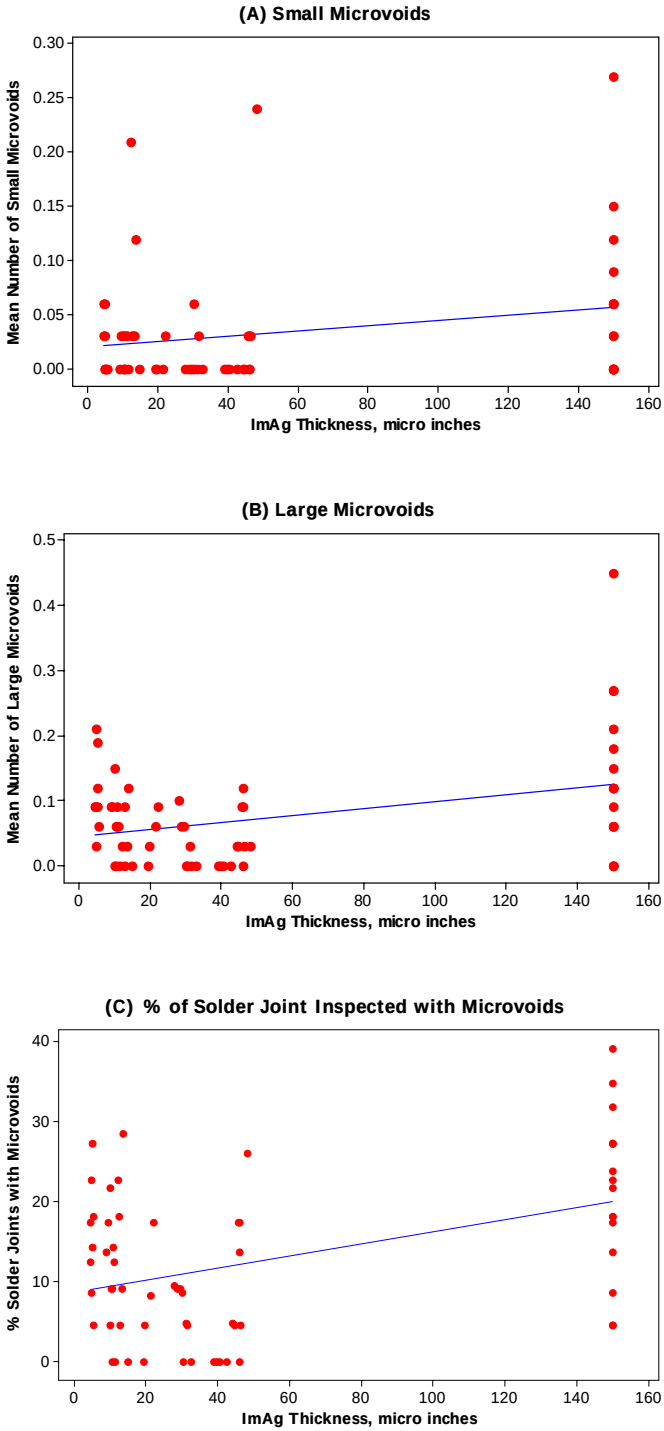


Figure 5 - Effect of ImAg Plating Thickness on (A) Small Microvoids, (B) Large Microvoids, and (C) % of Solder Joint Inspected with at Least One Microvoid

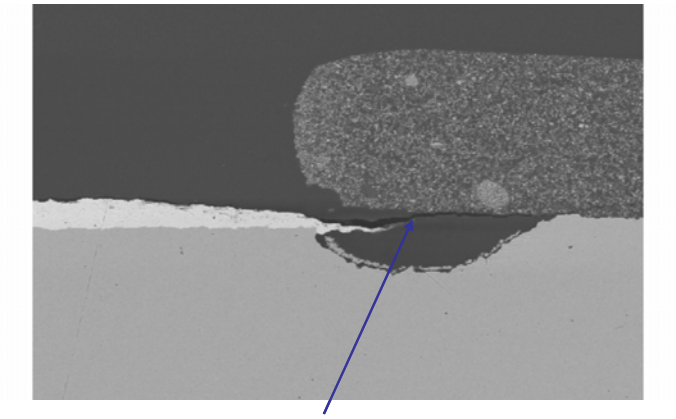


Figure 6 - Galvanic Attack from Thick Immersion Silver Plated at Low pH and High Silver Ion Concentration

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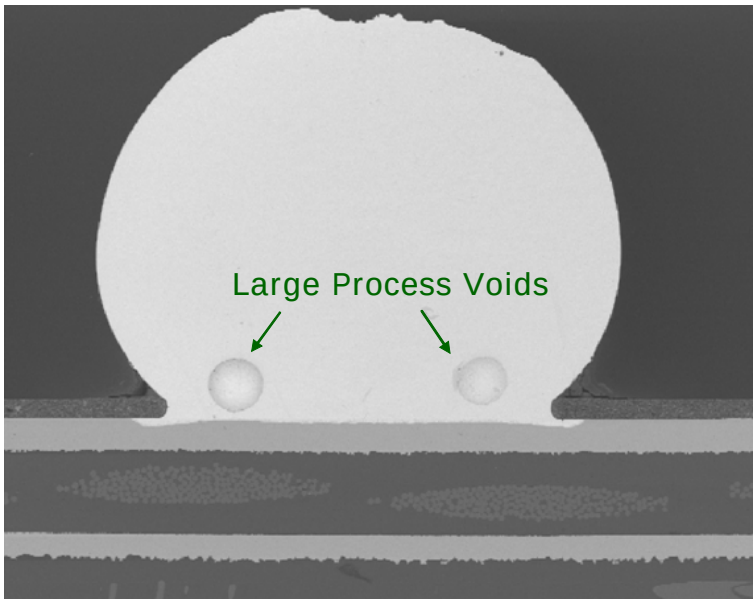

Figure 7 - Large Process Voids in Solder Joint on Solder Mask Defined Pad with Galvanic Attack

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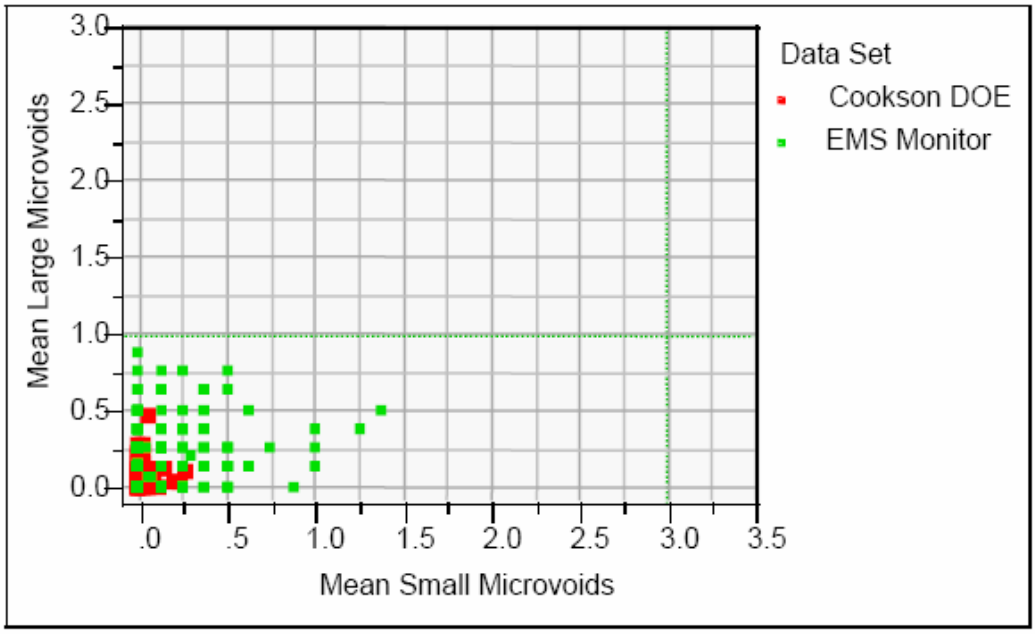

Figure 8 - Microvoid Density Distribution for the DOE Compared with the EMS Monitor Data of Our ImAg Process

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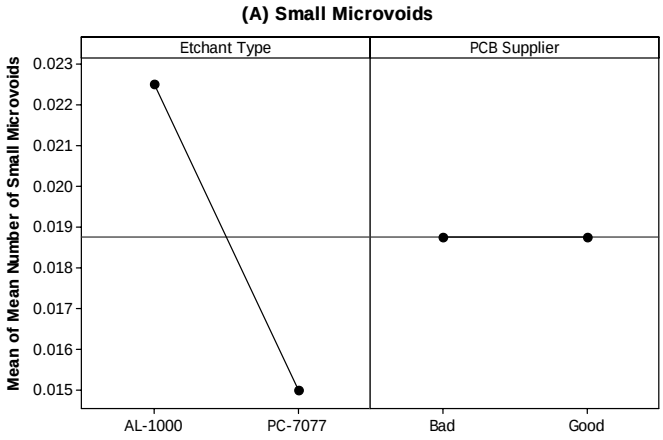

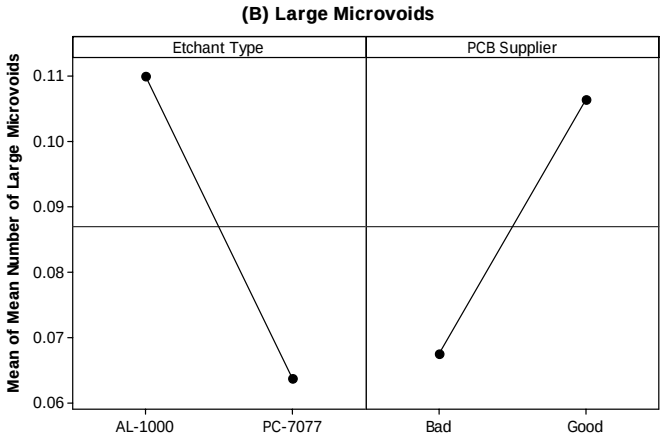

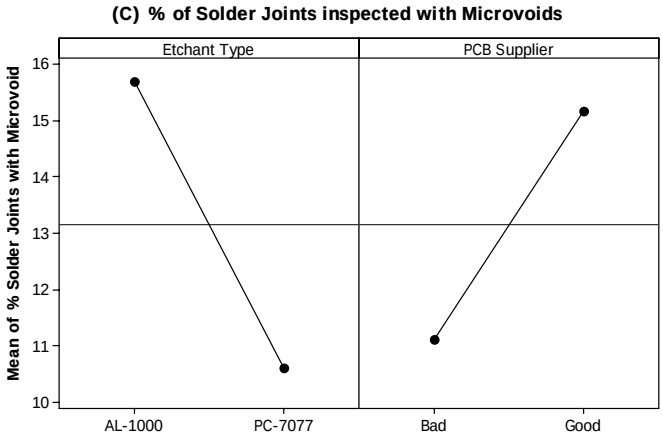

Figure 9 - Main Effects Plots from ImAg Plating from a Normal Bath for (A) Small Microvoids, (B) Large Microvoids, (C) % Solder Joints Inspected with At Least One Microvoid

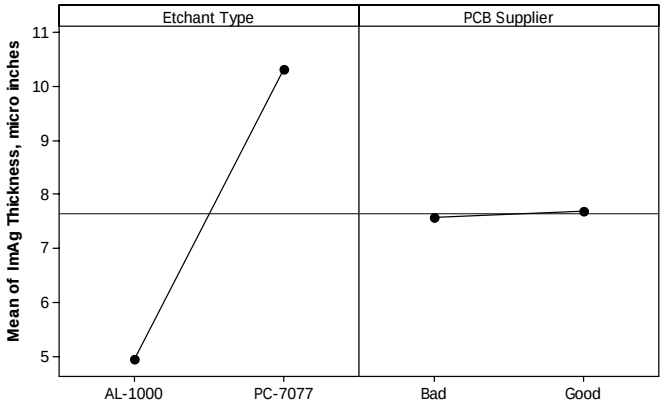

Figure 10 - Main Effects Plot for ImAg Thickness from a Normal Plating Bath

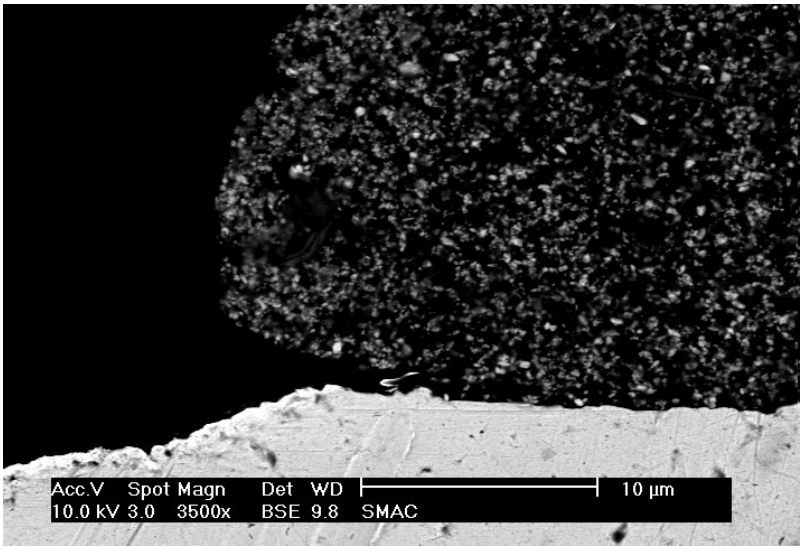

Figure 11 - Cross-Section Photo Showing the Lack of Galvanic Corrosion of the Copper Land under the Solder Mask for a Sample Plated with ImAg in a Normal Bath

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February 21, 2007

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Acknowledgement

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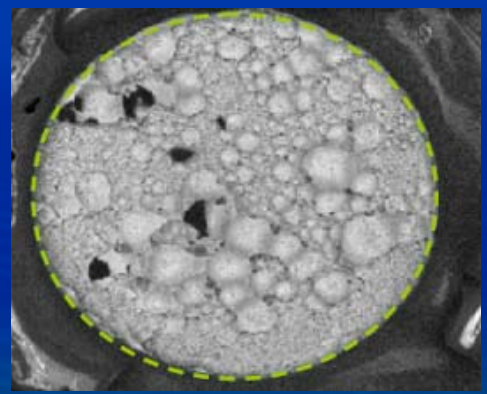
Outline

- Introduction
  - Effect of Microvoid on Reliability
  - Root Causes for Microvoid?
  - EMS Monitor Results
- Objective
- Design of Experiment
- Results
- Conclusion

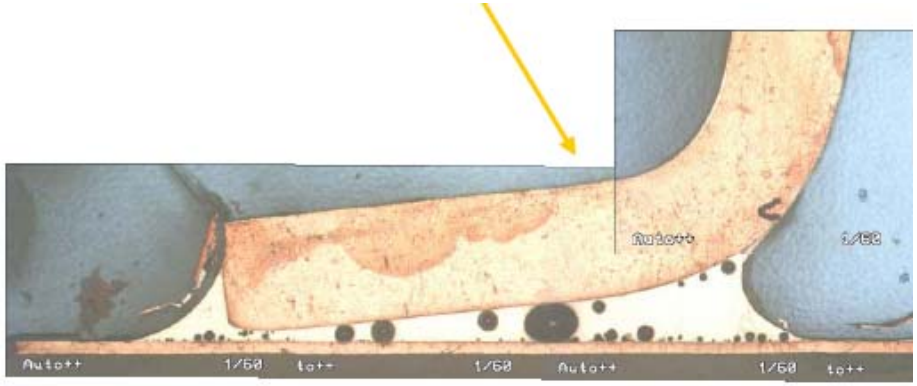
Planar Microvoids (Champagne Voids)

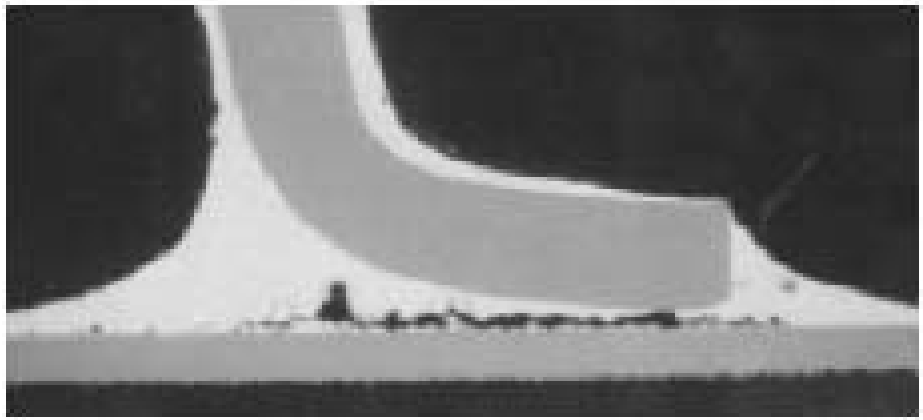
- A layer of voids in the ball-to-board interface, immediately above the Inter-Metallic Compound (IMC) layer
- Less than 0.002” (50µm) diameter
- *Not* process voids. *Not* Kirkendall voids that appear *below* the IMC *after* reflow
- The occurrence of microvoids can vary with ImAg chemistry supplier, PCB supplier, and batch-to-batch from a single PCB supplier
- More prevalent on, but not exclusive to, soldermask defined (SMD) pads



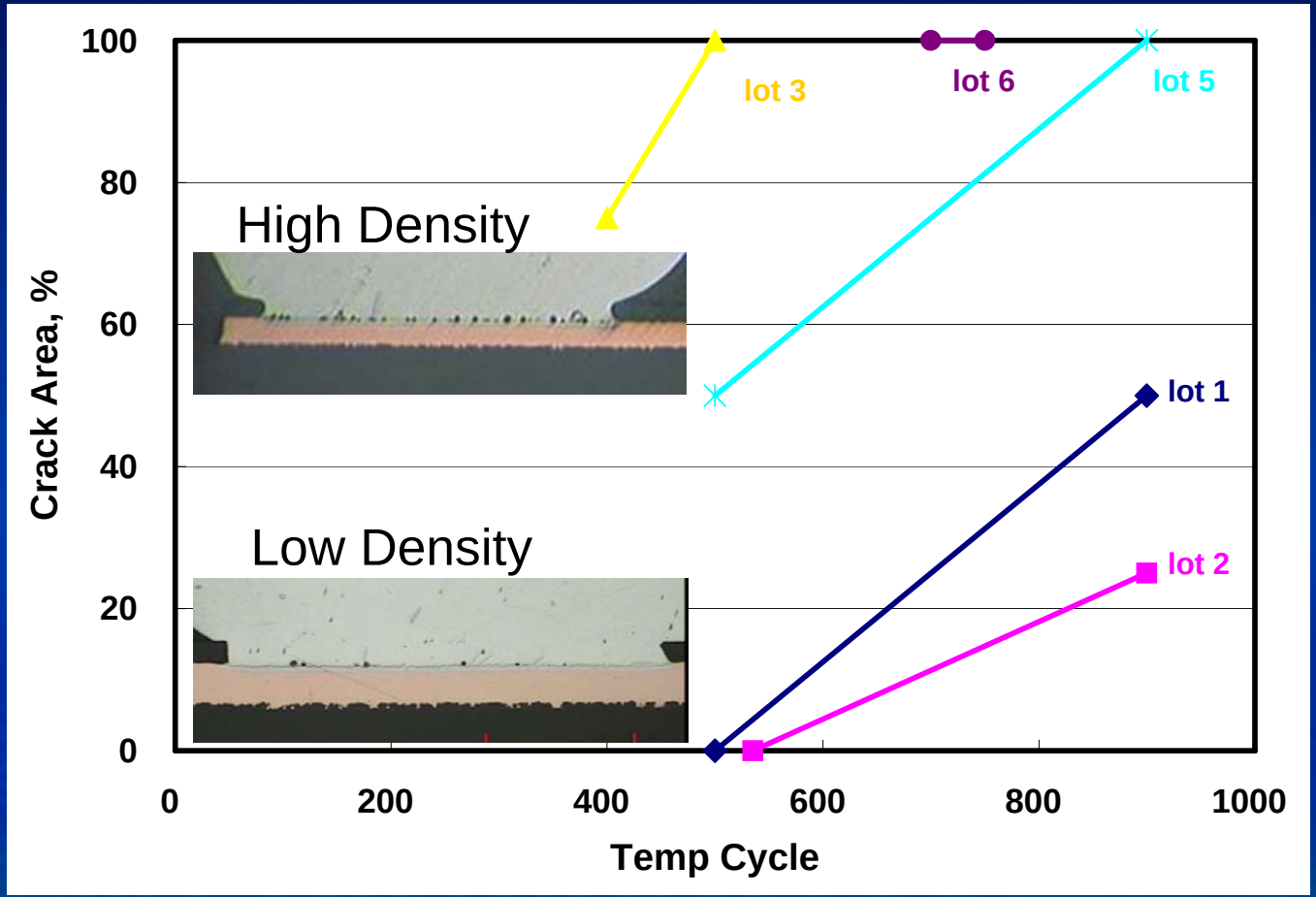
G. Arrigotti of Intel, IPC Committee 4-14, 2/9/06

Not Limited to BGA….





Effect of Microvoid on Solder Fatigue



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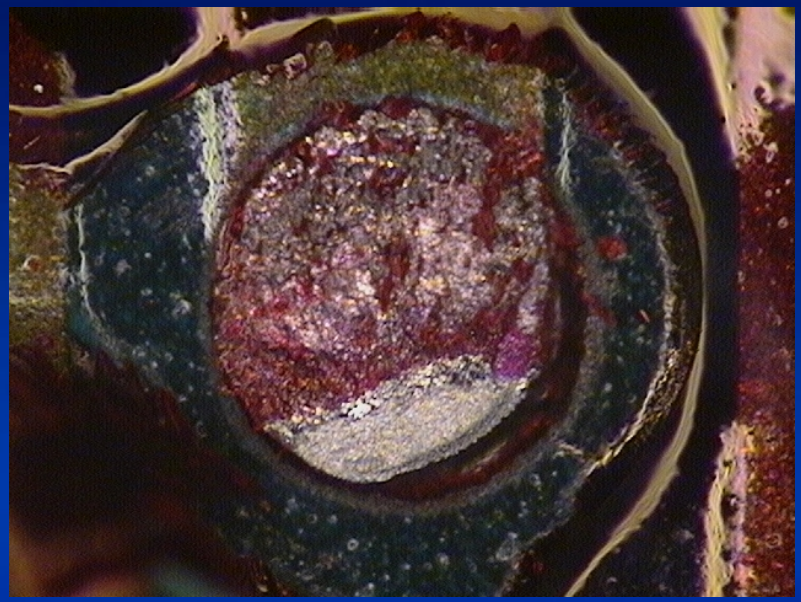
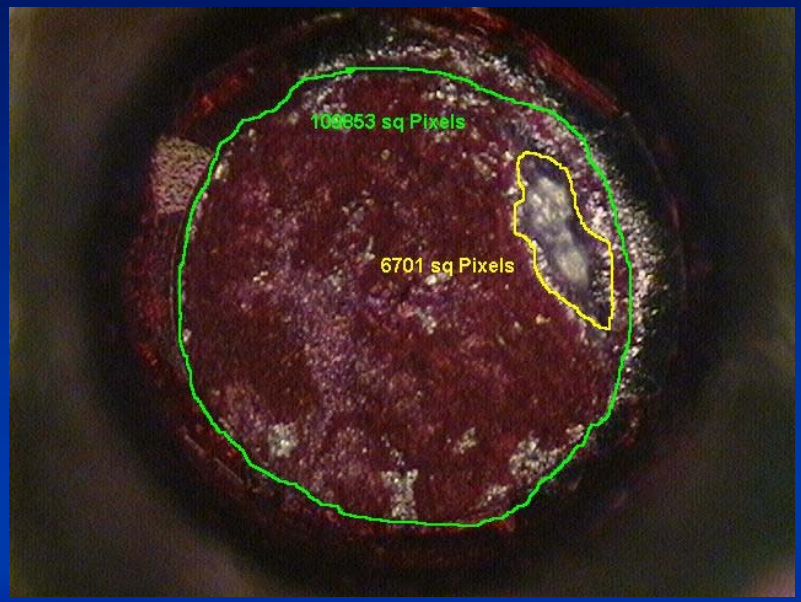
Solder Crack Area Metrology





- Solder crack area measurement
  - Dye and peel test followed by optical inspection
  - The measurement is based on grey scale image
  - The measurement variation
    - σ is 5% and 3 σ is 15%

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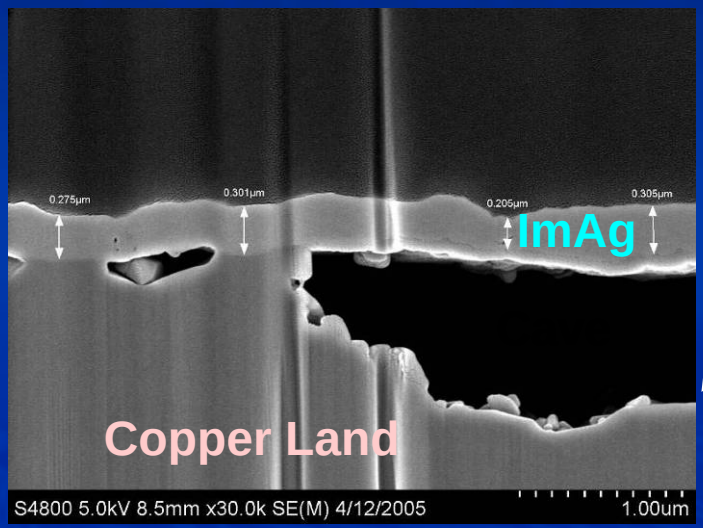
(A) “Cave” Theory for Planar Microvoids

‘Copper Caves’ are small (~1 µm) enclosed cavities in copper lands, under the ImAg plating, in as-received PCBs.

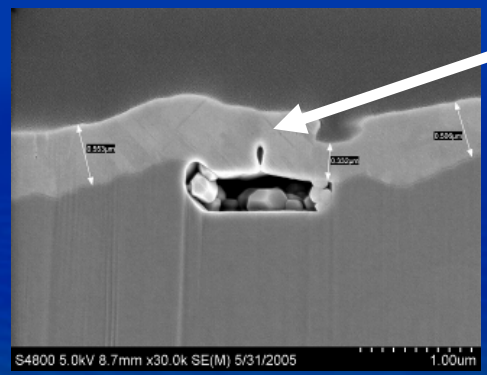


1 µm

Cave is fully enclosed:
ImAg forms a ‘roof’ over the cave.

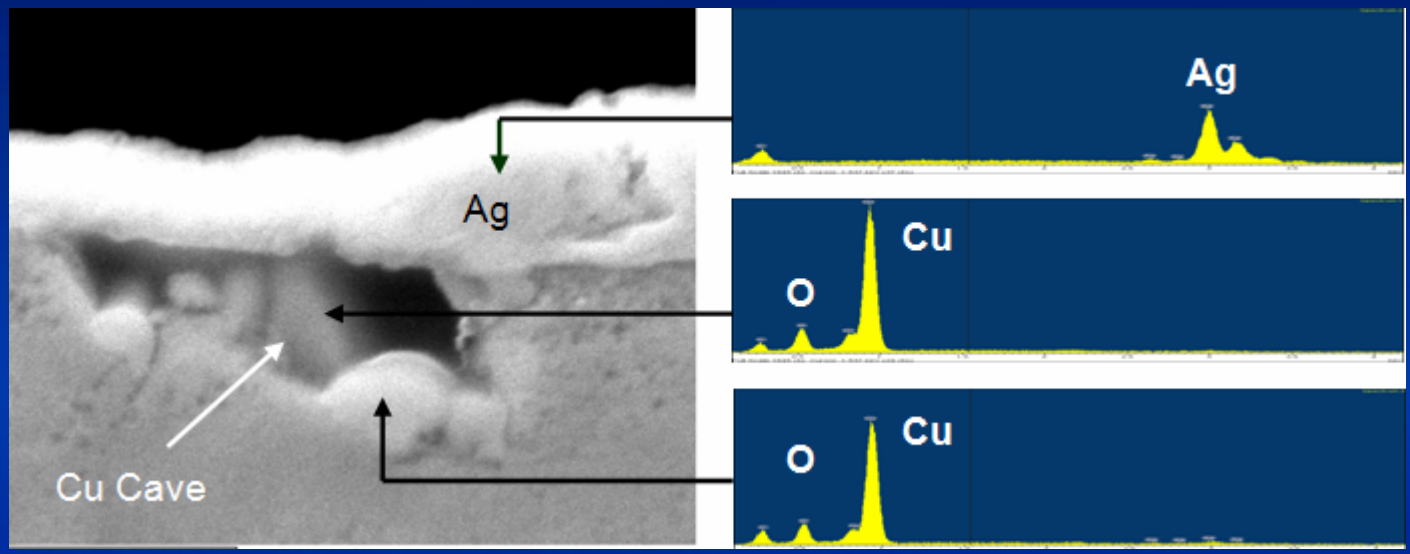
Walls and floor of cave are oxidized copper.

‘Chimney’



1 µm

Cu Cave “Dwellers”: Copper Oxide



- Copper Oxide in the Caves UNDER the ImAg Plating is playing a key role in Microvoid Formation
- Movies of Solder paste melting confirm this because microvoids form after solder melts and dissolves the ImAg

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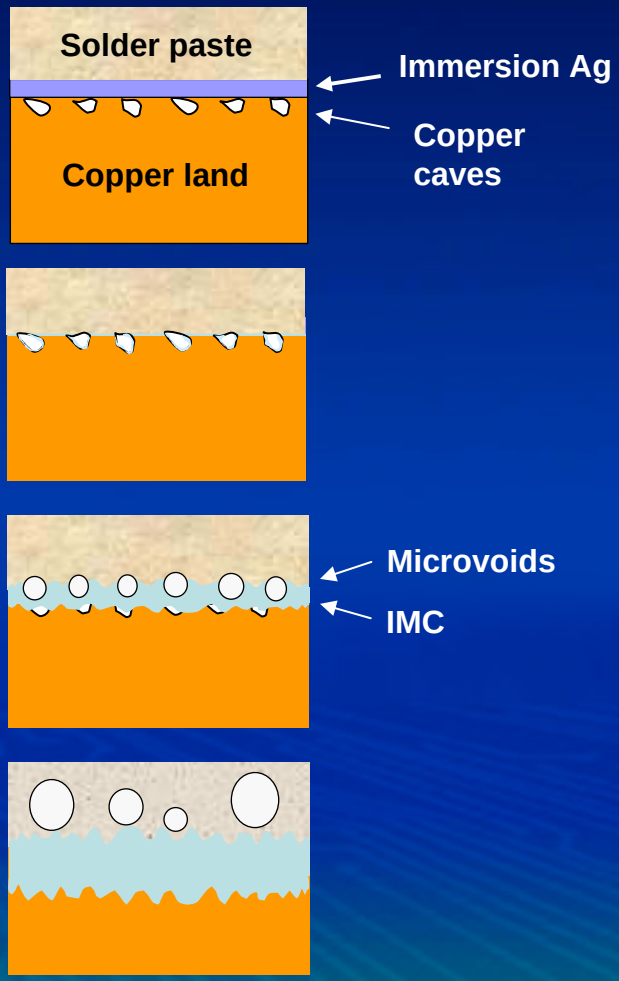
“Cave” to Planar Microvoid Mechanism



Copper Caves cause microvoids during SMT reflow.

After the silver dissolves into the solder, flux from the paste reaches the caves...

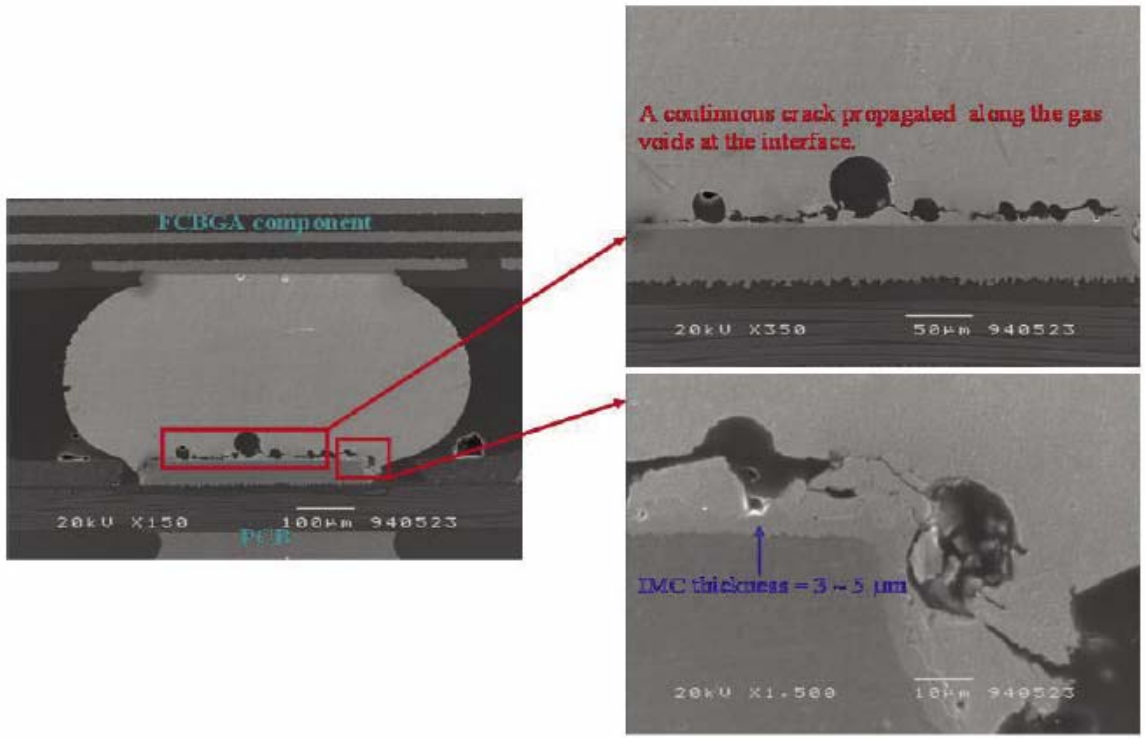
reducing the copper oxides in the caves, and producing gaseous bubbles…

which tend to stick to the IMC rather than rise (or just do not have enough time to rise), thus forming a plane of microvoids when the solder freezes.

(B) “Perfect Storm” Theory

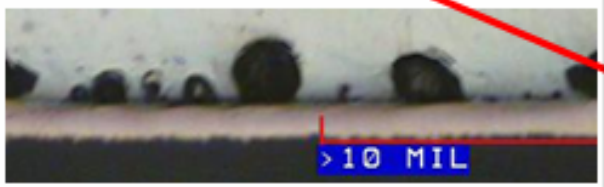
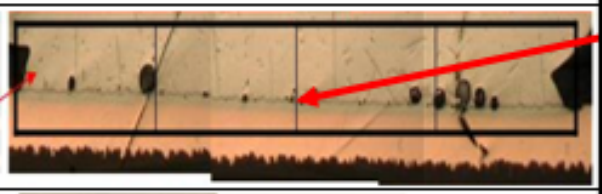
- Flux type
- High silver thickness
- Rough underlying copper
- Cool reflow soldering

(C) “Organic Residue” Theory



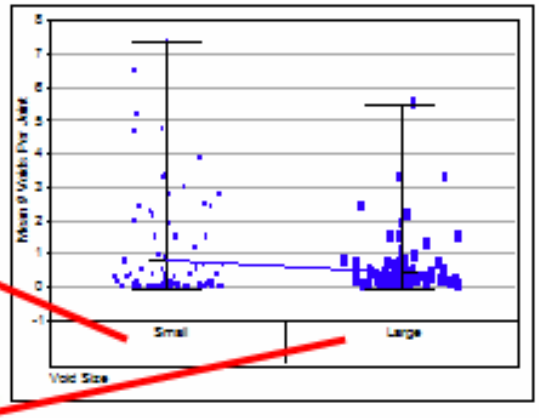
S.P. Yu et al, TPCA 2005

Time Zero Microvoid Characterization

Im/Ag plating lots for PCB	Time zero X-section for micro voids
Lots 1 & 2 (low microvoids)	
Lot 3 (excessive microvoids)	
Lot 4 (excessive microvoids)	
Lot 5 (excessive microvoids)	

Small * microvoids

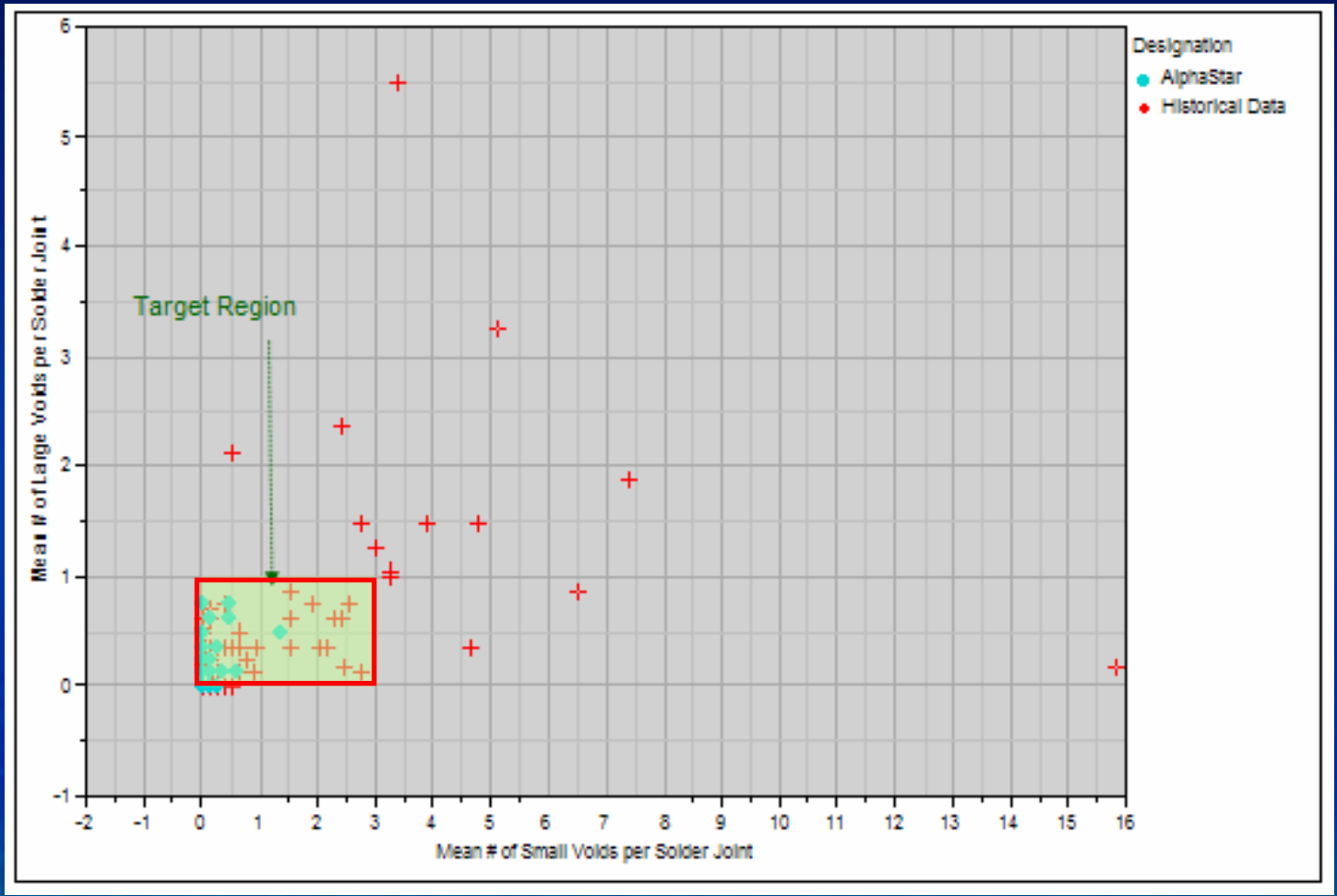
Large * microvoids



* = Smaller or larger than IMC thickness.

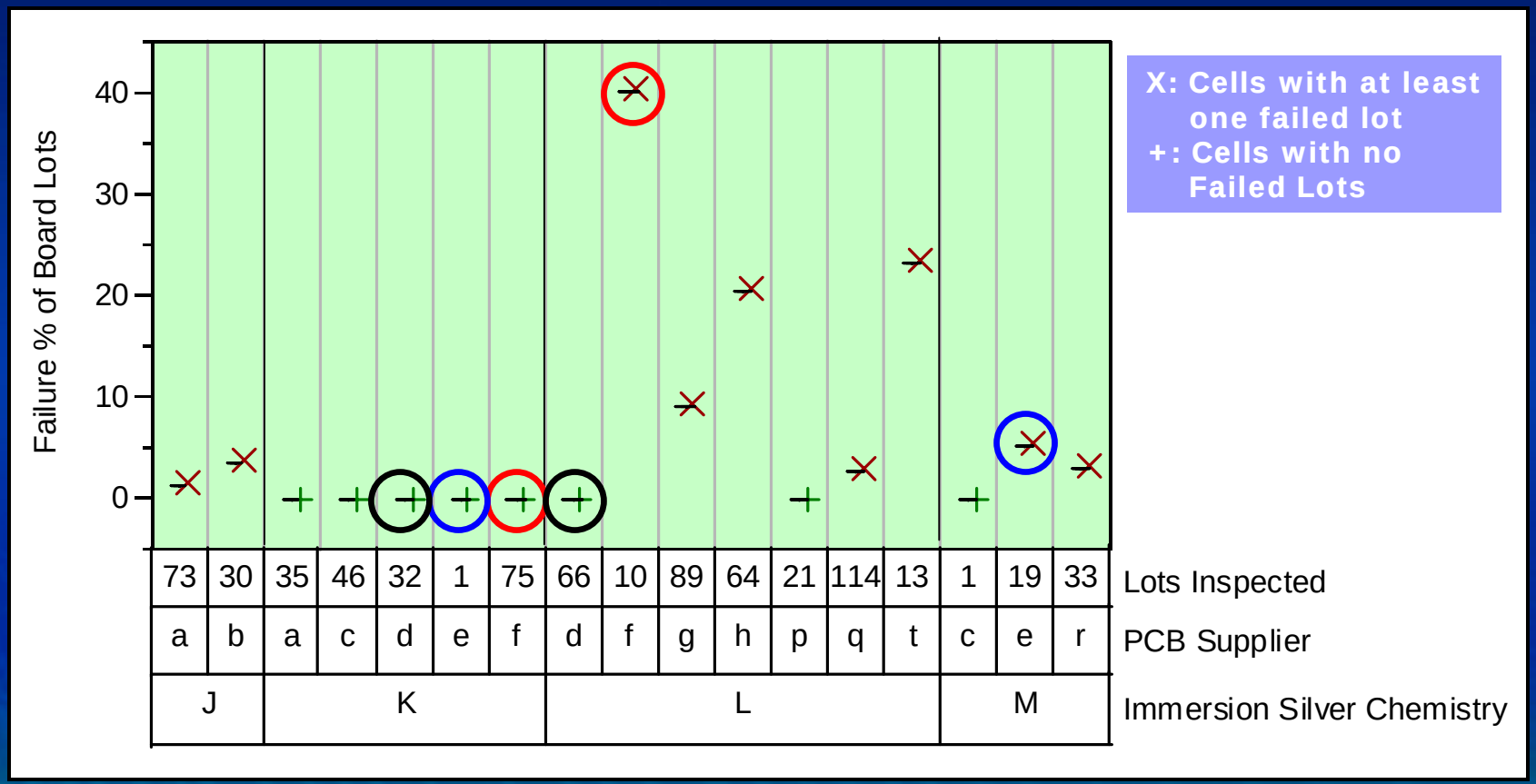
(Source: Intel Corporation approaches, experiments & tests are in pre-production environment. Intel makes no guarantee of the same or similar results in your pre-production or manufacturing environment.)

Microvoid Distribution of Historical EMS Data



(Source: Intel Corporation approaches, experiments & tests are in pre-production environment. Intel makes no guarantee of the same or similar results in your pre-production or manufacturing environment.)

EMS Results
Immersion Silver Chemistry and PCB Suppliers



(Source: Intel Corporation approaches, experiments & tests are in pre-production environment. Intel makes no guarantee of the same or similar results in your pre-production or manufacturing environment.)

Objective

- Determine if AlphaSTAR® immersion silver process generates microvoids when taken to the “limits” of it’s critical process conditions

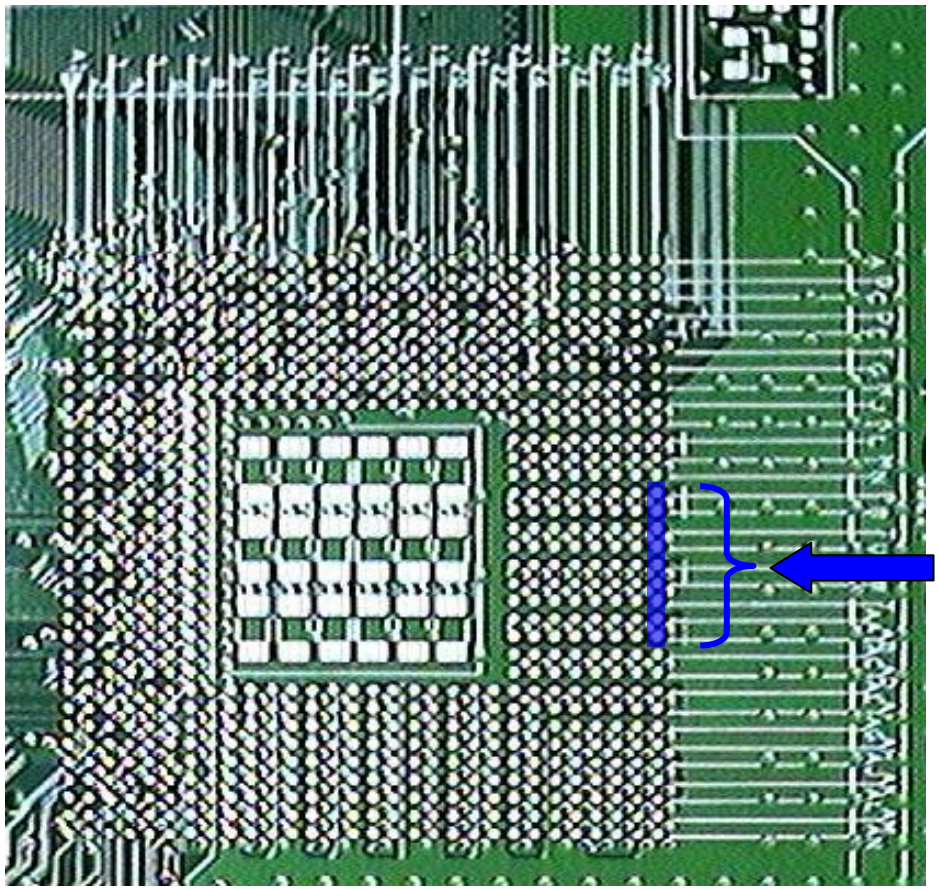
Design of Experiment

- 2^4 full factorial
  - Deposition Rate: Standard vs High (silver conc, temp, agitation, bath life, pH, etc)
    - Determined the limits of each variable that still produce an “acceptable” silver deposit
  - Plating time: Short vs Long
  - Etch: Matte (PC-7077) vs Semi-Bright (AL-1000)
  - Substrate: Good vs Bad (based on EMS historical data)

Design of Experiment

Leg #	Plating Conditions	Micro-etch	Plating Time, (min)	PCB Supplier
1	normal (pH=2.0 @RT, [Ag+]= 500 ppm)	AL-1000	Short (2.5)	Good
2		PC-7077	Short (2.5)	Good
3		AL-1000	Short (2.5)	Bad
4		AL-1000	Long (7.5)	Bad
5		AL-1000	Long (7.5)	Good
6	Low pH/High Ag (pH=0.86 @RT, [Ag+]= 1500 ppm)	AL-1000	Short (1.5)	Bad
7		AL-1000	Short (1.5)	Good
8		AL-1000	Long (4.5)	Good
9		AL-1000	Long (4.5)	Bad
10	normal (pH=2.0 @RT, [Ag+]= 500 ppm	PC-7077	Short (2.5)	Bad
11		PC-7077	Long (7.5)	Bad
12		PC-7077	Long (7.5)	Good
13	Low pH/High Ag (pH=0.86 @RT, [Ag+]= 1500 ppm)	PC-7077	Short (1.5)	Bad
14		PC-7077	Short (1.5)	Good
15		PC-7077	Long (4.5)	Good
16		PC-7077	Long (4.5)	Bad

BGA Land Pattern Distribution for Reflow Soldering



Solder Paste was printed on all lands of the Socket 775 except….

….These Lands were kept free of solder paste and balls; i.e. the lands had only plated ImAg;

This was done by taping the mini-stencil for solder paste application and solder ball placement;

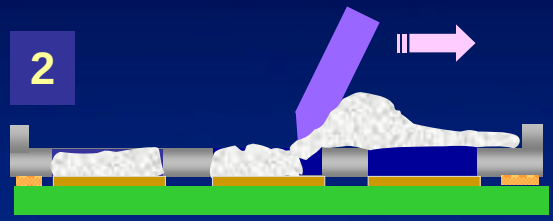
These ImAg lands were used to inspect for caves in the SEM

Procedures of SMT Processes and Examination

1

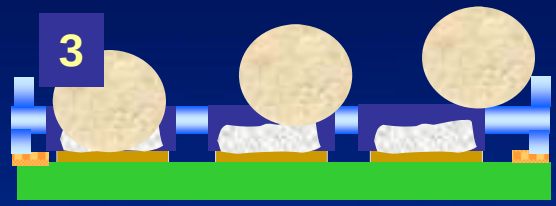
Incoming Coupon as plated

2

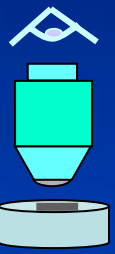


Print solder paste using mini-stencil

3

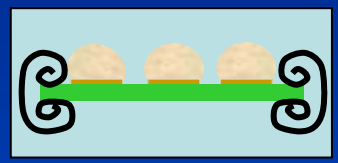


Place BGA solder spheres using expanded aperture stencil with relief

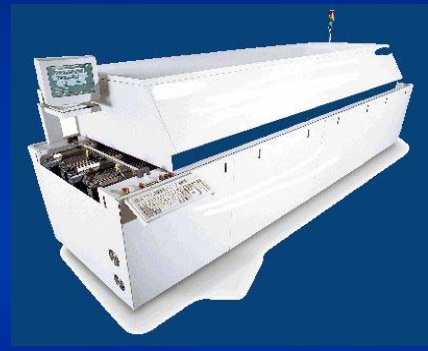


Prepare and Inspect X-section With Optical Microscope

5



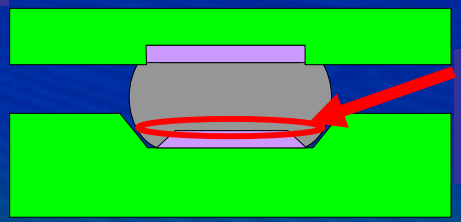
Prepare X-section



4

Reflow Soldering

6

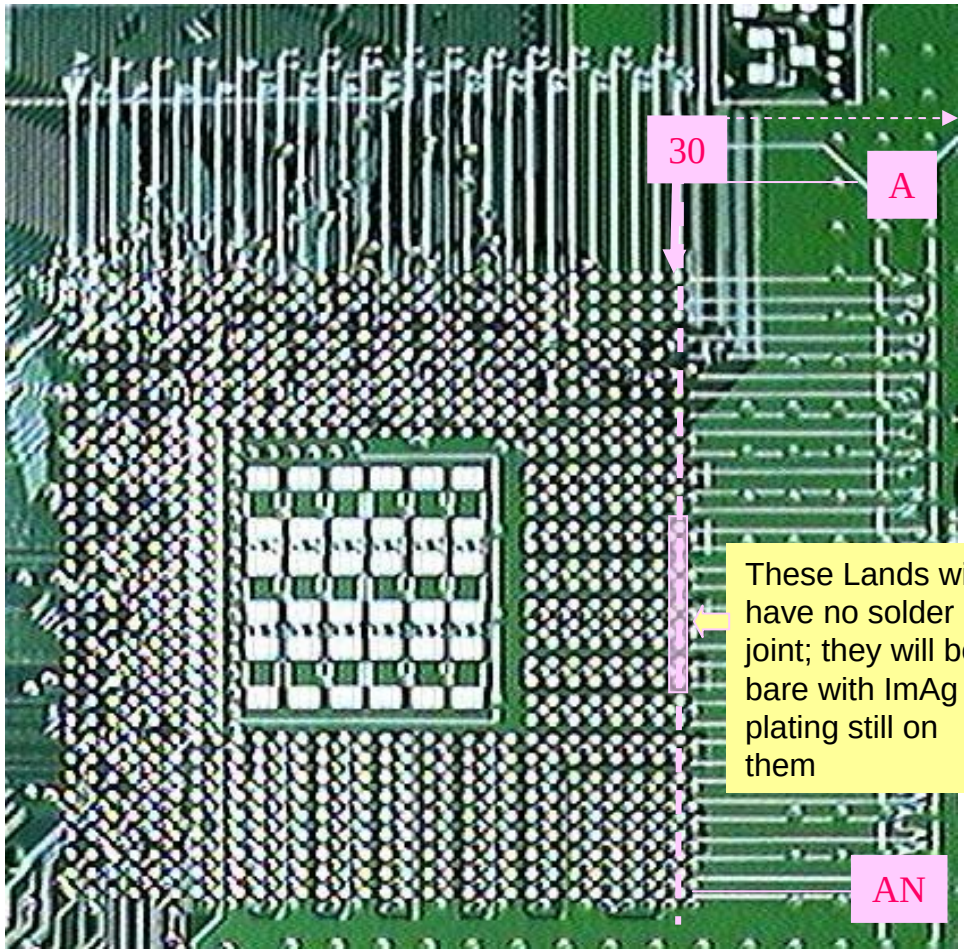


Inspect the area just above the lands for ALL solder joints in the cross-section

Cross-sectioning

(Source: Intel Corporation approaches, experiments & tests are in pre-production environment. Intel makes no guarantee of the same or similar results in your pre-production or manufacturing environment.)

Cross-Section Locations on the BGA Land Pattern



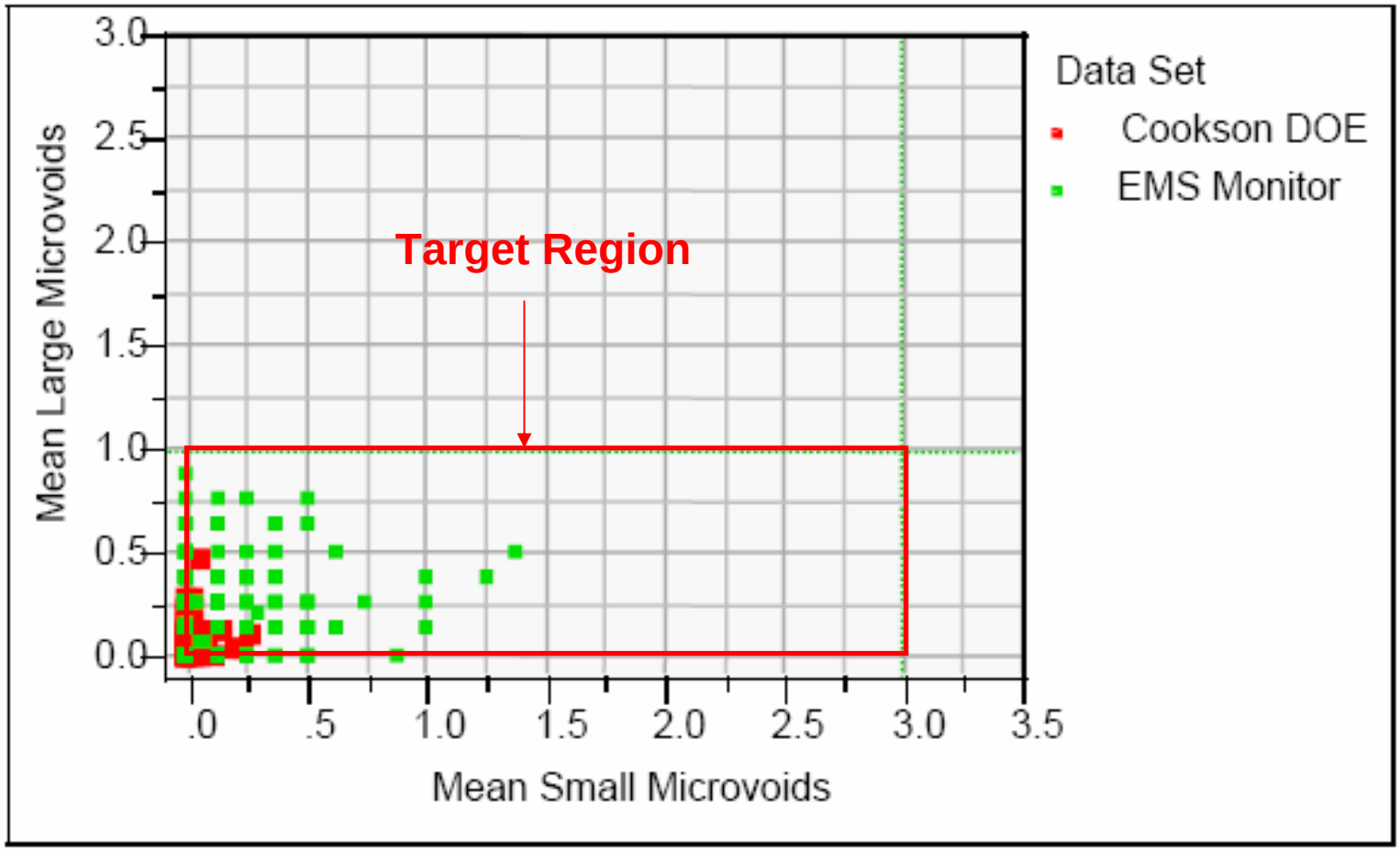
X-section
Row 30

Results of DOE (Leg 10)

Coupon	ImAg Thickness, micro inches	Number of Solder Joints Inspected	Total Number of Small Microvoids	Total Number of Large Microvoids	% of Solder Joints inspected with at least one Microvoid	Mean Number of Small Microvoids per Solder Joint	Mean Number of Large Microvoids per Solder Joint
R3181	10.06	33	1	0	4.55	0.03	0
R317R	10.11	33	1	5	21.74	0.03	0.15
R3180	10.32	33	0	2	9.09	0	0.06
R317T	10.48	33	0	0	0	0	0

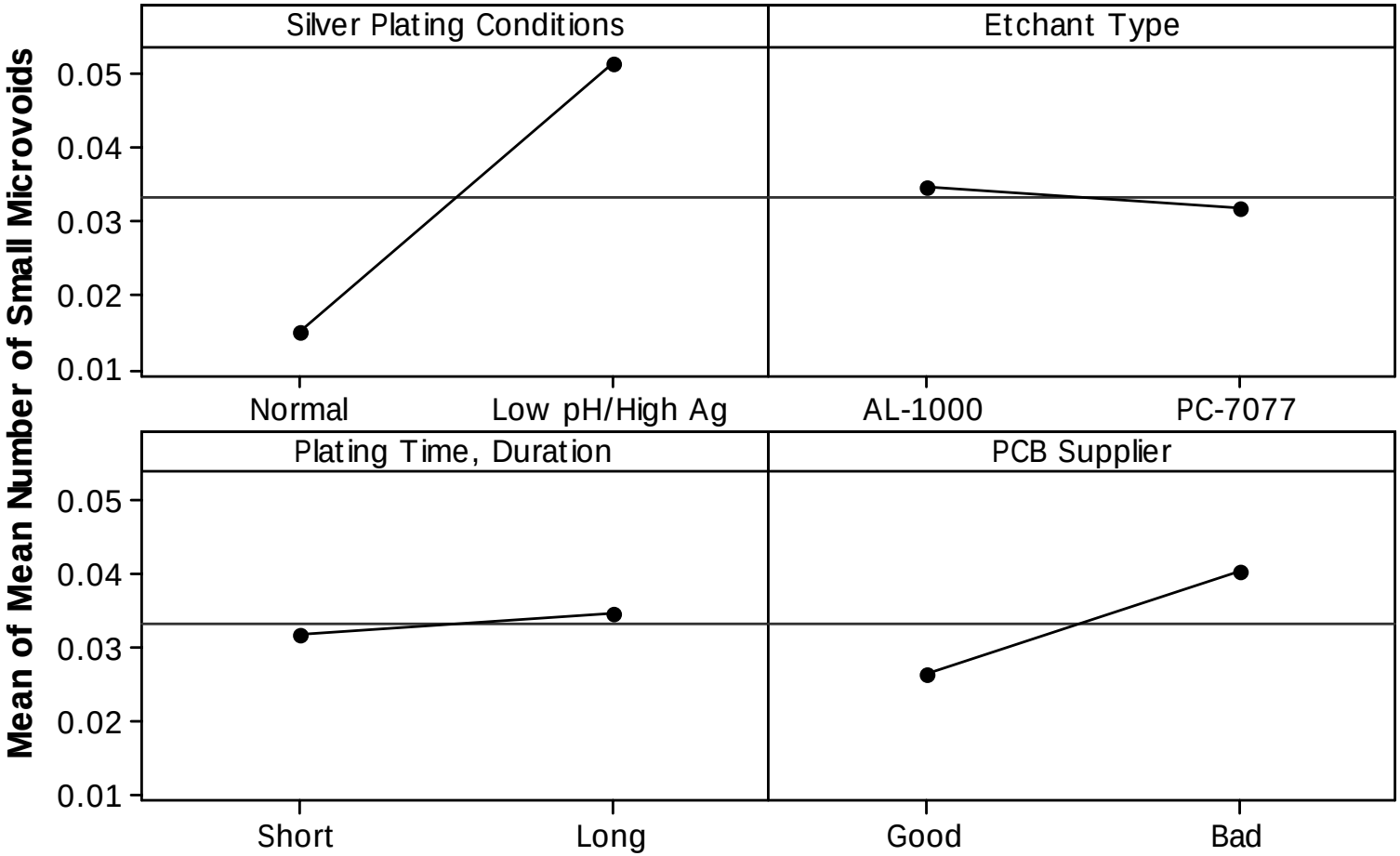
The % of solder joints with microvoids was a separate calculation done by the inspector, not derived from the Small and Large Microvoids data. More than one row may have been inspected for this particular data set. Whereas for Small and large Microvoids only the outer row was inspected.

Microvoid Density Distributions from DOE and EMS

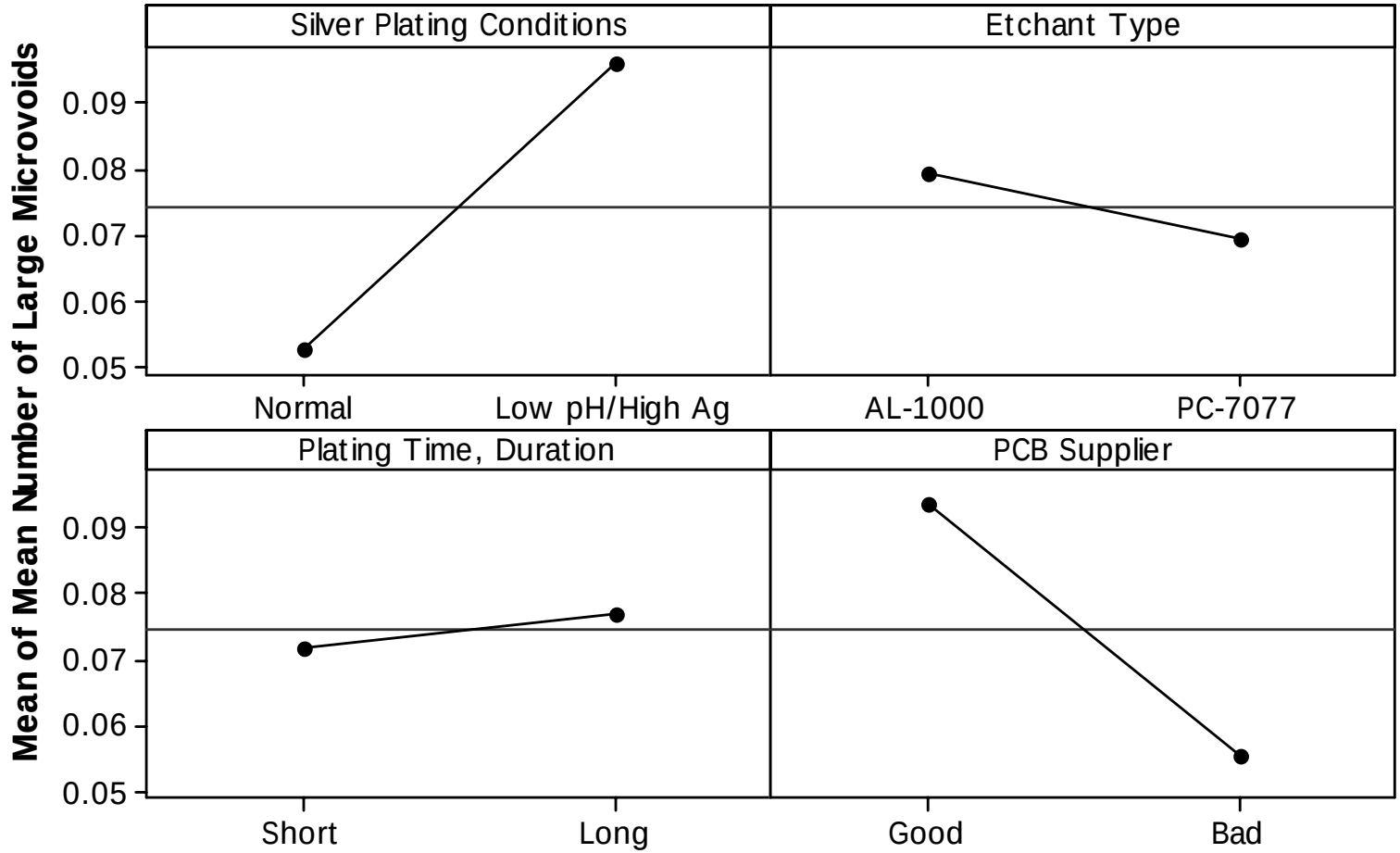


(Source: Intel Corporation approaches, experiments & tests are in pre-production environment. Intel makes no guarantee of the same or similar results in your pre-production or manufacturing environment.)

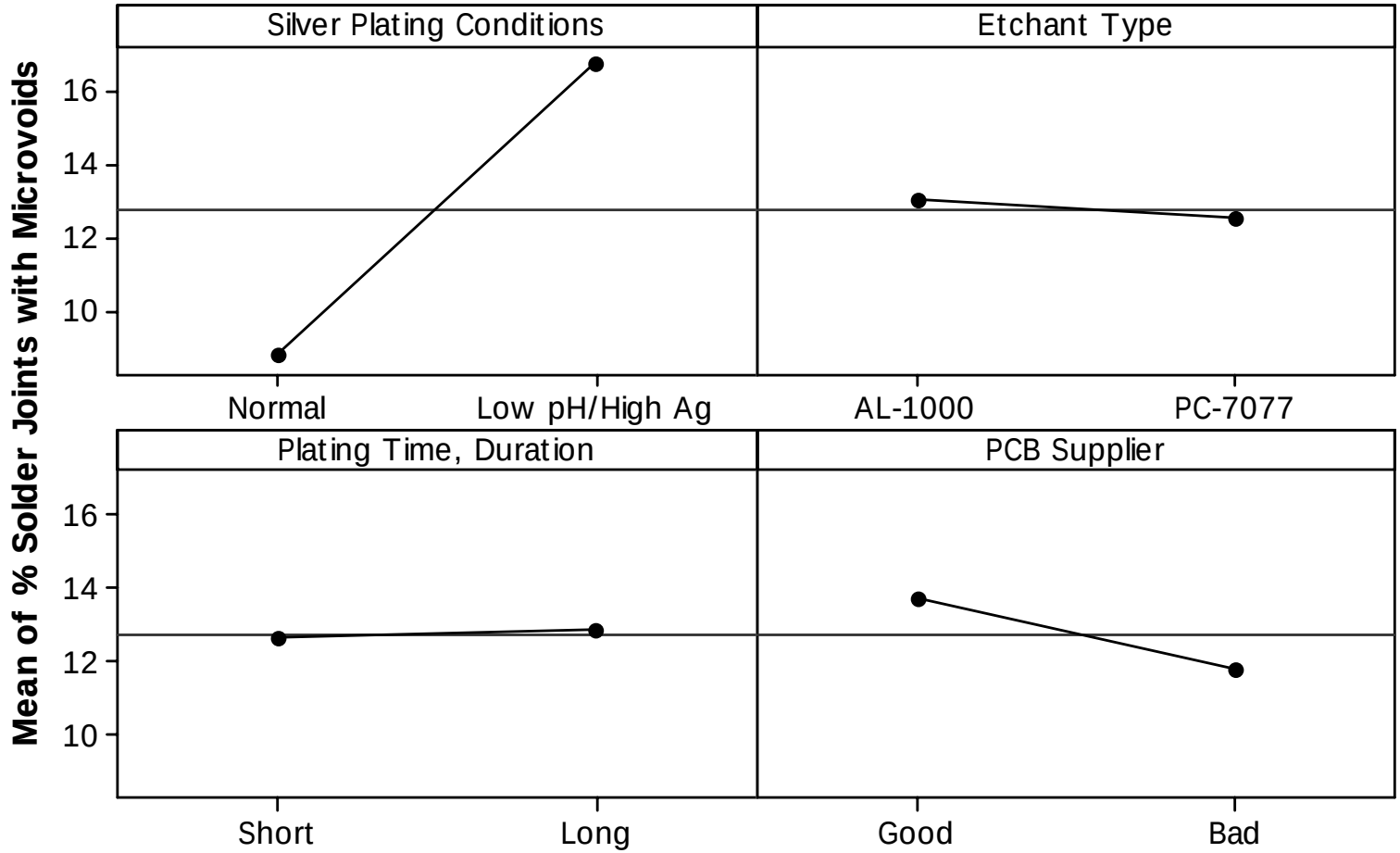
Main Effects Plots for Small Microvoids



Main Effects Plots for Large Microvoids

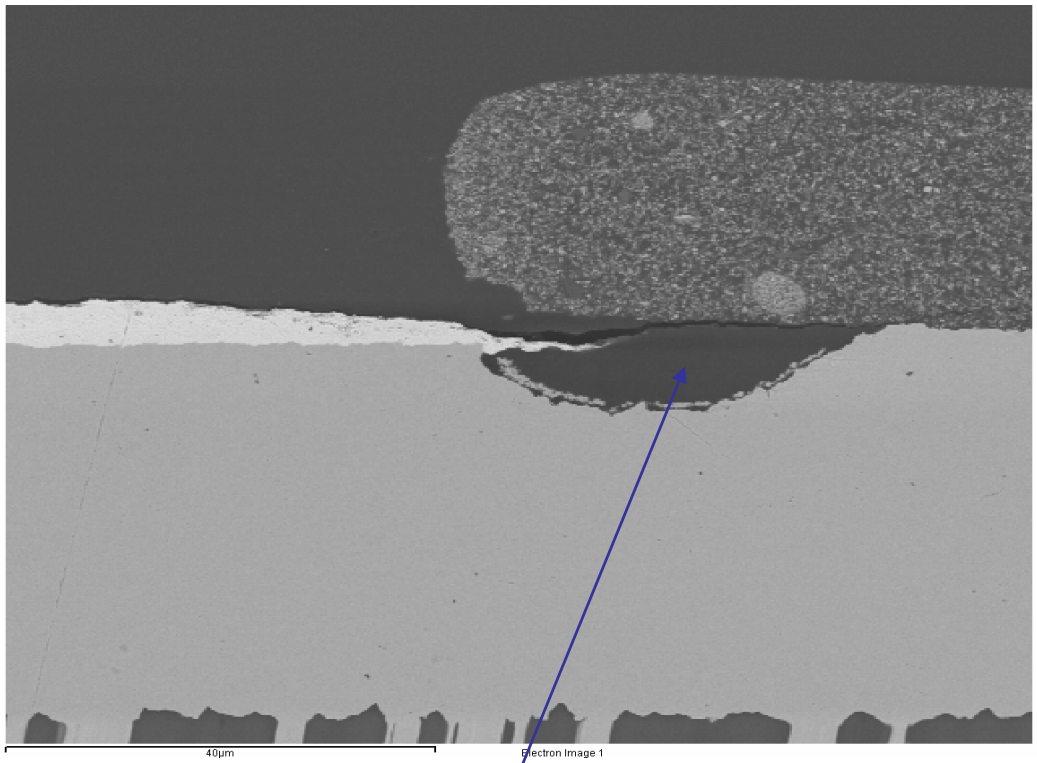


Main Effect Plots for % Solder Joints w/Microvoids



Galvanic Attack under Low pH/High Ag Condition

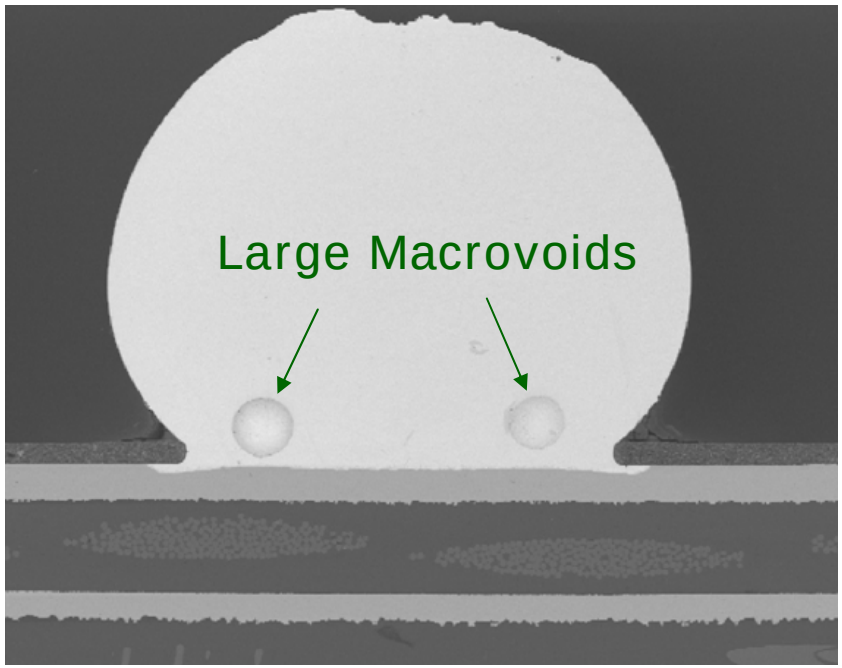
3.8 µm Ag →



8.5 microns deep, 37 microns long

(Source: Intel Corporation approaches, experiments & tests are in pre-production environment. Intel makes no guarantee of the same or similar results in your pre-production or manufacturing environment.)

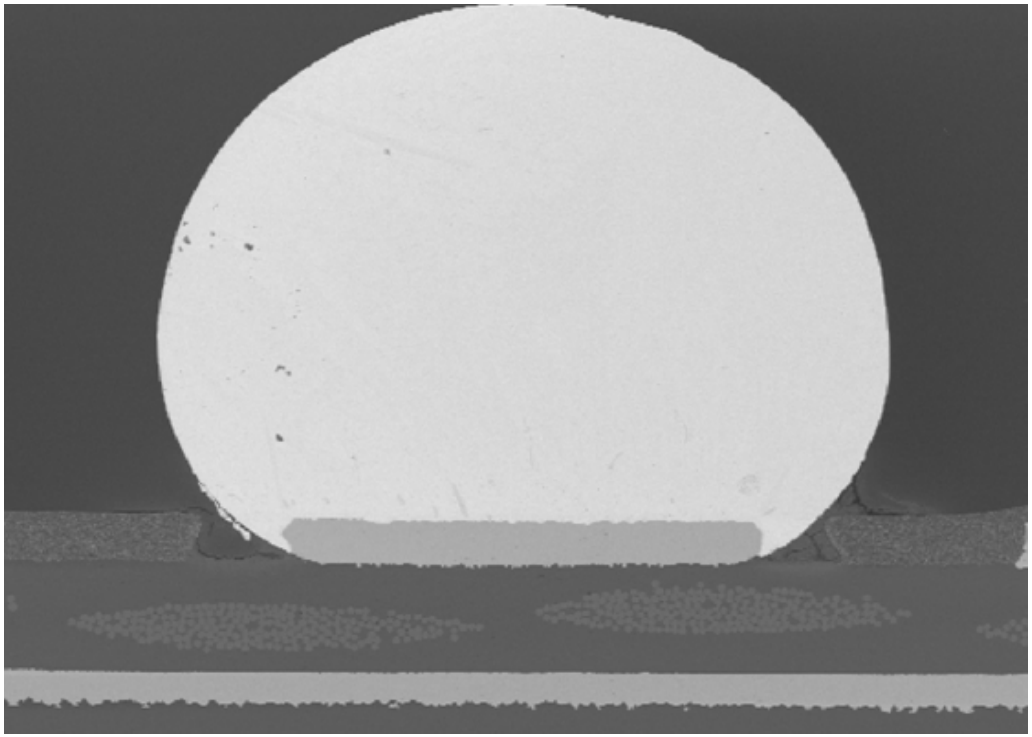
Large Process Voids Induced by Galvanic Attack



- Two large macrovoids observed close to region where crevice corrosion under solder mask has filled with solder
- These large macrovoids possibly formed by out gassing of copper oxide reduction products from the crevice corrosion region

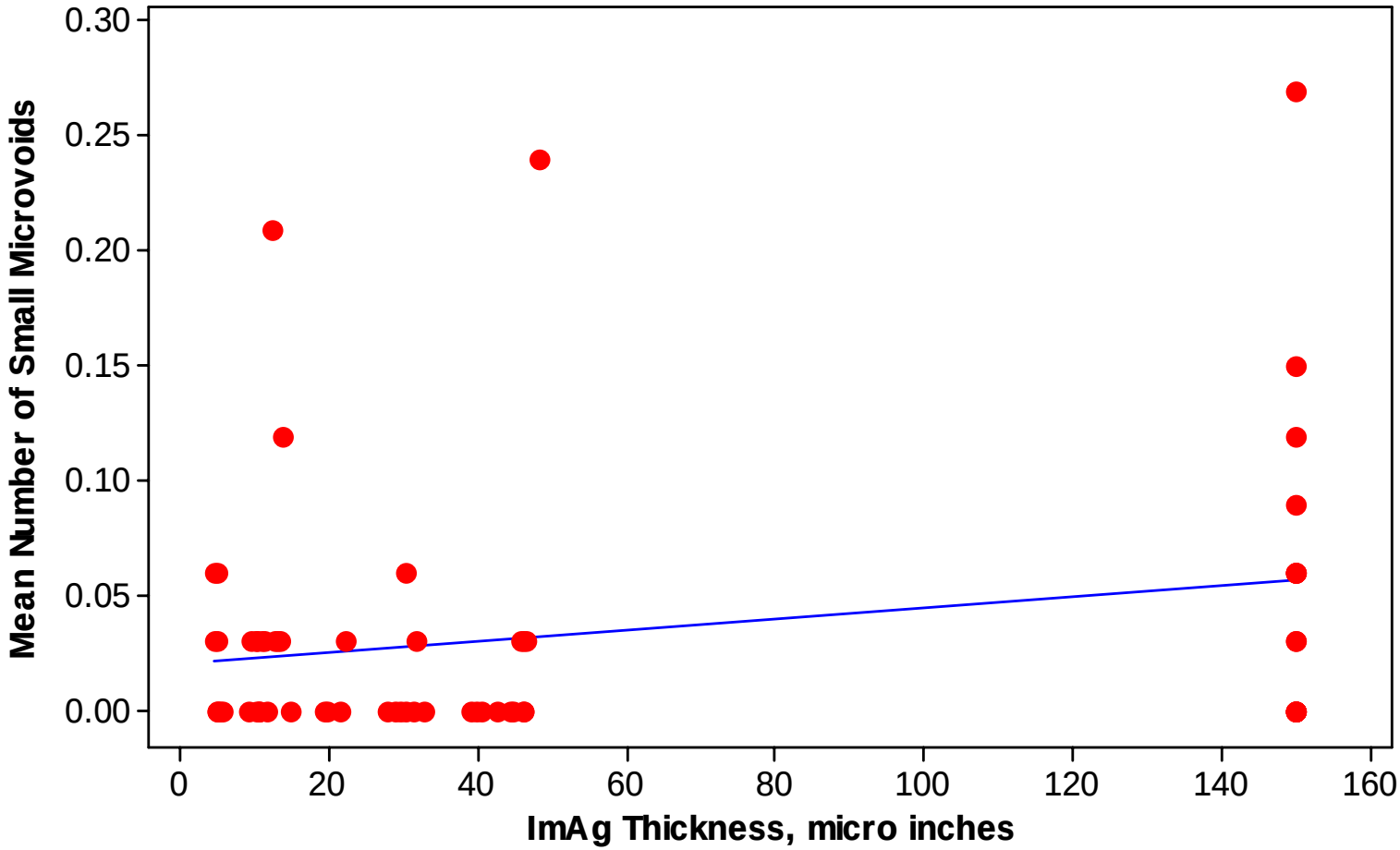
(Source: Intel Corporation approaches, experiments & tests are in pre-production environment. Intel makes no guarantee of the same or similar results in your pre-production or manufacturing environment.)

No Process Voids on Land Defined Pad

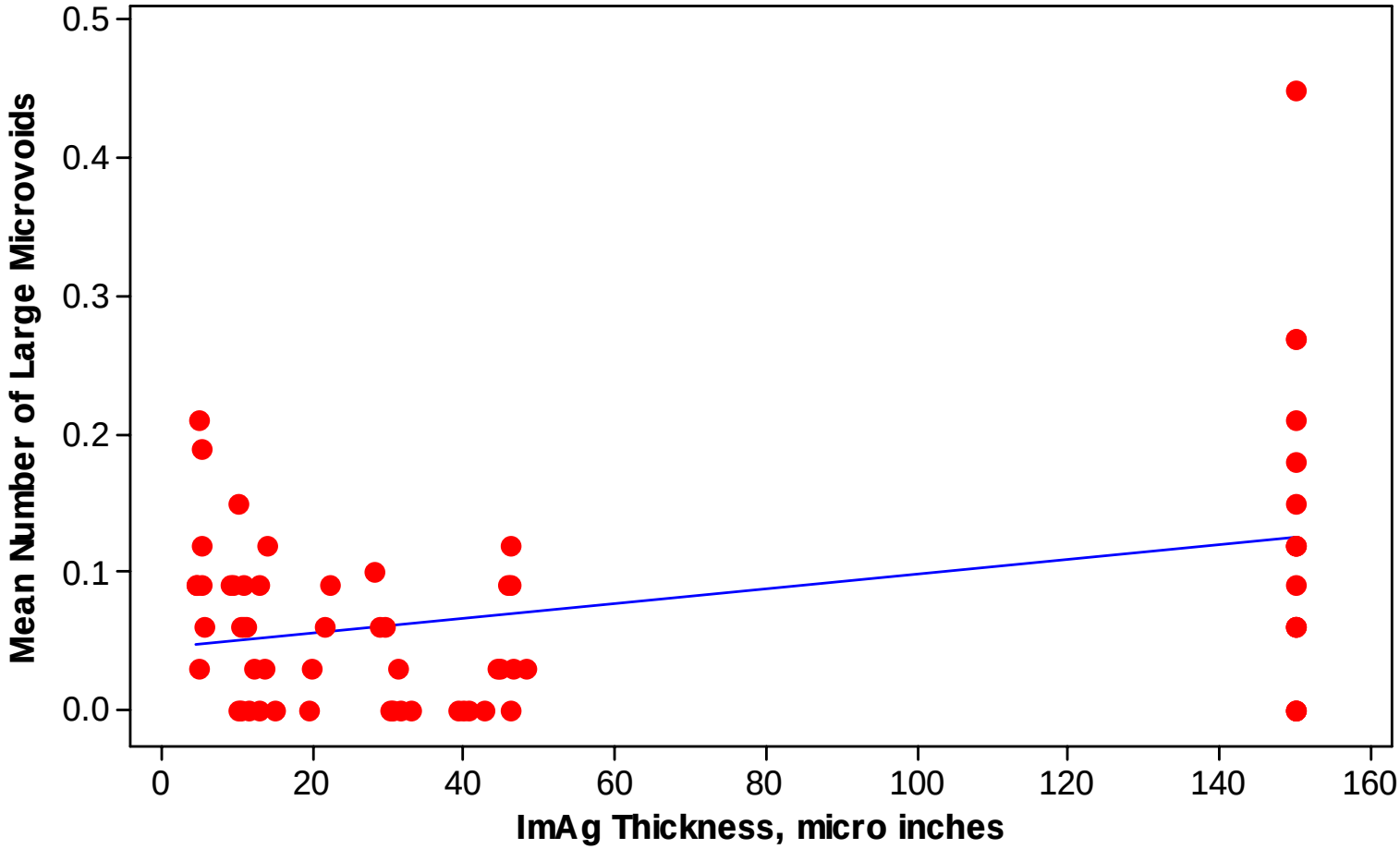


(Source: Intel Corporation approaches, experiments & tests are in pre-production environment. Intel makes no guarantee of the same or similar results in your pre-production or manufacturing environment.)

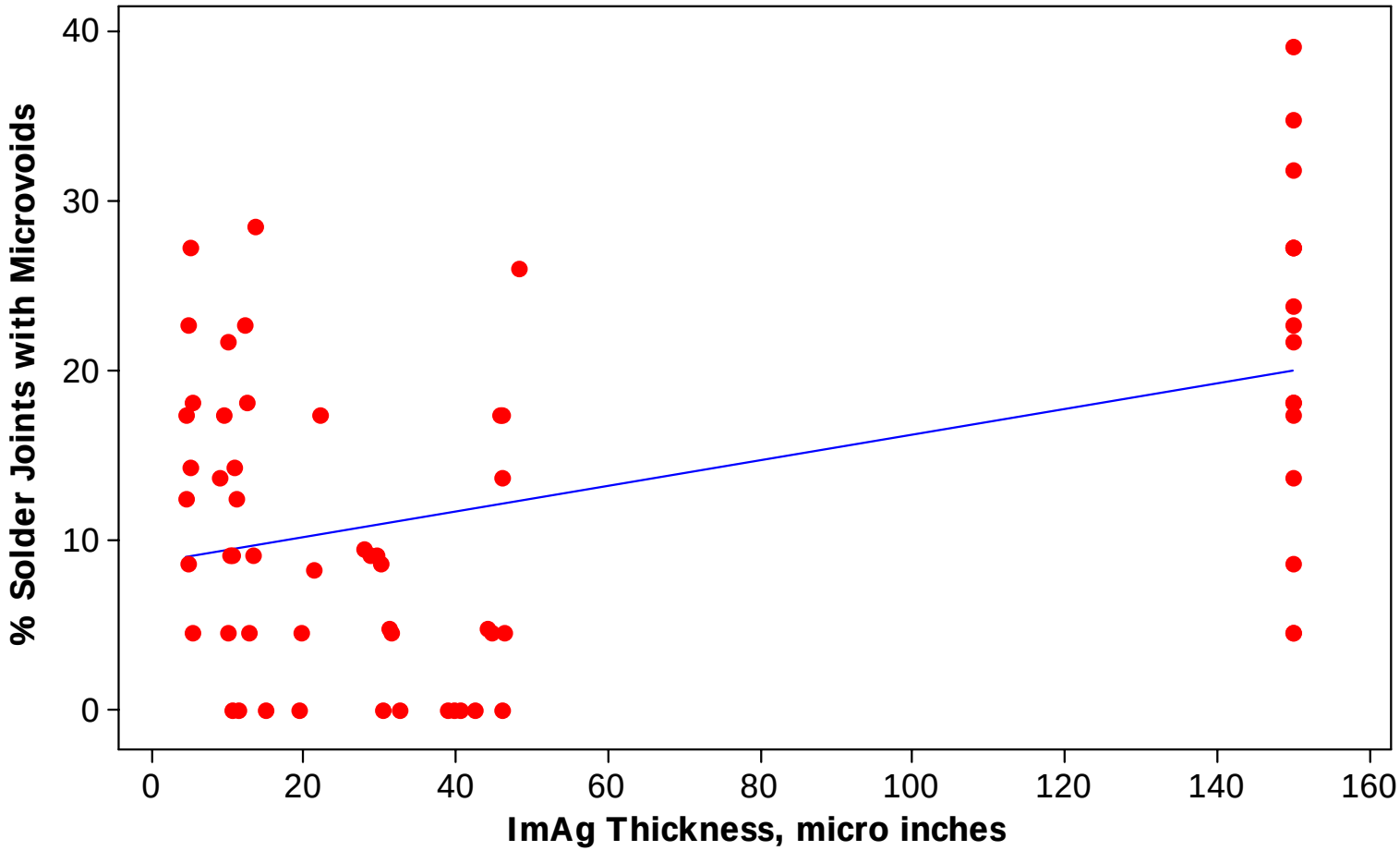
Effect of Silver Thickness on Number of Small Voids



Effect of Silver Thickness on Number of Large Voids



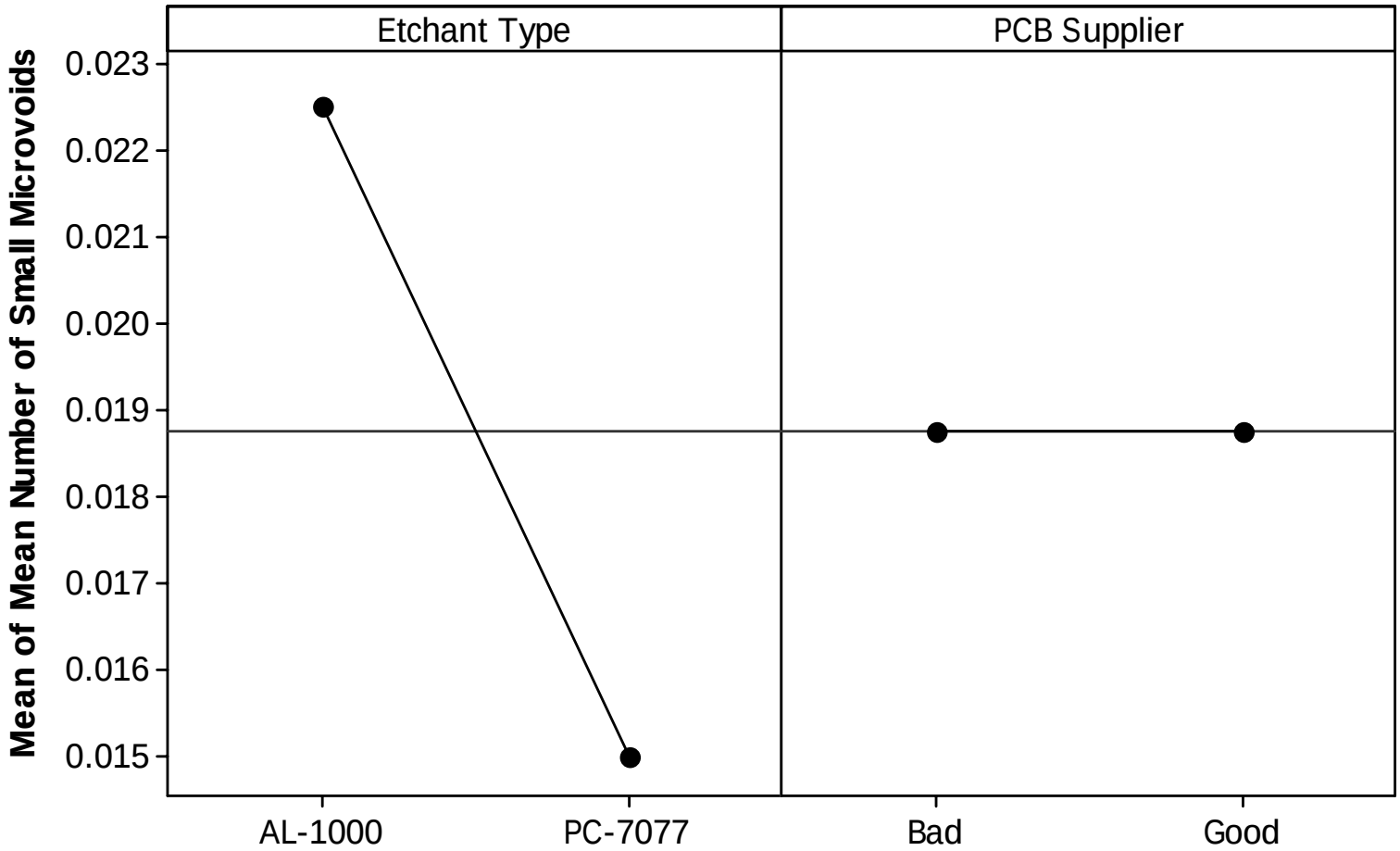
Effect of Silver Thickness on % Solder Joint w/Voids



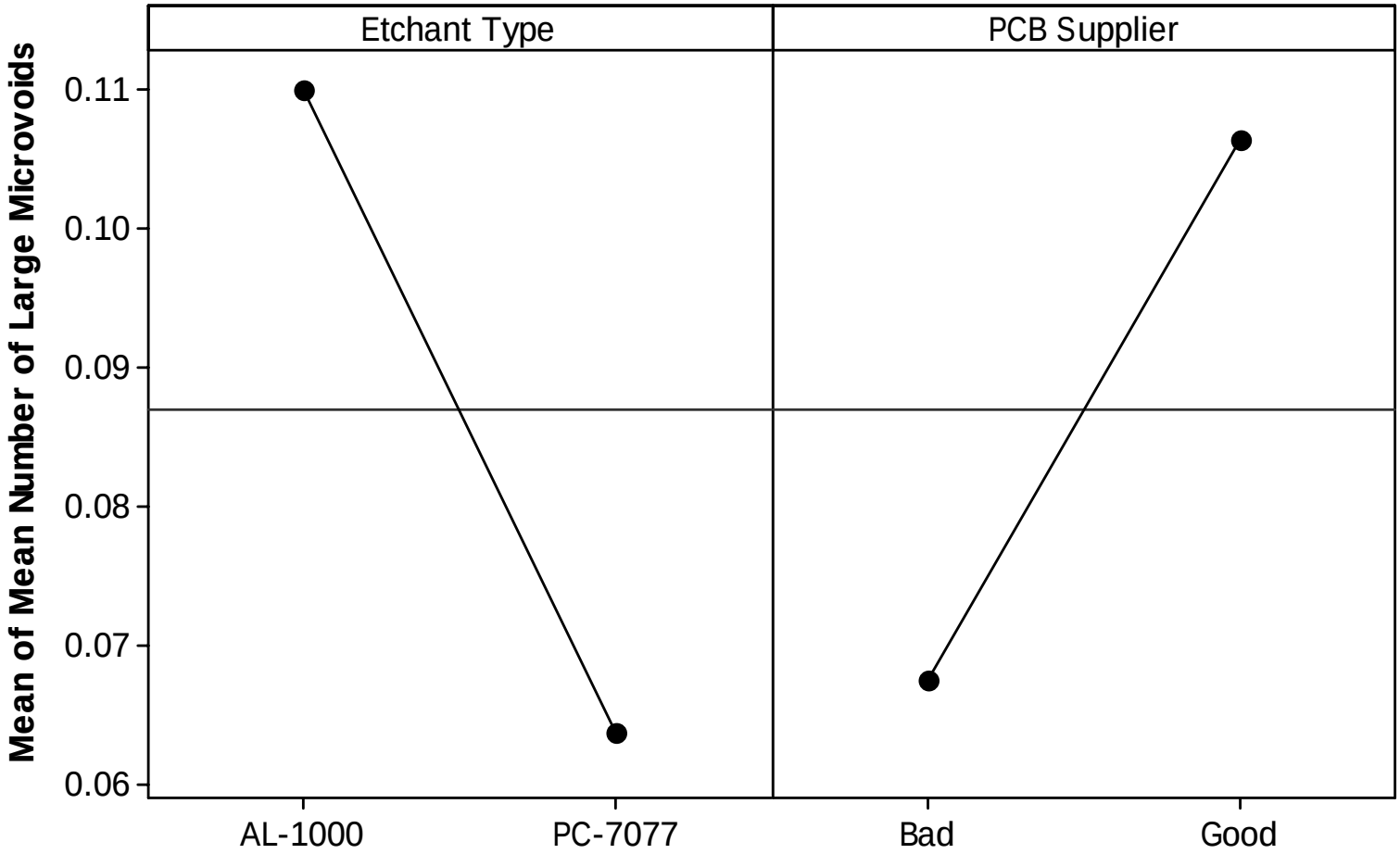
Effect of Silver Thickness on Microvoiding

- Very weak effect on microvoiding
  - *Though large microvoids effect is double that of small microvoids*
  - *Probably due to increased galvanic crevice corrosion Cu oxide product*
- Co-deposited organics from AlphaSTAR® do not cause significant amount of microvoids

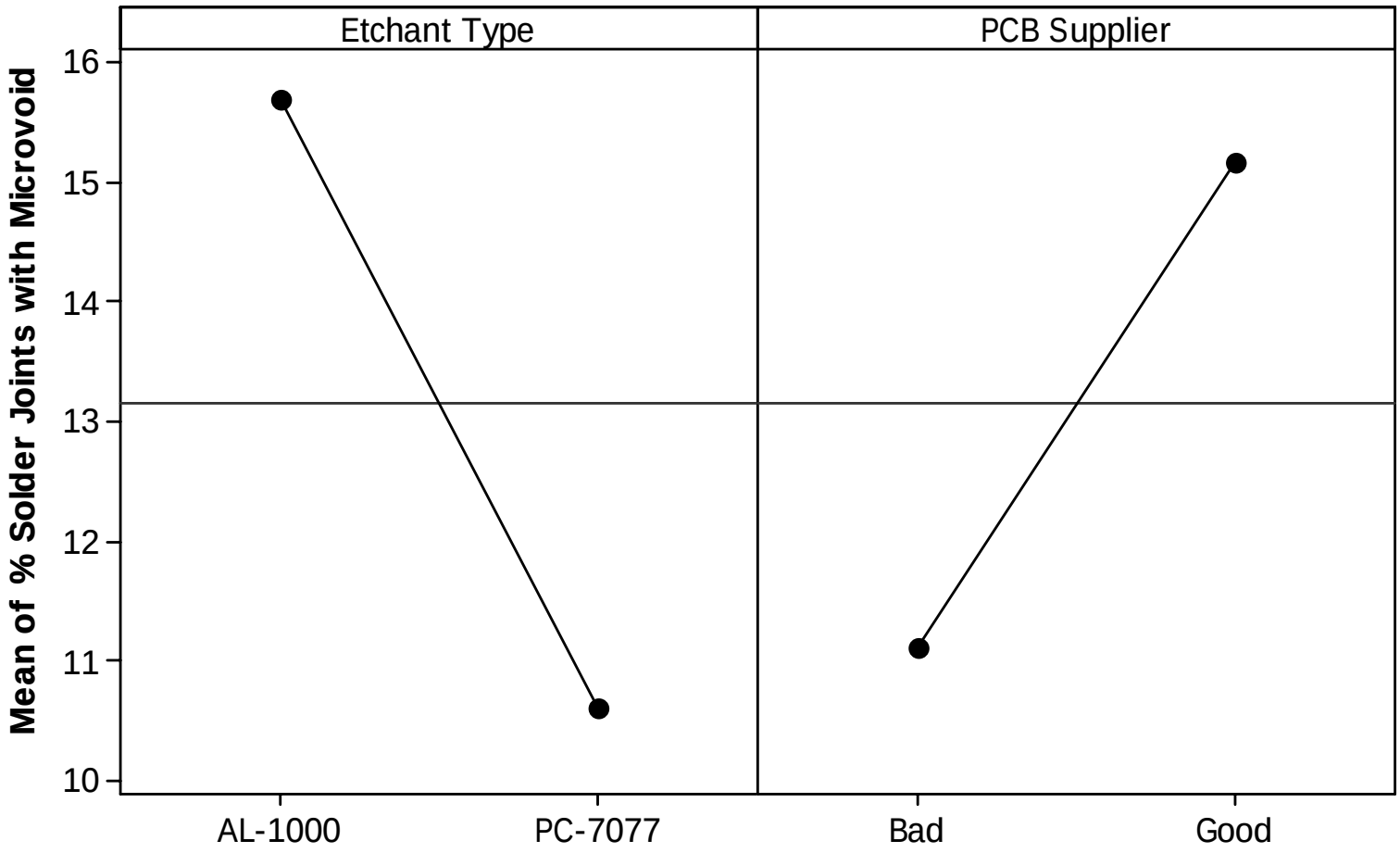
Main Effects Plots for Small Microvoids Normal Bath



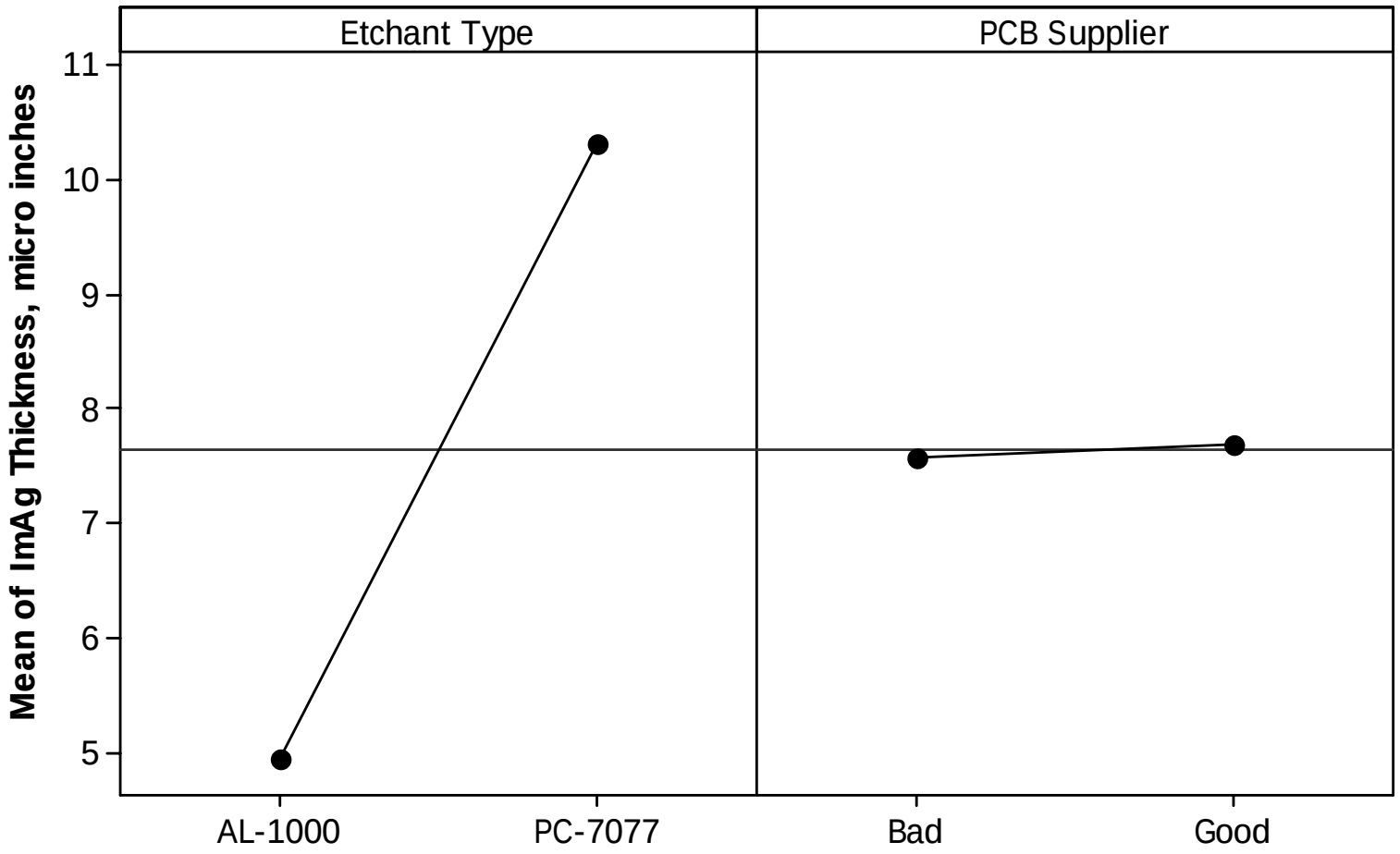
Main Effects Plots for Large Microvoids Normal Bath



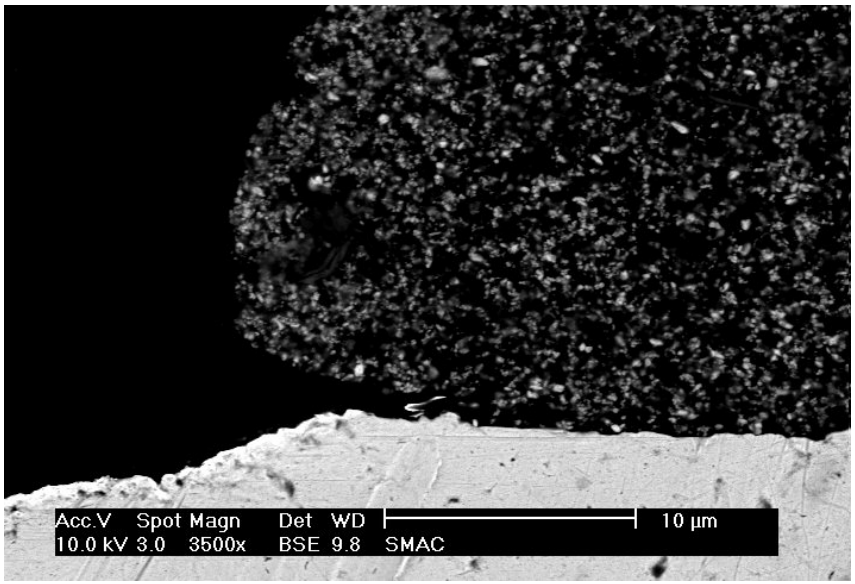
Main Effect Plots for % Solder Joints w/Microvoids Normal Bath



Main Effect Plots for Silver Thickness Normal Bath



No Galvanic Attack in Normal Bath



- This sample was from a short plating time duration leg

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Conclusions

- The new immersion silver process is intrinsically resistant to cave and microvoid formation, and capable of overcoming copper surface variation
- The fast deposition rate from low pH and high silver concentration results in higher microvoid densities
- Microetch has no significant effect on microvoiding, but the matte microetch results in a thicker silver
- The silver thickness has a weak effect on microvoiding
- Co-deposited organics from AlphaSTAR® do not cause significant amount of microvoids