Lessons Learned About Laminates during Migration to Lead-Free Soldering

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Abstract
This paper provides a high-level overview of many of the key lessons learned thus far in working with PCB fabricators in qualifying laminate/fabrication processes that will yield fundamental printed circuit board (PCB) attributes that will meet IBM server reliability requirements, with the additional requirement of being subjected to the higher temperature processes required for mixed-solder assembly and for totally lead-free soldering. Special focus is placed upon significant laminate integrity issues, the solutions of which will probably require far greater integration among different levels of the supply chain.

Introduction
Although assemblies used in servers are currently exempt from the European Union's recently enacted ban on the use of lead in solder, significant effort is underway within IBM to solve technical issues that would be associated with this change in the event that the exemption is terminated in the future. Additionally, technical issues need to be resolved in the evolving migration towards the use of mixed-solder assemblies, the use of eutectic tin/lead solder to attach BGA devices that market pressures drive towards being available only with SnAgCu (SAC) balls.

Among the main concerns being addressed in this effort are the effects of higher soldering temperatures upon the integrity and performance of key attributes of the PCBs that are anticipated to be used in these server systems. For the case of mixed-solder assembly, PCB surface temperatures are anticipated to be as high as 245^{o}C. For the case of PCBs that experience lead-free soldering processes, PCB surface temperatures are anticipated to range from about 235^{o}C to about 255^{o}C during SMT reflow and up to about 245^{o}C during controlled rework.

Of primary concern are the responses of the laminate to these elevated temperatures. It is well known that coefficient of thermal expansion (CTE) mismatches between the copper and the laminate within a PCB can result in exertion of stresses upon the copper that can result in opens within vias, opens at the interfaces between internal lands and plated-through hole (PTH) barrels, and even open traces. The integrity of the laminate itself can also be adversely affected, yielding such undesirable effects as pathways for potential dendrite growth and warpage that can adversely affect the integrity of various connections of other devices to the PCB.

This paper, which is a follow on to an earlier paper[1], describes much of what has been learned to date during testing of the effects of various higher-temperature soldering profiles upon the integrity of a range of PCB constructions. Also addressed are the subsequent effects of certain additional mechanical forces that are exerted during assembly, as well as assessments that address potential latent defects.

The majority of this work has involved the use of PCB test vehicles that include product features that are believed to be particularly vulnerable to the simulated thermal and mechanical stresses that are applied to them during higher-temperature assembly processes. The effects of simulated stresses on these features are monitored electrically and/or by means of visual observations of surfaces and cross-sections. Some aspects of these observations have been supplemented by visual observations of production PCBs that have been subjected to comparable thermal stresses.

Two different simulated reflow profiles are used. Test samples that target mixed-solder assembly processes experience five passes through a profile with a peak temperature of 245^{o}C, as is the case for one class of test samples (generally thinner) that target lead-free soldering. A second class of test samples (generally thicker) that also target lead-free soldering are subjected to a combination of three passes through a profile with a peak temperature of 260^{o}C, followed by two passes through a profile that peaks at 245^{o}C.

While heightened attention must be paid to the failure mechanisms that have historically plagued PCBs experiencing tin/lead soldering conditions, these studies have demonstrated that significantly heightened attention must be paid to laminate integrity issues, which are the main focus of this paper. The need to better understand these now more common failure modes has prompted auxiliary studies, including various thermomechanical studies and studies of moisture ingress and egress from PCBs, which will only be briefly discussed in this paper.

Table 1 - Fabricators and Laminates, Test Vehicle Thicknesses (mm)

	Laminate							
	1	2	3	4	5	6	7	8
T_g (°C)	180	175	175	135	210	170	175	180
T_d (°C)	325	350	365	360	400	340	340	340
Fabricator								
A							1.91	
B		3.30				2.54		3.30
C						3.30		
D	4.06							
E					4.83			
F				2.54				
G			4.06					
H			3.30					3.30
I			3.30					3.30

Experimental

*** Description of PCB Test Samples**

The vast majority of testing focused on PCBs that were produced with laminates that have been marketed as being compatible with lead-free soldering temperatures. The vast majority of these test PCBs were test vehicles that were produced, starting in late 2004, by nine PCB fabricators and involved eight different laminates (see Table 1). Seven of these laminates had an effective loss tangent of about 0.02. Laminate #5 had an effective loss tangent of <0.01. Each PCB fabricator utilized up to three different laminates. Some laminates were used by up to three PCB fabricators. Additional laminate/fabricator combinations will be tested in the future. Only minimal reference is given to the results of earlier studies, because, as has been the case for similar testing programs[2], this program has faced the consequences of a somewhat dynamic laminate marketplace.

The vast majority of testing involved custom test vehicles that were designed focus on specific PCB features that have shown vulnerability to undesirable changes when subjected to various applied stresses during assembly and/or during customer usage. Test vehicle designs were modified and/or new test vehicles were designed as new understanding of risks associated with higher-temperature exposures evolved with the project.

Each test vehicle of the suite consisted of a large number of specific risk sites. Each design can be modified to allow flexibility in the choice of layer count (and thus in overall thickness) without the need for rewiring. Thicknesses and layer counts have gravitated towards those shown in Table 2, with the majority of testing centering upon designs that are 2.54 or 3.30 mm thick.

Table 2 - Test Vehicle Thicknesses and Layer Counts

Thickness (mm)	Layers
1.91	14
2.54	20
3.30	26
4.06	28
4.83	32

Cloth styles were specified to include those that are used in typical products (e.g., 106, 1080, 2113), per their availability for the laminate used. Copper foil thicknesses of ½- and 1-oz were specified.

The risk sites of concern in most test vehicle designs are wired to allow the monitoring of resistance changes that may occur as the result of applied stresses. This includes monitoring of via integrity and of internal land-to-PTH integrity as test vehicles are subjected to thermal stresses, as well as for the formation of dendrites between adjacent vias under conditions of higher temperature, humidity and applied voltage. Some test vehicles provide circuitry for the detection of dendrite formation under these conditions between power planes and vias, as well as between power planes and PTHs that accommodate press-fit connectors of particular interest.

All risk sites involve through holes; no blind or buried vias are present. An overview of the diameters and pitches of the through vias present within the test vehicles is provided in Table 3.

Table 3 - PTH Diameters and Pitches within Test Vehicles

Diameter (mm)	Pitch (mm)	Comments
0.20	0.8	Various array sizes
	1.0	Various array sizes
0.25	0.8	
	1.0	
0.56		For press-fit connector
0.61		For press-fit connector
1.02		

The wiring of some risk sites within some test vehicles has evolved so as to accommodate new ideas for improved testing efficiencies and sensitivities. It is hoped that the structural integrity of the laminate can be monitored in the future through capacitance measurements in newer test vehicle designs.

Testing has not been limited to the use of test vehicles. A small number of production parts have been exposed to various SMT-like thermal profiles, followed by optical inspection of surfaces and of cross-sections. These parts were produced by various fabricators, using laminates that are marketed as being compatible with lead-free soldering conditions. DICY-cured laminates were included in the evaluation for benchmarking purposes.

All test samples involved an OSP surface treatment.

*** Simulation of Higher Temperature Soldering Processes**

The majority of test vehicle designs and a few production parts were subjected to multiple passes through an 8-zone Senju reflow oven or a 10-zone Electrovert oven. One or two different thermal profiles were established to simulate the global heating of the PCB during mixed-solder or lead-free soldering processes. This involved five passes through a profile with a peak temperature of 245°C for PCB thicknesses of up to about 2.54 mm. For thicker PCBs, three passes through a profile with a peak temperature of 260°C were followed by two passes through a profile with a peak temperature of 245°C. See Figure 1 for a representative profile involving a peak temperature of 260°C.

A small number of production parts were subjected to a vapor phase reflow process with a peak temperature of 240°C. The effects of localized heating associated with rework will be addressed in the future.

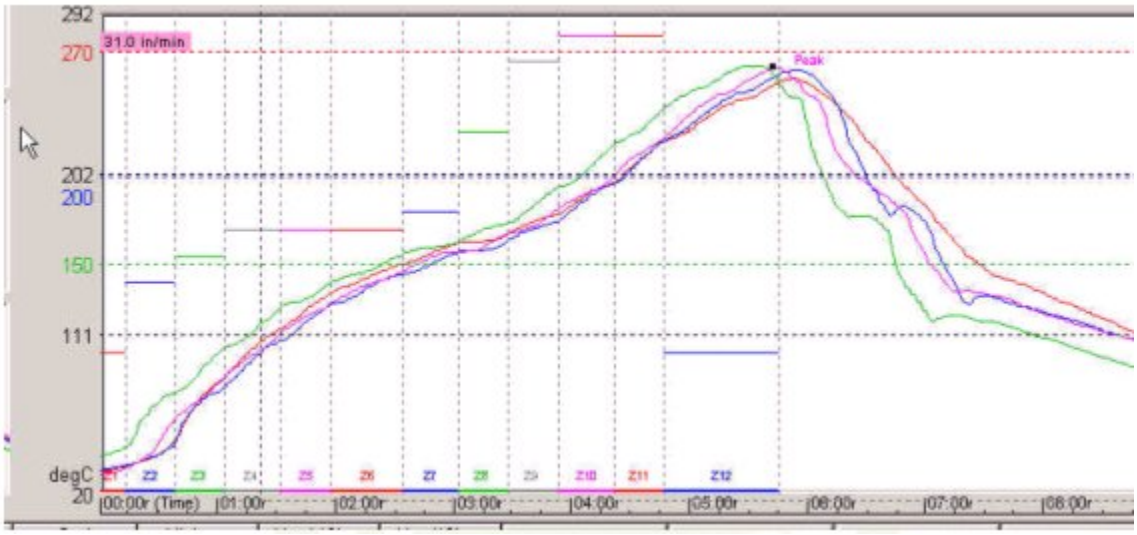

Figure 1 - Representative Thermal Profile

Some test vehicles were subjected to a 24-hour bake at 125°C prior to undergoing reflow simulation. A few test vehicles were subjected to 12- or 36-hour prebaking for experimental purposes.

*** Assessment of Blatant and Latent Defects**

The surfaces of test samples were visually inspected for signs of thermally-induced damage after undergoing five passes through simulated soldering. In some cases, test samples were also examined after each of the preceding passes.

One or two different press-fit connectors were inserted into accommodating arrays of PTHs in some test samples. Insertion forces were measured. These test vehicles subsequently underwent thermal cycling or insulation resistance testing, followed by cross-sectioning for a visual assessment for possible PTH and internal land damage.

Most test vehicles subsequently underwent reliability testing. One test vehicle design was subjected to multiple passes between -40°C and +90°C at one cycle per hour. Resistances were measured periodically, allowing monitoring of via integrity or integrity of the junction between internal lands and the barrels of larger PTHs. Most failures (as defined by a resistance change of at least 10% relative to the initial value for the net) were confirmed by inspection of cross-sections containing the suspected failure point, as localized by continuity testing.

Another test vehicle design was subjected to an insulation resistance test that involved application of a 15-volt bias between adjacent risk sites over an extended period at an environment of 50°C/80% RH. Resistances were measured periodically, allowing monitoring for the possible formation of dendrites between adjacent vias or between power planes and PTHs that accommodated press-fit connector pins. Apparent failure sites, as defined by sufficiently low resistances, were electrically isolated for identification of cause, which was dependent upon subsequent inspection of cross-sections.

A number of areas from each test sample were cross-sectioned for visual inspection after the test sample underwent simulated reflow assembly. Most of the test vehicles that were thus analyzed also underwent reliability testing prior to analysis. All cross-sections were taken in the vertical direction.

The test suite consisted of additional test coupons. This included interconnect stress test (IST) coupons with the added feature of PTHs that are each connected to a different power plane. For a number of IST coupons from some laminate/fabricator projects, capacitance measurements between adjacent power planes were performed[3] before and after these coupons were subjected to one or more passes through thermal profiles that were similar to the oven-based profiles that PCBs were subjected to.

Standalone 31.75 mm x 31.75 mm test coupons with 1.02 mm PTHs and unused lands on layers 2 and N-1 (or 3 and N-2) were also part of the test vehicle suite. In some cases, these were subjected to a solder float test. After a prebake at 100°C for a minimum of 6 hours, each coupon experienced six 10-second floats on molten solder (at 288°C), with a two-minute cooling period at room temperature between each pass. Carefully polished mounts were prepared for inspection of randomly selected rows of PTHs for signs of separation at internal land-to-barrel interfaces.

*** Material Characterization**

The kinetics of moisture absorption was measured gravimetrically as a function of time at 50°C/80% RH. Test samples were initially baked at 125°C for two hours in order to remove any adventitious moisture. Test samples were removed at regular intervals and blown dry with filtered, compressed air prior to being reweighed.

Thermomechanical analysis was conducted on rectangular samples excised from the appropriate test vehicle by means of a Perkin-Elmer TMA 7e equipped with a 1.00 mm diameter quartz probe and platform. Samples consisting of a 3 x 3 array of vias and samples devoid of any vias were evaluated. The probe was brought into contact with the sample under a normal force of 20.0 mN and the furnace ramped to either 260°C or 288°C at 5°C/min. Upon reaching the set point, the probe displacement was continuously monitored under isothermal conditions. During the isothermal hold, the probe height was observed to slowly but steadily decrease. Delamination was accompanied by an upward, often marked, displacement of the probe. The time to reach delamination was calculated from the beginning of the isothermal step. Delamination and/or cracking were confirmed by visual observations at 40X.

Observations and Discussion

*** Laminate Integrity**

For benchmarking purposes, a small number of DICY-cured laminate containing PCBs were exposed to a vapor phase reflow process with a peak temperature of 240°C. Consistent with other findings[4-8], visual inspection revealed internal laminate damage that was often severe enough to be observed on the PCB surface, sometimes even after only one pass through the reflow process. Others have demonstrated that these laminate-related issues may exist in various DICY-cured laminate-

containing PCBs, with signs starting to be exhibited after exposure to reflow profiles with peak temperatures as low as about 230°C[9].

All subsequent activities have focused on PCBs that were fabricated with laminates that are marketed as being compatible with the elevated temperatures associated with lead-free and mixed-solder assembly processes. The general trend noted in this study is that the properties of these laminates are potentially conducive to acceptable via reliability in the structures tested, but that unacceptable risks of damage to many of the laminates themselves exist when these are used in various PCB designs that are exposed to higher soldering temperatures.

Of particular concern are cracks that develop within the laminate as a result of exposure to higher soldering temperatures. Some of these cracks are readily apparent upon visual inspection of the PCB surface (see Figure 2). These "visible cracks" tend to appear away from design features such as via arrays.

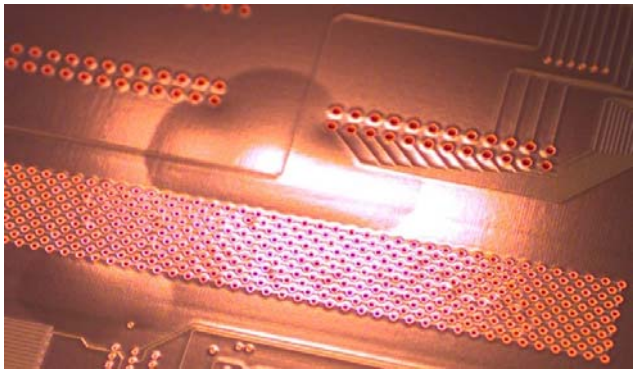

Figure 2 - Example of Externally Visible Delamination

Far more disconcerting are cracks within the laminate that appear deeper within the PCB (see Figure 3), with no clue of their presence provided by careful inspection of the external surfaces of the PCB, even if the cracks are fairly severe and/or widespread. Although these have been formally[2, 4] and informally reported by others, there is a sense by the authors that the industry as a whole will be better served by a broader discussion of this defect, which presents various reliability risks.

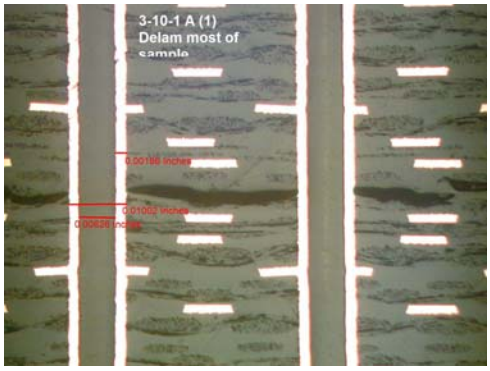

Figure 3 - Example of Internal Laminate Cracking

Various general trends about these laminate cracks have been revealed during visual observations of vertical cross-sections. It is anticipated that additional trends remain to be discovered. There is no doubt that even more trends, including relative contributions of the various contributing factors, would be revealed by studies involving more combinations of the key parameters revealed thus far.

The primary groupings of parameters of concern are the thermal profile, the PCB design, and the materials and processes used to fabricate the PCB.

The majority of observations are based upon testing of PCBs with ½- and/or 1-oz power planes. These observations are listed as follows (the results of limited observations for PCBs that include thicker copper foil layers involve additional parameters, which are listed later in the text).

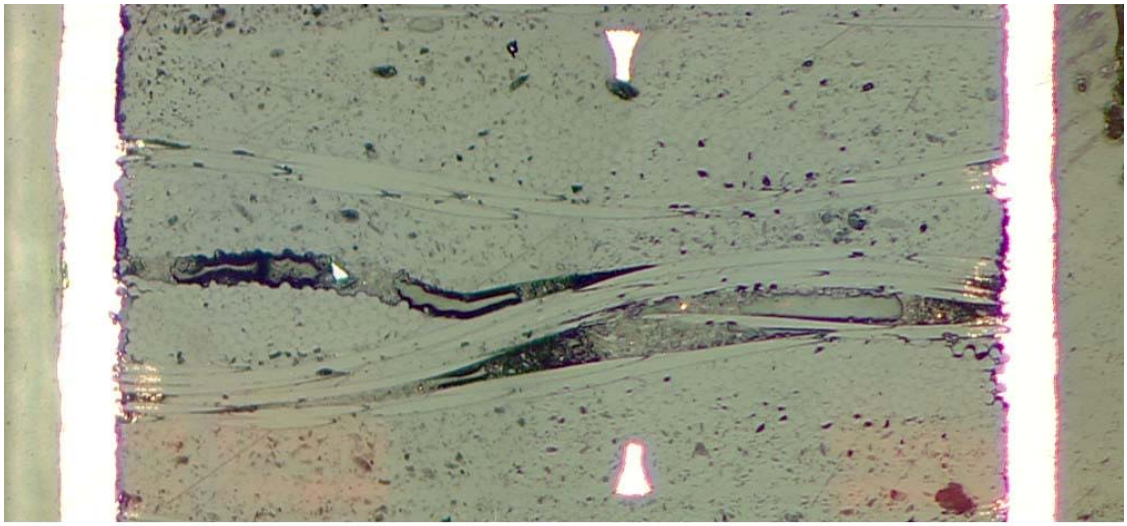

Figure 4 - Separation between Glass and Resin

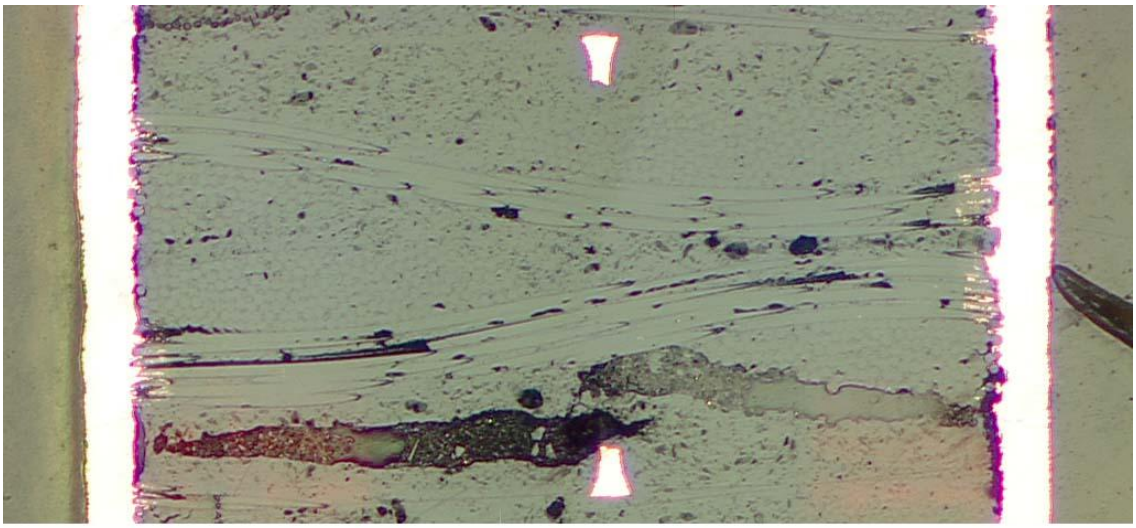

Figure 5 - Separation within Laminate Resin

* The laminate cracks are found in any or all of the three deepest laminate layers of the PCB. Both cores and prepreg may be affected (relative contributions have not yet been tallied).

* Cracks occur within the laminate, whether between the resin and glass (see Figure 4) and/or within the resin itself (see Figure 5). Where each crack originated is not evident from the cross-sections that have been inspected.

* The majority of laminate cracking has been observed during inspection of cross-sections prepared from test samples that have undergone 3-5 passes through a reflow profile that has a peak temperature of 260^{o}C.

* The only test samples that were assessed for the presence of laminate cracks after fewer passes were a small number of IST coupons, where capacitance between successive power planes was monitored after each pass through simulated soldering. In at least one case, capacitance changes were observed after only one pass through a 260^{o}C peak temperature profile (see Figure 6). Inspections of cross-sections of coupons that exhibited capacitance changes revealed the presence of laminate cracks (see Figure 7).

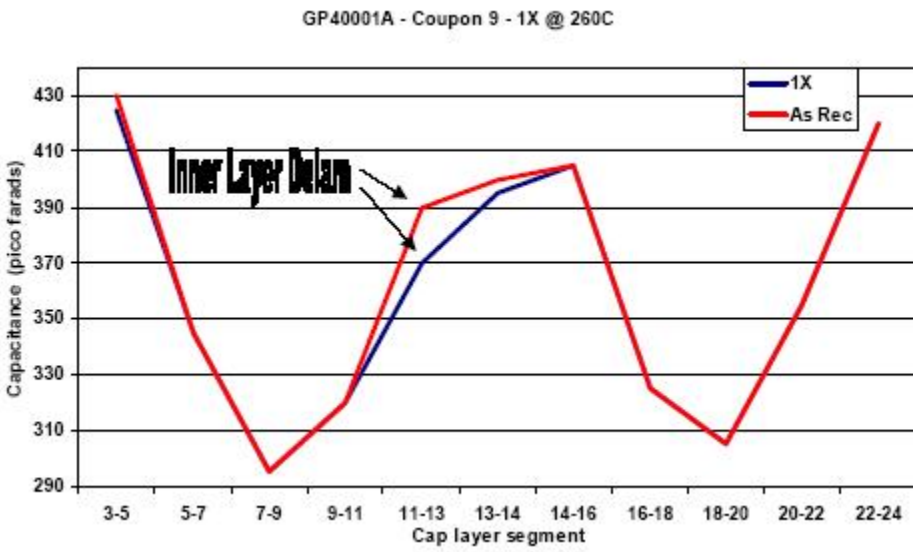

Figure 6 - Capacitance between Layers in IST Coupon, as-Received and After One Pass through 260°C Profile

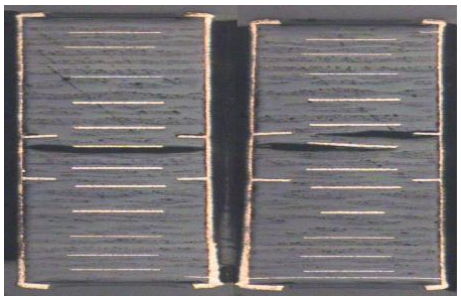

Figure 7 - Corresponding Laminate Crack

* The propensity for laminate cracking after exposure to peak reflow temperatures of 260°C increases with increasing PCB thickness, all else being equal. Significantly more laminate cracking has been observed in PCBs that are 3.30 mm thick than in PCBs that are 2.54 mm thick. The test vehicles provided by fabricator E with laminate 5 were the only exception, with no cracking noted in this low-loss laminate.

* Significantly less cracking has been observed after exposure to peak reflow temperatures of 245°C for PCBs that are up to 2.54 mm thick. The propensity for laminate cracking at this temperature for cards that are thicker than 2.54 mm has not been studied, but it is expected that the rate of increase of the propensity for laminate cracking with increasing thickness will be found to be greater at 260°C than at 245°C.

* The propensity for internal cracking is considerably higher for laminate within BGA sites than elsewhere. The only internal laminate cracks observed outside of BGA sites has been those that emerge from within BGA areas into surrounding, via-less areas. Two different examples of this are illustrated at two different magnifications. Figure 8 is a micrograph at higher-power magnification that shows fairly severe laminate cracking between vias (areas 2-4), with only minimal cracking extending beyond the array (area 1). Figure 9 is a micrograph at lower-power magnification that reveals laminate cracking (which cannot be seen in this photo), indirectly shown through significant buckling of power planes within the array area.

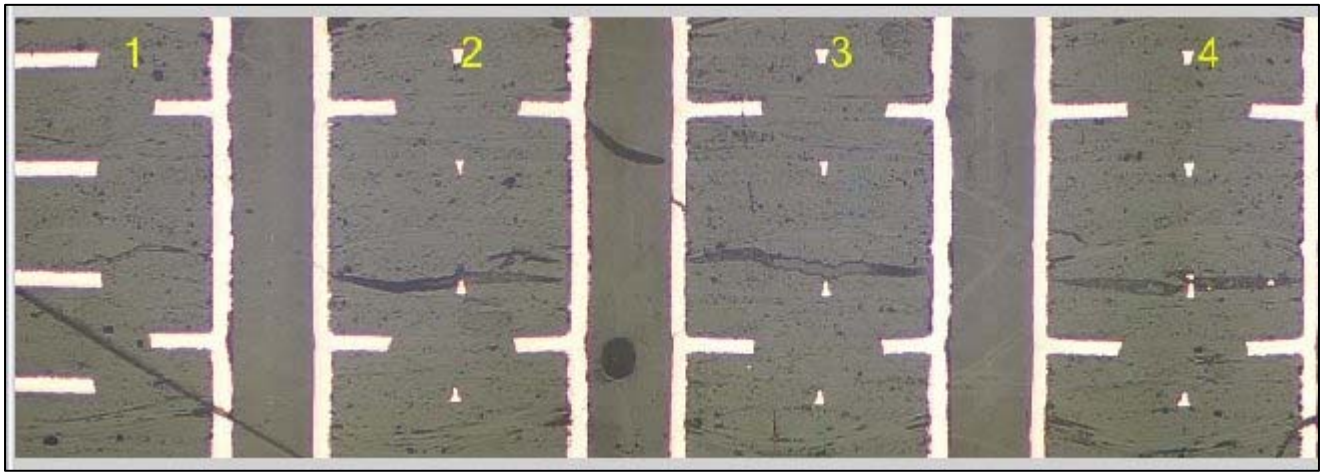

Figure 8 - Laminate Cracking Within Array

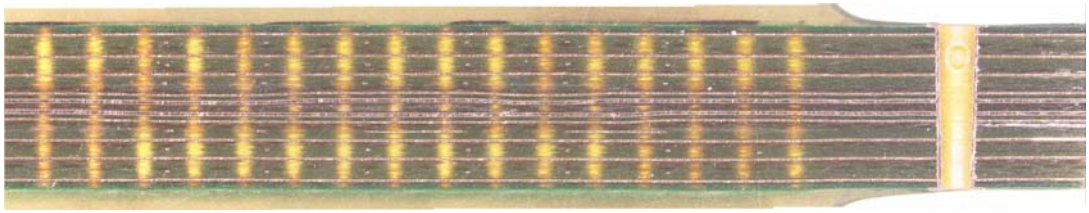

Figure 9 - Laminate Cracking Within Array

* Laminate cracking within BGA areas extends in a lateral direction, sometimes extending completely between adjacent vias. Cracking may appear in one or more large areas of the array.

* Lateral laminate cracks that are parallel with each other at different locations in the z-axis have not been observed in the area between adjacent vias within a particular core or prepreg layer, except for short distances.

* The propensity for cracking within BGA sites becomes increasing likely with decreasing via-to-via pitch. Laminate within arrays with larger via-to-via pitch becomes more likely to develop cracks as PCB thickness increases. Laminate cracking is common within 0.8-mm pitch arrays in PCBs that are 3.30 mm thick. The frequency of occurrence of laminate cracks in 1-mm pitch arrays increases in thicker PCBs.

* The propensity for cracking within tight pitched BGA arrays increases with increasing drill size. More cracking is observed within a 0.8-mm pitch array when the diameter of the drill is increased from 0.25 mm to 0.31 mm.

* In some cases, the propensity for cracking within tighter-pitched arrays increases with the size of the array. This has commonly been observed in 0.8-mm pitch arrays in test vehicles that are 3.30 mm thick (this has not been studied in thicker test vehicles).

* There are some indications that the likelihood for forming cracks near the center of the stack-up increases with the presence of fewer power plane clearances.

The likelihood of crack formation increases when 2-oz foil is substituted for 1-oz foil. For example, cracking that was observed in the laminate within a 1-mm pitch array within a test vehicle that was 3.18 mm thick was no longer seen when 2-oz power planes near the center of the test vehicle were replaced by 1-oz power planes in an otherwise identical test vehicle that was produced by the same PCB fabricator, using the same laminate.

Significant variations in the frequency of crack formation can occur as the result of fabrication processes and perhaps variations in the laminate.

* Variations in the frequency of laminate cracking were noted between two lots of test vehicles, separated in production by the PCB fabricator by a few days. The fabricator of these test vehicles was not aware of any changes in process and laminate used to produce the second lot of test vehicles.

* Two PCB fabricators produced the same test vehicle design, using the same laminate material and cloth styles, which was produced at the same laminate factory. The frequency of occurrence of laminate cracking was significantly higher for test vehicles produced by one of the fabricators.

As reported elsewhere for PCB fabricated with these types of laminates[4, 6, 10], the likelihood of crack formation was found to decrease if the PCB is baked prior to being subjected to higher-temperature reflow simulation. Limited testing with a group of thicker test vehicles revealed greater reduction in crack formation with increased baking time, up to a point. The positive effect of baking seems to be consistent with the positive effects of a decreased temperature ramp rate during reflow observed during another set of experiments.

Minimal testing has been performed with PCBs that contain power planes composed of 3- to 5-oz copper foil. As previously noted, an increased propensity for laminate cracking has been noted when 1-oz power planes were replaced by 2-oz power planes. This trend continues with the introduction of even thicker power planes. Whereas laminate cracking has been observed to be present near the deepest layers in PCBs with up to 1- or 2-oz copper foil, laminate cracks have been observed to move closer to layers with heavier copper foil that are located elsewhere in the stack-up (see Figure 10). PCBs with heavier copper foil have exhibited laminate cracks in arrays with PTH-to-PTH pitches larger than those associated with laminate cracking in PCBs with thinner power planes.

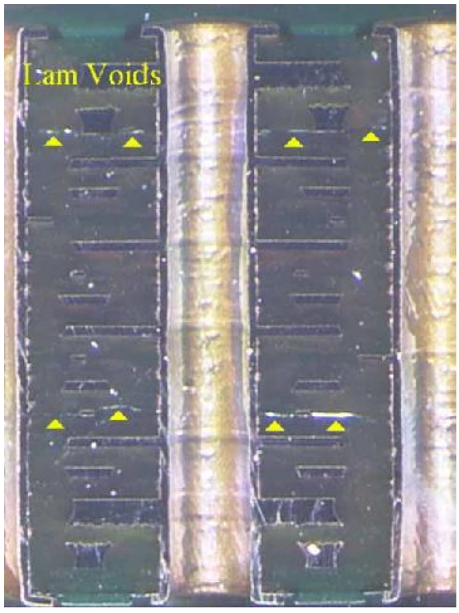

Figure 10 - Laminate Cracks in PCB with Heavy-copper Power Planes

Limited experiments involving a 24-hour prebake yielded minimal decrease in the occurrence of laminate cracks after a particular PCB with heavy-copper power planes was subjected to multiple passes through a 260°C peak temperature profile.

Externally visible cracks have been dealt with throughout the industry for many years. These are addressed in various specifications, including IPC 6012. Although the hidden laminate cracks described above are also addressed in various specifications, including IPC 6012, subjecting test vehicles to a typical eutectic tin/lead reflow soldering process simulation has not been observed to create internal cracks over the last 10+ years in this laboratory. The increased presence of these cracks dictates that further questions be asked and that serious actions be taken.

Laminate Cracks – Enhanced Testing and Detection

All of the observations reported above are based upon subjecting PCBs to thermal profiles that are intended to be simulations of actual soldering processes. This approach is necessary, given the much greater expenses associated with using actual assemblies for testing. Given the contribution of the thermal profile upon crack formation, it is important to understand what limitations may be involved with the use of thermal profile simulations and to adjust these as needed. Nevertheless, it is very important to point out that there have been a steadily growing number of undocumented reports within the industry of internal laminate cracks occurring within various production assemblies that experienced higher-temperature soldering processes.

Note that reflow ovens are not readily available to many investigators or quality control organizations. There is a need for more practical methods of simulating the thermal profiles associated with soldering processes.

The vast majority of information reported here about the presence and descriptions of internal laminate cracks has come from inspection of vertical cross-sections. Inspection of a cross-section can reveal considerable detail, but only of a limited field of view of the specimen. For testing that targets 260°C applications, the last (third) pass through a 260°C profile is probably one pass more than is likely to occur during normal assembly processes. However, based on observations that strongly hint that most laminate cracking is essentially initiated during the first pass, and given that fracture mechanics teaches us that cracks tend to propagate when exposed to sufficient stresses[11], it is intended that this last pass "develops" the crack for easier detection.

While still in an exploratory phase for a new laminate and/or design point, preparation and inspection of a considerable number of cross-sections may be required. Experience may provide enough guidance to reduce the extent of exploration, but increased due diligence may be required with the introduction of new risk factors.

Improved methods of detection of internal laminate voids are needed. Other less labor-intensive methods that at least direct the investigator to the best areas for preparation of cross-sections, or at best, offer standalone metrics, are desirable. Additionally, nondestructive tools that potentially allow test samples to be monitored as they undergo thermal stress are also desirable. Tools used for product quality monitoring may become necessary, too. Monitoring for changes in capacitance between adjacent power planes during reflow simulation appears to be a promising method.

As previously noted, laminate cracks that develop deep within a PCB have not been noted during visual observation of the external surfaces of the PCB. Of course, human vision is limited. Any attempt to monitor z-axis displacement during heating by using more precise mechanical techniques needs to use probes that are sufficiently small relative to the size of the laminate web of concern. Unfortunately, the diameter of the probes that are commercially available for use in thermomechanical equipment that measures z-axis expansion tend to be no smaller than about 1 mm. The inherent limitation of using a probe of this diameter is apparent from the results of t_{260} testing of samples with different via-to-via pitches. In one sample, t_{260} increased from 65.2 minutes to 71.1 minutes when moving from a featureless area to within an array of vias on a 1.27 mm pitch. In a different sample, t_{260} increased from 152.3 minutes to 161.3 minutes in moving from within an array of vias on a 1 mm pitch to another area on a 0.8 mm pitch. The results within the array areas are more indicative of support of the probe being provided by the copper than by the laminate.

Laminate Cracks – Concerns

A more precise understanding of the consequences of internal cracks is required, to the extent dictated by the OEM's expectations for performance and reliability for the product. Areas of concern include, but are not limited to the following:

* Laminate cracks provide a key prerequisite for conductive anodic filament (CAF) growth - the presence of a pathway between conductors that are at different voltages.

* Significant deformation of power planes has been observed near laminate cracks that formed after some test vehicles were subjected to higher-temperature reflow simulation (for example, see Figures 9 and 11). It is speculated that the forces responsible for this buckling might have been sufficient to initiate cracks and thus opens within traces, had they been present. In fact, there are undocumented reports[9] within the industry of open traces that have been discovered after assembly being in the immediate vicinity of internal laminate cracks.

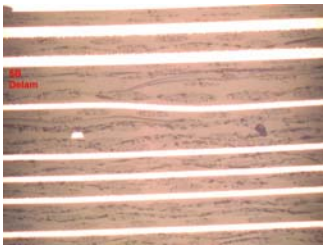

Figure 11 - Example of Power Plane Deformation near Laminate Cracks

* Fracture mechanics tell us that cracks tend to propagate when subjected to a sufficient level of stress[11]. This leads to speculation about the possibility of laminate cracks that are near external layers (e.g., in PCBs with heavy-copper power

planes) propagating during the insertion of certain press-fit connectors. It is further speculated that hairline cracks that evade normal observation may be present near external surfaces, facilitating the formation of pad craters.

* Of possible limited concern is the possibility of changes in the electrical performance of short but critical nets that exist near laminate cracks.

Internal Laminate Cracking - Proposed Mechanisms of Formation

Better understanding of the cause(s) of laminate cracking will probably lead to ideas for corrective actions. The following mechanism is proposed to explain most of the observations noted above. Many of these ideas are consistent with various studies and theoretical treatments for similar systems, including the strength of epoxy/glass interfaces[12-27] and thermally-induced delamination of electronic packages[28-40] (e.g., popcorning).

Moisture plays an important role in the proposed failure mechanism. The propensity for crack formation has been demonstrated to be reduced by baking at a temperature that is not expected to have a significant effect on the chemistry of the laminates studied here. These baking temperatures are unlikely to produce laminate breakdown products[41]. The positive effects of baking cannot be attributed to whatever stress relief this might provide[9]. Additionally, water plays a key role in crack formation in similar systems.

To understand the role of moisture in this failure mechanism, it is important to first consider that the laminate within a finished product is inherently punctuated with various voids within the resin and at interfaces such as those between the glass and the resin. Examples of these voids include areas within clearances that are not completely filled during the lamination process. Voids that are created by factors such as the mechanical stresses of drilling may also exist at the resin-to-glass interface near drilled holes, as is sometimes demonstrated by copper wicking that is readily apparent during inspection of cross-sections. Drilling of more brittle laminate has also been noted to result in the creation of very small microcracks near the drilled hole[9]. The extent of voids between resin and glass may vary according to the chemistry of the resin, the glass style, the coupling agent and the lamination process (both for cores and for prepreg layers), as well as the susceptibility of the coupling agent to hydrolysis.

In addition to whatever moisture may be present within the resin, moisture may also be present within some of the voids that exist within the laminate. Moisture may be introduced into the various aforementioned voids that emerge into the laminate from a drilled hole during the aqueous processes that the hole is subjected to prior to the creation of a sufficient moisture barrier during the plating process.

Upon heating, water within the resin and voids within the laminate will be driven towards the outer surfaces of the PCB. Moisture will seek the path of least resistance outward, being limited by the diffusivity of water through the materials within the PCB and the arrangement of these materials within the PCB. Whereas water cannot diffuse through copper and glass, it will find pathways through the resin and voids within the laminate. Entropic arguments suggest that water, especially at higher temperatures, will tend to migrate into voids while on its path outwards. This moisture exists as steam. The effective pressure of this steam against the boundaries of the void is dependent upon the temperature, the moisture concentration gradient within the surrounding laminate, and the effective diffusivity of water through the materials. The void will increase in volume if the pressure exerted by the steam exceeds the strength of the weakest interfaces on the periphery of the void. Essentially, the void can be viewed as the initiation of a crack, with propagation into a larger crack being driven by steam pressure[42]. This may be further enhanced by other factors, such as the chemical effects of water upon the strength of the resin-to-glass and the resin-to-filler coupling agents, expansion of the resin with increasing temperature, etc.

Cracks may tend to propagate even farther in locations where coalescence is possible, as may be the case, for example, if there are a number of preexisting resin-to-glass voids along the length of a glass strand. Cracks may continue to propagate with successive reflow and/or rework cycles.

It's reasonable to assume laminate cracking to be more likely in areas with higher moisture concentration, especially as these areas become more confined by copper, which serves both as a constraint to diffusion of moisture from the area, as well as a heat transfer medium. The higher propensity for crack formation in the deepest layers of a tight-pitch array of a PCB can thus be attributed to the high copper-to-laminate ratio, which provides higher rates of heat transfer and greater constraint to moisture movement. An increase in the average concentration of process-entrapped moisture with decreasing via-to-via pitch enhances this effect. Laminate cracking is predicted to become even more likely in structures in which there are fewer power plane clearances near the center layers of the PCB.

Enhanced risks are associated with PCBs with heavier-copper power planes. Although these are less likely to contain tighter pitched array areas, heat transfer will be facilitated by the thicker copper planes and there may be issues associated with the large volumes of resin-rich fill within clearance areas on these planes.

Internal Laminate Cracking - Potential Solutions

Observations noted above and the proposed failure mechanism lead to suggestions about a number of starting points for consideration as possible means of reducing the likelihood of crack formation. A system approach, involving more than one element of the supply chain, may be required, depending upon the PCB design, its applications and the intended lifetime of the product.

* Reduce the extent of voids within the laminate in the finished PCB.

* Reduce the moisture level within the PCB by the time it is subjected to high-temperature soldering processes. It will be important to ask "**how dry is dry"** for the particular PCB design, the assembly conditions and the customer product reliability requirements. Attention shall continue to be paid to the relative moisture capacity metrics provided by laminate suppliers (per IPC TM-650, Method 2.6.2.1) for each laminate. However, attention also needs to be paid to the moisture that is entrapped within the PCB during the fabrication process. Drying procedures that do not adversely affect other aspects of the PCB (e.g., solderability) may be required[43], with questions about whether this will be performed by the PCB fabricator or by the contract manufacturer needing to be answered. Questions about how the PCBs shall be handled after drying may also need to be addressed, with the possibility of a need to implement parts management in accordance with moisture sensitivity levels (MSLs) per IPC/JEDEC J-STD-020. Supply chain infrastructure and logistics must be addressed.

* Laminate Development and Selection. Consideration of longer t_{260} and t_{288} values and of higher T_d values are of value in laminate selection, but these metrics do not adequately address the laminate cracking phenomenon described in this paper. Laminates (and recommended fabrication processes) that reduce the amount of voiding should be considered, as should laminates with increased fracture toughness.

Greater emphasis on development projects that span the supply chain are needed. Feedback loops through the supply chain are needed to assess laminate candidates rather than predicting goodness on the basis of raw material properties that may no longer be applicable or adequate. New metrics may be required.

* Assembly Process Development. Processes that allow for slower, "non-explosive" evolution of moisture should be considered. In severe situations, vapor phase reflow may be the best alternative.

Until there is ample confidence that proper steps have been taken to reduce the likelihood of laminate cracks to an acceptable level, monitoring product for the propensity for cracking may be required. Practical methods of simulation and detection must be developed.

Via Reliability

All testing has involved test vehicles that were produced with laminates that were identified by preliminary testing as providing potentially acceptable via reliability for the diameters and PCB thicknesses of interest. In fact, this has been realized during this verification testing, provided that there was adequate via wall copper plating. Failures that are attributed to cracks within the via barrel have thus far been attributed to regions of abnormally thin copper that resulted from manufacturing anomalies such as contamination that hindered the flow of plating solution into isolated vias. It is expected[44] that the greater z-axis stresses exerted on the vias by the higher temperature soldering processes will result in greater sensitivity to manufacturing anomalies that have less effect upon via reliability when PCBs are subjected to the lower temperatures associated with eutectic tin/lead soldering processes.

All via reliability testing is preceded by simulation of higher-temperature reflow. Risk sites that are demonstrated to exhibit laminate cracking are excluded from test, as this otherwise undesirable phenomenon acts as a shock absorber, potentially giving the vias the appearance of being more robust than they would be in the presence of structurally intact laminate.

Innerplane Separation

Monitoring for potential development of separation between innerlayer lands and the barrels of large diameter PTHs was indirectly performed by monitoring resistance changes in daisy-chained nets after the test vehicles were subjected to reflow simulation (time-zero) and periodically thereafter during ATC cycling. In cases in which failures were noted, fewer (if any) failures were noted when identical test sites were exposed (as standalone 31.75 mm x 31.75 mm coupons) to a 6x solder float test. These results beg questions about the applicability of the 6x solder float test (at 288 ^{o}C) as an indicator of interconnect

failures upon exposure to higher-temperature soldering processes. This is consistent with increasing IP separation noted in IST testing with increased set temperatures[44].

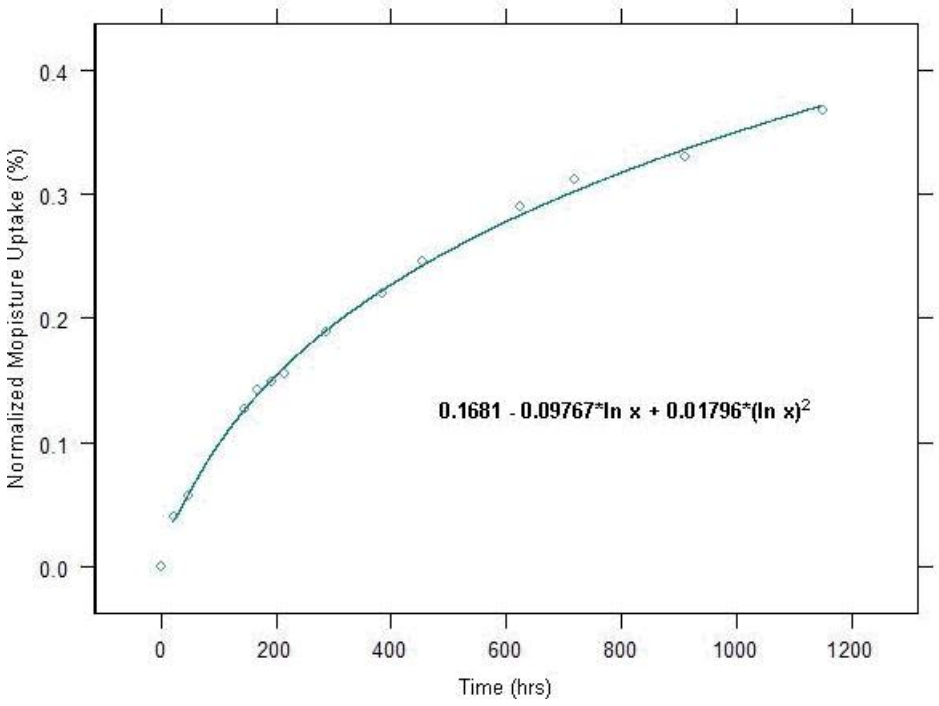

Figure 12 - Rate of Moisture Uptake by a Particular Insulation Resistance Test Vehicle

Insulation Resistance Testing

All insulation resistance testing is preceded by simulation of higher-temperature reflow. As is true for via reliability testing, risk sites that are demonstrated to exhibit laminate cracking are excluded from test, as the presence of laminate cracks are assumed to increase the likelihood of CAF formation.

An interesting set of paradoxes may exist if one attempts to perform standard insulation resistance testing with risk sites that have laminate cracks between vias. Whereas laminate cracks provide a path for CAF formation, the moisture that is required as an acceleration factor for CAF growth was expelled during the formation of the crack. It is not a simple matter of reintroduction of moisture into the insulation resistance coupon from the high temperature and relative humidity of the surrounding test environment. Figure 12 shows the rate of moisture uptake into an insulation resistance test coupon that is 2.54 mm thick. Migration of moisture into the deepest part of the PCB, where laminate cracking is most likely, will be even slower than shown here for the bulk of the test coupon. This begs questions about preequilibration times and how to account for an acceleration factor that may be changing during the test.

Conclusions

PCBs with certain design features that are fabricated with any of a number of different laminates that are marketed as being compatible with lead-free soldering temperatures have a propensity to develop cracks within the laminate upon exposure to these higher temperatures. These cracks, which increase the likelihood of opens and shorts, occur within the resin and/or at the glass-to-resin interface.

For PCBs with ½- and/or 1-oz copper foil planes, these laminate cracks tend to be located at or near the deepest layers of the PCB. The likelihood of finding indications of the presence of these cracks by means of observations of the outer card surfaces tends to decrease with increasing PCB thickness. The propensity for formation of these internal cracks generally increases with increasing peak soldering temperatures and possibly with increasing temperature rise rates. Formation of these internal cracks is highly dependent upon PCB attributes, tending to be more likely with increasing PCB thickness, decreasing via-to- via pitch, increasing array size (especially for tighter-pitched arrays), and possibly with increasing concentrations of power plane-to-via connections.

Minimal testing of PCBs has thus far demonstrated an increased likelihood for laminate cracks with increasing power plane thickness. As tighter-pitched arrays become less likely to be part of designs that involve thicker power planes, laminate cracking also becomes more prevalent in areas with larger PTH-to-PTH pitch.

Prolonged baking at 125°C prior to reflow tends to decrease the propensity for laminate cracking, but this becomes less effective for PCBs with thicker power planes.

A hygrothermal-based mechanism is proposed to explain the origin of this form of laminate cracking. The key elements of this mechanism include water that is introduced into small voids in the laminate between drilling and plating, its entrapment during plating, steam pressure that builds up within these voids during higher-temperature soldering processes, and the effects of this steam pressure upon various weak interfaces within the laminate (e.g., within the resin, between the glass and the resin, and possibly between the resin and fill material). These effects supplement other material effects (e.g., laminate expansion) that occur at higher temperatures. It is speculated that cracks may subsequently propagate during soldering steps and/or as the result of various applied mechanical stresses (e.g., insertion of press-fit connectors, vibrations felt by BGAs).

Concerns about the higher frequency of occurrence of these cracks, and the possible effects these cracks upon product reliability, demand attention. This includes development and application of better crack detection methods and predictive tests, as well as various corrective actions that will require better integration of members of the supply chain. These include reduction of voids within laminate of finished products, reduced moisture content during PCB fabrication and its subsequent maintenance (which may include adaptation of MSLs per J-STD-020), and/or development of new resins and coupling agents that are more resistance to internal steam pressure and thermal effects.

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Lessons Learned About Laminates during Migration to Lead-free Soldering

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February 22, 2007

Agenda

- Drivers
- Testing
  - Test Samples
  - Testing and Characterization
- Findings to Date
  - Laminate Integrity Issues → Key Focus
  - Internal Land-to-Barrel Integrity
  - Via Reliability
  - CAF

Drivers

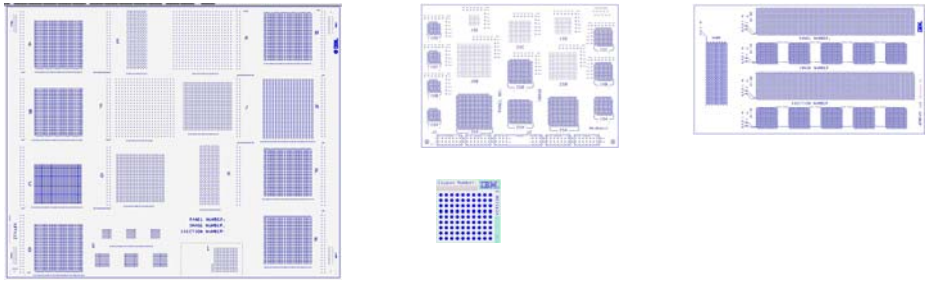
- RoHS Directive to Eliminate Lead from Solder
  - Server Exemption Until 2010 ??
  - Mixed-solder Assembly in Meantime
    - Sn/Pb Solder Attach of SAC-balled BGA
- Efforts Include Addressing Effects of Higher Soldering Temperatures Upon PCB Reliability
  - Target of 245 ºC for Mixed-solder Assembly
  - Targets of 245 ºC and 260 ºC for Lead-free Assembly

General Effects of Higher Temperatures

- Any Lasting Changes in Structure of PCB?
- Direct Effects Upon Organics and Entrapped Solvents
  - Chemical Changes
    - **Decomposition** [Laminate]
    - **Adhesives Bond Breakage** [Coupling Agents]
  - Physical Changes
    - **Expansion** [Laminate]
    - **Movement** [Entrapped Solvents, Decomposition Products]
  - Combinations
- Indirect Effects Upon Copper and Glass
  - Due to Above
- Reliability Effects
  - Blatant – After Assembly
  - Latent – Damage Initiated, Failing in Customer Environment

Test Samples

- Focus on Subjecting Test Vehicles to Stress Tests
  - Suite of Different Test Vehicles
  - Wired to Monitor Integrity of Various Risk Sites
    - Opens
      - Vias
      - Interconnects
    - Shorts
      - Via-to-via
      - Via-to-Plane
      - PTH-to-Plane (± Aggressive Press-fit Connectors)



  - Modular
    - Each TV for Different Stress Test
    - Layers for Wide Range of Stack-ups/Thicknesses w/o Rewiring
      - Focus on ½- and 1-oz Copper Foil
  - Update Designs as Learn

Test Samples

- Focus on “Lead-free Compatible” Laminates

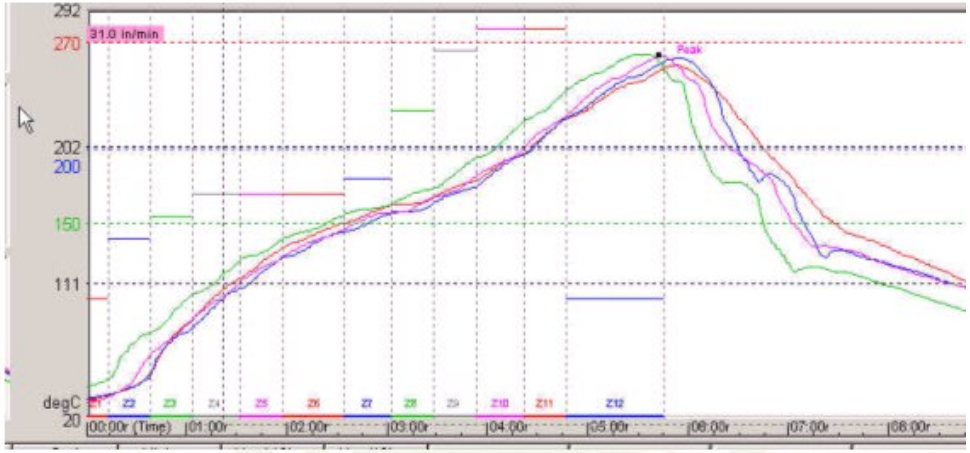
Fabricators, Laminates, Thicknesses (mils)								
Fabricator Code	Laminate Code							
	1	2	3	4	5	6	7	8
A							75	
B		130				100		130
C						130		
D	160							
E					195			
F				100				
G			160					
H			130					130
I			130					130
Properties								
T_g (°C)	180	175	175	135	210	170	175	180
T_d (°C)	325	350	365	360	400	340	340	340
Loss	0.02	0.02	0.02	0.02	<0.01	0.02	0.02	0.02

Thickness (mils)	Layers
75	14
100	20
130	26
160	28
195	32

Testing and Characterization

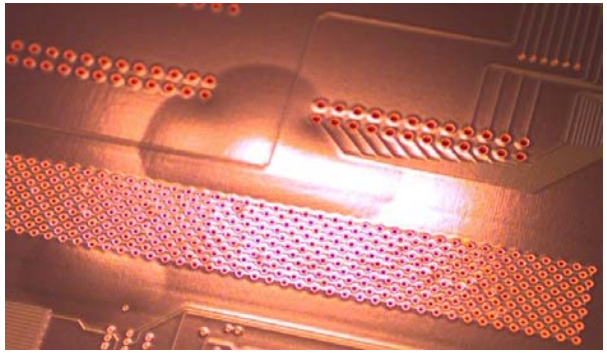
- Most TV Designs Through 5 Passes of Reflow Simulation at Contract Manufacturer
  - Some Through Prebake at 125 ºC
- Visual Inspection of Surfaces
- Press-fit Connectors
  - Insertion Forces
- Via Reliability Testing
- IR Testing
- Inspection of Cross-sections
- Some Auxiliary Studies

Thermal Preconditioning			
Thickness (mils)	Prebake @125 ºC	Passes	
		260 ºC	245 ºC
≤ 100	0		5
> 100	24 hrs	3	2

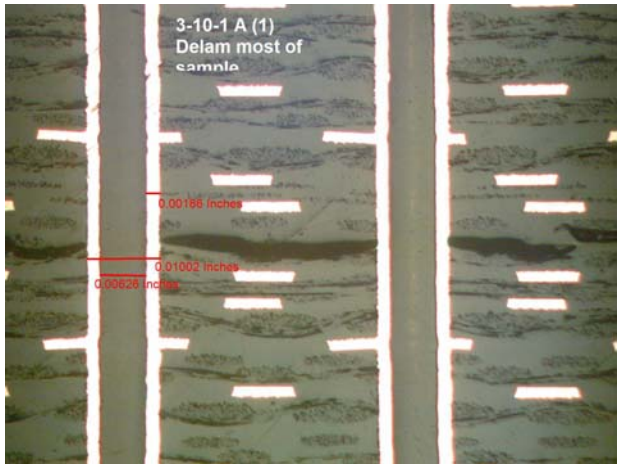


Visual Inspection

- Visual Inspection of Surfaces
  - Occasional Blistering in Featureless Areas

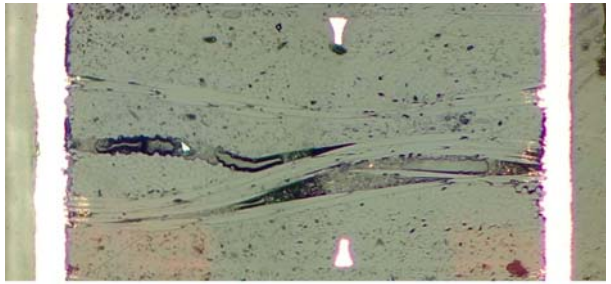


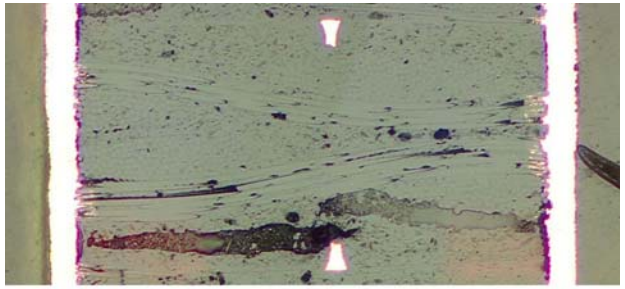
- Visual Inspection of Cross-sections
  - Laminate Fracture Near Center of Stack-up
  - **Not Visible During Inspection of Surfaces**
    - Too Small to Detect Mechanically, too
  - **Big Concern** – Key Focus of This Presentation
  - Key Parameters
    - Thermal Profile
    - PCB Design
    - Laminate
    - Fabrication Process



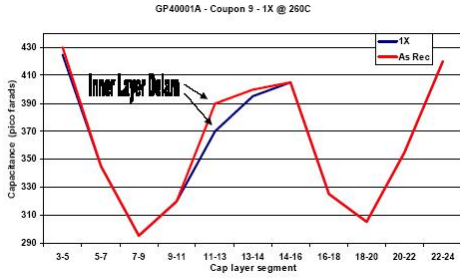
Laminate Cracks

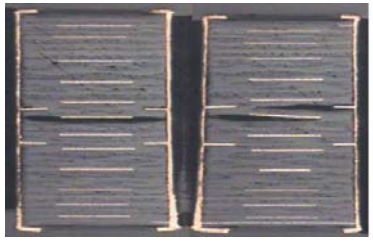
- Usually Found In Any or All of 3 Deepest Layers
- In BGA Areas
  - Lateral
  - Some Completely Between Adjacent Vias
- Within the Laminate (**not** Resin/Foil)
  - Resin/Glass Interface
  - And/or Within Resin Itself
  - Cross-sections Don't Reveal Crack Propagation Path





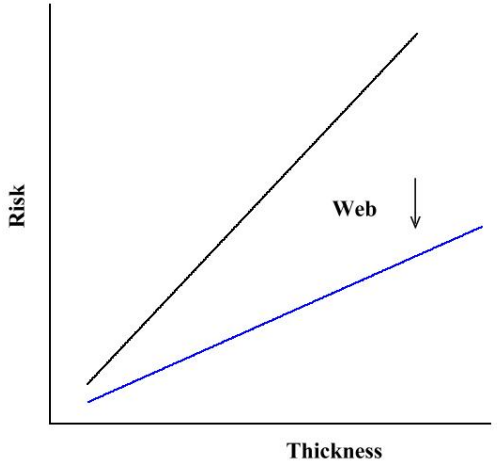
- Observed After As Few as 1x260 ºC by Capacitance Measurements (Bill Birch etal)





Laminate Cracks

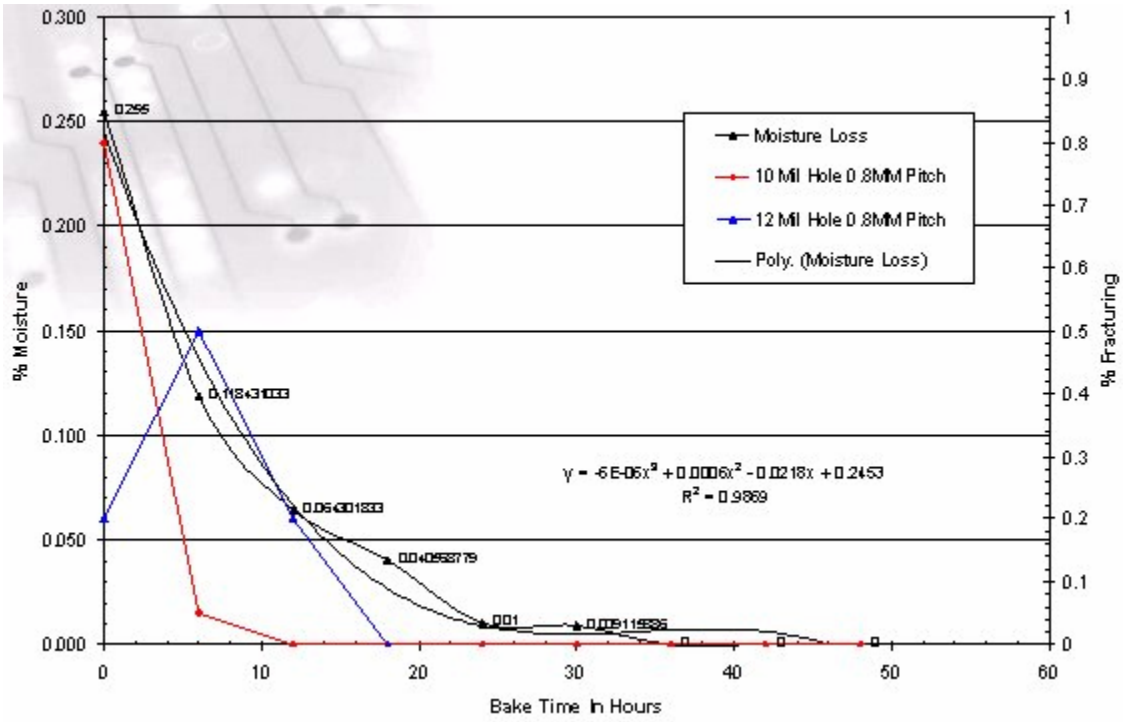
- Propensity Increases with Changes in PCB Structure
  - Decreasing Laminate Web Distance
    - Decreasing Via-to-Via Pitch
    - Increasing Drill Diameter
  - Increasing Array Size
  - Increasing PCB Thickness
- Indications of Increasing Propensity with…
  - Inclusion of 2-oz Foil Near Center of Stack-up
  - Decreasing Power Plane Clearances

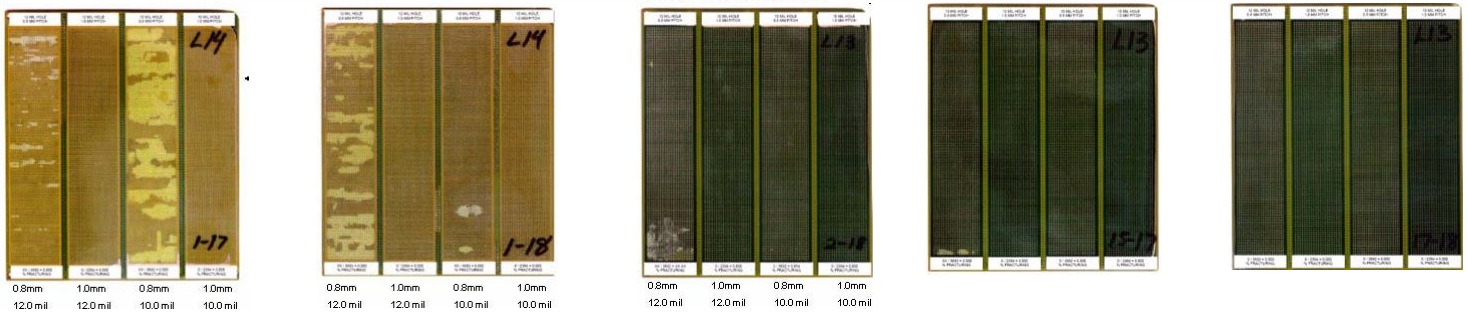


Laminate Cracks

- Propensity Effected by Fabrication Process
  - Lot-to-lot Variations for Fabricator G / Laminate 3
  - Significant Differences between Fabricators for Same Test Vehicle Design Point and Same Laminate
- Propensity Increases with Assembly Parameters
  - Increasing Peak Temperature
  - Increasing Ramp Rate
- Propensity Decreases with Increasing Prebake Time (125 ºC)
  - Up to a Point
  - Correlates With Weight Loss (see next page)

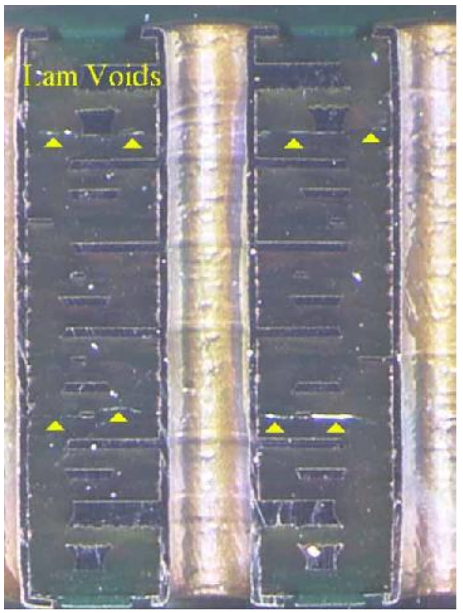
Moisture vs. Cracking





Laminate Cracks

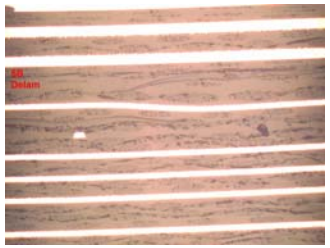
- Minimal Testing of PCBs with Thicker Copper Power Planes
  - Thus Far, Even More Concerns
  - In Featureless Areas – Visible on Surface
  - In Arrays – Not Visible on Surface
    - Tighter Pitches Not Required
  - May be Closer to Planes with the Thicker Foil
  - Prebaking Has Less Effect



Laminate Cracks - Concerns

- Creation of Paths for CAF Formation (Shorts)
  - Testing Paradox (see below)

- Formation of Opens
  - TVs Lack Traces
    - But See Power Plane Deformation
  - Industry “Buzz”
    - Implicated as Cause of Opens Seen at Final Test of Assemblies



- Signal Integrity
  - Electrical Properties of Air vs. Laminate
  - Critical, Short Nets

Laminate Cracks – Measurements

- Increased Emphasis on Simulation and Detection
  - Reflow Ovens and Reflow Simulation Tools
  - Detection Tools
    - Cross-sections Provide Details
      - But Limited View, Destructive, Labor
    - Electrical Changes
      - Capacitance
    - Other?

- Assess and Address Risks
  - Science and Engineering
  - Back to Basics

Laminate Cracks – Proposed Mechanism

- Model Based on
  - These Observations
  - Auxiliary Water Ingress/Egress Studies
  - Others' Studies
    - Integrity of Resin/Glass Interfaces
    - Thermally-induced Delamination of Electronic Packages (Popcorning)
    - Water Ingress/Egress

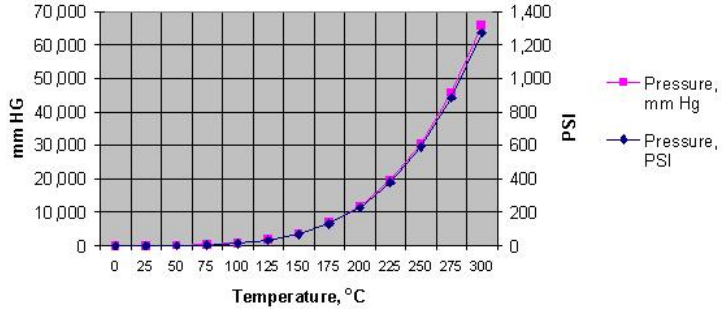
- Limited to Structures and Materials Studied Here
  - Other Mechanisms May Play Some Role
  - Other Mechanisms Play Larger Roles Elsewhere

Laminate Cracks – Proposed Mechanism

- Moisture Plays a Key Role
  - Likelihood Reduced by Prebaking at 125 ºC
  - Self-consistency of Model
- Voids/Gaps Near Drilled Vias Play a Key Role
  - Incompletely Filled Clearances
  - Drill-created Voids
    - Resin-to-Glass Interfaces (cf, Wicking)
    - Microcracks in Resin
  - Other Microcracks
  - Serve as **Crack Initiation Sites**
- Water Into Laminate Structure Through Drilled Holes
  - Aqueous Processes Between Drilling and Plating
  - Generally More than Still Present After Lamination

Laminate Cracks – Proposed Mechanism

- Upon Heating, Water Driven Towards Surface of PCB
  - Seeks Path of Least Resistance
  - Limited by Diffusivity of Structure & Materials



- Steam Within Voids Will Expand Voids
  - If Structure is Weak
    - Coupling Agents, Resin Toughness, etc
    - Synergistic w/ Hydrolysis of Coupling Agents, CTE Mismatches
  - If Diffusion is Limited (Copper & Glass Barriers, Diffusivity in Resin)
  - Vapor Pressure of Water is High in Voids (Bulk Water), Lower in Resin
    - Raoult's Law Suggests ~1% of Bulk Vapor Pressure in Resin

- Cracks Propagate Even Further if Can Coalesce
  - Facilitated by Built-in Pathways (e.g., Glass/Resin, Agglomerated Filler?)

- Original Smaller Voids/Microcracks Propagate into Larger Cracks

Laminate Cracks – Proposed Mechanism

- Importance of PCB Structure
  - More Likely in Areas With Longer Diffusion Paths
    - Near Middle of Stack-up
      - Thicker PCBs
    - More Copper Barriers (Higher Copper Surface Area-to-Resin Ratio)
      - Fewer Clearances
      - Tight-pitched Arrays
  - Higher Water Concentration in Tight-pitched Arrays
    - More Laminate Damage (“Voids”) Created During Drilling
    - Less Web Between Diffused-into Zone Around Each Via
  - More Likely in Areas with Faster Heat Transfer
    - Higher Copper-to-Surface Area Ratio in Tight-pitched Arrays

Laminate Cracks - Levers

- Reduce Propensity for Void Formation in As-Produced PCB
  - Raw Materials -- Resins, Coupling Agents, (Filler Dispersion?)
  - Processing
- Reduce Moisture Level
  - How dry is dry?
  - Fabrication
  - Storage
    - Need MSL Ratings?
  - Prebaking
    - Practical Issues
    - Solderability Effects
- Increased Fracture Toughness
  - Resin
  - Resin-to-Glass Bond
- Assembly Process
  - Vapor Phase
  - Reduced Ramp Rate

Via Reliability

- No Surprises
  - Enhanced Sensitivity to Manufacturing Anomalies
- Will Not Test If Laminate Cracks Present
  - Need to Reduce/Eliminate Propensity for Cracking
  - Falsely Better Lifetime

Land-to-Barrel Integrity

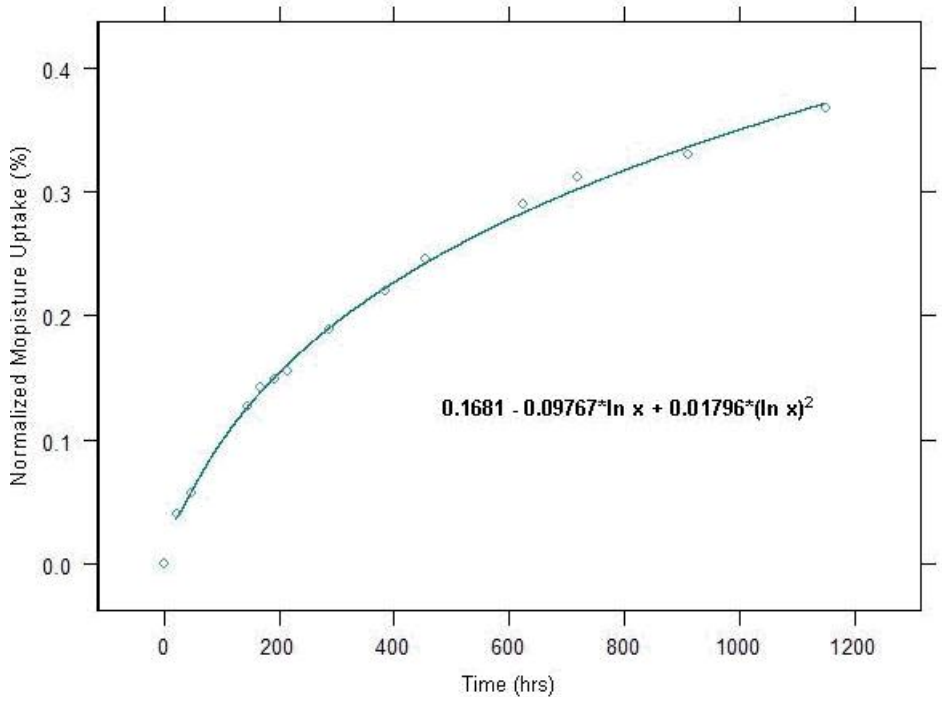
- 260 ºC Reflow Can Yield More Land-to-Barrel Separation Than 6x Solder Float at 288 ºC

- How Will PCB Fabricator Monitor Internal Land-to-Barrel Integrity?

CAF Testing

- Will Not Test if Has Exhibited Laminate Cracking

- Testing Paradox
  - Cracks Created by Rapidly Expelled Moisture
  - Moisture Required as Test Accelerant
  - Moisture Replenishment is Very Slow During Test
  - False Sense of Security?



Summary

- Various Reliability Tests of PCBs Built w/ “Pb-free” Laminates
- New and Enhanced PCB Reliability Issues Noted – Seen it All?
- Focus on Laminate Fractures Near Center Layers
  - Not Apparent during Inspection of Outer Surfaces
  - Resin-to-Glass Interface, Within Resin, Not Resin-to-Copper
  - Reliability Concerns – Opens, Shorts
  - Propensity for Formation Influenced by
    - Materials
    - PCB Design – Thickness, Pitch, Array Size, Clearances
    - Fabrication Process - Introduction of Moisture
    - Assembly Process – Peak Temperature, Ramp Rate
  - Voids / Cavities Propagate into Larger Cracks Due to Steam Pressure
    - Water Entrapment Between Drilling and Plating
    - Synergy - Hydrolysis of Coupling Agents, CTE Mismatch, etc
  - Levers to Pursue
    - Reduce Moisture Entrapment, Fewer Gaps, Baking
    - Higher Fracture Toughness – Resin, Glass-to-Resin Bond
    - Need MSL Ratings?
    - Special Assembly Processes (eg, Vapor Phase)

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