Lead Free Assembly Qualification of ALIVH Boards

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Abstract:
The migration to lead free reflow is bringing many challenges for the PCB industry. High Tg laminates, stability of materials thru 2X reflows, rework, moisture sensitivity etc. This requires careful evaluation of new laminate materials, balancing component layout and optimization of reflow profiles to minimize damage to PWBs. This is critical for thin PWBs (less than 0.1 mm) boards used in cell phones and other portable products that use build up microvia technologies.

The trends of increased functionality and reduced size of portable wireless products, such as handsets; PDAs are demanding increased routing densities for printed circuit boards. The handheld wireless product market place demands products that are small, thin, low-cost and lightweight and improved user interfaces. In addition, the convergence of handheld wireless phones with palmtop computers and Internet appliances is accelerating the need for functional circuits designed with smallest, low-cost technology.

Historically, the industry has met this challenge through high density interconnect technology and increased silicon integration and component miniaturization. Microvia high density interconnect (HDI) also known as build up technology, is one method for constructing circuit boards with high routing density demands. [1].

For HDI board, vias can be formed using unreinforced dielectric such as Resin Coated Foil (RCF), using processing techniques such as laser drilling or photoimaging. The vias are then metallized using electroless copper/electrolytic plating. The advantage of the HDI construction is the ability to create smaller vias (6 mils) and via pad sizes. This enables higher routing density, lower metal count, reduced board area and increased functionality as compared to conventional boards. HDI improves the wiring density by using build up microvias in the outer layers. However there is still dead space where components cannot be mounted and lines cannot be wired, because of staggered via hole structure.

On the other hand, ALIVH-G (Any Layer Interstitial via Hole) needs no through hole. This is because any two layers are electrically connected by IVH (Interstitial Via Hole). The IVH can be placed in any position. Since there is no through hole that disturbs interconnections between components, the dead space becomes reduced and the wiring capability is improved greatly. [2]

Past board technologies used stacked microvias on the outer layers. Current board designs use ALIVH-G technology. These vias are laser drilled and the interconnection technology used is conductive copper paste. The typical design rule is Lines/Space 100/100 micron and Via/Land is 200/400 microns. ALIVH-G technology makes a lightweight substrate (less than 100g)

The paper presents the evaluation conducted to ensure the stability of the laminate and microvias through the double-sided lead free reflow process. This was evaluated as a part of the phone product qualification.

Introduction:

Higher density packages and PWB applications requirements are driving the need for high-density interconnect design capabilities using microvias. The benefit of using ALIVH-G is the ability to incorporate high density, high performance area array packages to increase performance of handsets, PDAs etc. Microvias are typically formed on an epoxy resin laminate or dielectric layers of the PWB.

ALIVH-G technology is emerging in handset industry; however, production level reliability data for double-sided surface mount assembly and lead free reflow is not readily available. This requires users to establish their own reliability data.

This paper presents the assembly qualification of the ALIVH technology thru 2 passes lead free reflow and rework. Results of solder joint reliability testing, shear test and X-sectional analysis are presented.

PWB Design and Fabrication:
The PWB was designed as an 8-layer thin board 0.8 mm thick. The PWB had an ALIVH -G configuration with copper paste microvias in all layers. ALIVH-G type substrate uses epoxy glass instead of Aramid paper, which has higher moisture

absorption. This eliminates baking of the PWB prior to reflow. Table 1 compares the properties of ALIVH–G type substrate with conventional ALIVH and FR-4 substrate. [2]

Table 1. Properties of ALIVH-G type, Conventional ALIVH and FR-4 Substrate

Properties	ALIVH-G Type	Conventional ALIVH	FR-4
Water Absorption (wt %)	0.5	2.1	0.8
Tg (degrees C)	170	170	125
CTE (PPM/degrees C)	11	11	16
Flexural Modulus (Gpa)	30	13	21
Hardness (Gpa)	2.6	2.6	0.6
Density (g/cc)	1.9	1.4	1.9

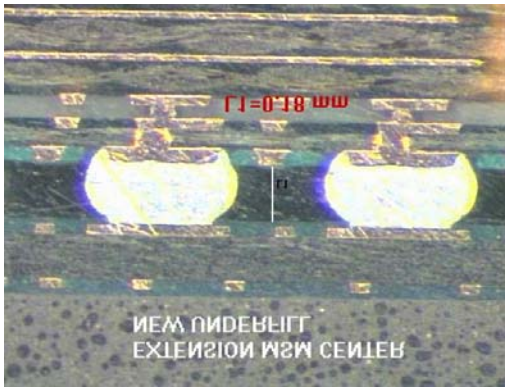

Figure 1. HDI PWB

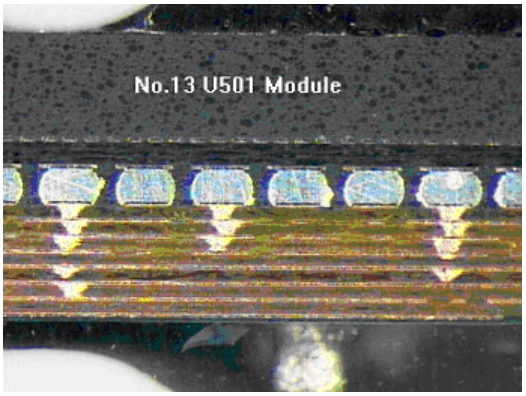

Figure 2. ALIVH PWB Board Assembly:

Board assembly process was a double-sided surface mount assembly soldering of ball grid array packages, connectors, chip resistors, capacitors, and diodes.etc. The assembly was reflowed in convection air at a peak temperature of 243C. The solder paste used for assembly was Tin/Silver/Copper)– SAC 305 - No clean version.[6].

Mask defined as well as Etch defined pads were used for soldering BGAs. This evaluation was necessary as historically KWC has used etch defined pads, while mask defined pads are commonly used in ALIVH technology. Shear testing was conducted to compare the differences. Shear values were also compared to existing etch defined pads used in HDI boards. Ball shear was also conducted by soldering 0.3 mm and 0.4 mm solder balls on the pads. No microvia damage was seen after shear, but etch defined pads showed lifted pads. Figure 3 and 4 show a comparison of etch Vs mask defined pads. Table 2 shows the shear values.

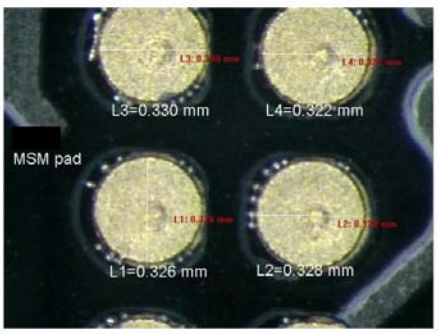

Figure 3 - Etch Defined Pad

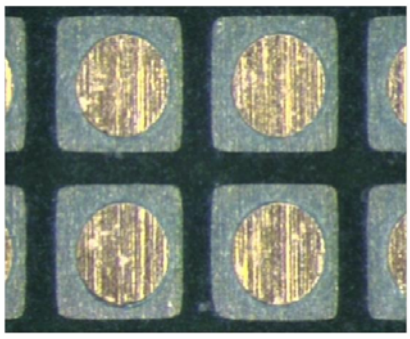

Figure 4- Mask Defined Pad

Table 2. Shear Test Post Reflow (Pounds)

	EMD # 1	EMD # 2	SMD # 1	SMD # 2
MSM	39.55	40.55	45.55	53.10
FLASH	22.25	25.20	47.60	31.20
U300	22.50	26.50	28.35	23.40
U101	35.05	34.10	38.85	23.35
U151	27.20	24.30	24.60	22.55
YJ4802(BATT)	34.10	39.75	44.15	36.41
QN601(CONN)	38.50	39.90	41.05	36.35
402 #1	2.35	2.40	1.60	2.80
402 #2	2.40	3.65	3.35	2.75
402 #3	2.15	2.65	2.50	2.00
402 #4	3.50	1.95	2.20	1.90

Post Reflow X-Sections:

X-sections were performed on the BGA packages and other components to evaluate the quality of the solder joints and ensure compliance to IPC 610 – Rev D for leaded packages and IPC 7095 for BGA packages. Also microvia integrity was evaluated with X-sectional analysis. X-sections showed acceptable solder joints and no degradation of microvias. [3, 4]. Figure 5 shows the X-sections on an etch defined pad and Figure 6 shows the X- section of a mask defined pad. The standoff height of the joint is higher for a mask-defined pad. For PWB assembly process, lot/lot consistency is essential. The tolerances of the etching process are preferred as compared to the solder mask apply process. However, due to shear values being higher for mask defined pads, a decision was made to go with mask defined pads for BGA packages.

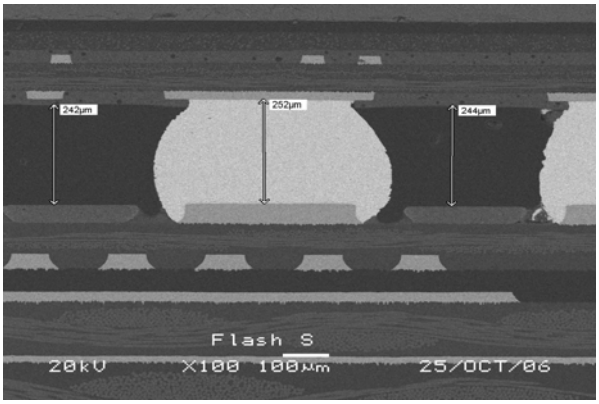

Figure 5 -BGA Solder Joint- Etch Defined Pads

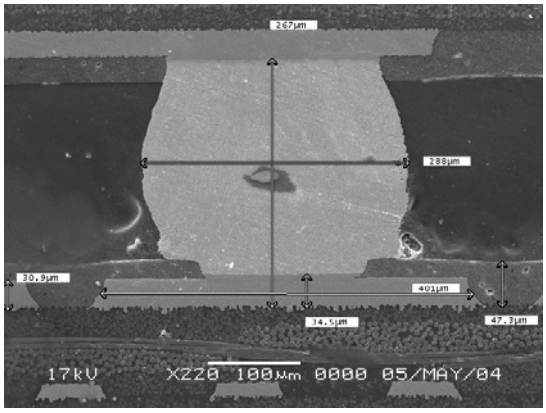

Figure 6 – BGA Solder Joint – Mask Defined Pads

Rework Process:
Rework of SMT packages is performed using hot air soldering tools and application heat using controlled ramp/soak profile. The concern was damage to microvia connections and PWBs pads during component removal and reattach. Component rework was performed 2X on the leaded packages and 1X on the Ball-Grid Array packages. All packages survived rework. There was no damage to PWB pads, or blistering of solder mask during rework. No damage was seen on microvia connections. Figure 7 and figure 8 show PCB surface after package removal showing no lifted pads.

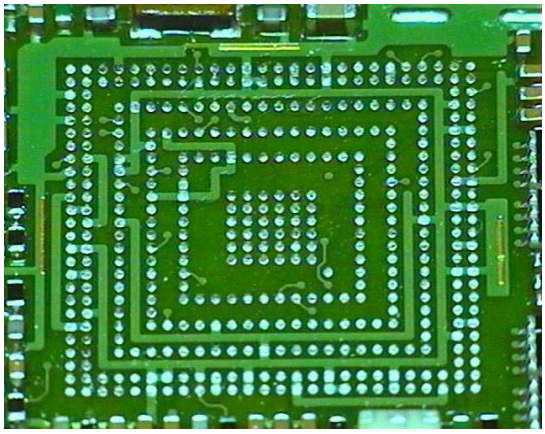

Figure 7- BGA Pads 0.3 mm after package removal

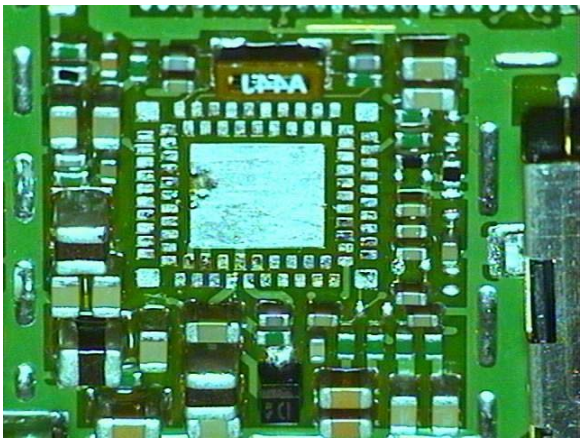

Figure 8 - BCC Pads after Package Removal

Solder Joint Reliability Test:
Solder joint reliability testing was performed for assembly qualification per IPC SM 9701. Assemblies were thermal shock tested from –25C to +125C for 500 cycles. [4] Temperature humidity testing was performed at 85C/85% Relative Humidity for 1000 hours. Samples were X-sectioned post-test to evaluate the joint quality. The joints appeared slightly grainy after thermal shock test and oxidized after temp.humidity testing, but no cracks were seen in the joints. No separation was seen where the microvia connected to the capture pad. Figure 9 and 10 show X-sections after temp.humidity test. Figure 11 and 12 show X-sections after thermal shock. No cracks on solder joints or separation of vias were observed.

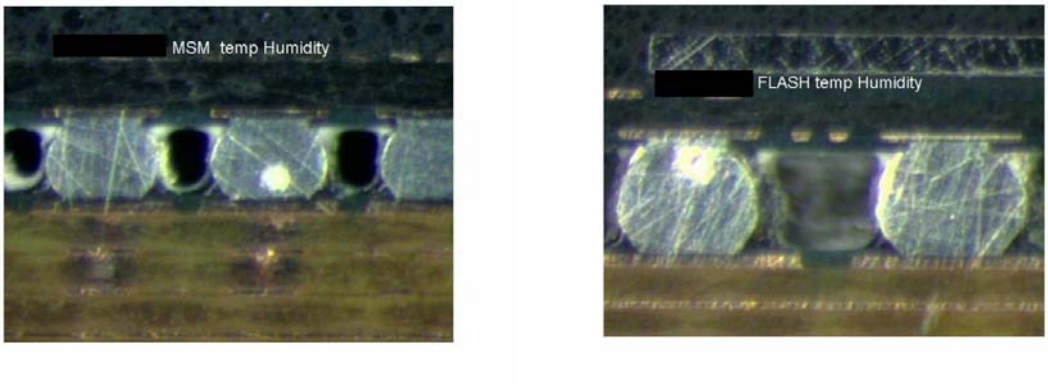

Figure 9–X-sections Post Temp. Humidity

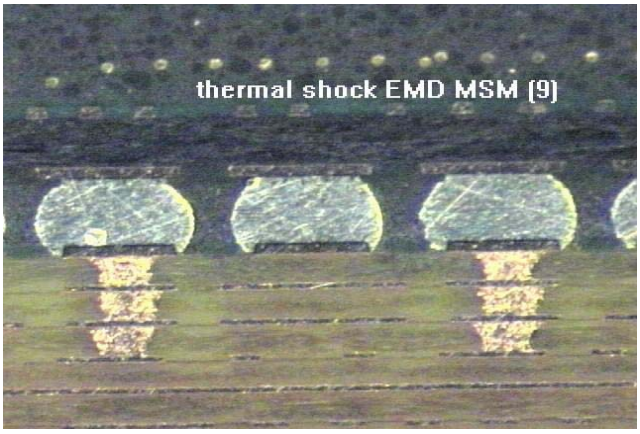

Figure10 –X - section Post Temp. Humidity

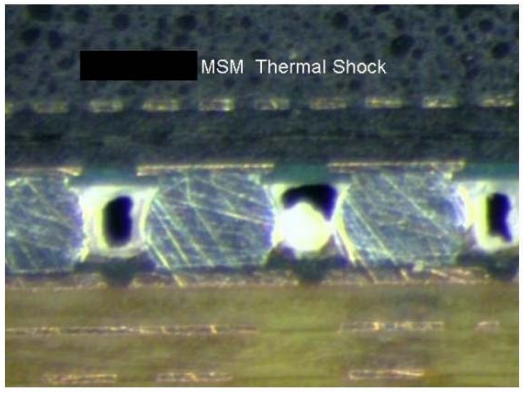

Figure11, 12- X-sections – Post Thermal Shock

Phone Level Drop Test:
Phone level drop tests were performed at 1.5 meters on a hard vinyl surface. Assemblies were X-sectioned post drops to evaluate solder joints and microvia connections. No solder joint failures or microvia cracks were seen after drop test. However, some pads ruptured from the PWB. This is contributed by the lower bond strength of copper to the ALIVH laminate.

Conclusion:
Stacked microvias ALIVH PWBs have demonstrated reliability thru 2X reflow and lead free rework operations. The assemblies have survived thermal shock and temp. Humidity test and drop shock testing. Since, no failures or cracks were seen in the joints or microvias, the assembly passed solder joint reliability qualification testing.

In order to better understand the ruptured pads after drop, dynamic high g shock testing will be conducted to understand the limits of the PWB to copper adhesion.

References:

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