Reliability of Mis-registered HDI Plated Through Holes

Ivan Straznicky, Jason Rose
Curtiss-Wright Controls Embedded Computing
Ottawa, Ontario, Canada

Abstract
Mechanically drilled through holes in PWBs form interconnects between copper layers through the use of copper pads. These pads are larger than the drill diameter to account for such factors as layer-to-layer misregistration during lamination, drill misregistration, and drill wander. The requirements for the pad's remaining annular ring after drilling are specified in IPC-6012, Qualification and Performance Specification for Rigid Printed Boards. For Performance Class 3 (High Reliability Electronic Products), these requirements are 0.001" minimum annular ring for internal layers, and 0.002" for external layers. Performance Classes 2 and 1 allow 90º and 180º breakout of the hole from the pad, respectively. This leads to the conclusion that breakout or tangency of the hole to the pad are less reliable than complete annular rings.

Testing was performed to determine the reliability of plated through holes that met Class 2 requirements compared to holes that met Class 3 requirements. Interconnect Stress Testing (IST) coupons were used as test vehicles, with drill location offsets applied to some coupons to force tangency or breakout (Class 2). In addition, two pad sizes were used, one representing standard density designs (larger pads) and the other representing higher density designs (smaller pads).

Results from IST showed that the higher density design practice had equivalent or higher reliability, even with tangency/breakout. Finite Element Analysis (FEA) is used to validate these results.

Introduction
Interconnects between copper layers in a PWB are often produced by drilling a through hole into the laminated layer stack and plating the hole with copper. This forms a copper barrel in the hole, creating the electrical path between two or more layers. Copper pads are used at the required layers to form a connection with the copper barrel. The pads are sufficiently larger than the drill diameter in order to account for such factors as layer-to-layer misregistration during lamination, drill misregistration, and drill wander. Many PWB manufacturers specify that the pad diameter be at least 0.3 mm [0.012"] larger than the drill diameter to account for these factors and still maintain the minimum annular ring requirements defined in IPC-6012, Qualification and Performance Specification for Rigid Printed Boards, Performance Class 3 (High Reliability Electronic Products). For Class 3 boards, these requirements are 25 µm [0.00098"] minimum annular ring for internal layers, and 50 µm [0.00197"] for external layers.

Due to continual increases in functional density of circuit card products, the interconnect density in PWBs has increased to the point where the IPC-6012 Class 3 annular ring requirements are becoming more and more difficult to meet. For example, 0.33 mm [0.013"] diameter drilled through holes with 0.64 mm [0.025"] diameter pads move to 0.25 mm [0.010"] diameter holes with 0.5 mm [0.020"] diameter pads to fit more interconnects within the same volume of PWB. Thus, with the registration capability mentioned above (minimum of drill + 0.3 mm or 0.012" for Class 3), there is an increasing likelihood that Class 3 annular ring requirements will not be met for higher density hole/pad cases (see Figure 1), with increasing chance of breakout.

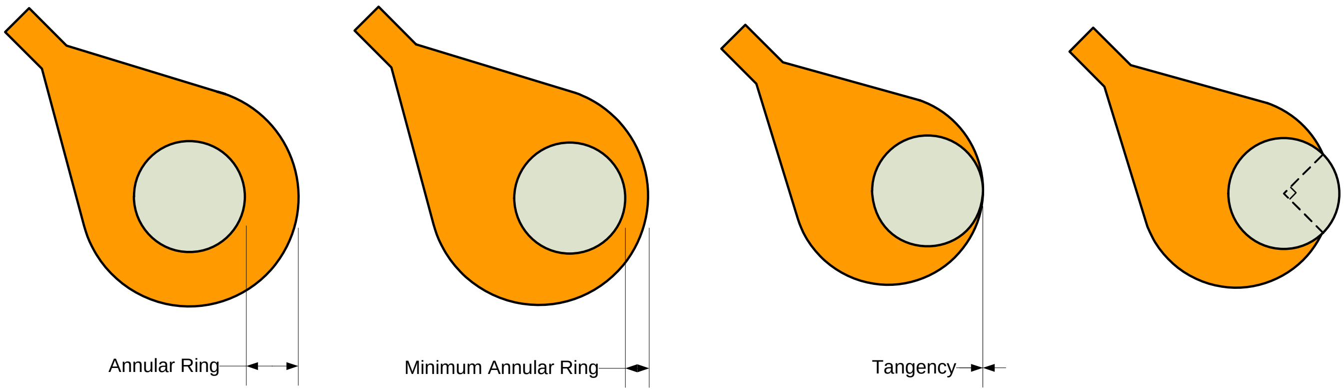


Figure 1 - Pad drawings showing (from left to right): Perfect registration of hole to pad (rare); Misregistration causing minimum class 3 annular ring; Smaller pad and misregistration causing tangency (rare); Smaller pad and misregistration causing 90° breakout (Class 2 limit). Note that the pads have a "teardrop" shape in line with the conductor track. This is used to minimize the possibility of creating an open solely due to misregistration.

It is generally assumed that the Class 3 requirements are more reliable than Class 2 and Class 1, which allow up to 90º and 180º breakout, respectively. However, there does not appear to be much test data to support this assumption, and what is available appears contradictory, e.g. "Breakout should be allowed without limit"[1], "… complete annular ring affords a performance benefit…"[2]. Thus, testing was conducted to determine the reliability impact of misregistration on plated through holes; particularly the impacts of tangency or breakout in smaller pads for high density interconnect (HDI) boards.

Test Vehicle

Interconnect Stress Testing (IST) coupons were used as test vehicles. The IST coupon design represented a high density single board computer with the following PWB features:

- 18 layers, 2 mm [0.08"] total nominal thickness
- Microvias from layers 1-2 and 17-18
- Buried vias from layers 2-17
- Through hole vias from layers 1-18
- High T_g FR-4 laminate material ($T_g \sim 170$ºC)

Due to the high interconnect density of the single board computer, 0.25 mm [0.01"] diameter holes with 0.5 mm [0.02"] diameter pads were considered for all buried vias and many through hole vias. Thus, the IST coupon used 0.25 mm as the drill diameter for both. Two different pad sizes were used; 0.5 mm [0.02"] to represent the high density case, and 0.64 mm [0.025"] to represent the standard Class 3 density case.

With the main objective of the testing being to determine reliability of plated through holes with sub-Class 3 annular rings, it was important to achieve at least a tangency condition on holes considered to be the least reliable. Based on extensive IST testing at the authors' company, the buried via holes from layers 2-17 are typically the least reliable. In consultation with the PWB manufacturer, a drill offset of 50 µm [0.002"] in the coupon's long axis (+X-axis in Fig. 2) was applied when drilling these holes on some of the IST coupons to promote breakout. Thus, a test coupon would belong in one of the following four categories:

- 0.025" pads
- 0.025" pads with 0.002" drill offset
- 0.020" pads
- 0.020" pads with 0.002" drill offset

These four categories of coupons were arranged on the fabrication panel (18" x 24") as shown in Figure 2. Five such panels were fabricated, for a total of 160 coupons. However, problems during routing removal of the coupons from the panel resulted in 91 coupons being acceptable for testing.

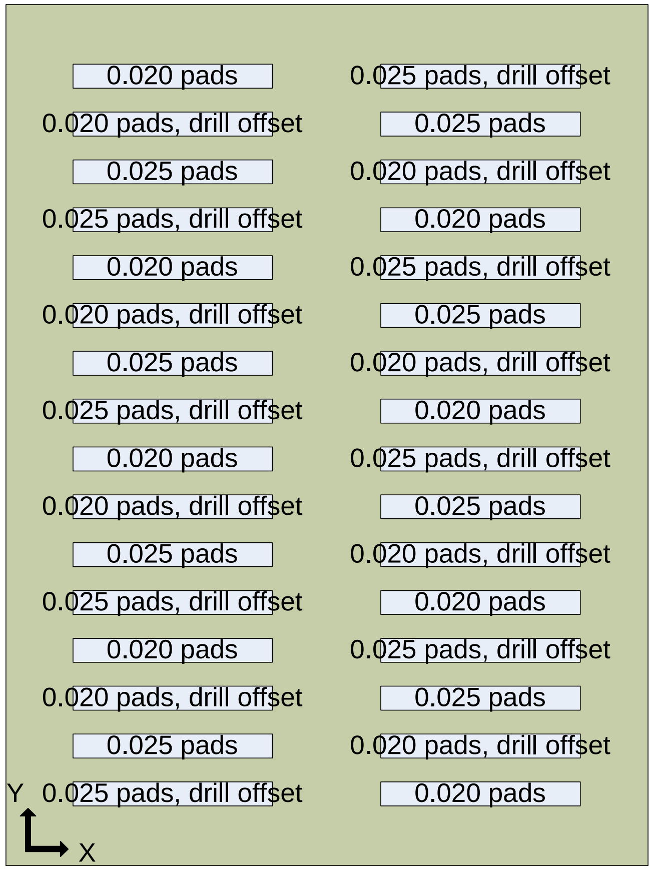


Figure 2 – IST Coupon Arrangement in Panel

Test Methodology

IST testing was used to generate cycles to failure (CTF) data that could be analyzed and compared. The IST sequence and parameters were as follows:

- Electrical resistance pre-screening of all circuits on each coupon
- Pre-conditioning of each coupon for 3 cycles between room temperature and 230ºC (to simulate assembly and rework processes)
- Temperature range of room temperature to 150 ºC
- Ramp times of 3 minutes heating and 2 minutes cooling
- Failure criterion defined as 10% resistance increase in buried via circuit.
- Failure analysis using vertical microsectioning

Of the 91 coupons available for testing, 70 were submitted for IST to have similar numbers and panel locations of samples between the 0.020 and 0.025 pad groups, and to reduce costs.

Test Results

Electrical Resistance Pre-screening

Prior to beginning IST thermal cycling, the results of the electrical pre-screening were reviewed for consistency with previous values of similar coupons. The values were close to previous values, indicating no anomalies. They were also consistent from coupon to coupon, with the buried via circuit resistance having a mean of 640 milliohms and a standard deviation of 28.2, in line with previous coupon lots showing consistent plating.

IST Results

The results of interconnect stress testing (IST) are summarized in the two-parameter Weibull probability plots below. Two plots are shown:

- Comparison of 0.64 mm [0.025”] pads to 0.5 mm [0.020”] pads (Figure 3)
- Comparison of 0.64 mm [0.025”] pads and drill offset to 0.5 mm [0.020”] pads and drill offset (Figure 4)

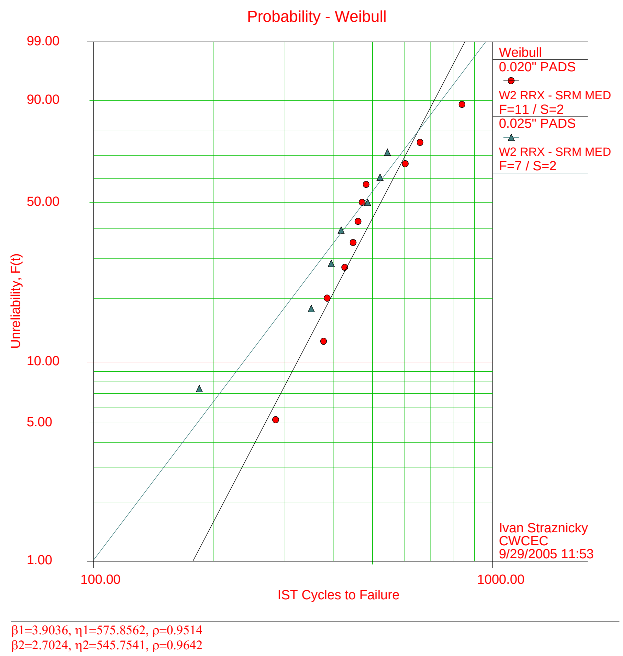


Figure 3 - Two parameter Weibull plot comparing 0.020 to 0.025 pads.

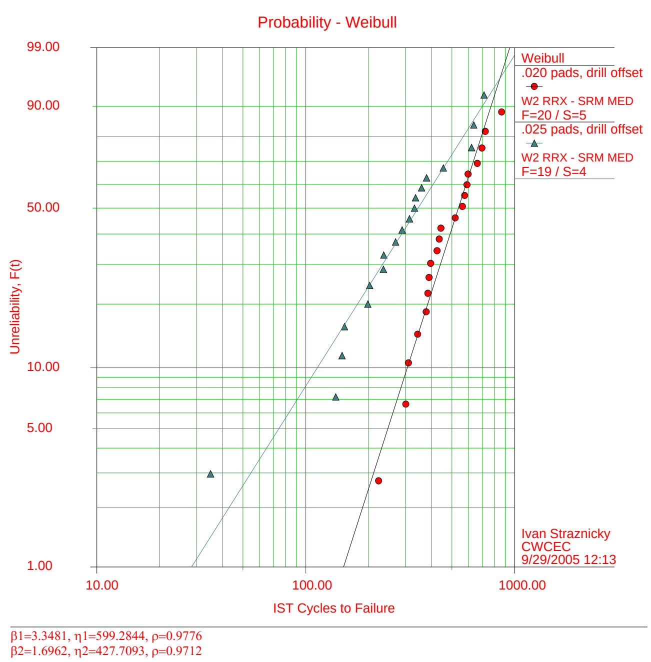


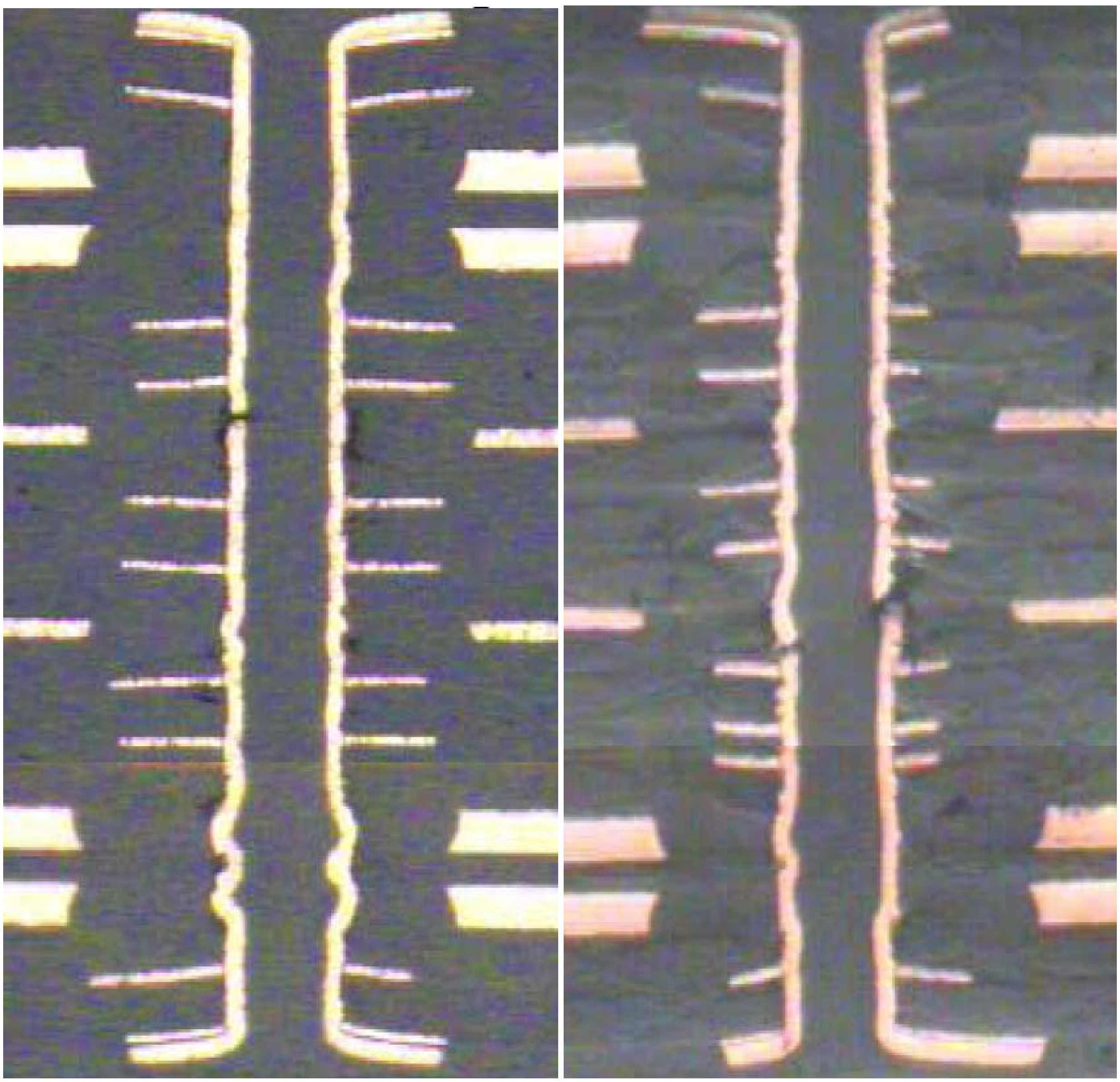
Figure 4 - Two parameter Weibull plot comparing 0.020 pad with drill offset to 0.025 pad with drill offset.

A comparison of the characteristic lives (point at which 63.2% of the test samples have failed), η1 and η2, in Figure 3 shows that the reliability of 0.25 mm [0.010”] drill diameter buried via holes in 0.5 mm [0.020”] pads is slightly better than in 0.64 mm [0.025”] pads, with the difference being rather small (576 CTF versus 546 CTF).

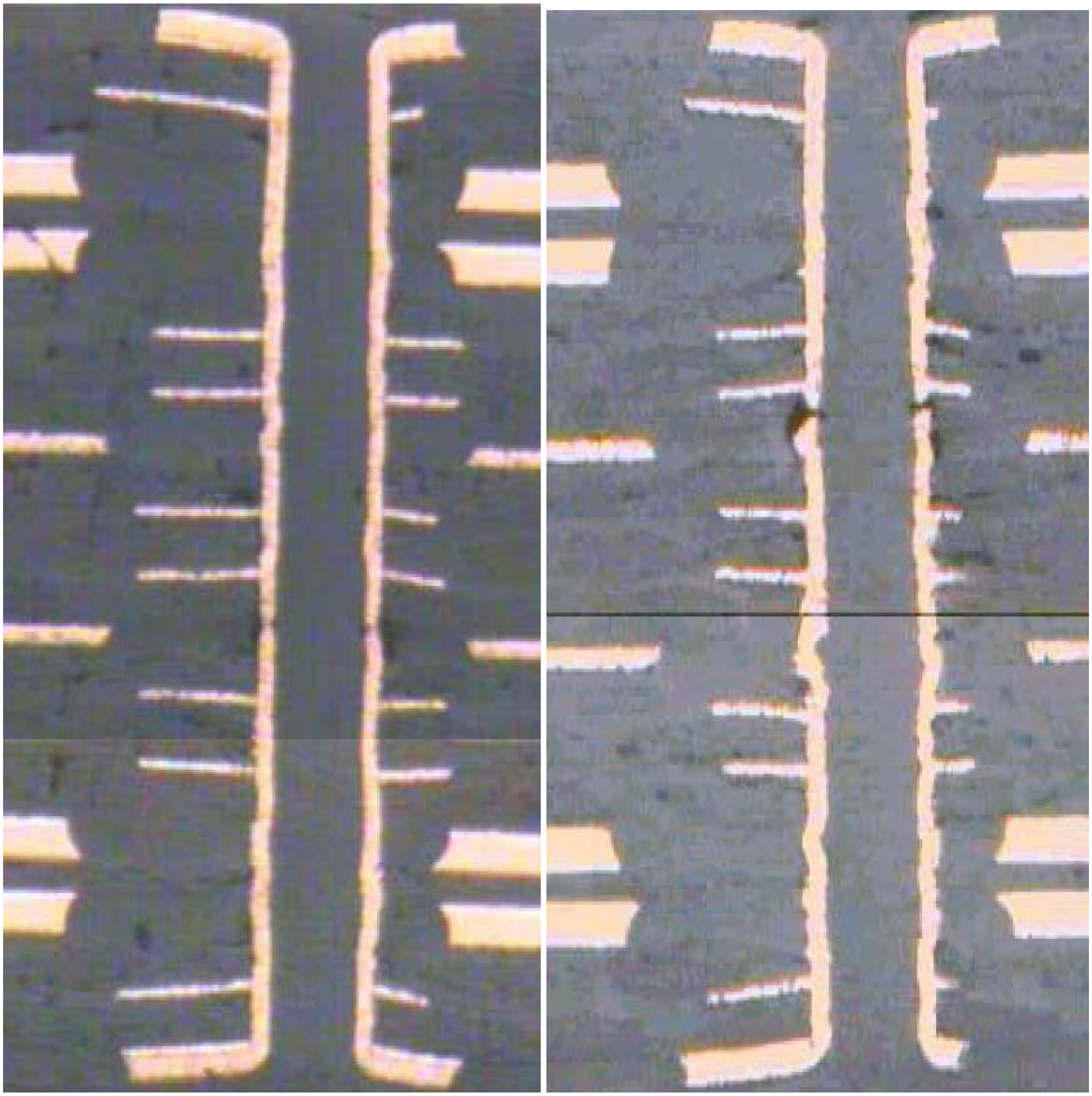
Figure 4 shows a larger difference between the characteristic lives, 599 cycles for 0.5 mm [0.020”] pads with drill offset compared to 428 cycles for 0.64 mm [0.025”] pads with drill offset. This was somewhat unexpected because it was thought that, with the 50 µm [0.002”] drill offset, break-out of the holes from the pads might occur on some of the 0.5 mm [0.020”] pad coupons, and that this would decrease reliability as implied by the IPC-6012 requirements (i.e. Class 3 better than Class 2). More investigation was required to attempt explanation of these results.

Failure Analysis – Vertical Microsectioning

As part of the IST methodology, vertical microsectioning was performed on several of the coupons that failed early in testing. Thermal imaging was used to isolate the failed interconnect(s) on each coupon. The sectioning attempts to show how the interconnect failed, e.g. barrel crack, barrel-to-pad separation, foil crack, etc. Figures 5 through 8 below show that the buried via hole failures were due to barrel cracks near the middle of the hole. This is a typical fatigue failure during thermal cycling caused by CTE (Coefficient of Thermal Expansion) mismatch between the copper barrel and the surrounding epoxy resin / glass laminate (in the axial direction).



Figures 5 & 6 - Vertical sections of failed buried vias from 0.025 pad coupon (upper) and 0.020 pad coupon (lower).



Figures 7 & 8 - Vertical sections of failed buried vias from coupon with 0.025 pads and drill offset (upper), and from coupon with 0.020 pads and drill offset (lower).

Copper thickness measurements along the barrels of all microsections confirmed that plating was consistent (as electrical prescreening results had indicated), with a minimum of 25 µm [0.001”] wall thickness.

Failure Analysis – Horizontal Microsectioning

Horizontal microsectioning was performed on fifteen of the tested coupons with drill offset to determine the amount of misregistration on the buried via holes. From the vertical sections above, it appeared that the middle layers with pads (i.e. 6, 7, 9, 10, 12, 13) had fairly consistent registration with respect to one another. Thus, layer 9 was chosen as the layer to investigate since it could represent 6 layers. Layers 2, 3, 16 and 17 appeared to be misregistered by 25-50 µm [0.001-0.002”] with respect to the middle layers and, in some cases, each other. Therefore, the measured registration between hole and pad on layer 9 would be a best case.

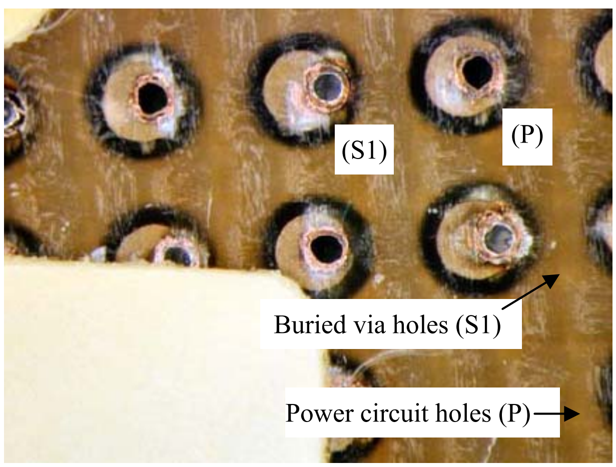
Table 1 - Horizontal microsectioning measurements for minimum annular ring at layer 9

0.020 pads with drill offset										
Coupon #	01-19	03-11	02-7	01-15	03-31	01-3	02-15	04-15	02-19	03-23
Min. annular ring (in.)	0.001	0.001	0.000	0.003	0.002	0.002	0.002	0.001	0.002	0.002
0.025 pads with drill offset										
Coupon #	02-21	01-25	05-1	05-5	05-13					
Min. annular ring (in.)	0.004	0.004	0.005	0.005	0.005					

Table 1 above shows that tangency was measured on layer 9 of only one coupon out of 10 for the case of 0.020 pad with drill offset. However, as noted above, layers 2, 3, 16 and 17 were misregistered with respect to layer 9. Thus, tangency or breakout very likely occurred at some of these layers when a minimum annular ring of 25-50 µm [0.001-0.002”] was measured at layer 9.

For the case of 0.025 pads with drill offset, five coupons were measured. As expected, each coupon had ample annular ring at layer 9, and a minimum of 50 µm [0.002”] was very likely at layers 2, 3, 16 and 17.

The photos below show some of the results from horizontal microsectioning.



(S1)

(P)

Figure 9 - Horizontal microsectioning photos of 0.020 pads with drill offset (layer 9), showing drilled hole to pad tangency on buried via. Note that holes with breakout are not buried vias, but power circuit through holes (P).

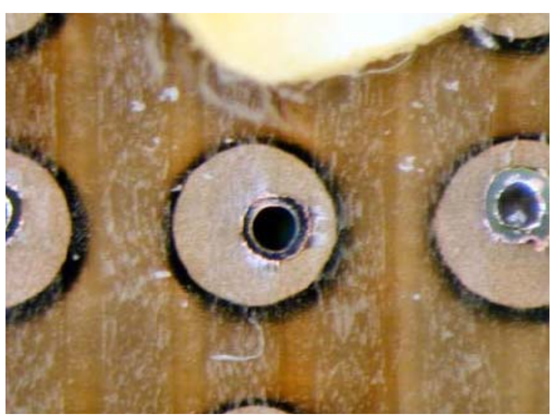


Figure 10 - Horizontal microsectioning photo of 0.025 pads with drill offset (layer 9), showing approx. 0.1 mm [0.004”] annular ring.

Discussion

The reason for the lower reliability of the 0.025 pad coupons, particularly with drill offset, was not immediately apparent. However, a review of published literature on the topic of plated through hole reliability yielded a logical explanation. One paper was particularly helpful[3]. It shows that, for the same drilled hole size, an increase in pad diameter results in a marked increase in total strain range (TSR). TSR is related to reliability through the Engelmaier model[4]:

$$N_f^{-0.6} D_f^{0.75} + 0.9 \frac{S_u}{E} \left[\frac{e^{D_f}}{0.36} \right]^{0.1785 \log\left[\frac{10^5}{N_f}\right]} = TSR \qquad (1)$$

where

N_f = Number of cycles to failure
D_f = Fatigue ductility coefficient (of electro-deposited copper)
S_u = Ultimate tensile strength (of electro-deposited copper)
E = Modulus of elasticity (of electro-deposited copper)

Equation (1) shows how increases in TSR decrease the number of cycles to failure (CTFs), i.e. reliability. Larger pad diameters increase the TSR "due to the increased loading afforded by the larger pad diameter"[3]. In other words, as the FR-4 laminate and epoxy resin surrounding the copper barrel expand and contract more than the barrel itself in the axial direction, the annular rings of the pads experience forces and moments that increase the strains on the barrel. Larger annular rings from larger pads offer more area further away from the hole axis and thus serve to increase these forces, moments, and strains, thereby resulting in lower reliability.

The above explanation matched what was seen in the test results of Figure 3, i.e. lower cycles to failure for the larger pad diameter. The larger difference between the CTFs of the drill offset cases (Figure 4) was hypothesized to be due to higher TSR from the combination of larger annular rings and their presence all around the hole (0.025 pad), compared with smaller annular rings and likely absences at portions of the hole due to tangency or breakout (0.020 pad). The partial pad absences may also help to explain the increase in reliability of the offset 0.020 pad case compared to the non-offset 0.020 pad case. Three-dimensional finite element analysis is planned to verify these hypotheses.

Conclusions and Recommendations

For the PCB test vehicle shown, the reliability of 0.25 mm [0.010"] drilled diameter buried via holes is better with 0.5 mm [0.020"] pads than with 0.64 mm [0.025"] pads, even with tangency/breakout occurring between the hole and 0.5 mm [0.020"] pad. This is in disagreement with IPC-6012, which implies that complete annular rings (Class 3) are more reliable than partial annular rings (Class 2). More testing and analysis should be performed to determine the reliability of other combinations of design, material and fabrication parameters that lead to sub-Class 3 annular rings, and compare these to cases with Class 3 annular ring.

References

1 Read, David, et al., "PWB Hole-to-Land Misregistration: Causes and Reliability", ITRI Project Final Report 97061201-G, June 12, 1997.

2 Jones, Ted, et al., "Reliability of Misregistered and Landless Innerlayer Interconnects in Thick Panels", ITRI Report 98103001-G, October 30, 1998.

3 Iannuzzelli, Ray, "Predicting Plated-Through-Hole Reliability in High Temperature Manufacturing Processes", Proceedings of 1991 Electronic Components and Technology Conference.

4 Engelmaier, Werner, "Interconnection Failures and Design Reliability for Plated-Through Holes/Vias (PTHs/PTVs)", Professional Development Course, IPC Printed Circuits EXPO/APEX Conference 2004.

INNOVATION IN MOTION

Reliability of Misregistered HDI Plated Through Holes

2007 IPC Printed Circuits Expo

Ivan Straznicky, P.Eng.
Curtiss-Wright Controls Embedded Computing
333 Palladium Dr., Ottawa, Ontario, Canada
613-599-9199 (Phone), 613-599-7777 (Fax)
ivan.straznicky@curtisswright.com

CURTISS WRIGHT Controls, Inc. Embedded Computing

Outline

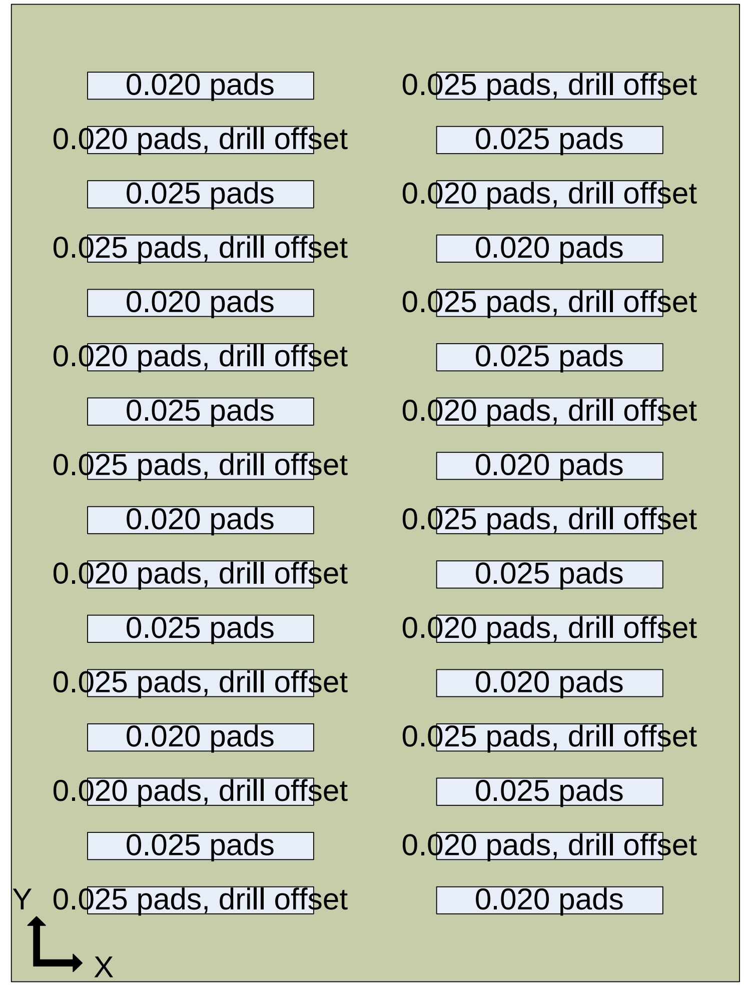
- Motivation
- Test Vehicle
- Test Methodology
- Results – Pre-screening, IST
- Failure Analysis - Microsectioning
- Discussion
- Conclusions and Recommendations

Motivation

- New, high density PWB design for rugged single board computer
- 18 layers, 2 mm [0.08”] max. thickness
- Blind microvias (1-2, 18-17), buried vias (2-17), some through vias (1-18)
- In order to squeeze the required interconnects into the available PWB volume, 0.25 mm [0.01”] dia. holes with 0.5 mm [0.02”] pads were considered for all buried vias.
- BUT, still needed to maintain high reliability.
- 0.25/0.5 mm holes/pads would not meet IPC-6012, class 3 annular ring, BUT were they reliable “enough”?

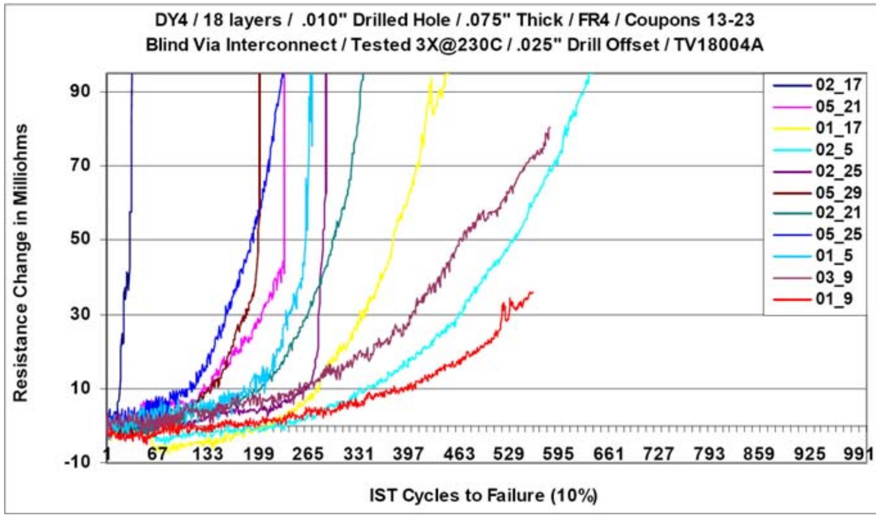
Test Vehicle

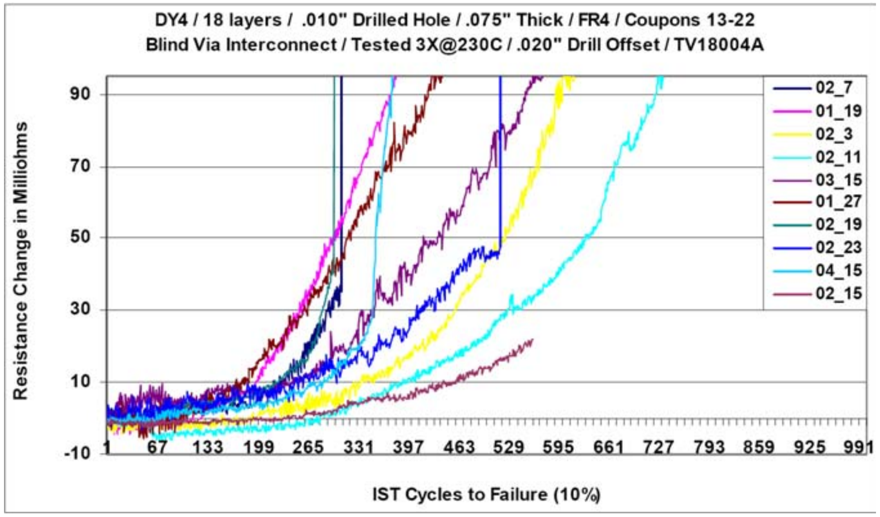
- Interconnect Stress Test (IST) coupons with same features as PWB design, e.g. 0.25/0.5 mm holes/pads
- To compare reliability, include coupons with 0.25/0.64 [0.01/0.025”] holes/pads
- To promote class 2 breakout, include coupons with 50 µm [0.002”] drill offset (+X direction)
- Arrange above coupons in panel to minimize possible location effects on results.



Test Methodology

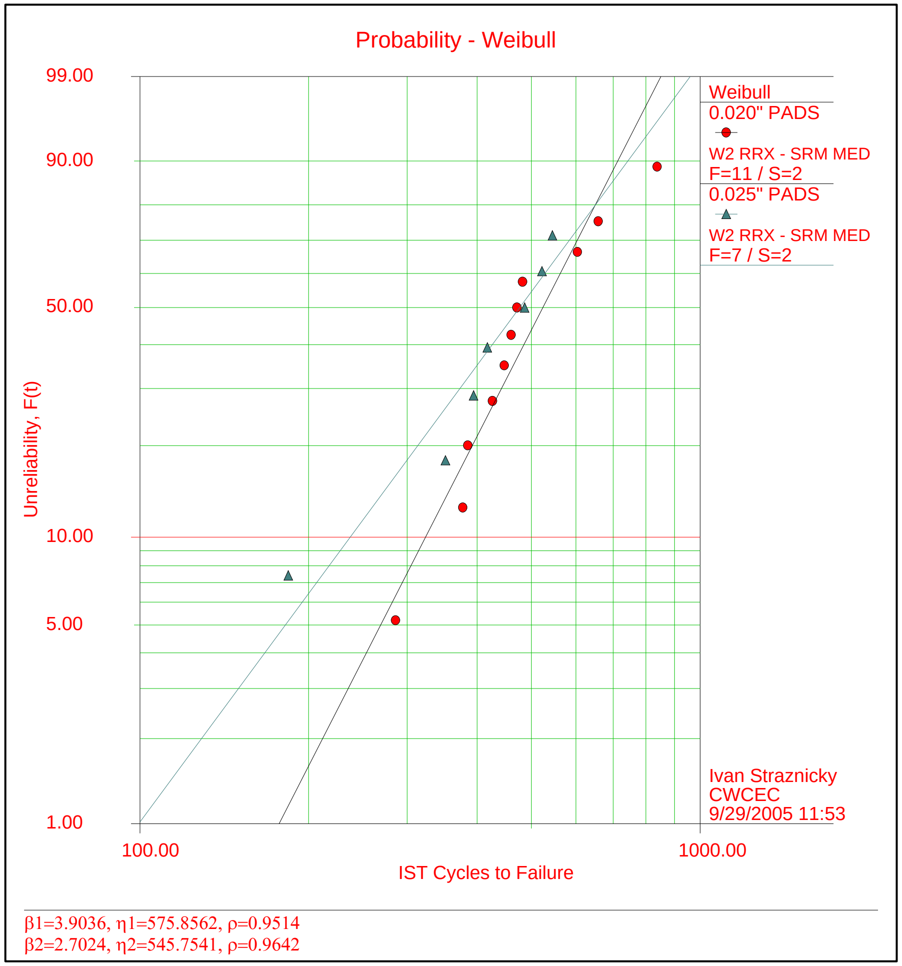
- Electrical resistance pre-screening
- Coupon pre-conditioning to represent assembly and rework
- Temperature cycling of RT-150°C
- Failure = 10% resistance increase in buried via circuit
- Failure analysis
- Compare reliability

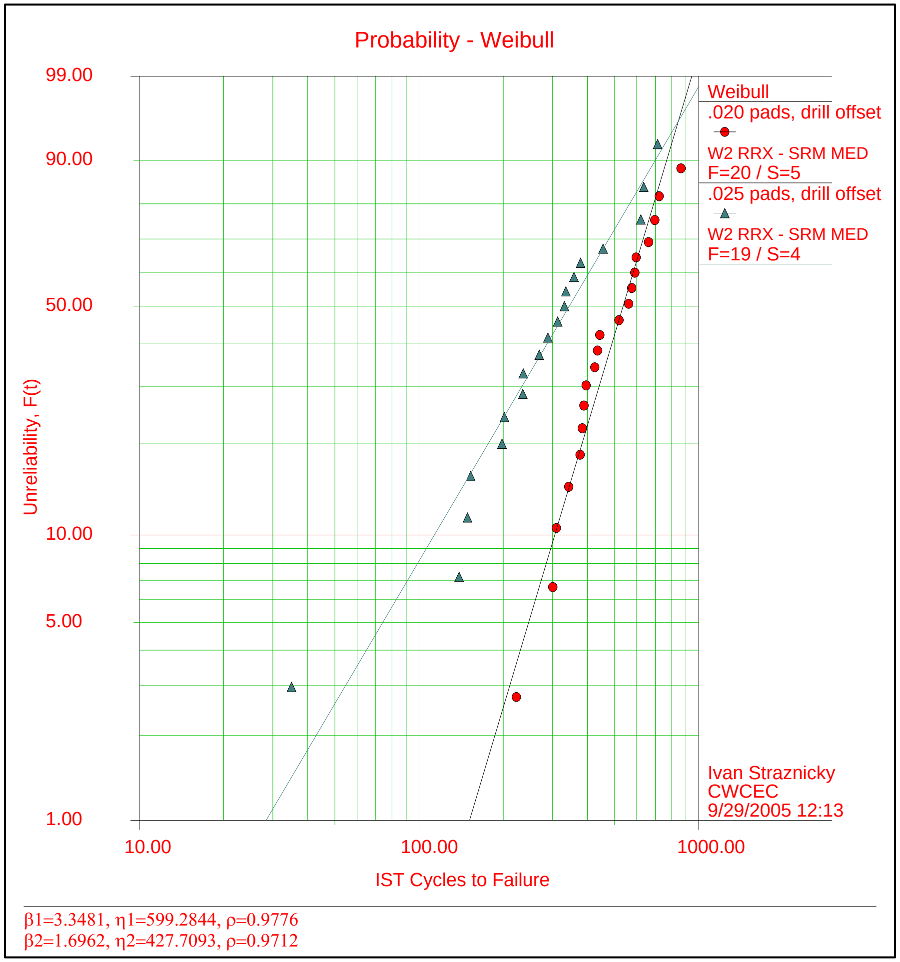




Test Results

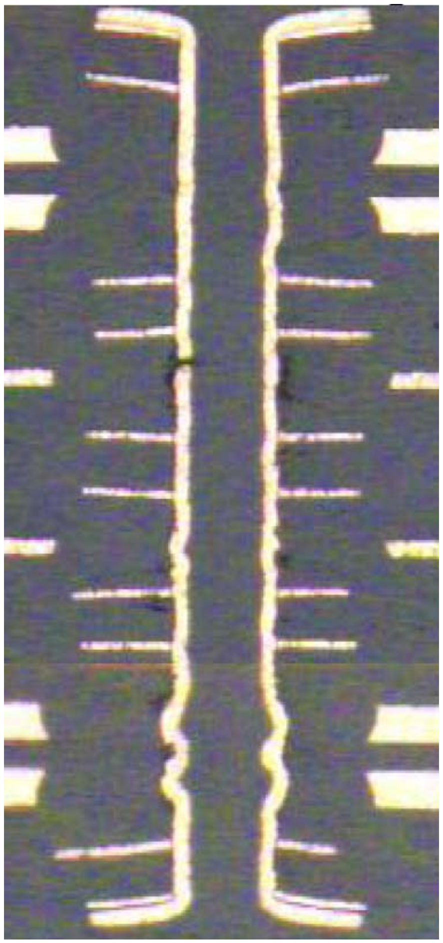
- Electrical resistance pre-screening – consistent values and comparable to previous “good” results
- Weibull plots of temperature cycling data – UNEXPECTED RESULTS !



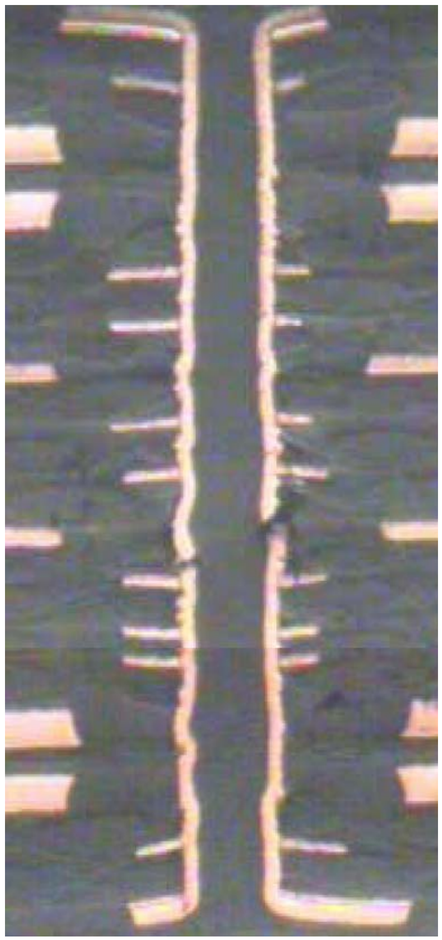


Failure Analysis

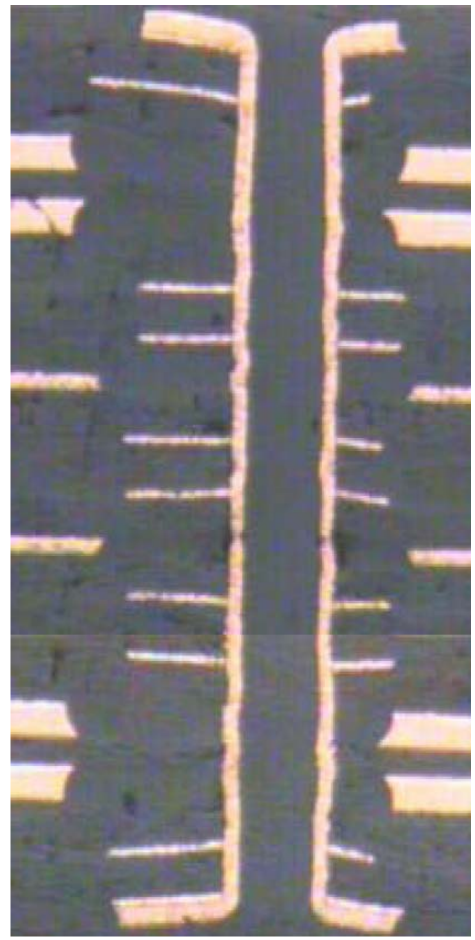
- Vertical microsectioning showed failure mode (barrel cracks), and good quality plating



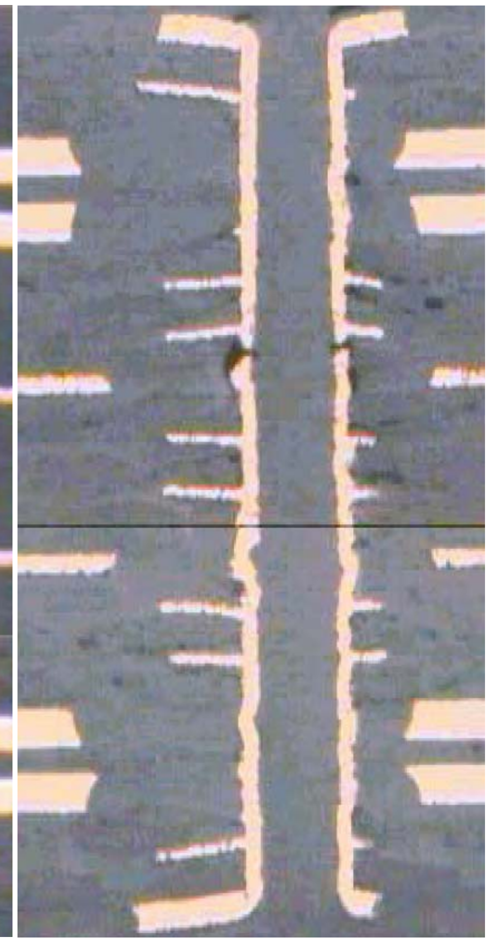
0.025 pads



0.020 pads



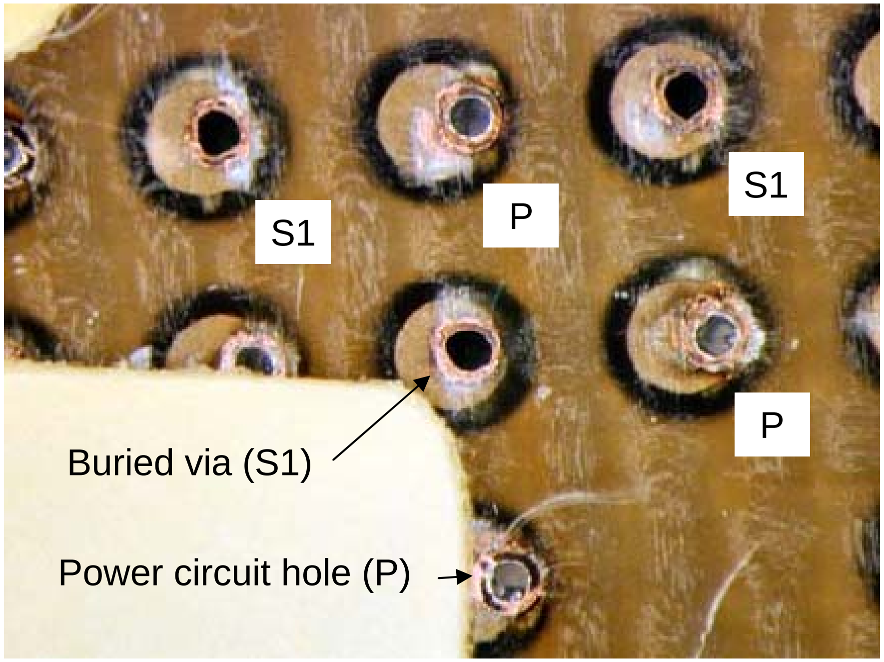
0.025 pads with offset



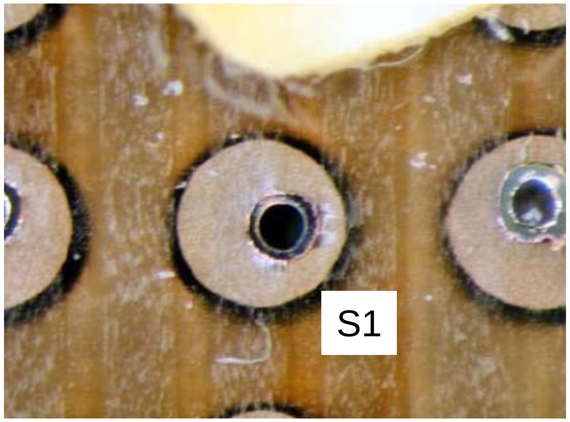
0.020 pads with offset

Failure Analysis (cont'd.)

- Horizontal microsectioning showed "tangency" on layer 9 for 0.020 pads with drill offset.
- Vertical sections showed misregistration between layer 9 and layers 2, 3, 16, 17, leading to conclusion that breakout was present on these layers.



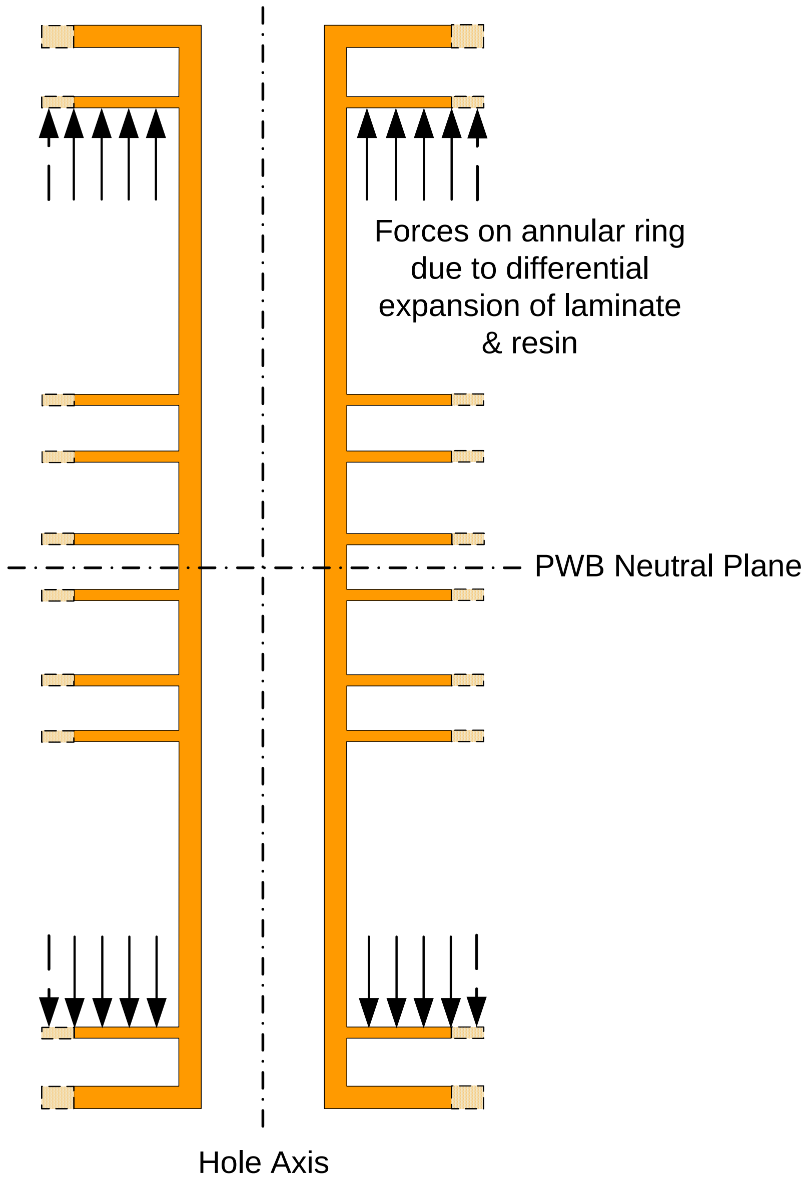
0.020 pads with offset (layer 9)



0.025 pads with offset (layer 9)

Discussion

- Why did 0.020 pads have better reliability than 0.025 pads? Simple mechanics.
- Reliability decreases as strain increases.
- Strain on barrel increases with larger loading area of larger pads.
- Previous FEAs confirmed this effect for perfectly registered holes (ref. Iannuzzelli, 1991 ECTC)
- FEA underway to analyze additional impact of misregistration



Conclusions and Recommendations

- Testing has shown that 0.25 mm [0.01”] diameter buried via holes have better reliability with 0.5 mm [0.02”] pads than 0.64 mm [0.025”] pads, even with misregistration causing tangency and breakout.
- Disagreement between these results and IPC-6012 annular ring requirements for high reliability product (class 3).
- More testing and FEA required to determine if these results are repeated for other combinations of design and fabrication parameters that lead to sub-class 3 annular ring.