Large and Thick Board Lead-Free Wave Soldering Optimization

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Abstract
This paper presents the results of our study on the development and optimization of lead-free wave soldering process for large and thick printed circuit boards (PCB), through multiple designs of experiments (DOEs) including many variables from design, material, component and process. Design variables were pin-to-hole ratio, pad diameter, annular ring diameter, component orientation, spacing, thermal relief pattern, internal copper thickness, and the number of copper layers connected to PTH barrel. Material and process variables included flux materials, flux amount, preheat temperature, solder pot temperature, conveyor speed, contact time, wave atmosphere and wave system. A variety of plated through hole (PTH) components were tested. Two board thicknesses (2.4mm and 5.0mm) and two board surface finishes (immersion silver and immersion gold) were used. The results showed that there were strong correlations between flux materials, process conditions and hole-fill. Bridging and insufficient solder defects were reduced by optimizing wave process parameters. Design parameter optimization could be used to improve the PTH hole-fill, and reduce defects of PTH bridging, insufficient solder on SMT components, and voiding in the PTH solder joint.

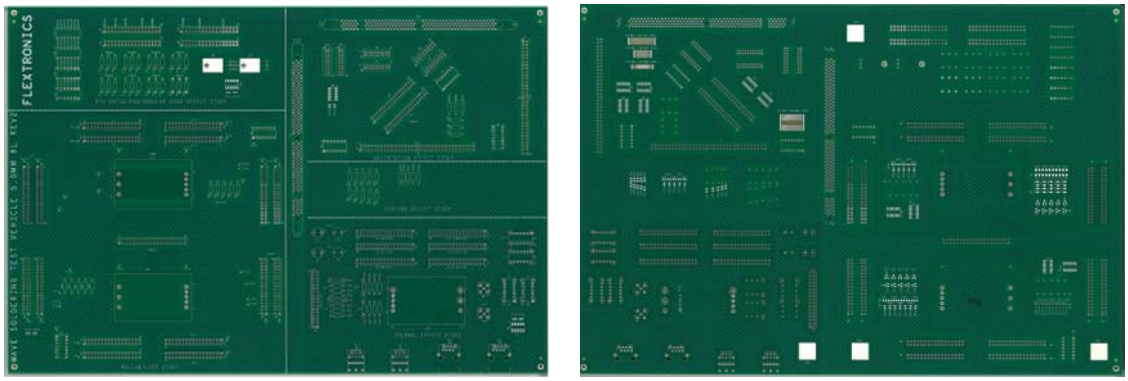
Introduction
Achieving acceptable wave solder through hole-fill on large and thick printed circuit boards (PCB) is a process challenge, even with tin-lead solder technology. The challenge is even greater with lead-free wave soldering due to the surface tension of lead-free solder alloys, currently available flux materials, components and process limitation, etc.

This paper presents our study on the process development and optimization of lead-free wave soldering for large and thick PCBs. Process and design variables will be discussed that help to improve solder joint quality and reliability.

Test Vehicle and Components
A specially designed 406mm x 305mm test vehicle was used for the lead-free wave soldering process development. Two board thicknesses (2.4mm and 5.0 mm) and two board surface finishes (immersion silver and immersion gold) were considered. The test vehicle has up to 14 layers with a maximum of 12 copper ground planes. It was designed into different areas for the study of the effects of pin-to-hole (P/H) ratio, pad/annular ring, spacing, orientation, and thermal relief, on hole-fill. In the P/H ratio area, five different P/H ratios (associated with five different hole sizes), ranging from 0.3 to 0.6, were designed for three different pin types: round, square and rectangular. Five different pad diameters and three different annular rings were included in the study. For the thermal relief study, we considered different thermal relief patterns, PTH components, the number of layers connected to the pin, as well as different copper thicknesses for the ground plane. Table 1 provides the design variables that were embedded into the test vehicle, and Figure 1 shows the images of the large board wave soldering test vehicle.

Table 1 - Design Variables of the wave test vehicle

Factors	# Levels	Levels
PCB Surface Finish	2	Immersion Ag, ENIG
PCB Thickness	2	2.4mm, 5.0mm
Pin to Hole Area Ratio	5	-2, -1, 0 (current design), +1, +2
Pad Diameter	3	-1, 0 (current design), +1
Annular Ring	3	-1, 0 (current design), +1
Component orientation	3	0, 45, 90 degree
# of layers connected to pin	3	-1, 0,+1
Copper thickness	3	0.5oz, 1.0oz, 2.0 oz
SMD to PTH spacing	5	5 different spacings
SMD to SMD spacing	5	5 different spacings



a) Topside b) Bottom side

Figure 1 - Lead Free Wave Soldering Test Vehicle.

A variety of through-hole components and selected surface mount components were tested. Some representative PTH components were headers, DIPs, aluminum capacitors, axial resistors, audio jack connector, BNC connectors, RJ45 connectors, DC-DC components, etc. A full list of the components is given in Table 2.

Table 2 - List of Components

Components	Qty/PCB	Component Type
Headers, 2x17pin, 100 mil pitch	40	PTH
Headers, 2x10pin, 50 mil pitch	6	PTH
DIP14,	14	PTH
Audio Jack	2	PTH
DIMM Connector	2	PTH
DC-DC Component	3	PTH
Axial Resistor	86	PTH
Radial Resistor	3	PTH
RJ45 Connector	2	PTH
BNC connector	2	PTH
Al Cap	4	PTH
Resistor 0402	20	SMT
Resistor 0603	40	SMT
Resistor 0805	40	SMT
Resistor 1206	20	SMT
SOT23	20	SMT
SO16	10	SMT

Process Experimental Details

Two major process DOEs were performed to optimize the wave soldering process using 5mm thick, immersion silver test vehicles. The verification runs were done on different board thicknesses (2.4mm and 5.0mm) and board surface finishes (immersion silver and immersion gold). Half fractional factorial design was used in the experiments. DOE 1 considered 4 factors: flux type, flux amount, preheat temperature and contact time. In DOE 2, pot temperature, conveyor speed, # of wave nozzles (chip wave on/off) and wave atmosphere were tested. The DOE1 and DOE 2 matrix are shown in Table 3 and 4, respectfully. Two replicates were run for each DOE and verification runs.

Table 3 - DOE 1 Matrix

FLux Type	Flux Amount	Preheat Temperature	Contact Time
Flux 1	Low	Low	Low
Flux 1	Low	Low	High
Flux 1	Low	High	Low
Flux 1	Low	High	High
Flux 1	High	Low	Low
Flux 1	High	Low	High
Flux 1	High	High	Low
Flux 1	High	High	High
Flux 2	Low	Low	Low
Flux 2	Low	Low	High
Flux 2	Low	High	Low
Flux 2	Low	High	High
Flux 2	High	Low	Low
Flux 2	High	Low	High
Flux 2	High	High	Low
Flux 2	High	High	High

Table 4 - DOE 2 Matrix

Pot Temperature	Conveyor Speed	Wave Nozzle	Wave Atmosphere
Low	Low	Chip wave on	Air
Low	Low	Chip wave on	Nitrogen
Low	Low	Chip wave off	Air
Low	Low	Chip wave off	Nitrogen
Low	High	Chip wave on	Air
Low	High	Chip wave on	Nitrogen
Low	High	Chip wave off	Air
Low	High	Chip wave off	Nitrogen
High	Low	Chip wave on	Air
High	Low	Chip wave on	Nitrogen
High	Low	Chip wave off	Air
High	Low	Chip wave off	Nitrogen
High	High	Chip wave on	Air
High	High	Chip wave on	Nitrogen
High	High	Chip wave off	Air
High	High	Chip wave off	Nitrogen

Results and Discussions

Hole-Fill

The main effect plots for hole-fill from DOE 1 and DOE 2 are shown in Figure 2 and 3, respectfully. As can be seen, the most important process factors that affected hole-fill are flux type, preheat temperature, contact time, solder pot temperature, wave configuration and wave atmosphere. Among these factors, contact time and solder pot temperature were the two most significant factors that influenced hole-fill. Longer contact time and higher solder pot temperature resulted in greater hole-fill. Choosing the right flux material is also important to achieve a good hole-fill. As shown in Figure 1, the PTH hole-fill was

significantly increased by using Flux B material. Turing on the chip-wave and using the nitrogen also helped to achieve better hole-fill.

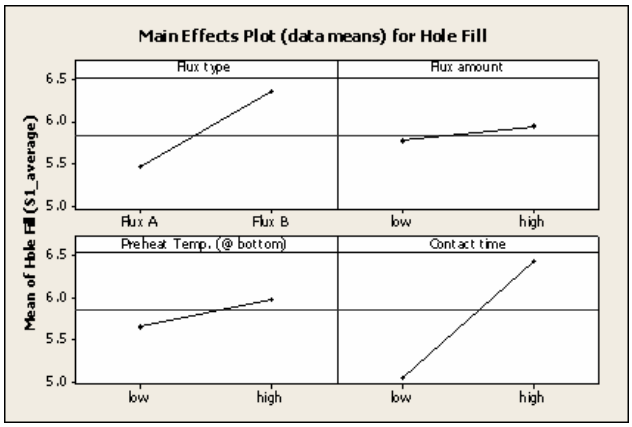


Figure 2 - Main Effect Plot for Hole-Fill from DOE 1.

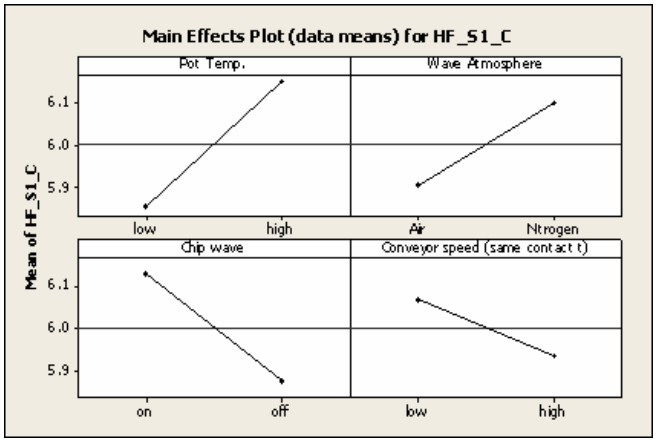
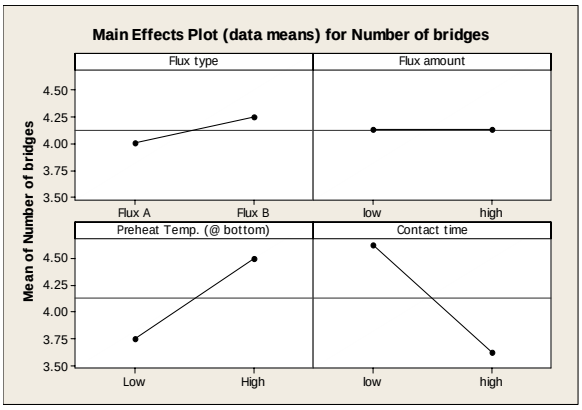


Figure 3 - Main Effect Plot for Hole-Fill from DOE 2.

Bridging

The results showed that flux type, flux amount, preheat temperature and contact time did not significantly affect the number of bridges on the PTH components (Figure 4). However, pot temperature, conveyor speed and chip-wave on/off had a major impact on the through-hole solder bridging (Figure 5). The number of solder bridges was dramatically decreased when the chip wave was turned off. Lower pot temperature or faster conveyor speed also helped to reduce the number of bridges.

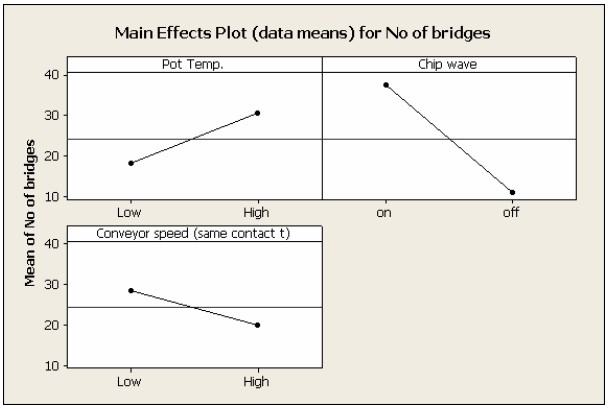
Besides process parameters and component pitch, design also played a large role in PTH bridging. The orientation of the component through the wave solder also affected bridging. It became more critical when the component pitch was small (2.0mm pitch) or when a long component such as a header or DIMM connector was wave soldered. More bridged pins were seen at the components in which their long body was sent in parallel to the wave than if it is perpendicular to the wave (Figure 6). This is consistent with our previous study[1], as well as experience with tin-lead wave soldering.



Estimated Effects and Coefficients for Number of bridges (coded units)

Term	Effect	Coef	SE Coef	T	P
Constant		4.1250	0.6124	6.74	0.000
Flux type	0.2500	0.1250	0.6124	0.20	0.843
Flux amount	0.0000	0.0000	0.6124	0.00	1.000
Preheat Temp. (@ bottom)	0.7500	0.3750	0.6124	0.61	0.557
Contact time	-1.0000	-0.5000	0.6124	-0.82	0.438

Figure 4 - Main Effect Plot of process vs. bridging from DOE 1



Estimated Effects and Coefficients for No of bridges

Term	Effect	Coef	SE Coef	T	P
Constant	24.31	1.840	13.21	0.000	
Pot Temp.	12.37	6.19	1.840	3.36	0.010
Chip wave	-26.63	-13.31	1.840	-7.23	0.000
Conveyor speed (same contact tine)	-8.63	-4.31	1.840	-2.34	0.047

Figure 5 - Main Effects Plot for Bridging from DOE 2.

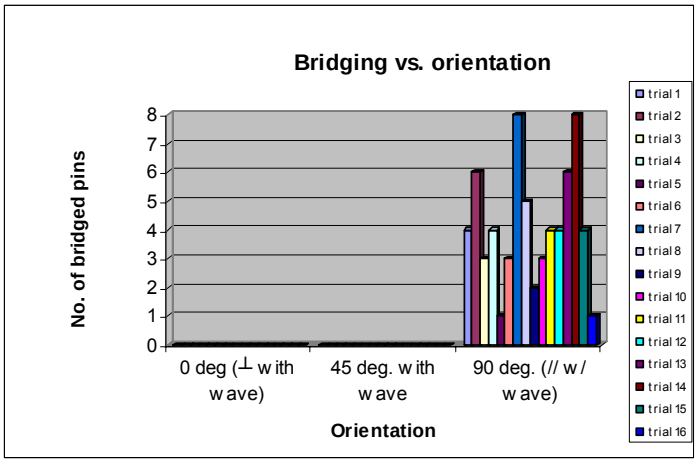


Figure 6 - Bridging vs. Component Orientation Through Wave

Insufficient Solder on SMT Components

The wave soldered SMT components were analyzed for the insufficient solder defect. Contact time and chip wave were the important factors that significantly affected the insufficient solder defect. The results showed that turning on the chip wave was the most significant factor that reduced the defects of bottom SMT insufficient solder (Figure 7), contrary to the bridging

analysis, in which the chip wave should be turned off in order to reduce the defects. Overall, whether the chip wave should be turned on or off should depend on the complexity of the products and the component mix.

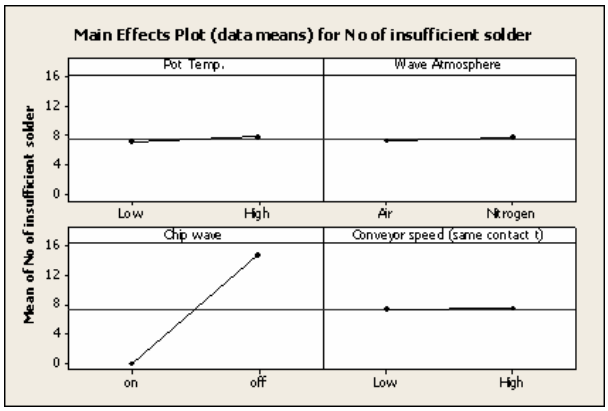


Figure 7 - Main Effects Plot for Bottom SMT Insufficient Solder from DOE 2.

Voiding

Lead-free wave soldering results in much more voids than tin-lead. The results from the DOEs revealed that voids could not be significantly improved by the process parameters. What can be done to reduce voiding in the PTH solder joint? We studied the impact of the pin-to-hole ratio and pin shape on voiding. The results showed that the P/H ratio significantly affected the voids in the PTH solder joints (Figure 8). The smaller the PTH ratio (or the larger the hole diameter), the less voiding was seen. Although more voids were seen on the components that had round pin shape as compared with square pins or rectangular pins (while the P/H ratio was the same), the effect of pin shape on voiding was not significant.

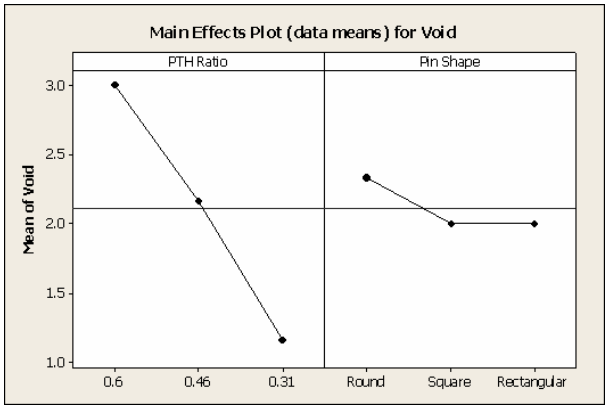
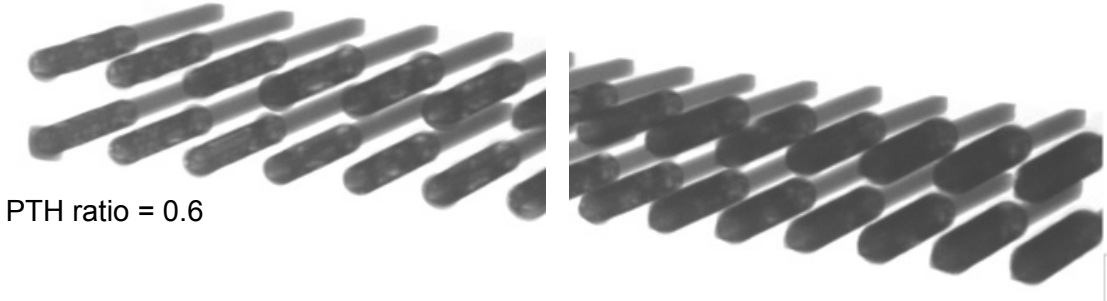


Figure 8 - The effect of PTH design on voiding. 1= little or no void; 2= some voids; 3 = very large voids or champagne voids.

Figure 9 shows the images of PTH solder joints in different hole sizes. From the left to the right, the P/H ratios are 0.59, 0.53, 0.46, 0.36 and 0.30 respectively. As can be seen from the picture, the P/H ratio of 0.59 had a lot of voids, whereas almost no void was seen on the solder joints with P/H ratio of 0.3.



Conclusions

A thorough study on the PCB design, materials, components and process parameters has been undertaken in order to optimize the lead-free wave soldering process for large, thick and heavy PCBs with thermal challenge. The results showed that the PTH hole-fill can be significantly improved by optimizing process parameters and design. The contact time and solder pot temperature are the key process factors influencing hole-fill. The occurrence of bridging is a function of component pitch, but bridging can also be reduced and even eliminated when proper process parameters and component orientation are chosen. When SMT components are wave soldered, turning on the chip-wave will help to reduce the insufficient solder defect. Voiding can be reduced through PCB design, and a pin-to-hole ratio of 0.3-0.4 is recommended to reduce voids in the PTH lead-free solder joints.

References

1. M. Arra, D. Shangguan, S. Yi, R. Thalhammer and H. Fockenberger, “Development of Lead-Free Wave Soldering Process,” IEEE Transactions on Electronics Packaging Manufacturing, Vol. 25, No. 4, Oct 2002.
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3. J. H. Vincent and G. Humpston, “Lead-free solders for electronic assembly,” *GEC J. Res.*, vol. 11, no. 2, pp. 76–89, 1994.