The Evolution of 3D IC Packaging for Portable and Hand Held Electronics

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Abstract
Increased electronic functionality can be achieved through the development of more complex silicon integration but that course generally requires a great deal of capital resources and an excessive amount of time. Hand-held communication and entertainment products necessitate a very short development cycle. And, with each generation offering more and more features and/or capability, rapid deployment of system level integration and miniaturization becomes a priority. In addition, the end user is expecting that each generation of product to be smaller and lighter that its predecessor. Companies are finding that for these rapidly evolving products, the multiple-die package concepts are proving superior to the system-on-chip alternative because it minimizes financial risk and has the potential for economically integrating several different but complementary functions. The paper developed for the IPC APEX program presents a view of current expectations for multiple-die BGA and CSP technology for wireless applications and review the evolution taking place in developing system-in-package capability.

Introduction
The revolution in performance driven electronic systems continues to challenge the IC packaging industry. And to achieve these goals, developers are relying more and more on innovative assembly techniques and process refinement to lower the cost of IC package assembly. To enable the IC to reach its performance potential and to facilitate the electrical and mechanical interface to the circuit board, many IC suppliers have abandoned lead-frame packaging and adapted a land or ball grid array interface format. This allows the developer to move all of the contacts under the package outline, providing a shorter package-to-board interface. Many of the fine-pitch ball grid array (FBGA) devices are only slightly larger than the die itself.

The demand for higher density IC packaging continues to dominate the development activity for both portable hand-held electronics as well as some products that are well outside the realm of portability. Many of these products must furnish complex graphic capability or manage and store large amounts of data. Because of the market demands for increased functionality in the IC packages supplied to OEMs, IC package assembly specialists are offering a number of multiple die configurations. Although many of these companies have resorted to die-stacking as an interim solution, many have found that without implementing more innovative package methods, the multiple-die and multiple-function or system-in-package offerings may never reach assembly process yield expectation or achieve manufacturing cost objectives. Many supplier companies are already converting to a 3D package format that allows the vertical joining (package-on-package) of individually packaged units. The examples shown in Figure 1 represent a sampling of alternative multiple die and package-on-package solutions developed for number of Tessera's licensee companies.

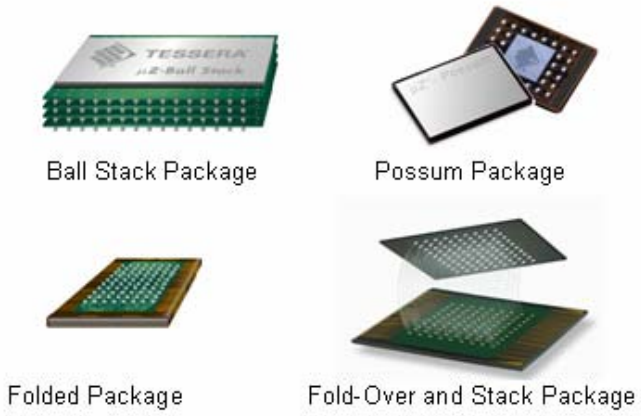


Figure 1. 3D multiple die and package-on-packaging variations

Market Drivers for High Density Memory

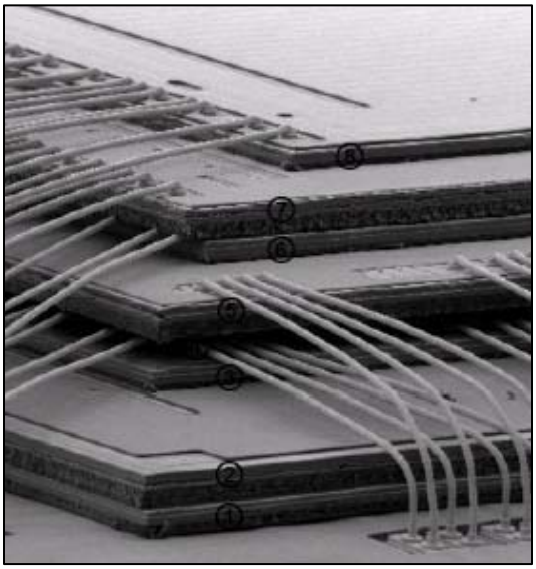
Two market trends that have been evident for some time are the need for increasing microprocessor speeds and the increasing demand for additional functionality in electronic systems. These market trends in turn are driving the demand for increased density of higher performance memory in systems such as high-end computers and servers (see Table 1). To address these requirements, memory module manufacturers, in particular, are looking to technologies capable of meeting these dual demands and at the same time, strive to keep overall packaging costs trending downward.

Table 1: Stacked Memory Market

Worldwide Stacked-Memory MCP Unit Forecast by Package Type (Millions of Units)											
	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
FBGA	61	66	97	204	397	541	607	662	709	808	818
TSOP	24	23	39	31	52	50	49	41	38	31	29
PBGA	1	8	14	11	9	7	6	2	1	1	1
Others	0	0	3	2	1	0	0	0	0	0	0
Total	**86**	**98**	**153**	**248**	**459**	**598**	**662**	**705**	**748**	**840**	**848**

Source: DataQuest

The most successful stacked die applications have been for stacking memory die, a relatively high-yield product. Companies have found that combining (stacking) already proven die within a single package structure a practical and economical solution. The die-stack package assembly process simply mounts one die on top of the other. The die sets are interconnected to a substrate interposer using conventional wire-bond technology. The die-stack configuration shown in Figure 2 is an example of what is currently being supplied for a custom application in the wireless phone market.



Source: Samsung

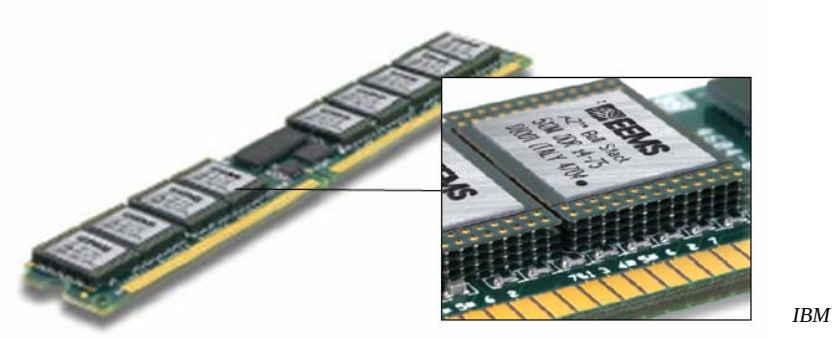
Figure 2. A custom eight die (flip-chip and wire-bond) assembly developed for the 3G phone market

The eight die configuration above includes two 1Gb NAND Flash die, two 256Mb SDRAM, two 256Mb NOR Flash die, one 128Mb UtRAM and one 64UtRAM die. This is a very impressive application for die stacking and the company, as the supplier of most or all die in the package are meeting satisfactory yields of the finished package. However, due to the complexity of the substrate interposer, variation in wafer fabrication processes and differing yield potential of die level products procured from multiple sources, meeting overall package level cost goals may not always be attainable.

New generations of dynamic random access memory (DRAM) and Double Data Rate (DDR and DDR2) technologies with center located bond pads are contributing significantly toward increased system performance, but, single-die packages cannot keep up with the demands of high-end processor technologies. And, although die stacking may be a solution for some memory applications, die stacking of these center-bond configured memory die is not really practical.

Package-on-Package for High Performance Memory

The newer generations of high-performance DDR memory have a relatively wide supply base, however, the die are rarely common in size from one supplier to another, even when they have the same memory capacity. They do have some commonality in that they are generally rectangular in shape and the wire-bond pads (as noted above) are located in the center of the die rather than at the perimeter as is typical for most silicon product. The 4 Gb DIMM module shown in Figure 3 was developed for the blade server products and has eighteen 4-layer µZ® Ball Stack packages surface mounted on both sides of the module substrate.



IBM

Figure 3. SIMM memory module using µZ®-Ball Stack package technology

The contact pattern and ball diameter for the memory ball stack package were designed to meet the single package outline requirements defined in JEDEC Standard 95-1, Section 6 '*Fine-pitch, Rectangular Ball Grid Array Package (FRBGA)*. The center-bond configuration of the memory die has proved ideal for mounting the die face-down on the substrate, enabling the circuit routing from the memory die bond sites to the ball contact pattern to be as direct as possible and the location of the ball contacts outside of the die element allows one package to sequentially mount on the top of one another.

Ball Stack Package Assembly

The micro Z-Ball Stack package (Hereafter referred to as the stack package.) assembly process is based on the already proven and mature technology developed for the micro BGA packages. The polyimide film substrate is furnished in a strip array format of twenty to thirty die attachment sites. The strip format furnishes an efficient method for sequentially processing of several individual device units at a time. In the assembly process, the silicon die are first placed (face-down) onto an elastomer attachment site on the polyimide base material and, from the opposite side, electrically interconnected through the slot feature in the substrate using conventional wire-bond methodology (see Figure 4).

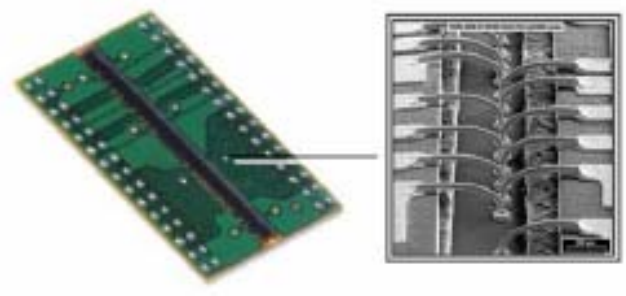


Figure 4. Center wire-bond detail of the memory.

The narrow rectangular slot opening in the substrate provides access for wire-bonding the memory die to the gold-plated land features on the substrates outer surface. The substrate design used for the test vehicle also allows for optional wire-bond configurations to selectively access individual memory die within the vertically stacked format After wire-bonding, the bond cavity is encapsulated to seal-off the exposed bond window followed by the ball attachment process. Following a mass ball

placement and reflow solder process the devices are singulated from the strip array format and electrically tested, graded and labeled, placed into standard partitioned carrier-trays and made ready for the next phase of the assembly.

Process for Package Stacking

In preparation for package stacking, the base or bottom packages are first transferred from their carrier-tray to a multiple unit alignment fixture. The actual stacking process begins with the transfer of the second layer package to a dip-fluxing station to uniformly coat the bottom half of the ball-contact. With flux applied, the upper level packages are sequentially placed atop the base packages and repeated for each package layer prior to reflow soldering as illustrated in Figure 5.

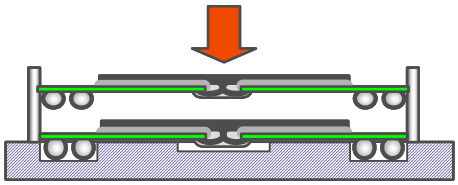


Figure 5. The stack package process enables the joining of two or more pretested devices within a single package outline.

The loaded fixture is then transferred to a forced air/gas convection oven for mass reflow to complete the interlayer solder joining of all package layers. Because of the relatively thin composite of elements within each section of the package, the overall height of the finished stack package is minimized (ultimately determined by the number of packages joined in the stack). Following a cleaning process and a final electrical continuity test of the multiple package assembly, the stack packages undergo a final physical inspection before transfer to partitioned trays for shipping to customer sites.

Possum Package-on-Package

The possum package process is a unique configuration made possible by joining two lead-bond µBGA packaged devices together. Rather than stacking a secondary µBGA device on the top surface of a primary base package, the secondary device is mounted to a land pattern provided on its bottom (or lower) surface, the same surface that contains the spherical alloy contacts for the eventual board or module interface. The advantage of this package-on package configuration is that (like the stack process described above) each IC package section becomes a fully tested subsystem that can be certified by the supplier before joining together (see Figure 6).

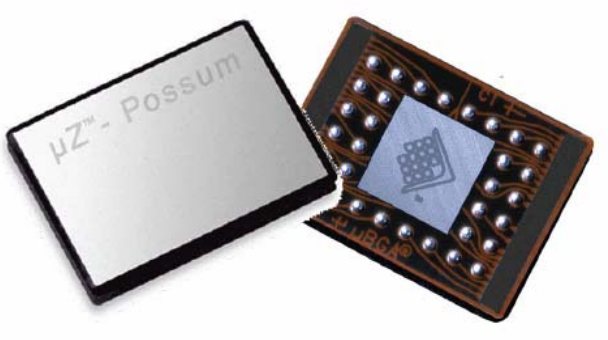


Figure 6. Two pretested BGA package units joined together to become a single package outline.

Each package section is die-size, adapting the classic micro BGA lead-bond and encapsulation process. The primary package is furnished with 300 to 350 micron diameter solder ball contacts to provide a standoff height adequate for attaching the secondary package on its lower surface. The secondary package is furnished with solder bumps rather than sphere contacts to maintain the lowest possible profile for bottom clearance (see Figure 7).

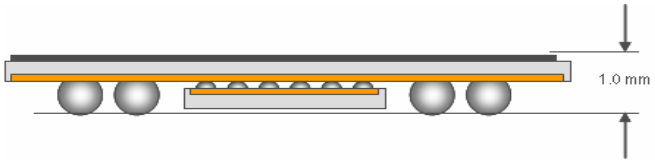


Figure 7. The possum two section IC package

With the primary and secondary packages pre-tested, the two sections are joined together using a reflow solder process typical of that described for the final ball stack assembly process.

3D Folded Package Methodology

Multiple die package applications requiring two, three or more die can be attached in series onto a foldable, multiple site flexible polyimide film substrate. The three die configuration shown in Figure 8, for example, was developed for Intel to accommodate two Flash memory die and one SRAM die.

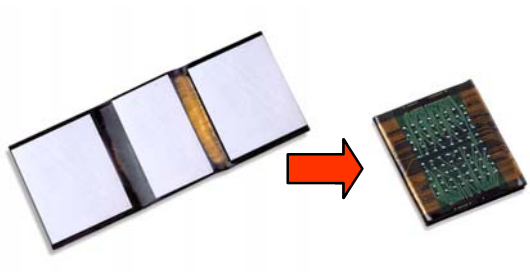
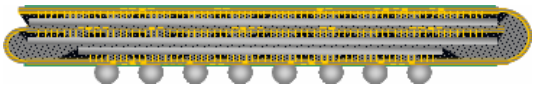


Figure 8. The three die µZ®-Folded package outline is only slightly larger than the largest die in the set.

The folded, multiple die package assembly process begins with die attach, the leads are terminated to the die pad and encapsulated. Using thinned die and the relatively low profile of the 'S' shaped lead-bond process allows the overall cross-section of the package to remain thin When folded, the tree die configuration requires no more area than a single die package. The folding and bonding process actually takes place while all of the die elements are retained in the multiple package strip format (typical of other micro BGA packaging processes). The primary difference is that the folding and boding process is performed before singulation. To retain the folded configuration, an adhesive film is applied to the top surfaces of the two outside die. The extended areas are then folded over and secured for curing to complete the bonding process. Following a cure cycle, the solder ball contacts are applied, the folded strip is cleaned and unit parts are finally singulated and made ready for testing (see Figure 9).



Intel

Figure 9. The 1.0 mm high finished folded package encases two Flash die and one SRAM die.

Folding after singulation is possible but somewhat awkward, requiring more complex handling and alignment challenges.

About the micro BGA Lead-Bond Process

The lead-bond process initially developed for the single die micro BGA package technology has been successfully applied to multiple die packaging, offering uncompromised conductivity and reliability. The technology is especially suited for packaging ICs that need a very low finished profile height. The leads is actually an integral part of the base substrate and during the lead-bond process reshaped into an '*S*' configuration as shown in Figure 10. The symmetrical profile of the lead, when encapsulated, absorbs a majority of the physical stress and strain that can occur between dissimilar materials when exposed to high and low operating temperature.

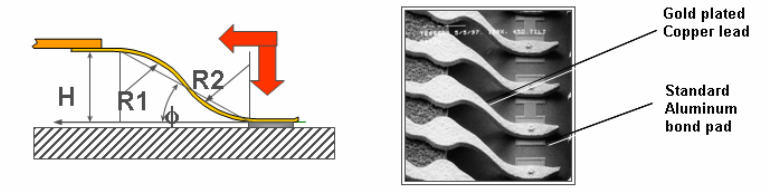


Figure 10. The 'S' shaped bond lead allows flexure within the package during variations in thermal conditions.

The lead design developed for this process employs a narrow section of the copper foil bridging across an ablated section of the substrate. The exposed conductor is plated with a thin layer of gold alloy to accommodate die-to-substrate interface.

During the lead-bond process a narrow cross-section of the conductor 'breaks-away' from one edge of the ablated section of the substrate, re-shaped and thermo-sonically connected to the corresponding die-bond pad. Following the lead-bond process, the package is encapsulated with a silicone based compound. The encapsulation has been formulated (after curing) to allow a controlled movement of the 'S' shaped lead during thermal excursions to buffer the physical strain of the solder joint at the board level interface.

Fold-Over and Stacked Packages

The fold-over package shown in Figure 11 was developed to join a complex logic function with several variations of memory. The base package substrate has been designed to mount a single die element with an extended portion of the substrate, when folded over, will accommodate the mounting of second pre-packaged device. Because of the overall interface complexity of this application, the substrate developed required two conductive layers on the polyimide film dielectric. The copper conductor layers furnish the in-package interconnect to the top surface as well as package-to-board or module interconnect. The substrate is configured in a three section strip format and uses wire-bond technology for the base die-to-substrate interface. Following the wire bond process, the assembly is transferred to a mold fixture where the extended substrate section is folded over the wire bonded die and encapsulated using a unique edge-mold process.

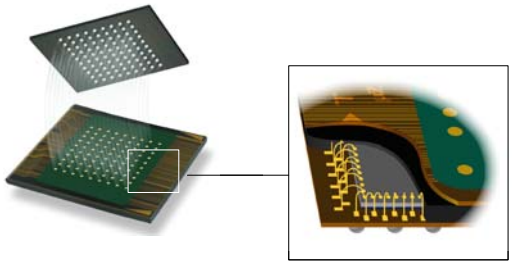
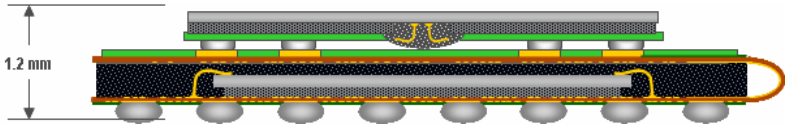


Figure 11. A Fold-Over and Stacked package.

Following the molding process, the spherical contacts are placed and attached using a reflow solder process. The three assembled base units are finally singulated and made ready for electrical testing.

The fold-over extension of the base package can be configured to accept any number of commercial or custom fine-pitch array package types. By providing the memory interface on the topside surface of the logic package, commercially available array packaged products can be soldered directly to base package. The example shown in Figure 12 shows the top surface of a face-up, wire-bonded folded and packaged die with a mounting site on its top surface for mounting a commercially packaged BGA memory device.



Intel

Figure 12. The Folded and Stacked package enables board level sequential assembly of components supplied from multiple sources.

Through this process of folding and package stacking, two or more pre-tested parts become a single, high yielding multiple-function component. Whether or not to join one package to the other before or during the board level assembly process is a decision that may be influenced by the requirement for in-process configuration flexibility. For example, the base fold-over package can be furnished by vendor 'A' while the memory sections of the stack are supplied by vendor 'B', 'C' or 'D'. After all, memory functions are available from a greater number of sources and the testing for memory is very different than that used for logic functions.

Solutions for the Next Generation of IC Packaging

To resolve current expectations for the next generation of multiple function packaging for hand-held and portable electronic applications we have developed a new and innovative vertically stacked package methodology that offers a practical high-yield solution for higher density memory as well as a broad range of system-in-package applications. One of the challenges that will need to be overcome is the limitations of circuit routing the higher I/O devices. When packaging the more complex die in a ball grid array format, the size (diameter) of the ball contact often restricts the space needed for inter-package and

intra-package circuit routing. Fine-pitch BGA, for example, may have a contact spacing of 500 microns and ball contact diameter of 250-300 microns. The spacing between these contacts is only 200 to 250 microns, barely enough space to route a two 40 micron wide circuit conductors. Although many of these high I/O packaged devices will rely on micro-via and multiple layer circuit board technology, the space restriction for circuit routing often forces the designer to resort to excessively complex circuit board fabrication technologies. To solve this potential complexity, a solution for improving in-package interconnection and package-to-board efficiency has evolved. Rather than relying on attached alloy spheres for the package contacts, the new package is furnished with smaller, conical shaped contacts. These contacts that are no greater than 180 microns at the mounting plane. The smaller contact features enable the use of a smaller land pattern (200 microns) for package stacking (see Figure 13) and solder attachment. This smaller land pattern provides the additional space needed for the routing of three 40 micron wide circuit conductors.

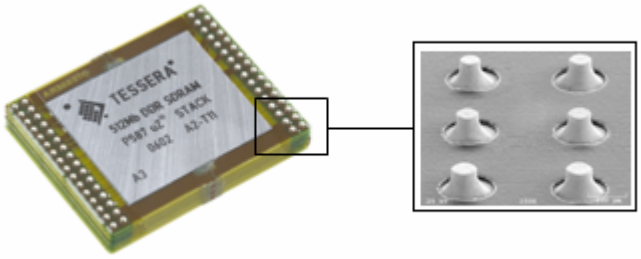


Figure 13. Six layer stacked DDR memory package (Assembly is only 1.2 mm in total height)

This contact profile was developed specifically for high-density 3D package stacking applications and offers a practical high-yield solution for a broad range of system-in-package applications. The substrate for the package also relies on a polyimide film as the substrate dielectric, however, the package substrate fabrication process is very different than those previously described (see Figure 14). The primary difference is, the dielectric is applied to a unique tri-metal base composition rather than using a metalized film as its base.

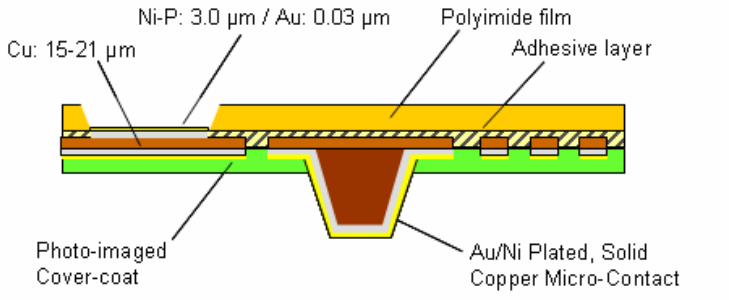


Figure 14. Substrate cross-section view.

The tri-metal base alloy begins as a rolled copper foil that is furnished in thicknesses up to 180 microns. One side of the copper foil is electroplated with a thin (0.8 to 1.0 micron) nickel. The nickel plated surface is then electroplated with 9 to 18 microns of copper. The heavy layer of copper will eventually provide the actual contact features while the thin layer of copper on the opposite side of the nickel will be reserved for in-package circuit routing.

Package Assembly

The package assembly process is based on the already proven and mature assembly technology. As with the processes described earlier, the individual package substrate is initially retained in the array strip format for efficient wire-bond assembly processing. The contact pattern furnished on the opposite side of the substrate also serves as the attachment sites for the next package layer. This provision for vertical interconnect between package layers ensures the efficient transfer of electrical signals between each package layer, ultimately terminating at the PCB or module surface.

In preparation for the stacking process, a specially formulated high temperature (Pb-free) solder paste is deposited at each interface contact land then transferred to a multiple site alignment fixture. The actual stacking process begins when transferring the second layer package atop the base packages. The joining (stacking) process is repeated for each package layer and, when completed (typical of the ball stack process), the stacked units are transferred to a forced air/gas convection oven for mass reflow to finish the interlayer solder joining of all package layers Because of the relatively thin composite of

elements within each section of the package, the overall height of the finished package is minimized. The total package height is ultimately determined by the number of packages joined in the stacked example shown in Figure 15.

Figure 15. Four layer stacked SRAM package assembly.

Following cleaning and a final continuity test of the multiple package assembly, the stacked packages undergo a final physical inspection before transfer to partitioned trays designed for shipping to customer sites. In regard to board level assembly, the solid copper MicroContacts are furnished with a thin Ni/Au alloy plating so they are compatible with either eutectic or lead-free alloy solder processes.

Conclusion

The expanding functionality expectation for portable and hand-held electronic products has opened up a whole new category of IC package technology. This factor has increasingly become an issue and is evidenced by the physical restriction on the number of ICs that can be designed onto the circuit board. Package performance is also an issue. Until recently, the component packaging industry did not directly concern itself about system level performance, but, as multiple die are configured into a single package outline, the whole system performance issue must be kept in view. Any comparison, however, should be done at the equivalent system level; one composed of single device packages and the other with multiple die packages and their interface methodology. As noted above, the perimeter located contact pattern of the package is designed to allow one package to sequentially mount on the top of one another providing the interface between package layers and the eventual termination to the board or module level assembly. These features are an integral part of the substrate, not attached features typical of the ball grid array contacts. This, in turn, allows the overall profile of each package section to be very thin.

Because all of the package assembly processes shown can utilize the well established BGA manufacturing infrastructure, the technology is transferable to multiple sources of supply. Several concerns, however, still remain for multiple die and mixed function system-in-package technologies. The management of multiple IC vendors and establishing reliable sources for bare die and/or wafers is a primary issue. Other issues include estimating compound yield of less mature ICs, controlling overall product quality, reliability and how to accommodate incompatible die shrinks. In regard to the universal trend to consider long term environmental goals, all package technologies described above are RoHS compliant, furnishing a 100% lead-free and bromide free process.

Note: In keeping with IPC presentation guidelines it should be noted that the technical information presented in the paper focused on patented package assembly methodologies and fabrication processes and are availble only from authorized licensees.. In addition, the acronyms used above are registered trademarks of Tessera, Inc. headquartered in San Jose, California.

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Los Angeles, California – 22 February 2007

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Tessera, San Jose, California USA

Topics of Discussion

- **This presentation furnishes a view of current expectations for multiple-die BGA and CSP technology for wireless and other miniature electronic applications**
- **In addition, we will review the dynamic evolution taking place in developing more efficient system-in-package capability.**

Drivers for Enhancing IC Performance

- The revolution in performance driven electronic systems continues to challenge the IC packaging industry.
  - In an effort to achieve these goals, developers are relying more and more on innovative package assembly techniques and process refinement to lower the cost of IC package assembly.
- To enable the IC to reach its performance potential many IC suppliers have adapted the land or ball grid array interface format.

Moving all of the contacts under the package outline provides a shorter package-to-board interface.

3

Drivers for Miniaturization…

- With each generation of electronics developed for wireless consumer applications, companies' will attempt to-
  - Reduce the product size.
  - Improve product performance and reliability.
  - Offer more features and/or capability.
- Additional functionality, however, will typically require significantly more sophisticated electronics.

Without miniaturization, increased functionality will likely impact both product size as well as manufacturing cost.

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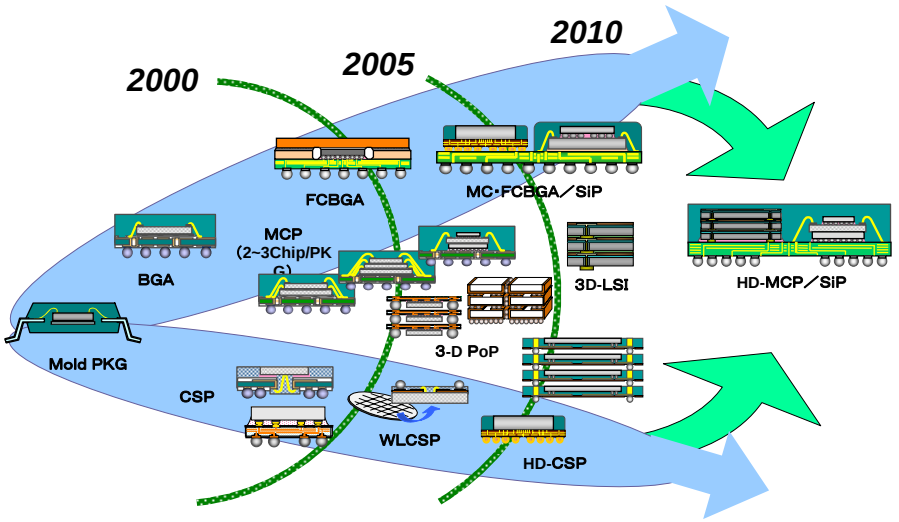
IC Package Evolution



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Higher Density IC Package Assembly

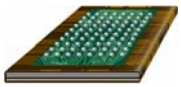
- The demand for higher density IC packaging continues to dominate the development activity for both portable hand-held electronics as well as some products that are well outside the realm of portability.
- To meet market demands for increased functionality in the IC packages supplied to OEMs, IC package assembly specialists are offering a number of multiple die configurations.
  - Die-stack package
  - Folded package
  - Stacked package

6

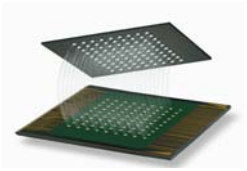
Tessera's µZ® 3D Multiple-Die Package Solutions

Ball Stack Package

Possum Package



Folded Package



Fold-Over and Stack Package

7

Market Trend for IC Packaging

- **Two market trends that have been evident for some time**
  - **Increasing microprocessor speeds**
  - **Increasing demand for additional functionality**
- **These market trends in turn are driving the demand for increased density of higher performance memory in systems.**

8

High Density Memory Market Forecast

Worldwide Stacked-Memory MCP Unit Forecast by Package Type (Millions of Units)

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Others	0	0	3	2	1	0	0	0	0	0	0
Total	86	98	153	248	459	598	662	705	748	840	848

Source: DataQuest

Companies have found that combining (stacking) already proven memory die within a single package structure a practical and economical solution.

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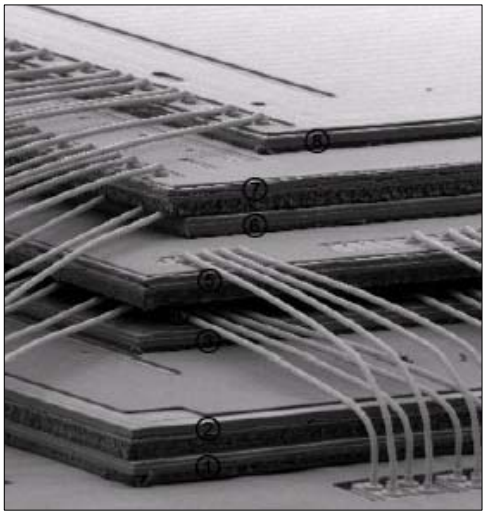
Die Stack Packaging for Memory



Samsung

⑧ 64Mb UtRAM
⑦ 128Mb UtRAM
⑥ 256Mb NOR Flash
⑤ 256Mb SDRAM
④ 256Mb NOR Flash
③ 256Mb SDRAM
② 1Gb NAND Flash
① 1Gb NAND Flash

10

Package-on-Package for High Performance Memory

- The newer generations of high-performance DDR memory have a relatively wide supply base, however, the die are rarely common in size from one supplier to another, even when they have the same memory capacity.
- They do have some commonality in that they are generally rectangular in shape and the wire-bond pads (as noted above) are located in the center of the die rather than at the perimeter as is typical for most silicon product.

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Die Size for DDR 1 and DDR 2

256M DDR1 and DDR2

Micron	5.02 x 8.94 mm
Mosel	4.72 x 8.89 mm
Hynix	5.17 x 8.84 mm
Infineon	4.89 x 8.70 mm
Samsung	5.48 x 11.21 mm
Nanya	---
Elpida	5.78 x 10.90 mm

512M DDR (0.11 µm)

Micron	9.28 x 9.84 mm
Mosel	8.93 x 8.93 mm
Hynix	7.10 x 15.3 mm
Infineon	8.93 x 8.93 mm
Samsung	9.59 x 9.59 mm
Nanya	9.27 x 9.27 mm
Elpida	5.78 x 10.9 mm

512M DDR (0.09 µm)

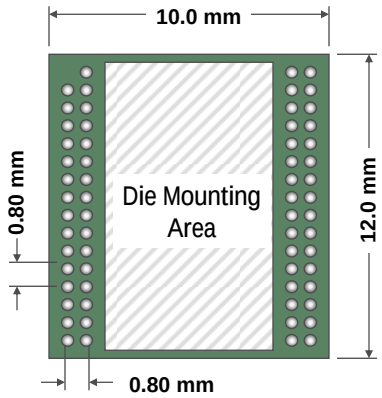
Micron	7.52 x 7.52 mm
Mosel	7.03 x 7,03 mm
Hynix	6.28 x 10.73 mm
Infineon	7.03 x 7.03 mm
Samsung	7.55 x 7.55 mm
Nanya	9.06 x 9.06 mm
Elpida	7.49 x 7.49 mm

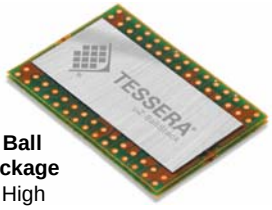
512M DDR 2 (0.11 µm)

Micron	---
Mosel	---
Hynix	6.28 x 10.73 mm
Infineon	---
Samsung	---
Nanya	9.50 x 9.50 mm
Elpida	8.66 x 10.24 mm

12

Ball Stack Substrate Development



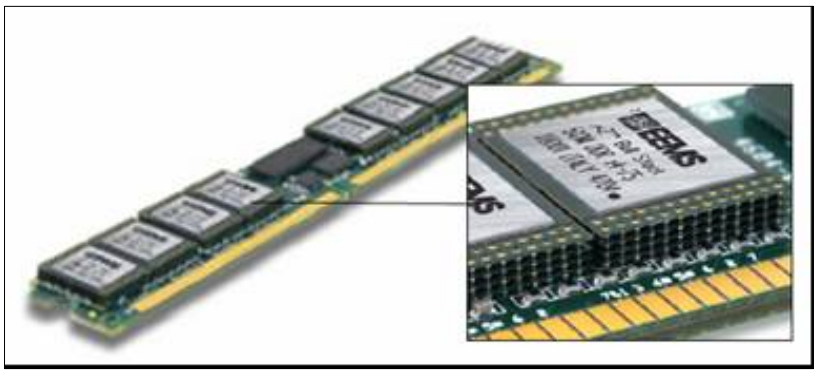


2 Layer Ball Stack Package
1.2 mm High

4 Layer Ball Stack Package
2.3 mm High

13

High Density Memory Module Development



The 4 Gb DIMM module was developed for the IBM blade server product has eighteen 4-layer µZ® Ball Stack packages surface mounted on both sides of the module substrate.

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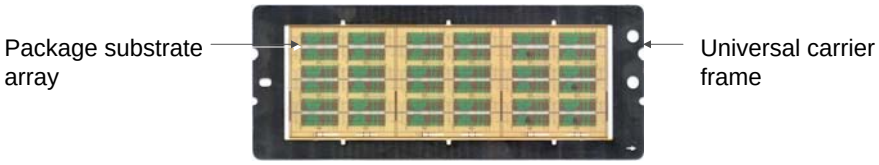
Ball Stack Package Assembly

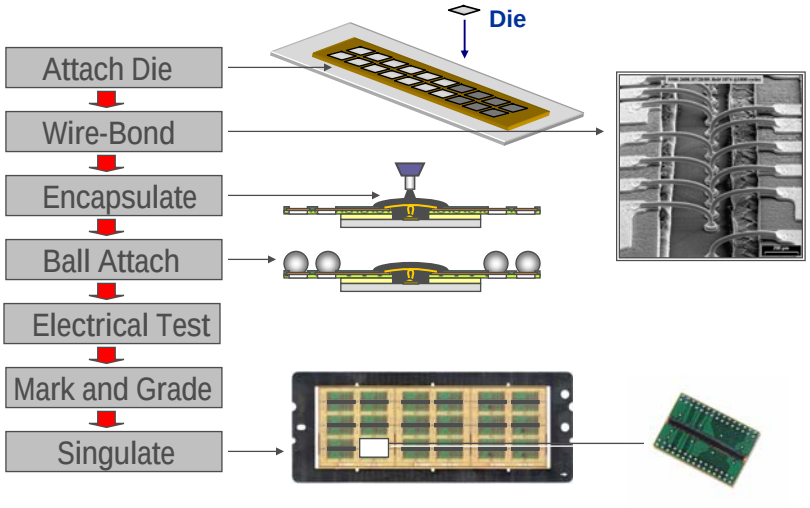
- The µZ-Ball Stack package assembly process is based on the already proven and mature technology developed for the µBGA® package.
  - The polyimide film or B-T epoxy substrate is furnished in a strip array format of twenty to thirty die attachment sites.



The strip format furnishes an efficient method for sequentially processing of several individual device units at a time.

15

Basic Ball Stack Package Assembly Process



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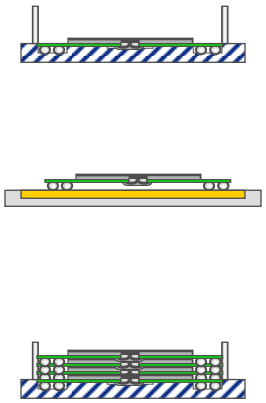
Process for Package Stacking



- the base or bottom packages are first transferred from their carrier-tray to a multiple unit alignment fixture.
- The actual stacking process begins with the transfer of the second layer package to a dip-fluxing station to uniformly coat the bottom half of the ball-contact.
- with flux applied, the upper level packages are sequentially placed atop the base packages and repeated for each package layer prior to reflow soldering

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µZ® -Possum Package-on-Package

- The Possum package process is a unique configuration made possible by joining two lead-bond µBGA packaged devices together.
- The secondary device is mounted to a land pattern provided on its bottom (or lower) surface, the same surface that contains the spherical alloy contacts for the eventual board or module interface.
- The advantage of this configuration is that each IC package section becomes a fully tested subsystem that can be certified by the supplier before joining together

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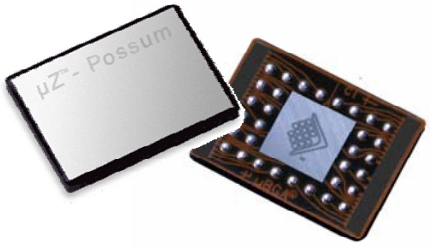
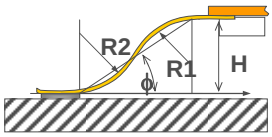
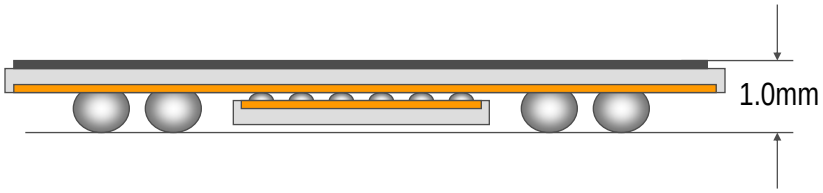
Possum Package-on-Package





Low profile
lead-bond



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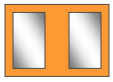
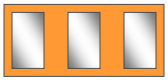
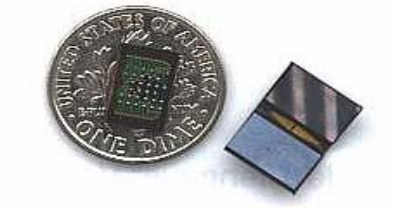
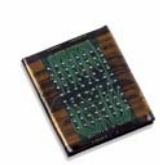
µZ® Fold-Over Packaging







µZ Fold-Over two die Flash
memory package



The three die µZ Fold-Over two
Flash memory die and one
SRAM die

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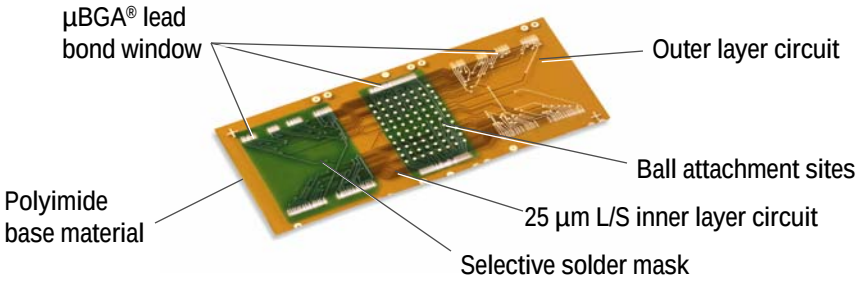
Folded Package Substrate

- Multiple die package applications requiring two, three or more die can be attached in series onto a foldable, multiple site flexible polyimide film substrate.



Configuration developed for Intel

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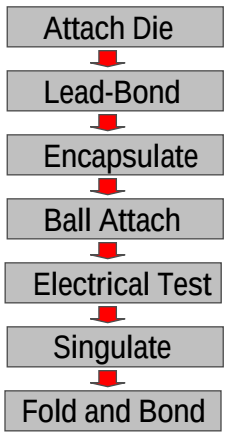
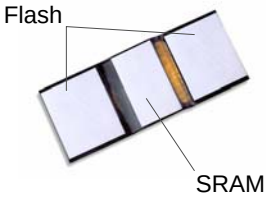
3 Die Assembly Process Overview





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About the µBGA® Lead-Bond Process

- The lead-bond process initially developed for the single die µBGA package technology has been successfully applied to multiple die packaging, offering uncompromised conductivity and reliability.
- The technology is especially suited for packaging ICs that need a very low finished profile height.
  - The leads are an integral part of the base substrate and during the lead-bond process reshaped into an '*S*' configuration
  - The symmetrical profile of the µBGA lead, when encapsulated, absorbs a majority of the physical stress and strain that can occur between dissimilar materials when exposed to high and low operating temperature.

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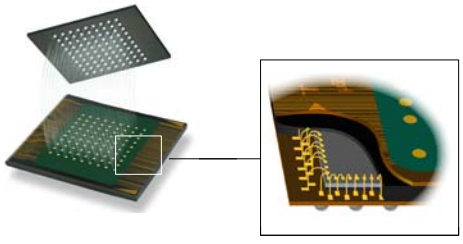
µZ® Fold-Over and Stacked Package

- The fold-over package was developed to join a complex logic function with several variations of memory.



The base package substrate has been designed to mount a single die element with an extended portion of the substrate, when folded over, will accommodate the mounting of second pre-packaged device.

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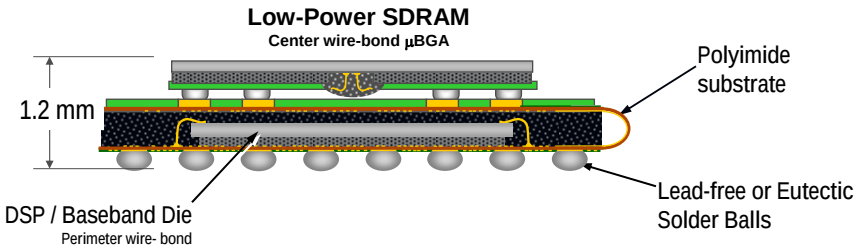
µZ® Fold-Over and Stacked Package cont.

- The fold-over extension of the µZ Fold-Over base package can be configured to accept any number of commercial or custom fine-pitch array package types.



By providing the memory interface on the topside surface of the logic package, commercially available array packaged products can be soldered directly to base package.

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Solutions for the Next Generation of IC Packaging

- There is a need to resolve current expectations for the next generation of multiple function packaging for hand-held and portable electronic applications
  - One of the challenges to overcome is the limitations of circuit routing the higher I/O devices.
- When packaging the more complex die in a ball grid array format, the size (diameter) of the ball contact often restricts the space needed for inter-package and intra-package circuit routing.
- Fine-pitch BGA may have a contact spacing of 500 microns and ball contact diameter of 250-300 microns.
  - The spacing between these contacts is only 200 to 250 microns, barely enough space to route a two 40 micron wide circuit conductors.

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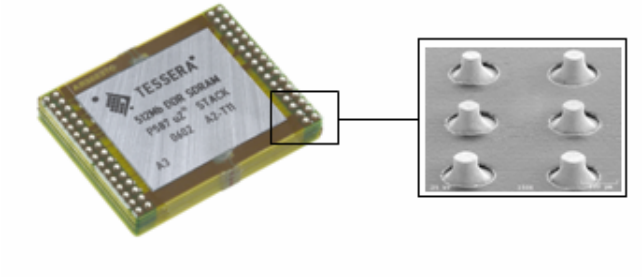
MicroContact Array Package Technology

Tessera has developed a new and innovative vertically stacked package methodology that offers a practical solution for higher density memory as well as a broad range of system-in-package applications.



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Solutions for the Next Generation of IC Packaging

- Rather than relying on attached alloy spheres for the package contacts, the new MicroContact package is furnished with smaller, conical shaped contact that are no greater than 180 microns at the mounting plane.
  - The smaller contact features enable the use of a smaller land pattern (200 microns) for package stacking and solder attachment.
  - This smaller land pattern provides the additional space needed for the routing of three 40 micron wide circuit conductors.

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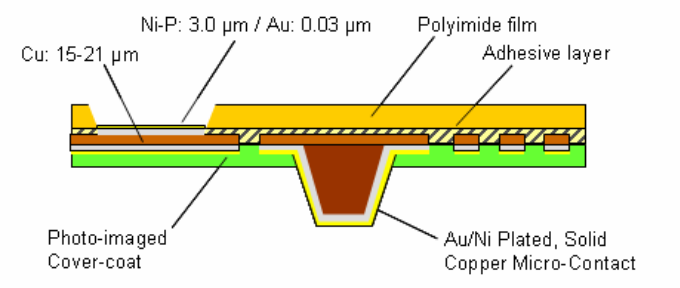
MicroContact Substrate

- The MicroContact, a contact profile was developed specifically for high-density 3D package stacking applications and offers a practical high-yield solution for a broad range of system-in-package applications.



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MicroContact Package Assembly

- The package assembly process is based on the already proven and mature technique developed for the µBGA® package assembly technology.
- As with the processes described earlier, the individual package substrate is initially retained in the array strip format for efficient wire-bond assembly processing.

The contact pattern furnished on the opposite side of the substrate also serves as the attachment sites for the next package layer.

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Summary and Conclusion

- The expanding functionality expectation for portable and hand-held electronic products has opened up a whole new category of IC package technology.
- This factor has increasingly become an issue and is evidenced by the physical restriction on the number of ICs that can be designed onto the circuit board.
- System package performance is also an issue...

Until recently, the component packaging industry did not directly concern itself about system level performance!

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Summary and Conclusion cont.

- As multiple die are configured into a single package outline, the whole system performance issue must be kept in view.
  - Because all of the package assembly processes utilize the well established µBGA® manufacturing infrastructure, the technology is transferable to multiple sources of supply.
- Several concerns, however, still remain for multiple die and mixed function system-in-package technologies.
  - The management of multiple IC vendors
  - Establishing reliable sources for bare die and/or wafers
  - Estimating compound yield of less mature ICs,
  - Controlling overall product quality, reliability
  - How to accommodate incompatible die shrinks.

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IPC Disclosure Statement-

Note: In keeping with IPC presentation guidelines it should be noted that the technical information presented in the paper focused on Tessera's patented package assembly methodologies and fabrication processes developed for the MicroContact substrate and are available only from authorized licensees of Tessera.

In addition, the acronyms 'µBGA' and 'µZ' are registered trademarks of Tessera, Inc. headquartered in San Jose, California.

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