IPC Electronics Midwest 2010

HDI Training & Implementation at Eagle Test Systems

Ron Evans

Eagle Test Systems

Biography:
VP of Operations

Mr. Evans has three decades of manufacturing technology, product development, operations, sales and marketing experience. This experience encompasses a wide range of technologies including machining, metal fabrication, optics, plastics, printed wiring board fabrication, electronic assembly, system integration, and semiconductor test.

Mr. Evans is an executive with successful P&L responsibility, experience with conceiving, developing and executing the strategies and initiatives that drive revenues, growth, competitive market positioning, profits, and shareholder value. This broad experience includes national and international businesses, start-ups, turnarounds, mergers & acquisitions, and playing an integral role in delivering hundreds of millions in new business revenue during his career.

Mr. Evans' has held positions at Brunswick Corporation – Defense Division, The National Center for Manufacturing Sciences (NCMS), USRobotics/3Com, Westell Technologies, and he is currently the VP of Operations & Supply Chain Management for Eagle Test Systems located in Buffalo Grove, IL. The successful growth of Eagle Test resulted in its acquisition by Teradyne Inc. during Q4 of 2008. Mr. Evans has published dozens of articles and papers, holds several patents, and holds BS from the University of Maryland, and MBA from NSU in Ft. Lauderdale, Florida. Mr. Evans is also a two time recipient of IPC's Best Technical Paper Award.

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Todd Henninger

Coretec USA Inc.

Biography:
Field Application Engineer

Todd has been in printed circuit board manufacturing industry for 20 years, with technical expertise in rigid and flexible circuits. He is IPC certified (C.I.D. and C.I.T.) with a primary focus on helping PCB designers understand and optimize their boards for functionality, manufacturability, and cost minimization. Todd also assists customers in the design and use of emerging technologies, including high-density interconnect (HDI) structures.

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HDI Training & Implementation at Eagle Test Systems

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Ron Evans, ETS Operations & Supply Chain Management
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Abstract
Eagle Test Systems (ETS) a Teradyne Company established a team during 2009 to develop a training exercise that would bring High Density Interconnect (HDI) knowledge to new products. A digital module was chosen as a redesign candidate to convert from standard printed circuit board technology to HDI with the help of an experienced third party CAD design house (DDI). The goal of the project was to take the existing digital module and reduce its mechanical size and features by approximately 50%; while maintaining or improving its electrical characteristics. One successful prototype lot was designed, fabricated, assembled, tested, and compared to the existing product performance. The design and fabrication process utilized while performing these tasks was documented and used to train ETS CAD designers, product development, manufacturing, and test engineers on HDI technologies.

1.0 Introduction

HDI is an essential technology required by electronic designers and manufactures to achieve the increased density requirements of modern day electronic products. Today's demand for higher density electronics has made obsolete many components of the 60 year old Printed Circuit Board (PCB) design and manufacturing techniques. Design requirements for smaller holes, thinner materials, smaller copper traces, and faster electrical performance is pushing current manufacturing, assembly, and design practices into obsolescence. Older PCB technologies such as mechanical drilling and surface mount discrete components are being replaced with HDI methodologies around the world with Asia leading the adoption of HDI design practices. North American leaders in product development (like ETS) were lagging the rest of the world due to lack of training, understanding, and implementation of HDI technologies. ETS had HDI obstacles toward implementation that included:

- Lack of on-site knowledge of how to properly design an HDI board;
- How does Eagle Test staff learn about the design models available for use;
- How does a designer obtain the CAD tools necessary for stack-up, architectures, channel routing, and boulevard routing;
- How does the designer understand the signal integrity and performance of HDI features;
- Where does the company get HDI designed boards manufactured;
- What are the material selections for HDI designs;
- What are the assembly issues related to HDI products;
- How does one design electrical tests for HDI products

Training was needed for Eagle Test Systems to overcome implementation obstacles and also learn how to quantify the benefits of HDI designs on Eagle Test/Teradyne products.

Typical HDI Benefits:

- Stable voltage rails
- Removal of decoupling & bypass surface layer capacitors
- Removal of surface layer resistors
- Lower cross talk and noise
- Much lower RFI/EMI noise and improved shielding
- Closer ground planes
- Closer distributed capacitance
- Minimal stubs
- Surface ground planes with via-in-pads cut emissions

- Lower order of magnitude interconnect electrical parasitic
- Improved power distribution system
- Reduced circuit board size, Improved panelization
- Reduced layer count
- Reduced circuit board thickness
- Improved reliability due to smaller hole aspect ratios and less solder joints
- Simplified routing due to reduction in traces and vias
- Increased product functionality
- Increased number of PCB boards on a panel
- Lower assembly costs
- Reduced test times

Products designed using HDI technology typically yield product improvements through the following summary of results: >50% more wiring density, >50% reduction of surface mount discrete components, >50% reduction in physical size, >30% thinner boards, lower cost of assembly, lower layer counts, improved electrical performance, and lower overall cost.

HDI Training for design, development, manufacturing, and test engineers is essential for Eagle Test System – A Teradyne Company, to stay competitive.

2.0 Design and Training Partner

Several members of the ETS project team had worked with HDI technologies since the early '90s. However, in order to proceed with HDI training and technology implementation at ETS, it was decided to partner with an experienced PCB design and prototype shop that is currently providing HDI designs. DDI Design Group, Toronto, Canada (formerly Coretec) was chosen as the trainer over several potential other companies due to their in-depth knowledge, industry experience with HDI, over 25 years of electronic design experience, and common design software tool sets to Eagle Test Systems.

2.1 Design Layout of Existing Digital Module PCB

The existing product is 0.075" thick, 12 layers, with 6 signal layer board that is 11.29 sq in^2. The stack-up and physical design of the current production digital module is shown in Figure 1. A comparison of the differences in density between the current digital module-R1 and the new HDI digital module-R2 is presented in **Addendum A.** The new design is 0.040" thick, 6 layers, with 2 signal layer board that is 6.24 in^2.

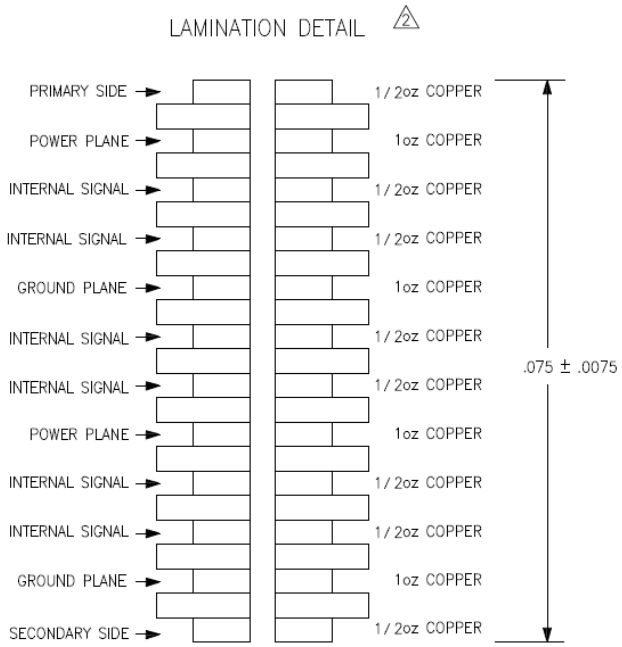


Figure 1 Existing Digital Module-R1

2.2 Design Layout of HDI Digital Module – R2

To begin the design work, a Statement of Work (SOW) was written defining the effort required to plan and execute the redesign of a digital assembly into a test vehicle used for training purposes only.

The test vehicle was used to emulate product features and performance. The test vehicle reduced layer count, size, component count, and thickness. The SOW included the associated program management, engineering support, costs, and communications required to effectively complete this training project.

The test vehicle enables the ETS team to evaluate the effectiveness of Embedded Passive (EP) materials and High Density Interconnect (HDI) technologies in increasing component density, lowering product costs, and improving by-pass decoupling of digital Integrated Circuits (IC). These pre-competitive technologies, if effective, will enable ETS to more easily introduce new features to existing products and lower lifetime costs of new products through decreased Printed Wiring Board (PWB) size requirements or increase functionality in existing footprints.

2.3 Selection of Test Vehicle

DDI redesigned the digital module into an HDI test vehicle to demonstrate the stated benefits of the introduced technologies through the potential increase in functionality and board size reduction. HDI technologies including microvias, buried vias, and blind vias were used with embedded capacitance materials to increase routing density and minimize surface layer routing. All work was performed with the goal of maximizing the stated benefits of the introduced technologies on the final test vehicle. The final digital module-R2 is show in **Figures 2A through 2D**.

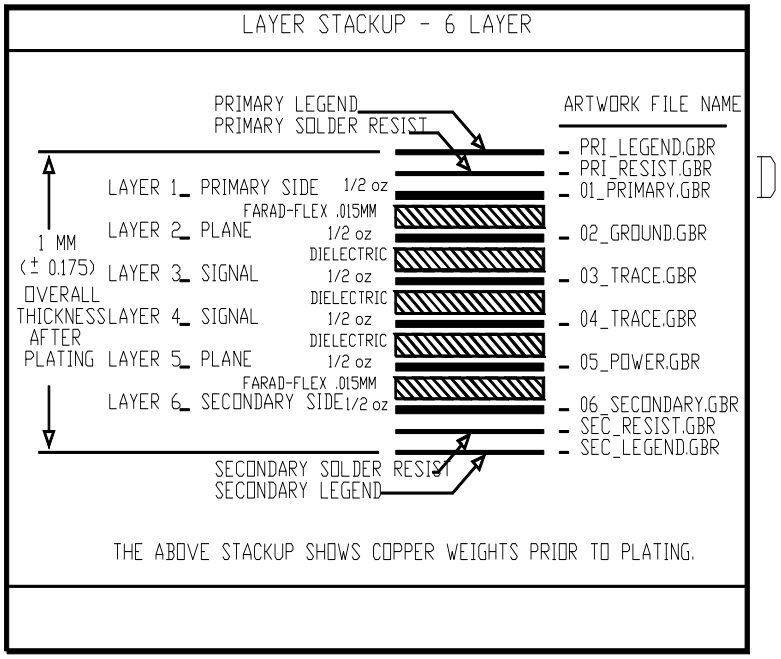
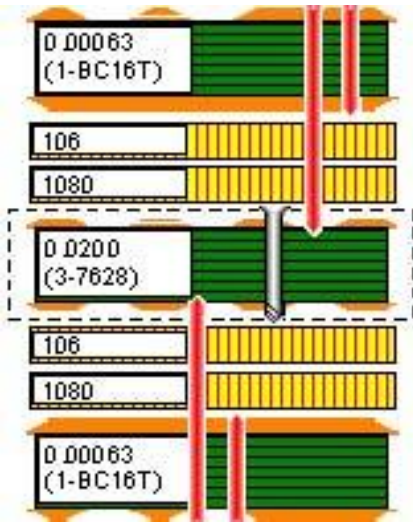


Figure 2A New Digital Module-R2



Description

Taiyo 400-MP
½ oz Mix (Std Plt)
BC16T
½ oz P/G
370H
½ oz Sig (Std Plt)
370H
½ oz Sig (Std Plt)
370H
½ oz P/G
BC16T
½ oz Mix (Std Plt)

Figure 2B Module-R2 Rigid Drill Stack

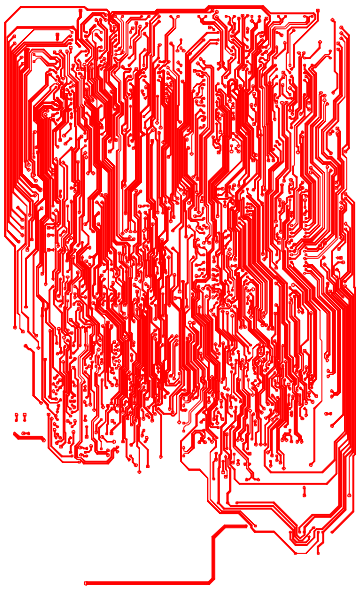


Figure 2C Digital Module-R2 Layer 3

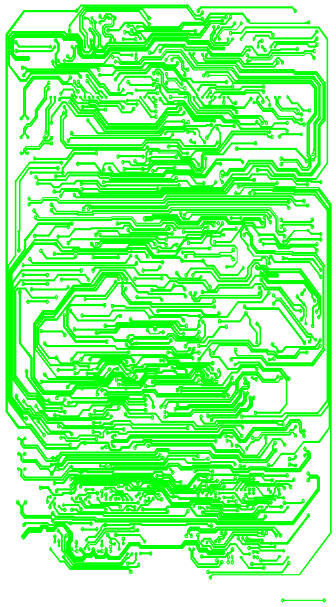


Figure 2D Digital Module-R2 Layer 4

This final design went from six signal layers to two and was used by a DDI FAE to demonstrate the proper engineering design principles to ETS engineers and designers.

3.0 Methodology

3.1 Design Inputs & Customer Responsibilities - ETS

ETS provided:

1. Complete ORCAD schematic, conversion to DxDesigner, components file, net list, footprints, and CAM data
2. Design guidelines and constraints (both electrical and mechanical)
3. Technical guidance and final design approval
4. Assembly rules

3.2 Project Deliverables - DDI

The DDI deliverables included the following:

1. PADS database
2. Fabrication drawing (pdf)
3. Artwork data (RS-274X format)
4. Assembly drawing (pdf)
5. CAM data (.ASC)
6. Prototype PCBs

3.3 Applicable Standards

The test vehicle was designed to meet IPC 6012 Class 2 standards. It was also designed to meet both ETS and DDI Design for Manufacturability (DFM) standards.

3.4 Physical PCB Design

The physical PCB design phase of this project consisted of the tasks explained in Sections.

3.4.1 Component Selection

ETS engineers worked with members of the DDI Design Team, and the DDI Field Application Engineer (FAE) to review the design constraints related to embedded passive placement and trace rerouting. The team also selected an appropriate number of by-pass capacitors to embed using the chosen EP materials.

3.4.2 Design Database Update

Once the component selection task was completed, the "selected" discrete components were converted to EP shapes and assigned to their proper layers. At the same time, the schematic was updated by ETS to reflect those component(s) that had been selected for embedding capacitors (in planar capacitance form).

3.4.3 PCB Design & Verification

A joint review between Eagle Test and DDI designers was completed to verify the manufacturability of the design to DDI standards. A Design for Manufacturability (DFM) check was done.

3.4.4 Trace Routing

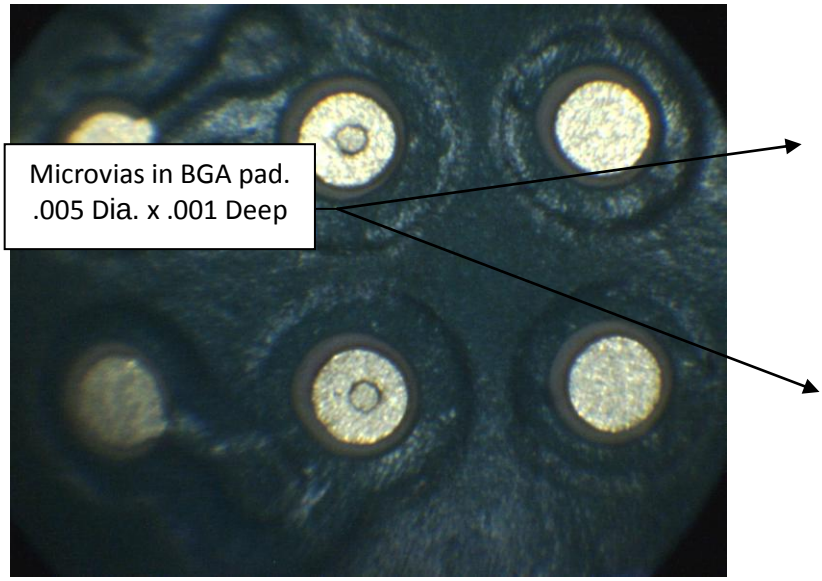
Upon approval of the component placement, signal routing commenced. Routing was performed by DDI 100% manually. Layers 1, 2, & 3 were done separately from Layers 4, 5, & 6 and then connected to form final product.

3.4.5 PCB Fabrication & Assembly Drawing Creation

When the PCB design was completed and approved, documentation and data was created. A second designer checked the set of documents prior to release. The new design is shown in Section 2.3.

4.0 Technology

Several technologies were used to create the HDI design. In addition to build-up and sequential build-up of the drilled laminates, the combination of microvias, blind, and buried vias was used. Microvias are < 6 mil laser drilled vias that can have aspect ratios of 9.5 to 1 (drilled hole diameter to laminate thickness). Common laser drill machines consist of TEA $C0_2$ and Nd/YAG lasers. The lasers are tuned for the CO_2 to ablate the woven glass & resin while the Nd/YAG laser ablates the metal. Laser machines are capable of creating thousands of microvias in minutes compared to hours for mechanical drills. The benefit of microvias is that they are placed in surface mount pads and go down only one or two layers. By significantly reducing drilled holes that go through all the signal layers, routing density is greatly increased.



The HDI design also incorporates Embedded Capacitance (EC), EC technology, in the form of Oak-Mitsui *Faradflex* material. *Faradflex* is an ultra-thin dielectric material used to reduce the overall impedance of power distribution systems and free up surface real estate by reducing the number of necessary discrete decoupling and bypass surface mount capacitors. BC16 variety of *Faradflex* was selected in this case for its capacitance value of (250 pF/cm^2 @ 1 MHz) and relative cost effectiveness to other varieties. Reducing the physical size of a PCB is enabled by the combination of microvias that reduce drilled holes and EC which reduces surface capacitors.

5.0 Testing

5.1 In Circuit Testing (ICT) Testing

The HDI digital module test vehicle was not designed for ICT testing. This was a training project and no funds were budgeted for an ICT fixture.

5.2 Functional Testing

The design of the HDI digital module allowed functional testing using assembly Diagnostics and Calibration software. Digital module-R1 was reduced in physical size, but a larger panel was incorporated to allow for the existing connectors to be used to interconnect with the product motherboard allowing complete testing of the module and the product upper level assembly. The HDI artwork was placed into the current digital module form factor to show physical size reduction and to allow electrical and mechanical connections with existing product motherboard. The form factor is shown in **Addendum A** photographs.

1. **Boundary Scan Test**: All modules were programmed and tested without failures on boundary scan fixture.

2. **Bench Test**: Product high level assemblies were built with new digital modules and known good mother board and other assemblies.

3. **System Diags**: The boards passed hundreds of diagnostics tests successfully.

4. **System Cal**: System cal/check **consistently passed 20 laps** on functional tester. Here is a brief comparison of cal/check using original digital modules on a good product board and using new modules on the same board.

HDI digital modules passed all the validation testing except one intermittent diagnostic subtest failure. This diagnostic test was intermittent. The nature of failure implies that it is a timing related failure. Production released diagnostic and calibration software was used for testing. In order to fix the one timing diagnostic subtest the released software would need to be re-tuned for the HDI prototype digital module to make this subtest pass consistently on all test platforms. Since this was a prototype build, that work was not performed.

The new HDI digital model was also swapped out with failing existing production digital modules on assembled product. The new HDI digital modules allowed the failing assemblies to pass.

Based on the validation performed, it can be concluded that the prototype digital module built using HDI technology (reduced PCB layer count and reduced number of bypass capacitors) performs as good as the production module.

Multiple laps of cal/check were run on a tester using a known good product board with original digital modules as baseline measurements. Following is a cal report summary that shows the worst 5 Cpks for the known good product motherboard with original digital modules. Cpk of 1.5 is used in production to screen diagnostic timing tests. Product assemblies with 1.5 Cpks or greater pass production functional test and are allowed to move on to system integration.

Table 1 - CALIBRATION REPORT – Original Digital Module

Time: 0.8 hrs Laps: 8

BOARD	PIN POS	S/N	STATUS	WORST			
				CPK	PLOT	TEST	
Product	0	2821	PASS	1.06	3982	Product-0 Extend Bit Pin8, Tg5	
				1.75	3393	Product-0 BitWt FD2 Pin8, Tg6	
				1.78	3990	Product-0 Extend Bit Pin9, Tg5	
				1.79	3375	Product-0 BitWt FD2 Pin8, Tg4	
				1.82	3466	Product-0 BitWt FD3 Pin9, Tg6	

The test boards ran 10 laps of cal/check using the exact same setup on a known good product mother board with new digital modules. Following is a cal report summary that shows the worst 5 Cpks for the known good board with new digital modules.

Table 2 - CALIBRATION REPORT – New Digital Module

Time: 1.1 hrs Laps: 10

BOARD	PIN POS	S/N	STATUS	WORST			
				CPK	PLOT	TEST	
Product	0	2821	PASS	1.11	4172	Product-0 DRV Deskew Pin12, TG5	
				1.61	3339	Product-0 BitWt FD2 Pin8, Tg0	
				1.63	3356	Product-0 BitWt FD1 Pin8, Tg2	
				1.72	3340	Product-0 BitWt FD3 Pin8, Tg0	
				1.79	3366	Product-0 BitWt FD2 Pin8, Tg3	

5. **System Cal**: Step 4 was repeated on a different tester. Baseline measurements were taken; cal/check on new modules was successfully run overnight to imitate the regular test process.

6.0 Training

The following is a description of the training performed at ETS by DDI:

6.1 On Site Training

Training was provided by a DDI FEA at the ETS facility for 6 hours. Attendees included Hardware Engineers, PCB Designers, Manufacturing Engineers, and Test Engineers.

6.2 Topics and Techniques

ETS designers and engineers were trained in the proper design of planar embedded capacitors and microvias using PADS 2007.1. These techniques were illustrated through a review of the HDI module test vehicle redesign performed by the DDI design team. Supplemental PADS 2007.1 design training for this project was provided remotely (e.g. web conference) by a member of the DDI design team.

6.3 Test Vehicle Prototype Assembly

Only one prototype run of the HDI assembly test vehicle was assembled. A total of five modules were assembled using the current digital module BOM.

7.0 Benefits and Design Comparison

This table is to highlight the benefits and increased wiring density that was achieved from the redesign of digital assembly.

Digital Module HDI Benefit Summary and Cost Comparison

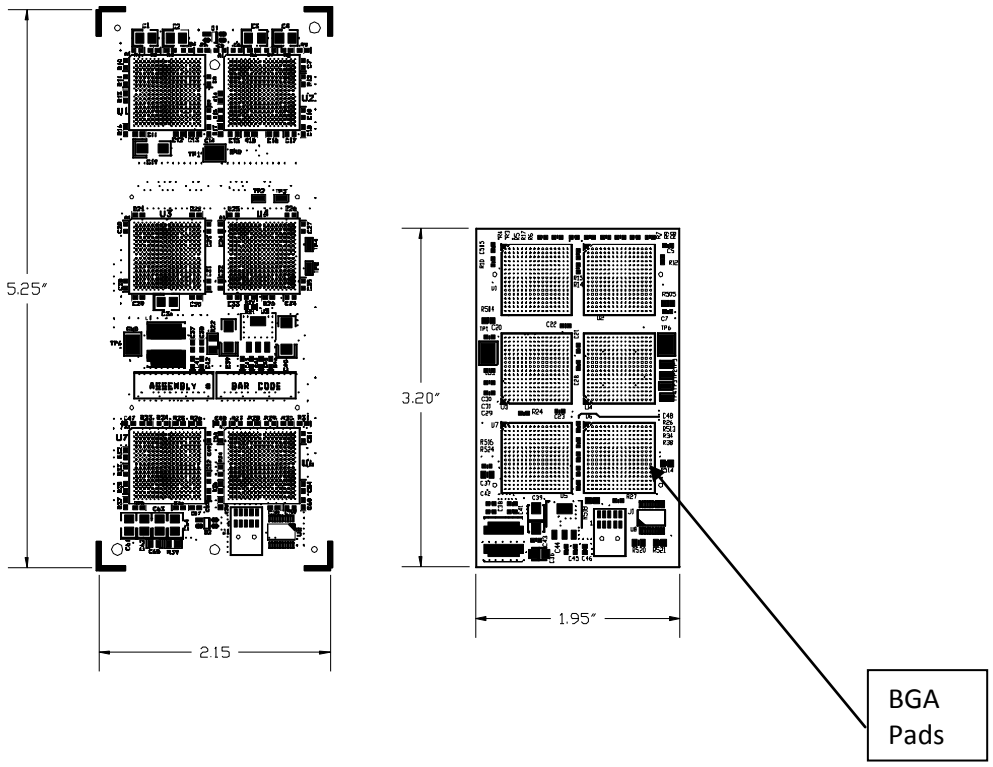
Benefit Estimate of Digital Module Board Conversion to HDI

Benefit Area	Current PCB Design	HDI Design*	Savings Description	Costs
BI-Pass Capacitor Reduction	72	47	Material Savings	$ (0.50)
			Annual OH cost savings of carrying 3 unique P/Ns for bi-pass Caps	$ (150.00)
			Assembly Cost per Placement	$ (1.25)
Mechanical Drilled Via Reduction	2149 Drilled Vias	133 Drilled Vias	1/2 hour drill time duration; < 15 minutes for 2-up to < 2 minutes for laser drill	
Laser Drilled Via Reduction	0 Laser Vias	1788 laser vias	1/2 hour drill time duration; < 15 minutes for 2-up to < 2 minutes for laser & mechanical drill	
Layer Count Reduction	12L	6L	50% decrease in layer count; while increase in wiring density due to via hole reduction	
Test Pad Reduction	418	0	Surface Area Savings	
Board Area Reduction - Sq. Inch	11.29 (5.25" x 2.15")	6.24 (3.20" x 1.95")	Board area reduction of 44% Due to: Mechanical drilled hole reduction, via-in-pad, discrete part removal, removal of signal, PWR, GND, traces from surfaces, moving parts closer together and reduction of test pads.	
Board Thickness	.075"	.040"	Board can be made thinner with less layers	
Board Cost	$ 34.00	$ 50.00	50% Less layers/44% Smaller Board. Cost increase comes from 2 Embedded Capacitance (EC) layers.	$ 16
Assembly Cost	$ 388.91	$ 383.56	EMS Partner	$ (5)
Estimated Total Per Board Savings				**$ (9)**

8.0 Future Work

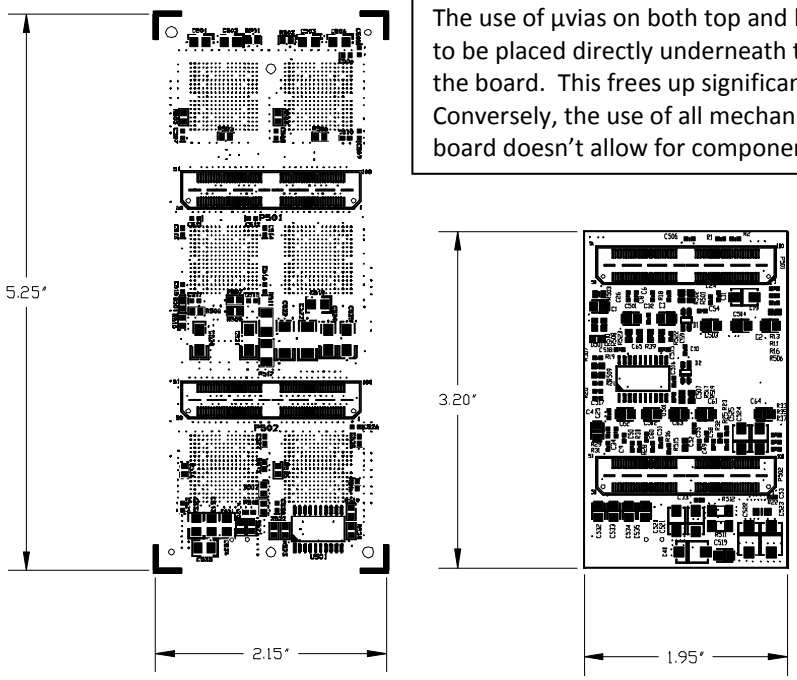
Based upon this work performed on the Digital Module, HDI technology is being used on additional products.

Addendum A

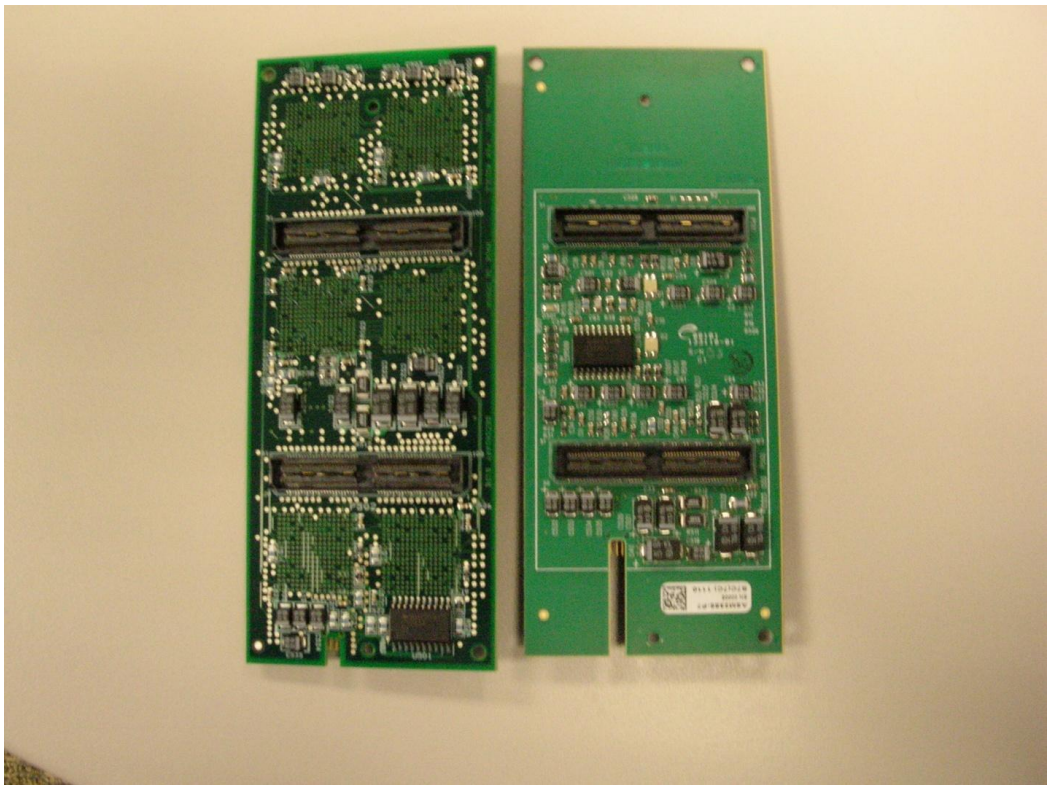


Primary Side Digital Module-R1 PCB vs. HDI Digital Module-R2 PCB

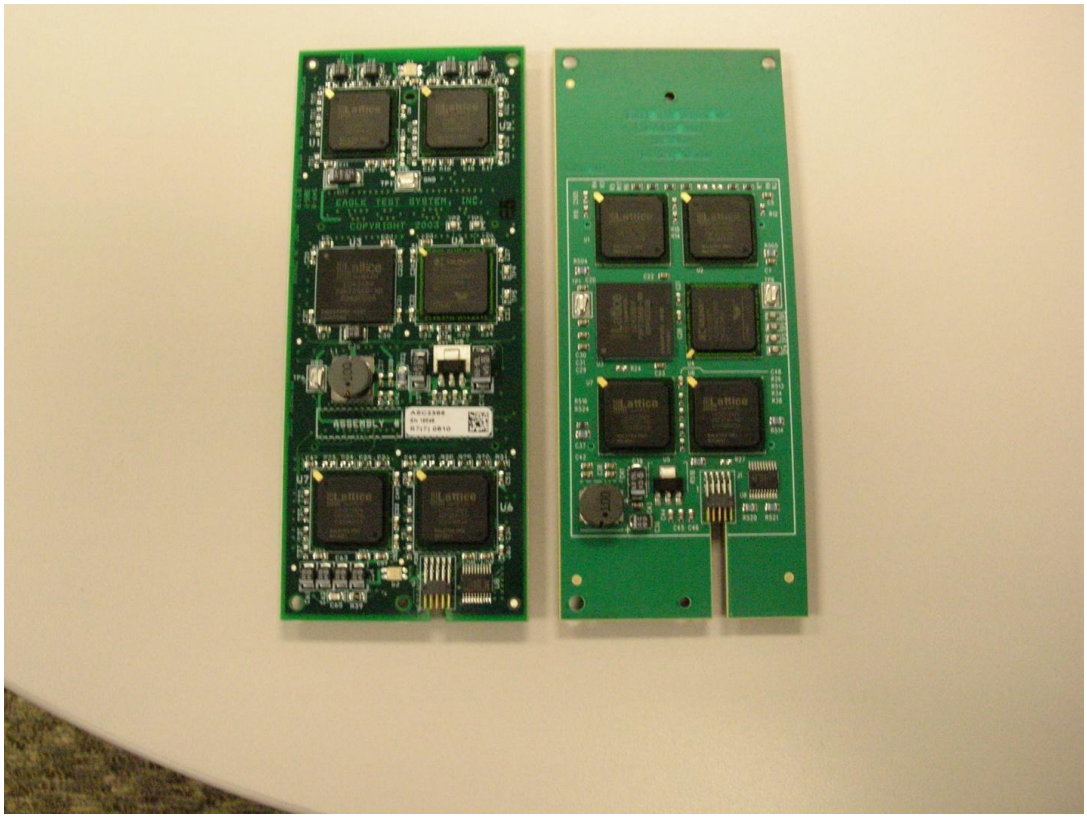
Note:
The use of µvias on both top and bottom sides allows components to be placed directly underneath the BGAs on the bottom side of the board. This frees up significant component real estate. Conversely, the use of all mechanically drilled holes on the current board doesn't allow for component placement under BGAs.



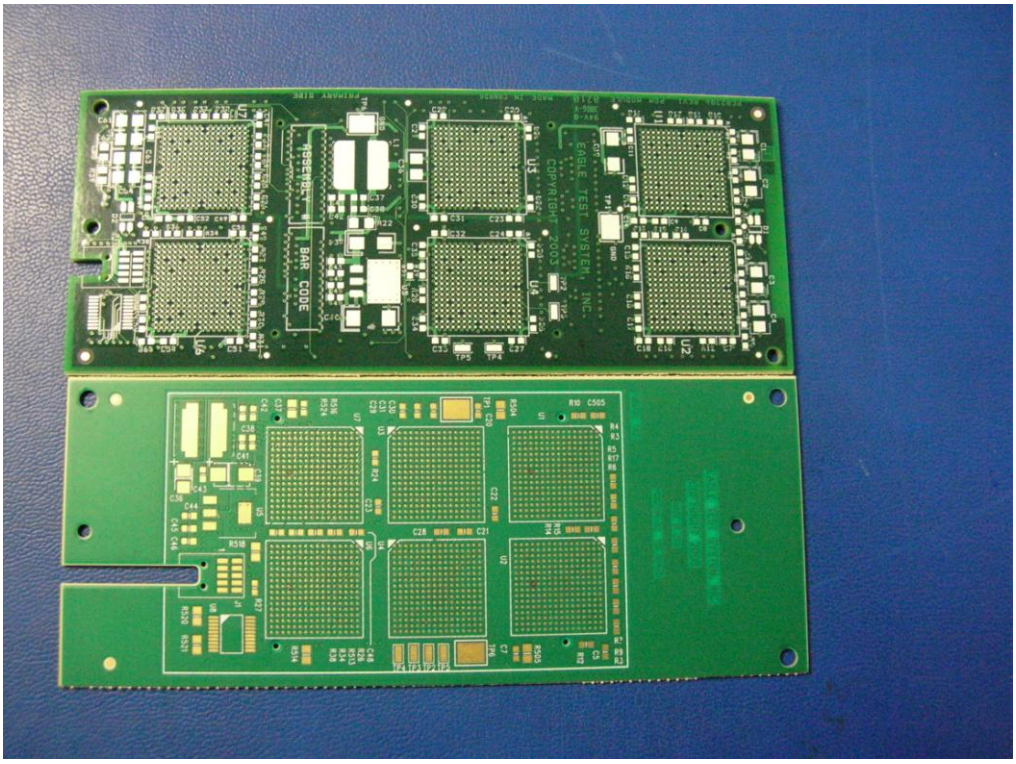
Secondary Side Digital Module-R1 PCB vs. HDI Digital Module-R2 PCB



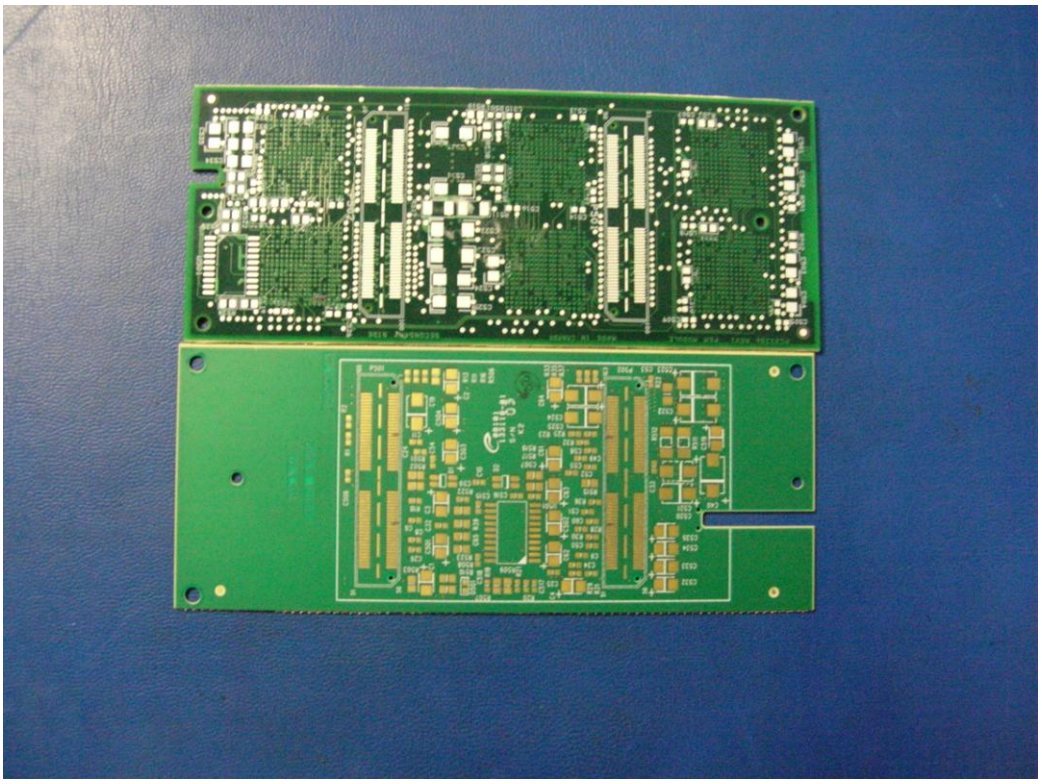
Current Digital Module Assembly vs. HDI Digital Module Bottom Side



Current Digital Module Assembly vs. HDI Digital Module Top Side



Digital Module PCB-R1 & Digital Module-HDI R2 Top Side



Digital Module PCB-R1 & Digital Module HDI-R2 Bottom

Electronics IPC Midwest

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Association Connecting Electronics Industries

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HDI Training & Implementation

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- The design and fabrication process utilized was documented and used to train ETS CAD designers, product development, manufacturing, and test engineers on HDI technologies.

HDI Training & Implementation

- ETS' HDI implementation obstacles:
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  - How does a designer obtain the CAD tools necessary for stack-up, architectures, channel routing, and boulevard routing;
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  - How does one design electrical tests for HDI products

- Training was needed for Eagle Test Systems to overcome implementation obstacles and learn how to quantify the benefits of HDI designs on Eagle Test/Teradyne products

HDI Training & Implementation

Typical HDI Benefits:

- Stable voltage rails
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- Removal of surface layer resistors
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- Much lower RFI/EMI noise and improved shielding
- Closer ground planes
- Closer distributed capacitance
- Minimal stubs
- Surface ground planes with via-in-pads cut emissions
- Lower order of magnitude interconnect electrical parasitic
- Improved power distribution system
- Reduced circuit board size, Improved panelization
- Reduced layer count
- Reduced circuit board thickness

HDI Training & Implementation

Typical HDI Benefits: Continued

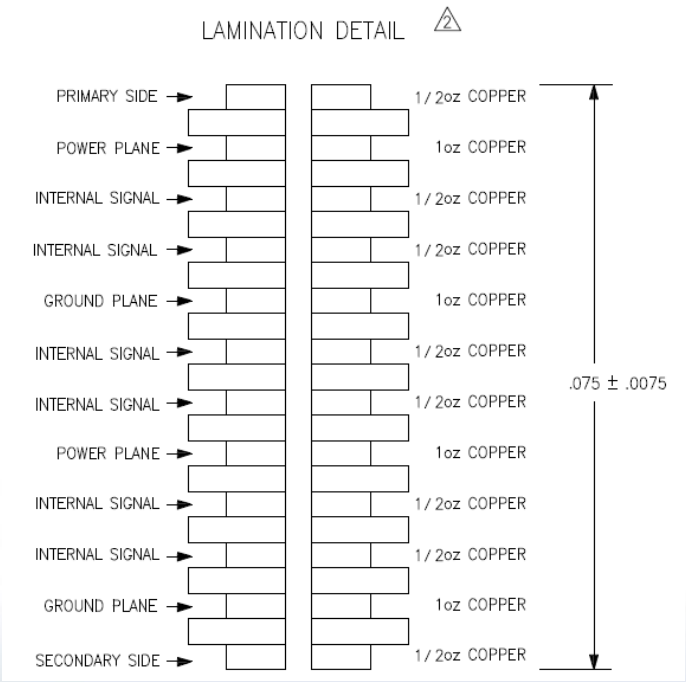
- Reduced layer count
- Reduced circuit board thickness
- Improved reliability due to smaller hole aspect ratios and less solder joints
- Simplified routing due to reduction in traces and vias
- Increased product functionality
- Increased number of PCB boards on a panel
- Lower assembly costs, faster TACT
- Reduced test times

Additional Benefits:

- Products designed using HDI technology typically yield product improvements: >50% more wiring density, >50% reduction of surface mount discrete components, >50% reduction in physical size, >30% thinner boards, lower cost of assembly, lower layer counts, improved electrical performance, and lower overall cost.

HDI Training & Implementation

Design Layout of Existing Digital Module PCB – R1



The existing product is 0.075” thick, 12 layers, with 6 signal layer board that is 11.29 sq in^2. The stack-up and physical design of the current production digital module is shown above.

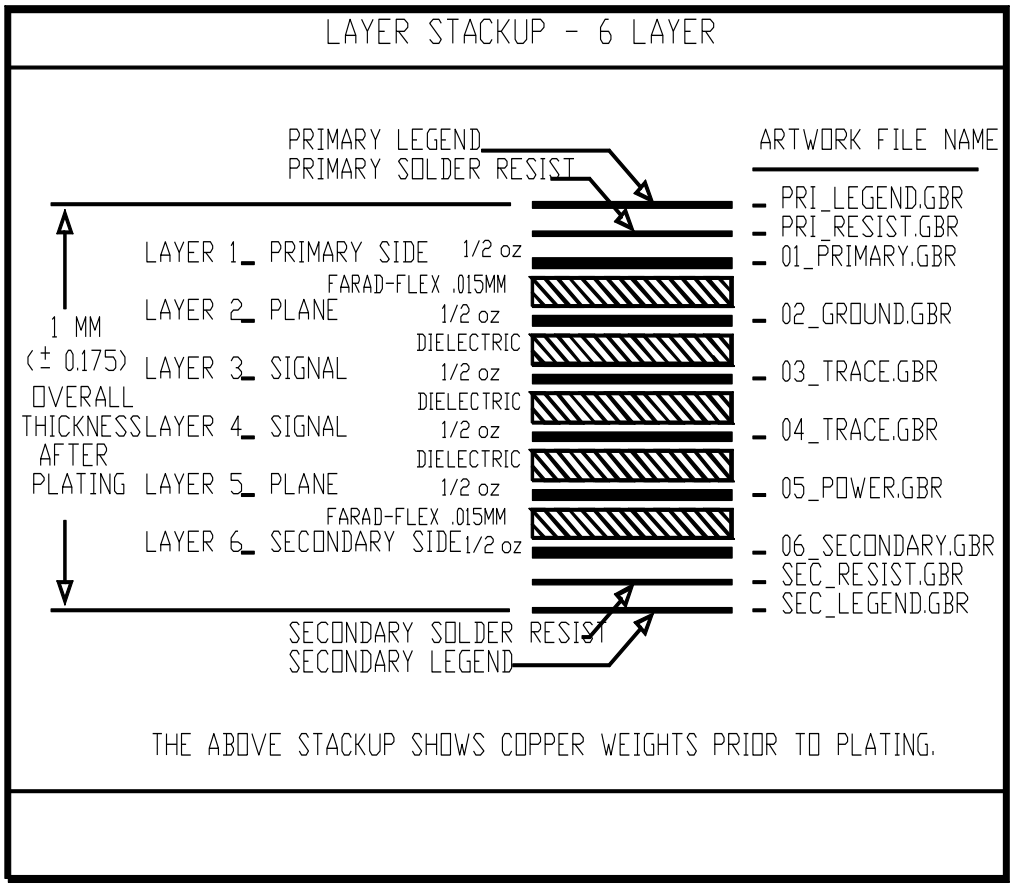
HDI Training & Implementation

Design Layout of HDI Digital Module – R2

- Before starting the design work, a Statement of Work (SOW) was written defining the effort required to plan and execute the redesign of a digital assembly into a test vehicle used for training purposes only.
- The test vehicle was used to emulate product features and performance.
- The test vehicle enables the ETS team to evaluate the effectiveness of Embedded Passive (EP) materials and High Density Interconnect (HDI) technologies in increasing component density, lowering product costs, and improving by-pass decoupling of digital Integrated Circuits (IC).
- DDI redesigned the digital module into an HDI test vehicle to demonstrate the stated benefits of the introduced technologies through the potential increase in functionality and board size reduction.
- HDI technologies including microvias, buried vias, and blind vias were used with embedded capacitance materials to increase routing density and minimize surface layer routing.

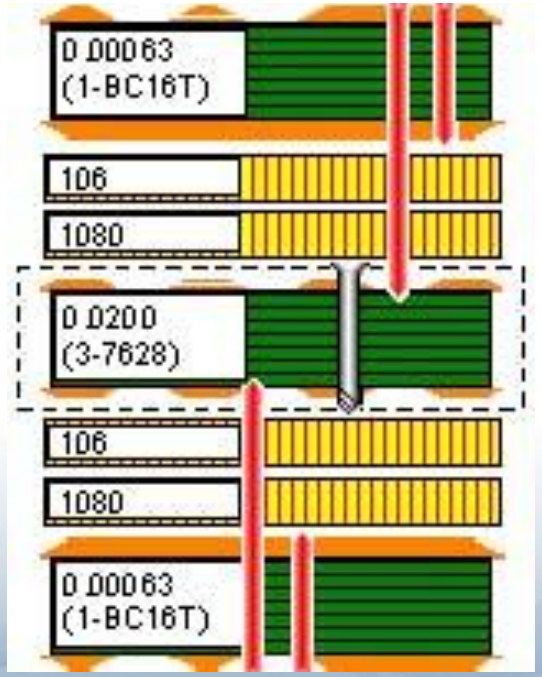
HDI Training & Implementation

New Digital Module-R2



HDI Training & Implementation

Module-R2 Rigid Drill Stack

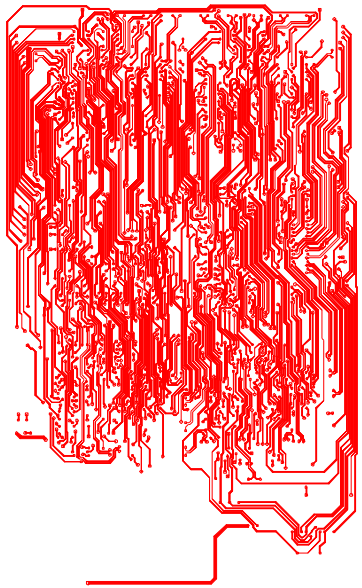


Description

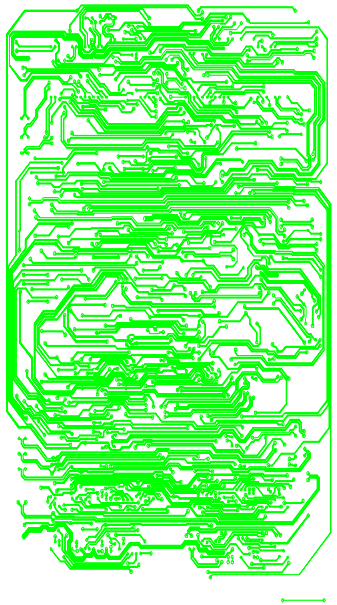
Taiyo 400-MP
½ oz Mix (Std Plt)
BC16T
½ oz P/G
370H
½ oz Sig (Std Plt)
370H
½ oz Sig (Std Plt)
370H
½ oz P/G
BC16T
½ oz Mix (Std Plt)
Taiyo 4000-MP

HDI Training & Implementation

HDI Reduced Signal Layers from 6 to 2



Digital Module-R2 Layer 3



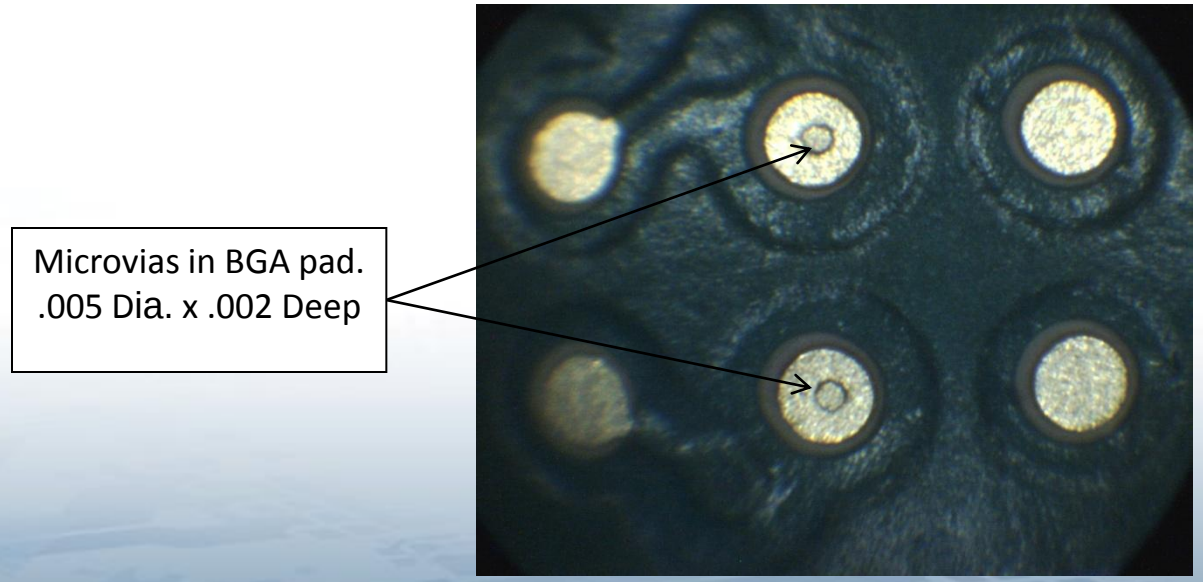
Digital Module-R2 Layer 4

The new design is 0.040” thick, 6 layers, with 2 signal layer board that is 6.24 in^2.

HDI Training & Implementation

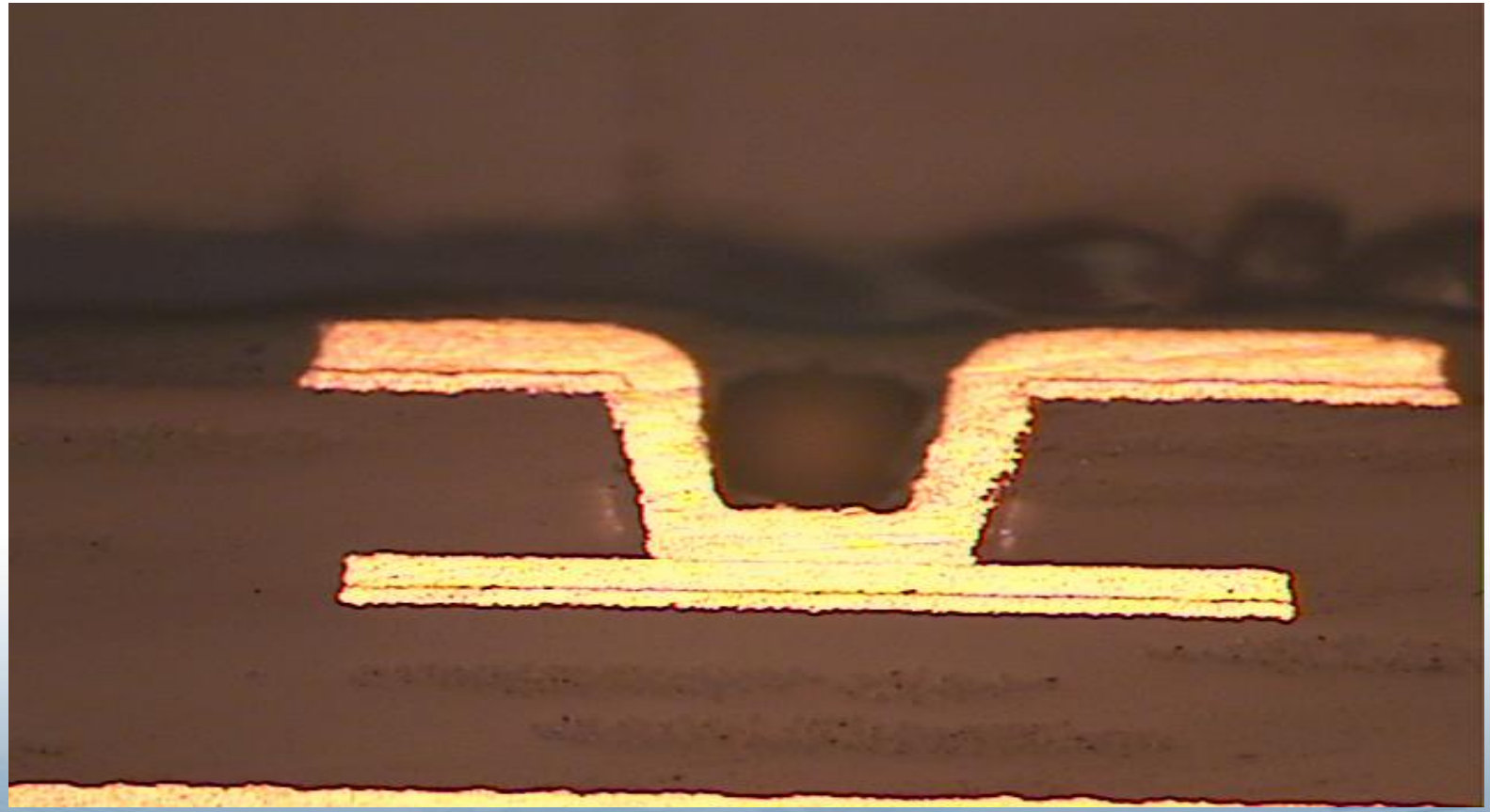
Several technologies were used to create the HDI design

- In addition to build-up and sequential build-up of the drilled laminates, the combination of microvias, blind, and buried vias was used
- Microvias are < 6 mil laser drilled vias that can have aspect ratios of 9.5 to 1 (drilled hole diameter to laminate thickness)



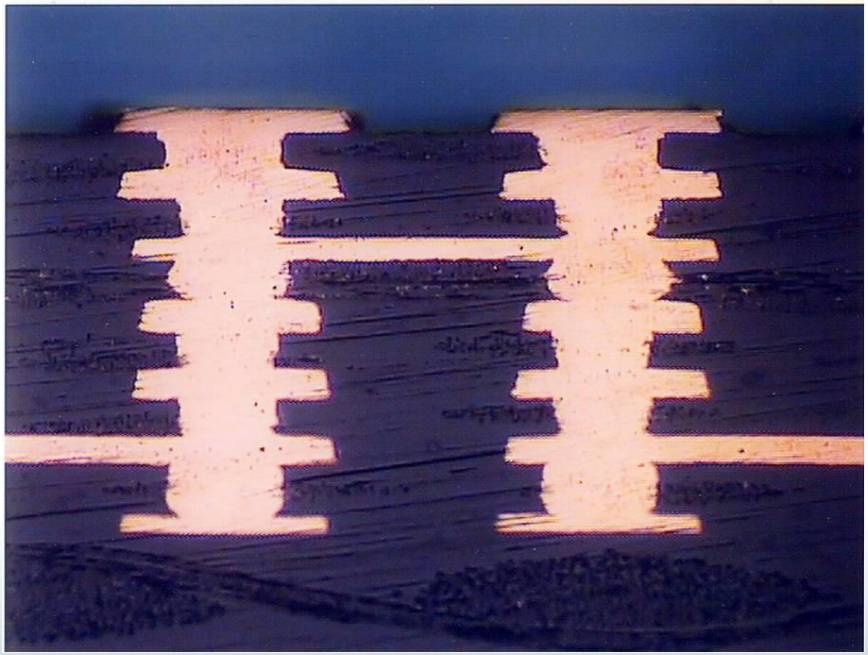
HDI Training & Implementation

Laser Drilled µvias

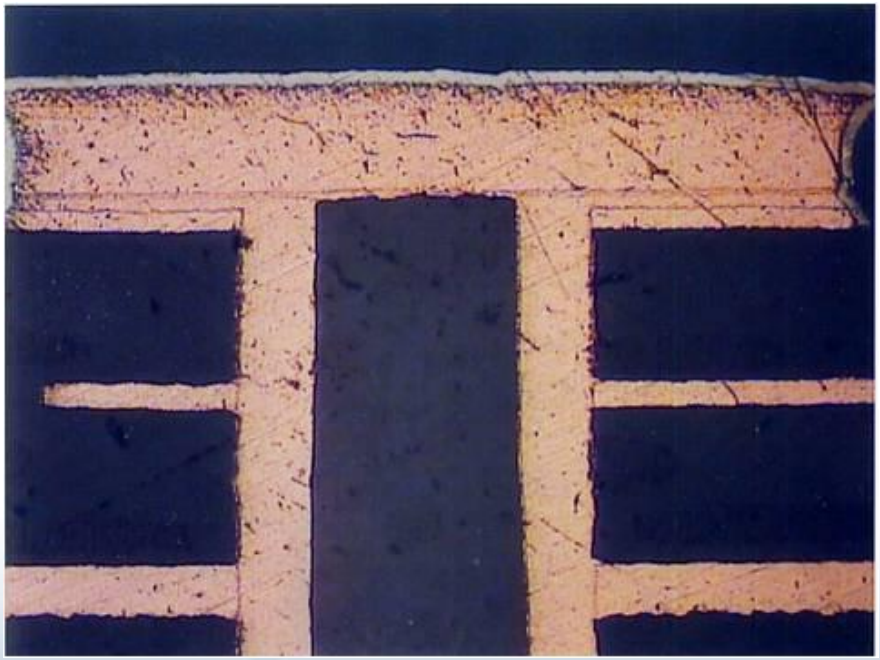


HDI Training & Implementation

Cu Filled µvias

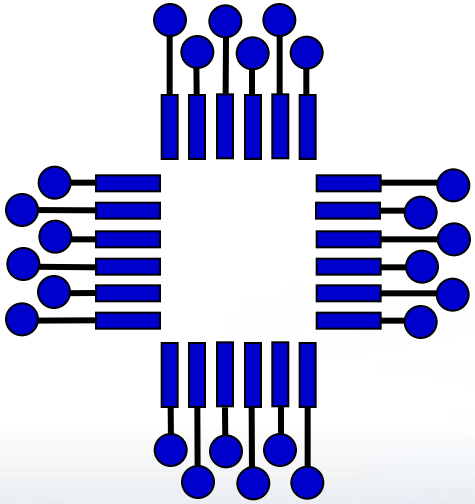


Epoxy Filled µvias

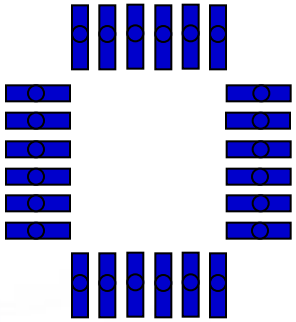


HDI Training & Implementation

Conventional Technology

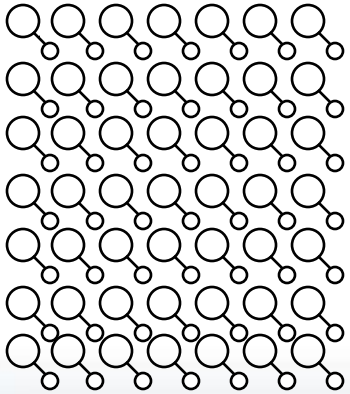


Via-in-Pad Technology

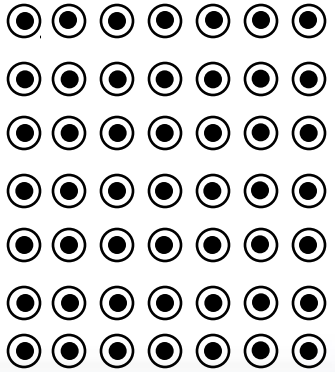


QFP Land Pattern

Conventional Technology



Via-in-Pad Technology



BGA Land Pattern

HDI Training & Implementation

The HDI design incorporates Embedded Capacitance (EC)

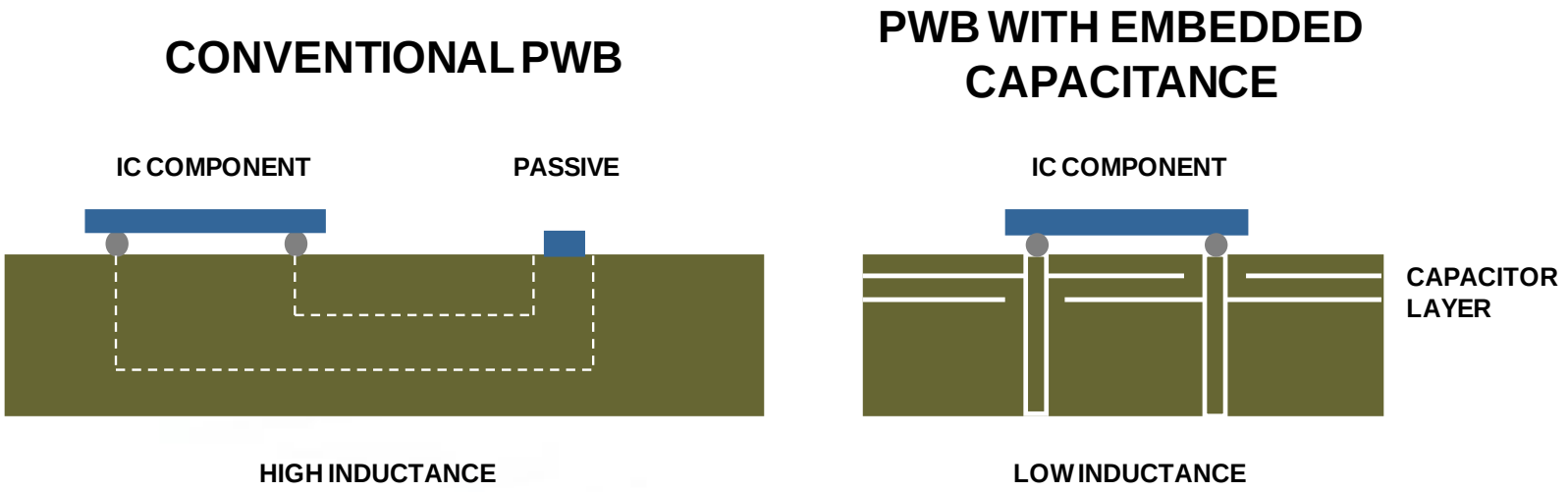
- EC technology, in the form of Oak-Mitsui *Faradflex* material.

- *Faradflex* is an ultra-thin dielectric material used to reduce the overall impedance of power distribution systems and free up surface real estate by reducing the number of necessary discrete decoupling and bypass surface mount capacitors.

- BC16 variety of *Faradflex* was selected in this case for its capacitance value of (250 pF/cm^2 @ 1 MHz) and relative cost effectiveness compared to other varieties.

- Reducing the physical size of a PCB is enabled by the combination of microvias that reduce drilled holes and EC which reduces surface capacitors.

HDI Training & Implementation



- Remove the surface capacitors and re-route through the capacitive layers.
- Always “on”.

HDI Training & Implementation

Testing

- The design of the HDI digital module allowed functional testing using assembly Diagnostics and Calibration software.

- The HDI artwork was placed into the current digital module form factor to show physical size reduction and to allow electrical and mechanical connections with existing product motherboard.

- Based on the validation performed, it can be concluded that the prototype digital module built using HDI technology (reduced PCB layer count and reduced number of bypass capacitors) performs as well as the production module.

- Multiple laps of cal/check were run on a tester with a known good product board, using original digital modules as baseline measurements.

HDI Training & Implementation

- **High Level Assembly Testing**

CALIBRATION REPORT – Original Digital Module

Time: 0.8 hrs Laps: 8

BOARD	PIN POS	S/N	STATUS	WORST			
				CPK	PLOT	TEST	
Product	0	2821	PASS	1.06	3982	Product-0 Extend Bit Pin8, Tg5	
				1.75	3393	Product-0 BitWt FD2 Pin8, Tg6	
				1.78	3990	Product-0 Extend Bit Pin9, Tg5	
				1.79	3375	Product-0 BitWt FD2 Pin8, Tg4	
				1.82	3466	Product-0 BitWt FD3 Pin9, Tg6	

HDI Training & Implementation

- **High Level Assembly Testing**

CALIBRATION REPORT – New Digital Module

Time: 1.1 hrs Laps: 10

BOARD	PIN POS	S/N	STATUS	WORST			
				CPK	PLOT	TEST	
Product	0	2821	PASS	1.11	4172	Product-0 DRV Deskew Pin12, TG5	
				1.61	3339	Product-0 BitWt FD2 Pin8, Tg0	
				1.63	3356	Product-0 BitWt FD1 Pin8, Tg2	
				1.72	3340	Product-0 BitWt FD3 Pin8, Tg0	
				1.79	3366	Product-0 BitWt FD2 Pin8, Tg3	

HDI Training & Implementation

Training

- Training was provided by a DDI FEA at the ETS facility for 6 hours. Attendees included Hardware Engineers, PCB Designers, Manufacturing Engineers, and Test Engineers.

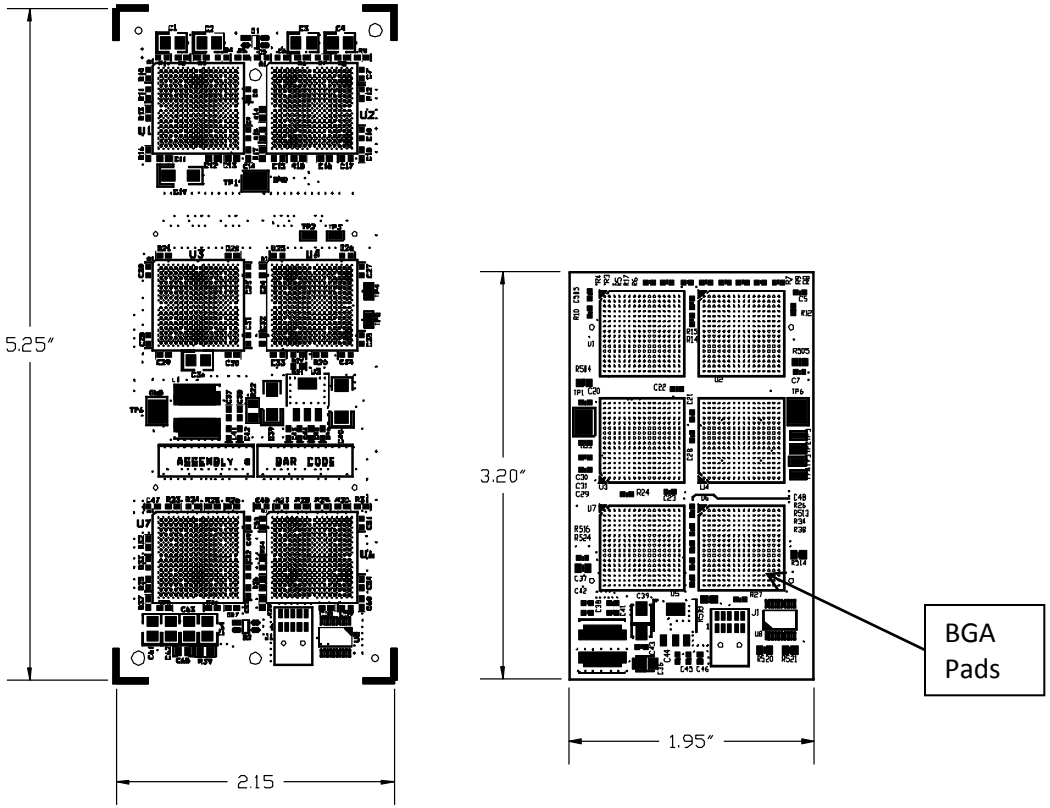
- ETS designers and engineers were trained in the proper design of planar embedded capacitors and microvias using PADS 2007.1.

- These techniques were illustrated through a review of the HDI module test vehicle redesign performed by the DDI design team.

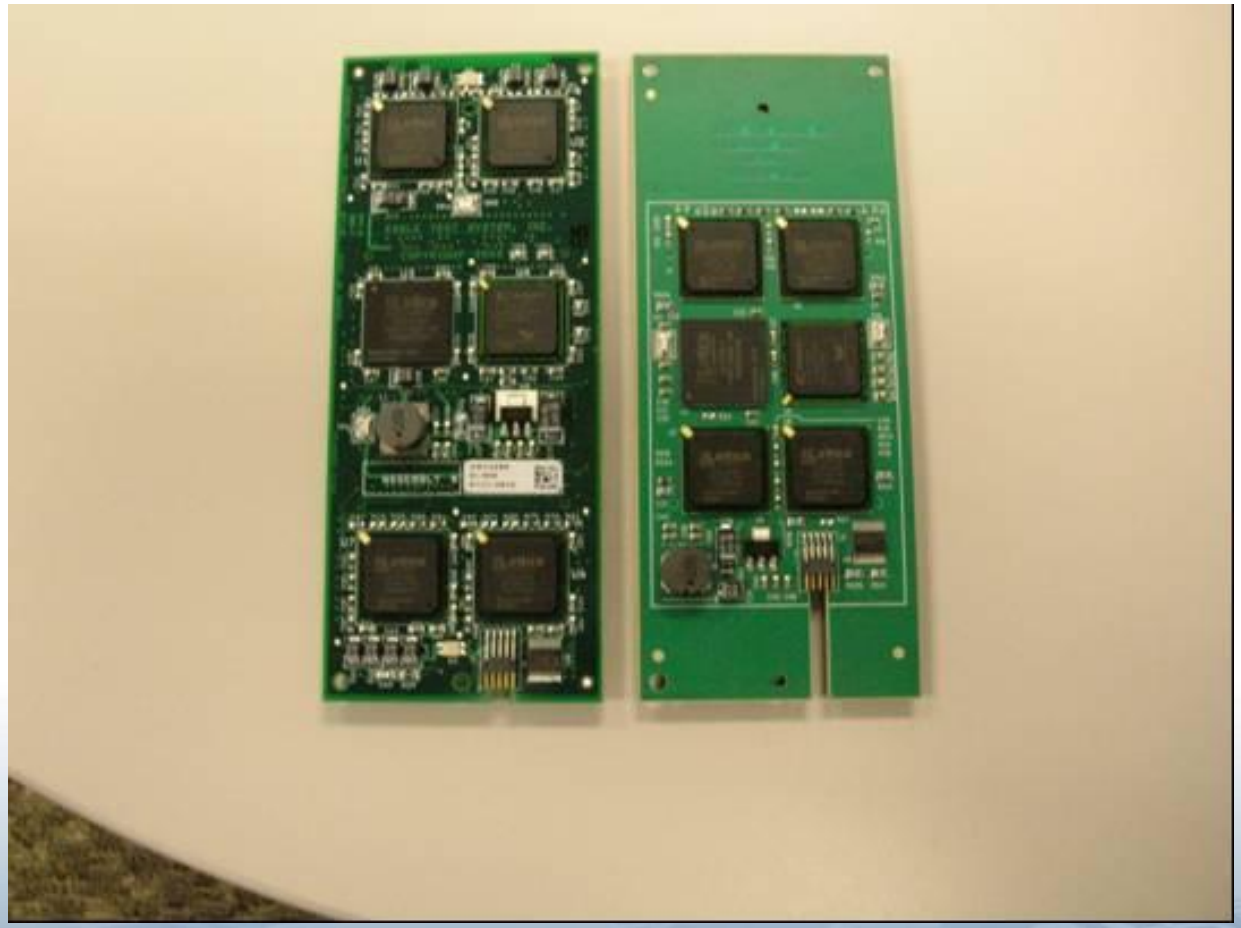
- Only one prototype run of the HDI assembly test vehicle was assembled. A total of five modules were assembled using the current digital module BOM.

HDI Training & Implementation

Current Digital Module-R1 PCB vs. HDI Digital Module-R2 PCB



HDI Training & Implementation



Current Digital Module Assembly vs. HDI Digital Module Top Side

HDI Training & Implementation at Eagle Test Systems - A Teradyne Co.

Benefit Estimate of Digital Module Board Conversion to HDI				
Benefit Area	**Current PCB Design**	**HDI Design***	**Savings Description**	**Costs**
BI-Pass Capacitor Reduction	72	47	Material Savings	$ (0.50)
			Annual OH cost savings of carrying 3 unique P/Ns for bi-pass Caps	$ (150.00)
			Assembly Cost per Placement	$ (1.25)
Mechanical Drilled Via Reduction	2149 Drilled Vias	133 Drilled Vias	1/2 hour drill time duration; < 15 minutes for 2-up to < 2 minutes for laser drill	
Laser Drilled Via Reduction	0 Laser Vias	1788 laser vias	1/2 hour drill time duration; < 15 minutes for 2-up to < 2 minutes for laser & mechanical drill	
Layer Count Reduction	12L	6L	50% decrease in layer count; while increase in wiring density due to via hole reduction	
Test Pad Reduction	418	0	Surface Area Savings	
Board Area Reduction - Sq. Inch	11.29	6.24	Board area reduction of 44%	
	(5.25" x 2.15")	(3.20" x 1.95")	Due to: Mechanical drilled hole reduction, via-in-pad, discrete part removal, removal of signal, PWR, GND, traces from surfaces, moving parts closer together and reduction of test pads.	
Board Thickness	.075"	.040"	Board can be made thinner with less layers	
Board Cost	$34.00	$50.00	50% Less layers/44% Smaller Board. Cost increase comes from 2 Embedded Capacitance (EC) layers.	$ 16
Assembly Cost	$388.91	$383.56	EMS Partner	$ (5)
Estimated Total Per Board Savings				**$ (9)**