IPC Electronics Midwest 2010

To Void or Not To Void - That Is the Question

David Hillman

Rockwell Collins

Biography:

Metallurgical Engineer in the Advanced Operations Engineering Department

Mr. Hillman graduated from Iowa State University with a B.S. (1984) and M.S. (2001) in Material Science & Engineering. In his present assignment he serves as a consultant to manufacturing on material and processing problems. He served as a Subject Matter Expert (SME) for the Lead-free Manhattan Project in 2009. He has published numerous technical papers with the 2008 SMTA International Conference on Soldering & Reliability being selected as "Best of Conference". In 2008 he was the recipient of the SMTA "Member of Technical Distinction" Award. Mr. Hillman was awarded the Da Vinci medal as a Rockwell Engineer of the Year for 1994. He serves as the Chairman of the IPC JSTD-002 Solderability committee. Mr. Hillman served as a Metallurgical Engineer at the Convair Division of General Dynamics with responsibility in material testing and failure analysis prior to joining Rockwell. He serves as a member of the SMTA Journal and Soldering & Surface Mount Technology Journal Technical Paper Review committees. He is a member of the American Society for Metals (ASM), the Minerals, Metals & Materials Society (TMS), and Surface Mount Technology Association (SMTA) and the Institute for Interconnecting and Packaging of Electronic Circuits (IPC).

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Bev Christian, Ph.D.

Research in Motion Limited

Biography:

Bev Christian has been at Research In Motion for the past 10 years where he is currently the Director of Materials Interconnect Research. He previously ran a materials lab at Nortel in Belleville, Ontario and received several awards for his environmental work, including three President's Awards. His specific areas of interest include solderability, lead free solders, environmental issues and contamination. He is a member of ASM, SMTA, and sits on various IPC standards committees. Dr. Christian has been named a Member of Technical Distinction of the SMTA.

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Void or Not to Void

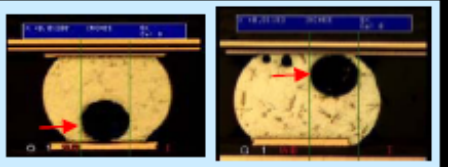
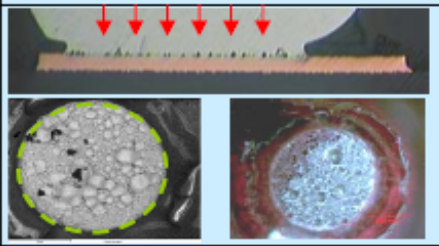
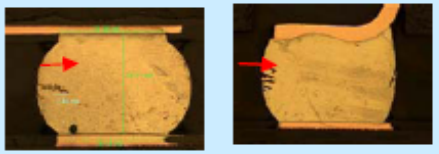
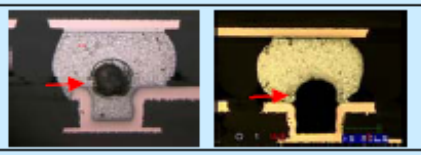
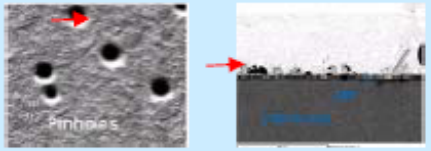
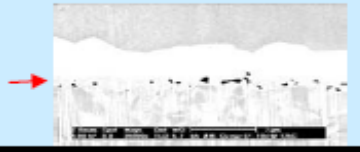
D. Hillman and B. Christian
Rockwell Collins and Research In Motion

IPC Midwest Conference 2010

Agenda

- Background
- Let's Make a Void (or Not)
- Let's Make a Void (or Not) 5 Years Later
- Future Work
- Conclusions

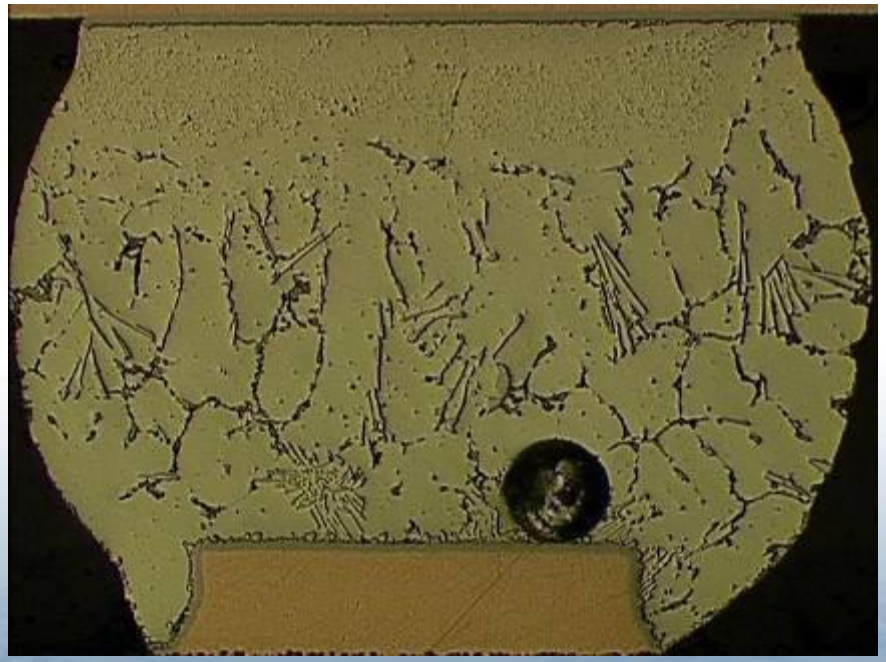
Background: What is a void?

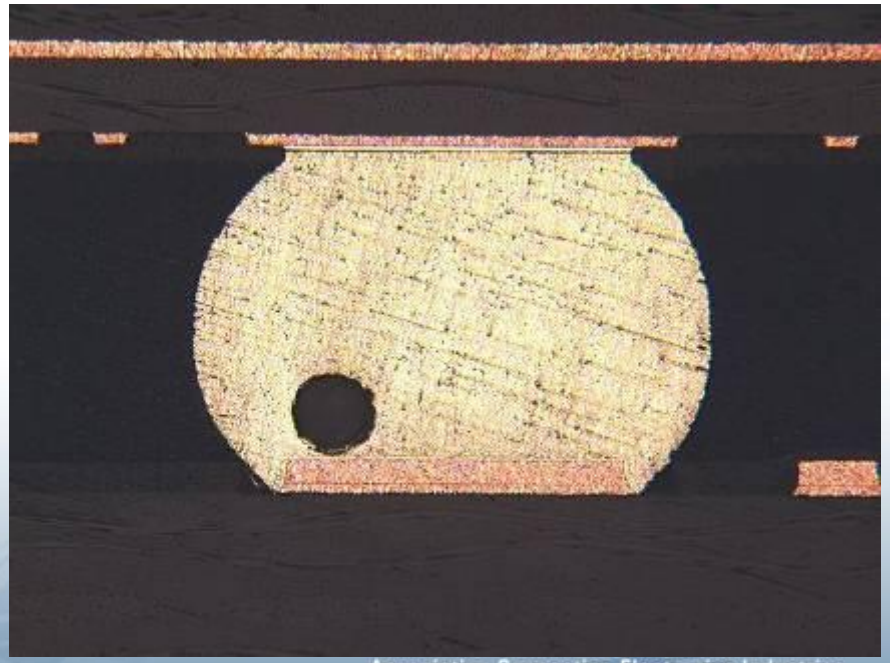
Type of Voids	Description	Photos
Macro Voids	Voids generated by the evolution of volatile ingredients of the fluxes within the solder paste; typically 4 to 12 mils (100 to 300 µm) in diameter, these are usually found anywhere in the solder joint; IPC's 25% max area spec requirement is targeted toward process voids; NOT unique to LF solder joints. Sometimes referred to as "Process" voids	
Planar Micro Voids	Voids smaller than 1 mil (25 µm) in diameter, generally found at the solder to land interfaces in one plane; though recent occurrence on Immersion Silver surface finish has been highlighted these voids are also seen on ENIG and OSP surface finishes; cause is believed to be due to anomalies in the surface finish application process but root cause has not been unequivocally determined. Also called "champagne" voids	
Shrinkage Voids	Though not technically voids, these are linear cracks, with rough, `dendritic` edges emanating from the surface of the solder joints; caused by the solidification sequence of SAC solders and hence, unique to LF solder joints; also called sink holes and hot tears	
Micro-Via Voids	4 mil (100 µm) and more in diameter caused by microvias in lands; these voids are excluded from 25% by area IPC spec; NOT unique to LF solder joints	
Pinhole Voids	Micron sized voids located in the copper of PCB lands but also visible through the surface finish; Generated by excursions in the copper plating process at the board suppliers	
Kirkendall Voids	Sub-micron voids located between the IMC and the Copper Land; Growth occurs at High Temperatures; Caused by Difference in Inter-diffusion rate between Cu and Sn. Also Known as "Horsting" Voids.	

Graphic Courtesy of Raiyo Aspandiar, Intel

What is a “macro” void?

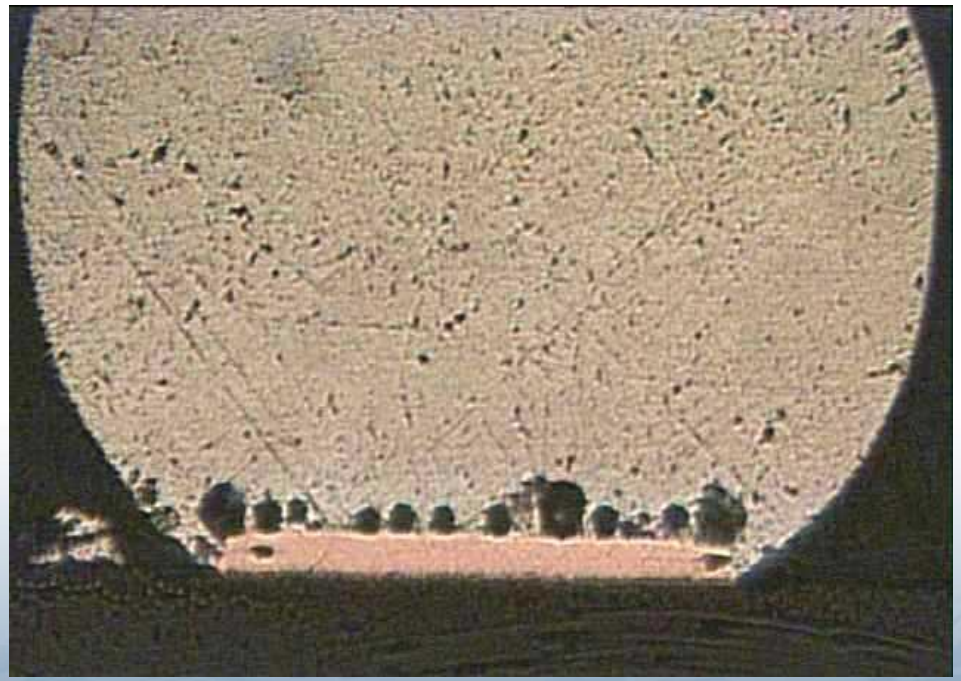
- Also named “process” voids
- Macro voids typically have a volatile flux content evolution root cause

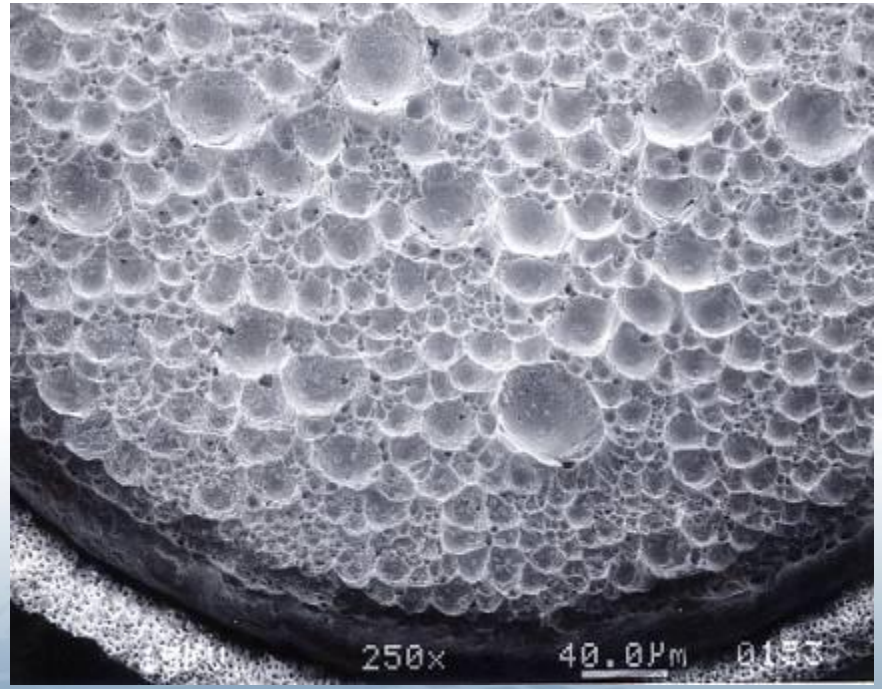




What is a “planar” void?

- Also named “champagne” voids
- Planar voids typically have an incorrect plating process root cause

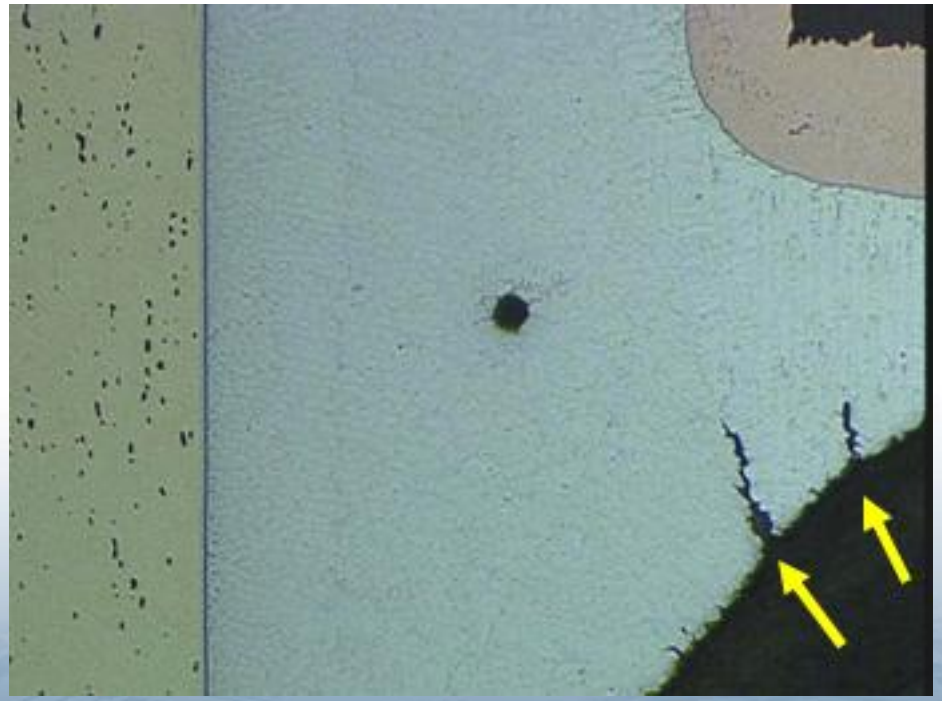


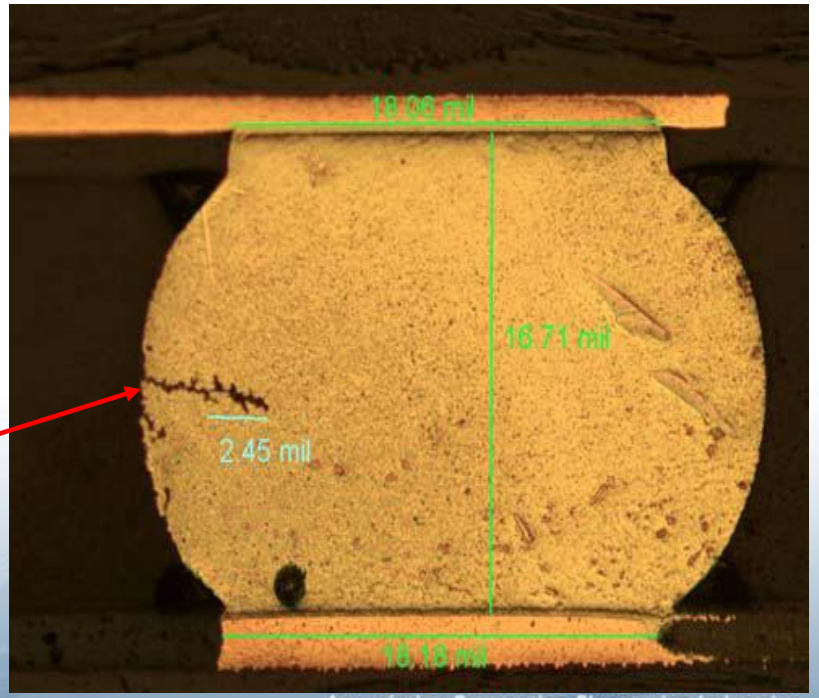


Photos Courtesy of Don Cullen, MacDermid

What is a “shrinkage” void?

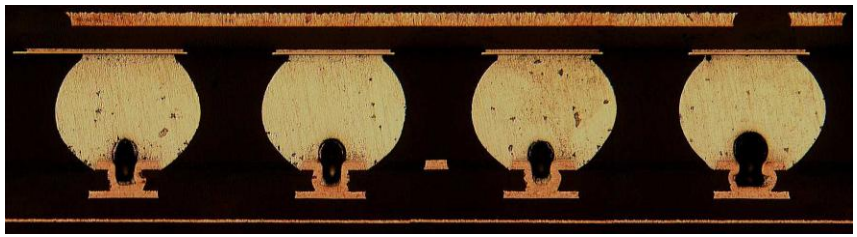
- Also named “hot tear” voids
- Shrinkage voids have a solder alloy solidification root cause

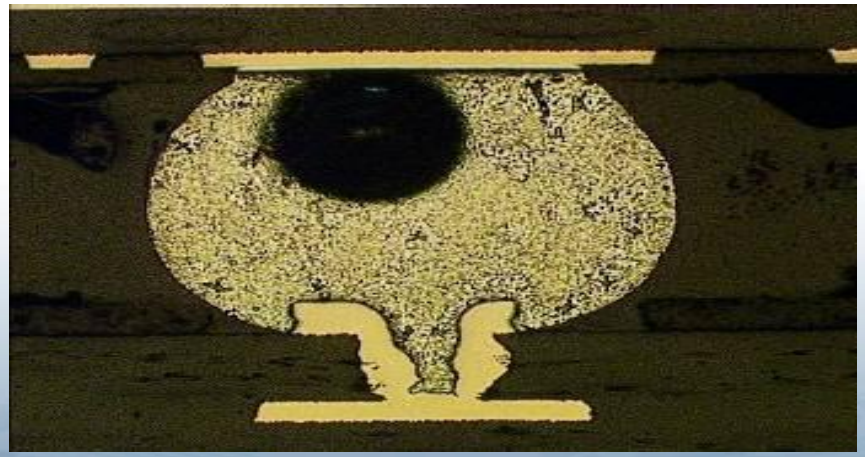


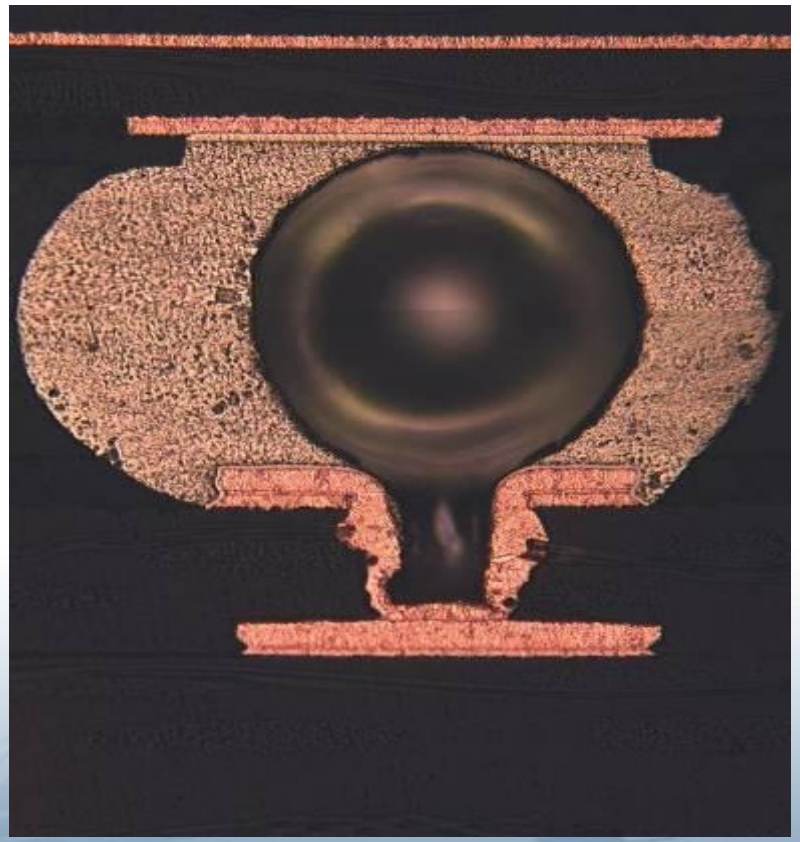


What is a “microvia” void?

- Microvia voids typically have a volatile flux content evolution/microvia interaction root cause

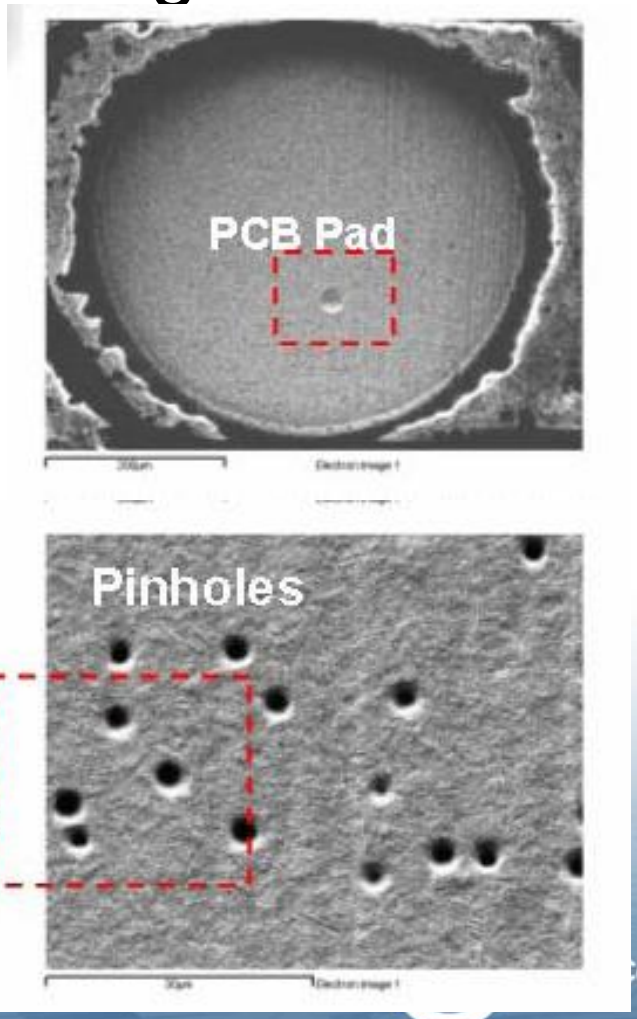


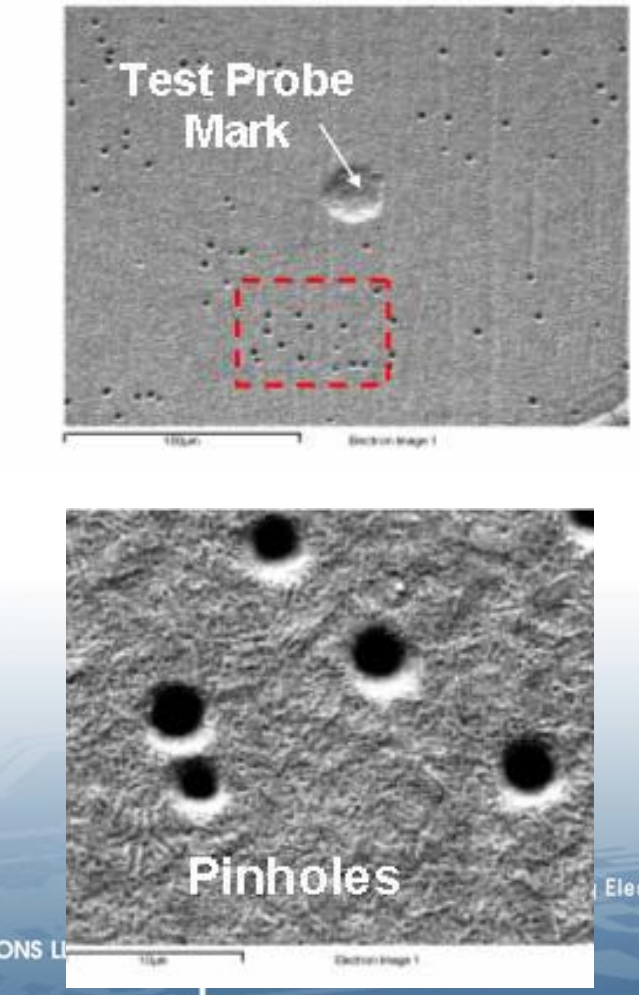




What is a “pinhole” void?

- Pinhole voids typically have a incorrect plating root cause

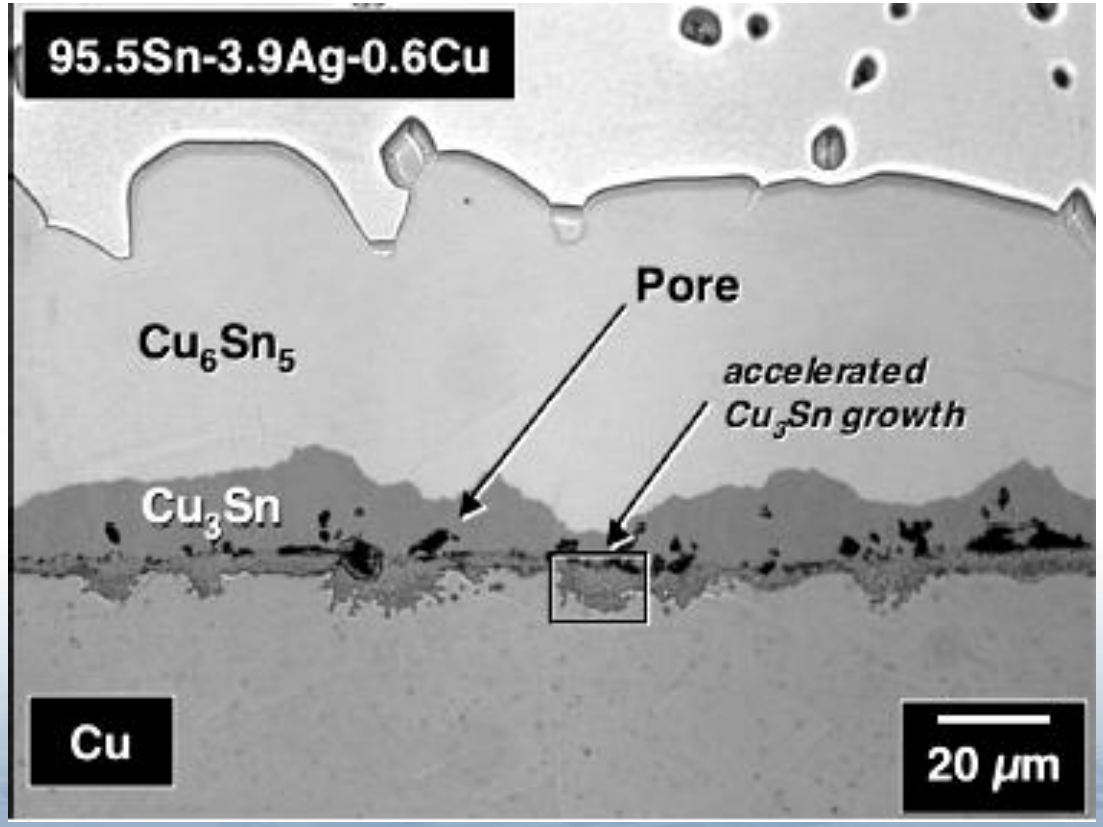




Graphic Courtesy of Raiyo Aspandiar, Intel

What is a “Kirkendall” void?

- Kirkendall voids typically have a solder diffusion root cause – very controversial topic



Graphic from Vianco reference: P. Vianco et al, “Solid State Intermetallic Compound Layer Growth Between Copper and 95.5Sn-3.9Ag-0.6Cu Solder”, Journal of Electronic Materials, Vol. 33, No. 9, 2004.

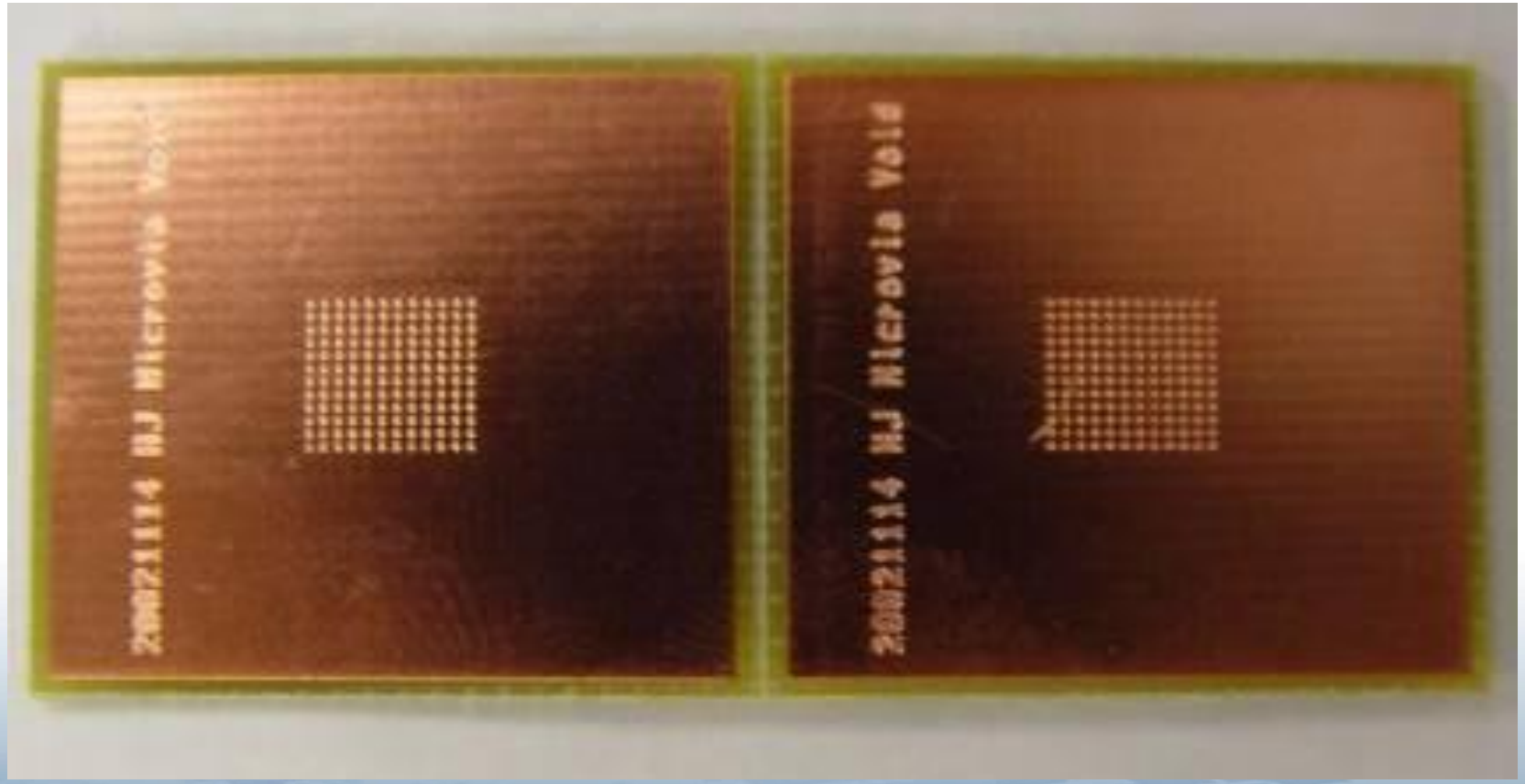
Macro voids: Good or Bad?

- Some say small macro voids are good – because they are crack arrestors
- Most believe that large voids in the middle of a solder joints are not a problem – unless they are HUGE
- Most would agree that the larger a void is in the areas where the solder joint necks down, the worse it is

Is it possible to make voids on demand? (Let's Make a Void (or Not)

- Several studies have been carried out to look at the effect of voiding on solder joint reliability.
- In several the amount of voiding has actually been quite small – voids < 10% of the joint area. This must be quite frustrating to the researchers – voids when you don't want them in production and then not there when you want to do research on them!

Dr. Ning Chen Lee's Void Test Board

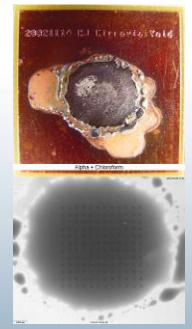


Solvents added to solder paste

- carbon disulfide (b.p. 46˚ C)
- acetone (56.06˚ C)
- chloroform (b.p. 61.1˚ C)
- tetrahydrofuran (b.p. 65˚ C)
- n-hexane (b.p. 68.7˚ C)
- ethyl acetate (b.p. 71.11˚ C)
- water (b.p. 100 ˚ C)
- m-xylene (b.p. 139 ˚ C)
- glycerol (b.p. 290 ˚ C)

Results?

- **Nothing significant!**
- **None with chloroform ☹**
- **Addition of solvents in various concentration did not lead to production of significant voiding**
- **Carbon disulfide (b.p. 46˚ C)**
- **Chloroform (b.p. 61.1˚ C)**
- **No solvent added**



Let's Make a Void (or Not) 5 Years Later

- **Background II – Current IPC JSTD 001 Specification Requirement:**

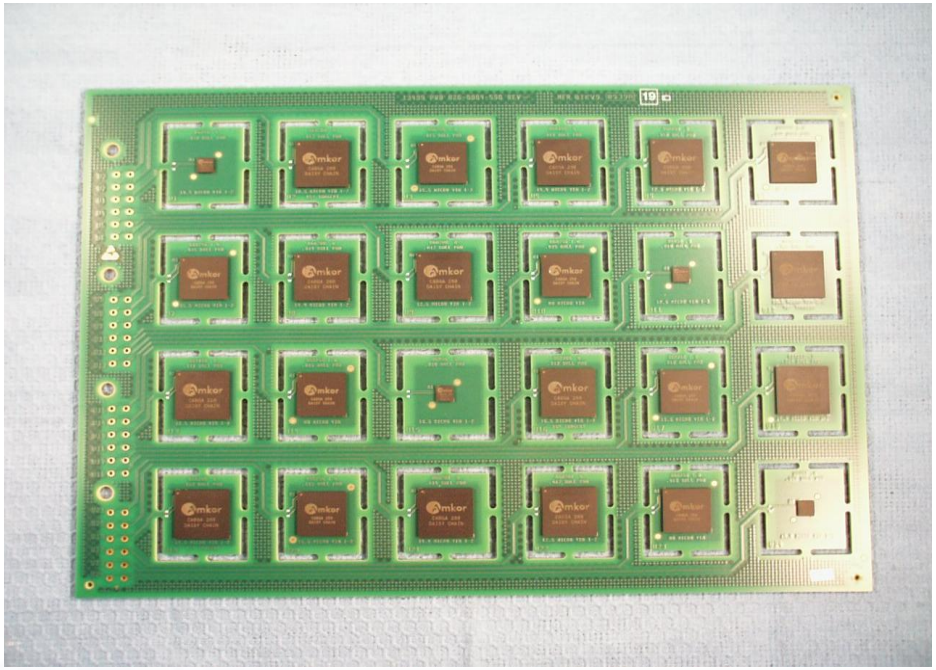
"25% or Less of ball X-ray Image Area"

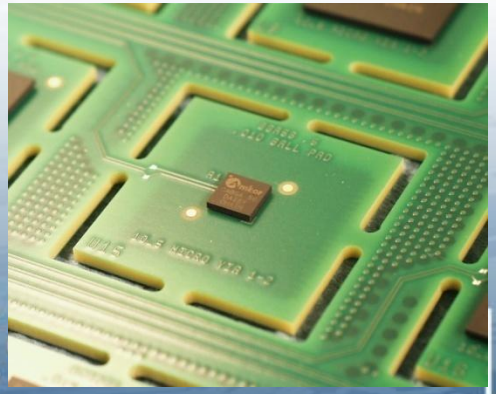
- **The Requirement was Not "Made Up"!**
  - **Data Submitted to JSTD-001 Committee for Field Data for Class 3 Airborne Flight Critical Product – All Inspected per 25% Requirement**
- **But – Technology Has Changed! Time for a New Investigation**

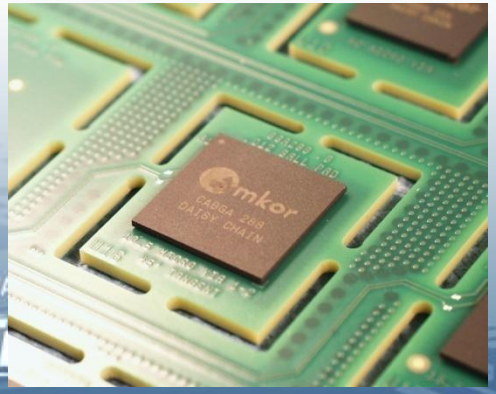
Let's Make a Void (or Not) 5 Years Later

Test Vehicle:

- 0.5mm 56 I/O BGA
- 0.8mm 288 I/O BGA
- 1.0mm 256 I/O BGA
- Type 1 Micro Vias in Pads with 4 Pad Sizes
- 16 Layer, 0.086" thick, ENIG PWB







Let's Make a Void (or Not) 5 Years Later

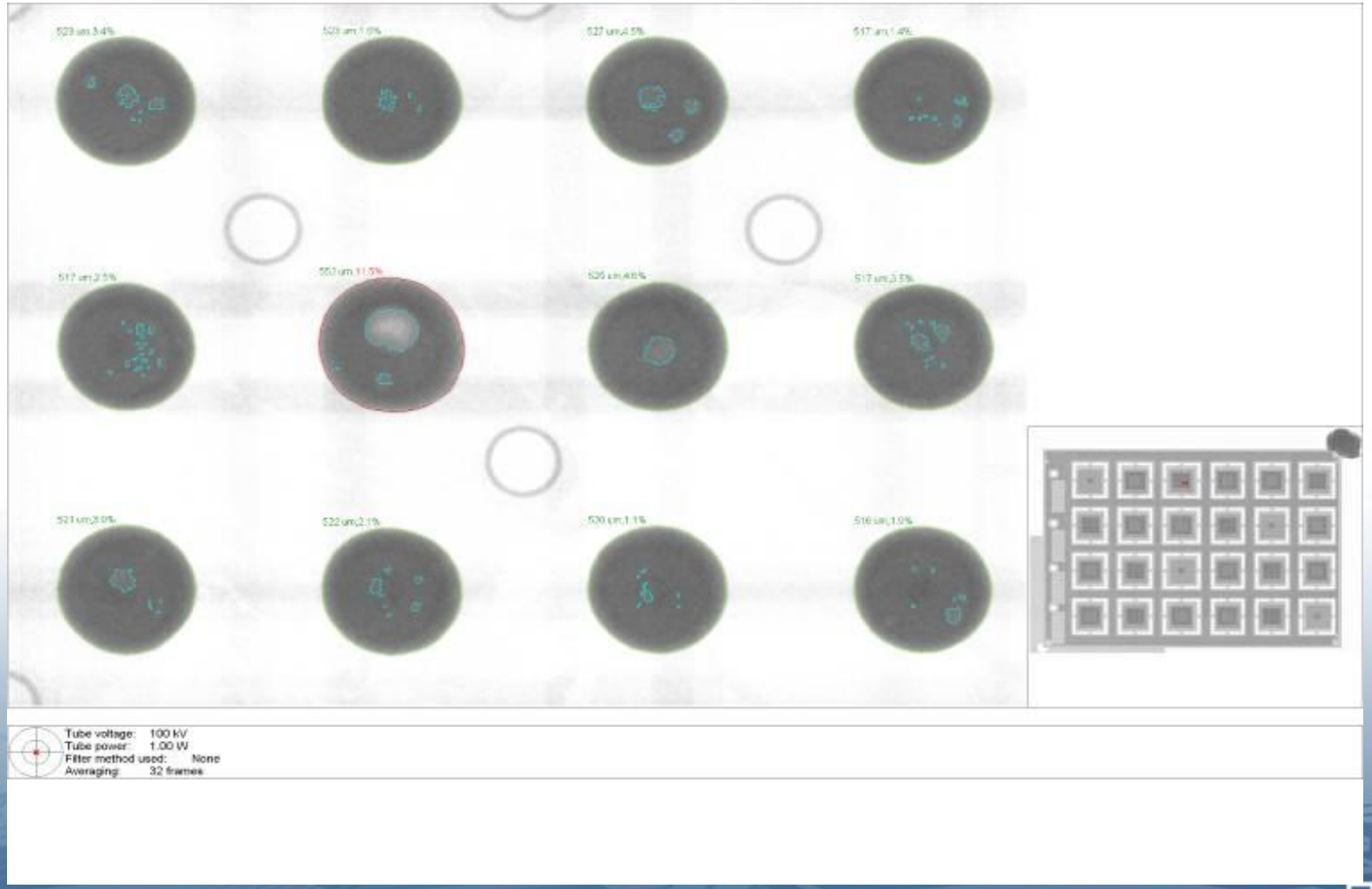
- Process Trial:
  - 40 Test Vehicles Total
  - Total Number of Solder Joints: 229,120
  - Total Number of Voids Exceeding the JSTD-001 Requirement:

10! (aka ten)=0.004%

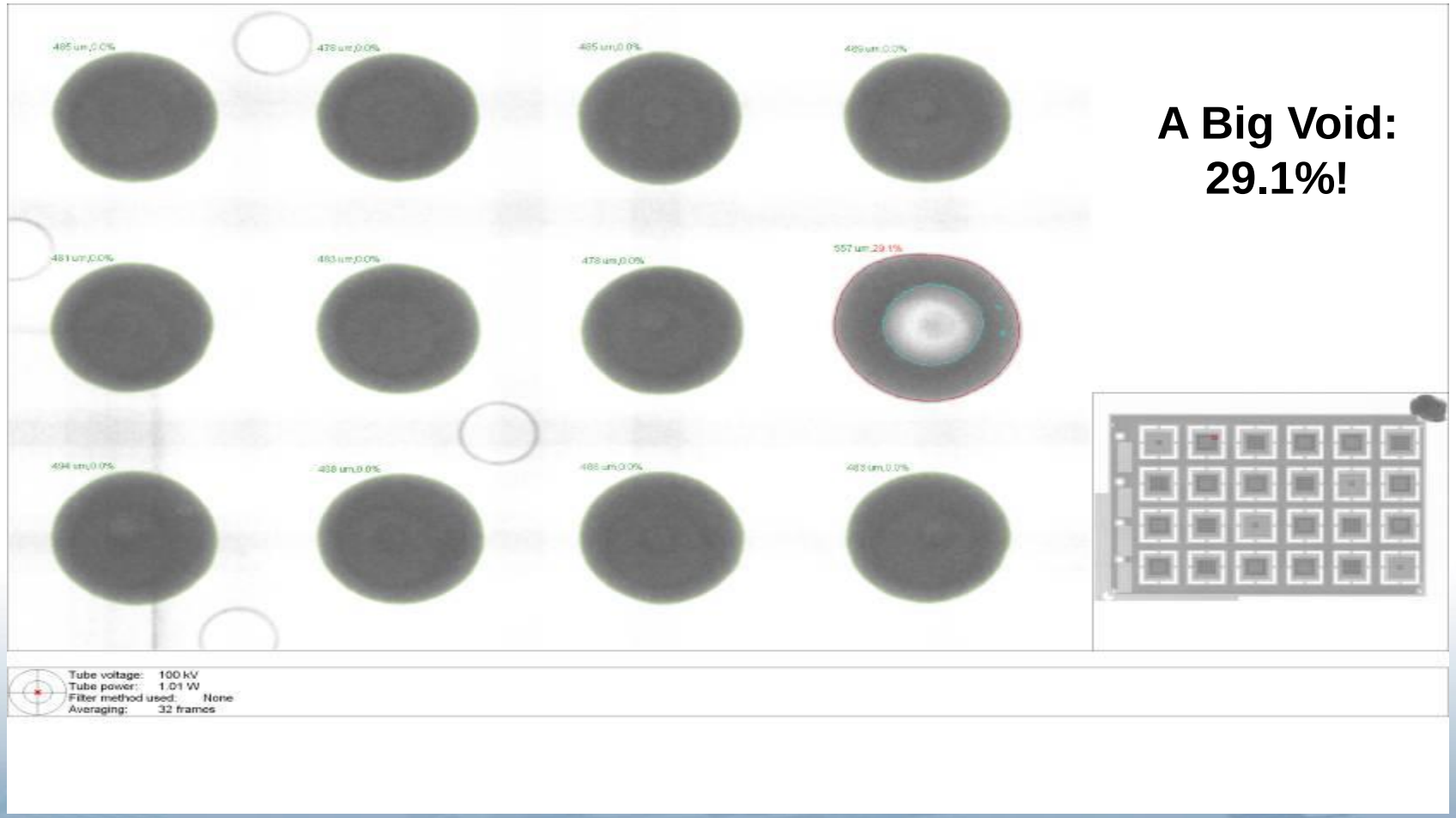
Let's Make a Void (or Not) 5 Years Later

- Collaborative Effort with Dr. David Bernard of Nordson DAGE:

Average Void: 1%-5%



Let's Make a Void (or Not) 5 Years Later



Let's Make a Void (or Not) 5 Years Later

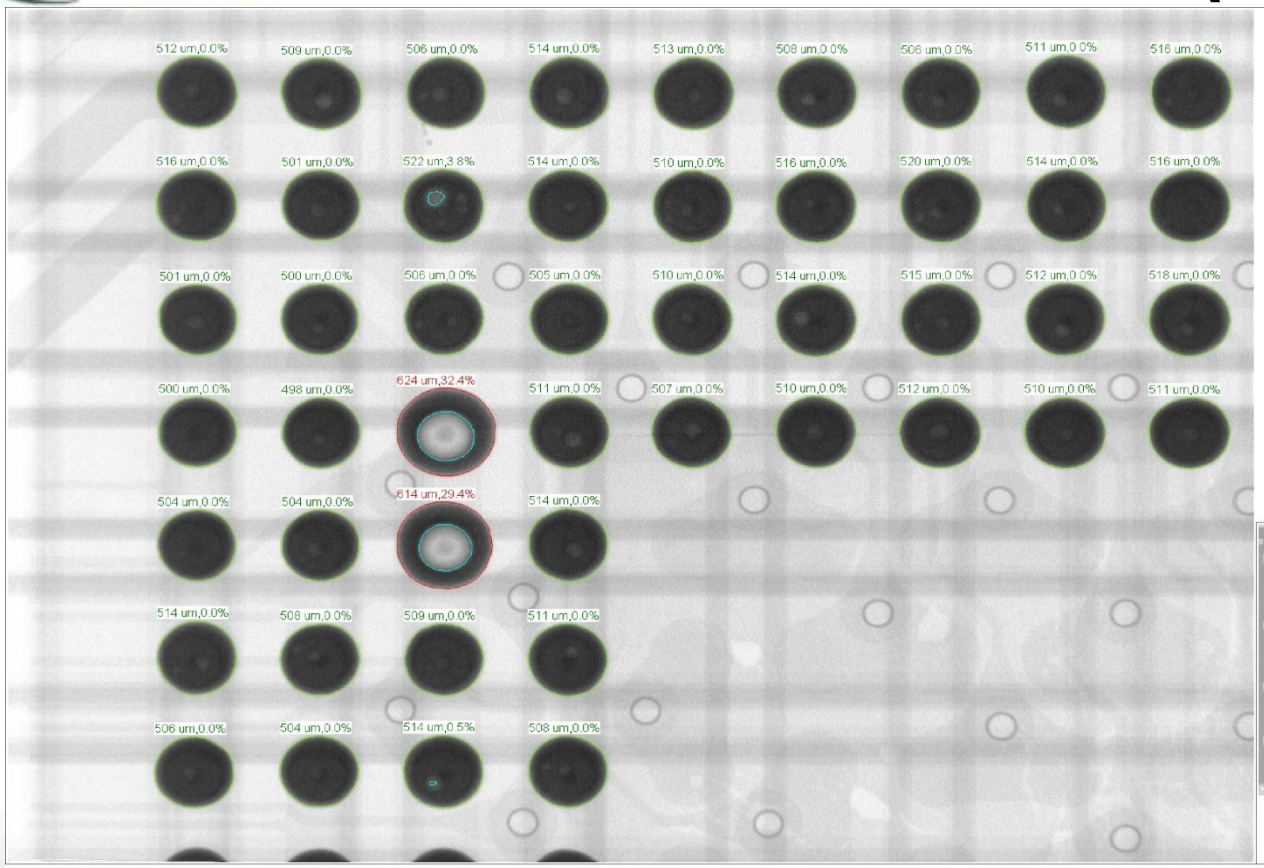
- Ok, We Need Some Help – Let's Ask TechNet!
- A Few of the "Suggestions":
  - Use a Water Soluble Solder Paste
  - Print Test Vehicle and Let Sit for 30 Minutes
  - Misprint and Clean
  - Extend Time Above Liquidus (TAL)
  - Contaminate the Pads (huge choice selection)
  - Turn off the Nitrogen Atmosphere
  - Pressure Cook the Test Vehicles Before Trial
  - Shorten Preheat and High Peak Temperature

Let's Make a Void (or Not) 5 Years Later

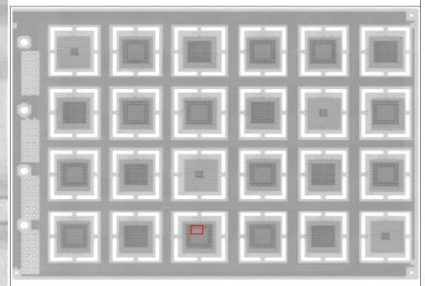
- New Trial Run – 15 Test Vehicles
- What We Changed:
  - Used a Water Soluble Solder Paste
  - Turned off the Nitrogen Atmosphere
  - Increased Reflow Oven Belt Speed
  - Increased Peak Reflow Temperature

- The Results……..

Let's Make a Void (or Not) 5



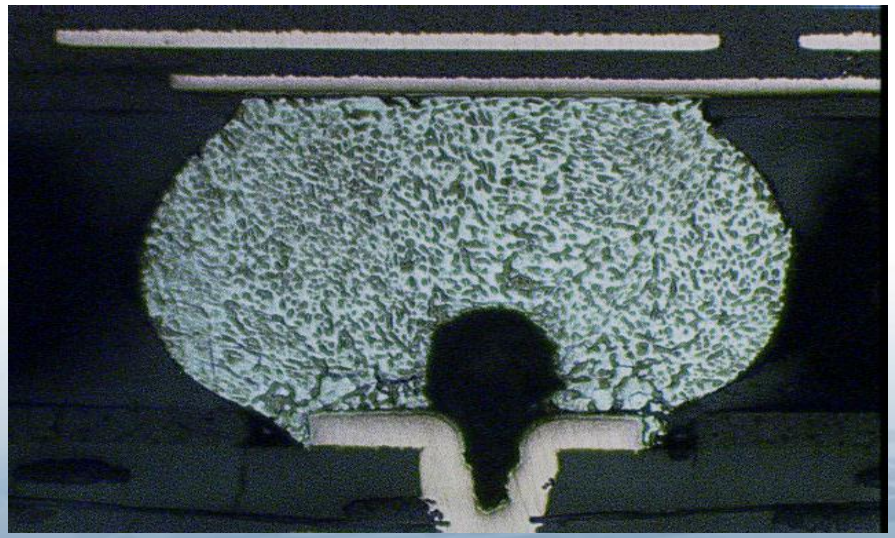
Big Voids:
29% & 32%!



Tube voltage: 120 kV
Tube power: 1.52 W
Filter method used: LowMediumMag
Averaging: 128 frames

Future Work

- **Conduct Thermal Cycle Testing**
  - **Conduct Failure Analysis**
  - **Correlate Void Size/Location Vs Thermal Cycle Failure Data**
  - **Submit Data to IPC JSTD 001 Committee for Review**



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Questions ?

RIM

Rockwell Collins

Canon Communications LLC

Association Connecting Electronics Industries

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