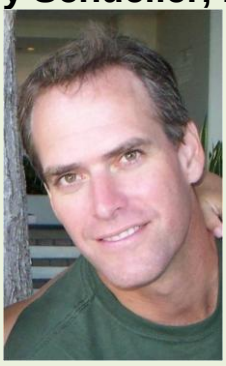
IPC Electronics Midwest 2010

Design for Reliability: The Next Generation

Randy Schueller, Ph.D.



DfR Solutions

Biography:

Randy received his Ph.D. in materials science engineering in 1992 and began working in the electronics industry with 3M where he led a team in the development of many IC packaging products. This was followed by 4 years as Director of IC Packaging and Engineering at Extreme Devices. Randy then moved to Dell in 2003. As Sr. Manager of Dell's Component Engineering and Failure Analysis Groups he helped drive lead-free solutions across all of Dell's product lines (including servers). Two years ago Randy moved to Minneapolis and accepted a position with DfR Solutions as a Sr. Member of Technical Staff. Randy has 15 patents and has authoring and presenting over 40 papers for the electronics industry.

Executive Summary

As margins on electronics technology have continued to erode, an increasing number of organizations have implemented design for reliability practices to ensure device performance while meeting tight product development guidelines. There are numerous aspects of DfR principles, including specification development, part selection and derating, design review by failure mod (DRBFM), and physics of failure (Pof). Often overlooked by the "science of success," Pof will play a crucial role in future design activities as an increasing number of technologies are designed with limited lifetimes. Components of concern have broadened from the traditional LEDs and electrolytic capacitors into sub-90nm integrated circuits and solder joint fatigue. This presentation will provide a history and overview of PoF and where it fits into the overall scheme of DfR. Of critical importance will be a discussion on which organizations and standards bodies will start to require PoF and how to implement PoF into your design activities to ensure product success and compliance with the next generation of industry specifications.

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Design for Reliability: The Next Generation

Dr. Craig Hillman, Jim McLeish, Nathan Blattau and Dr. Randy Schueller

DfR Solutions

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Design for Reliability (DfR)

- DfR: A process for ensuring the reliability of a product or system during the design stage *before* physical prototype

- Reliability: The measure of a product's ability to
  - …perform the specified function
  - …at the customer (with their use environment)
  - …over the desired lifetime

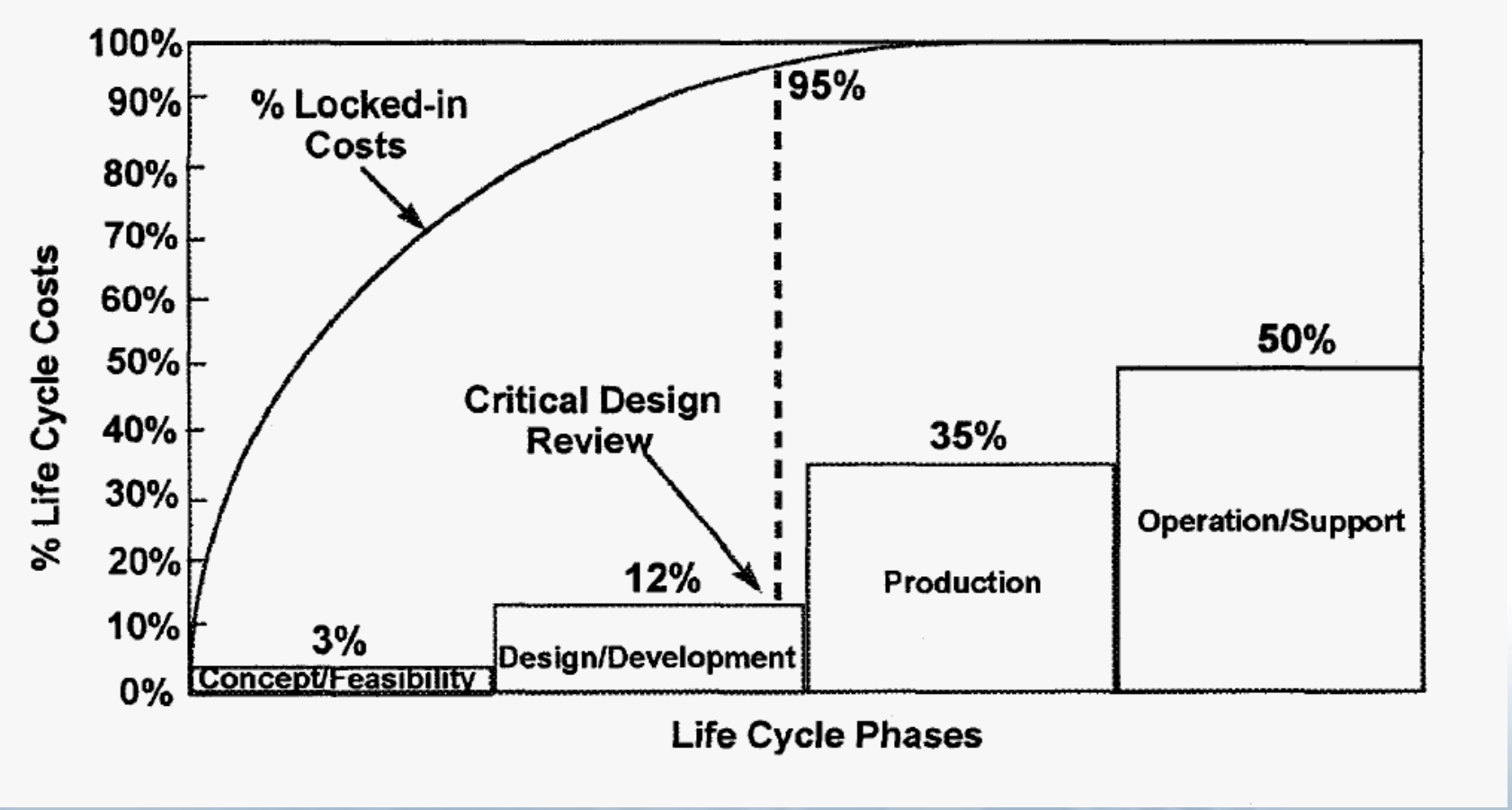
History

- DfR has been a concept promoted by electronics community since the early 1950's

- DARPA identified DfR as an "Area of Promise" to resolve issue with Defense Systems Reliability in 1958

Identification of Certain Current Defense Problems and Possible Means of Solution, INSTITUTE FOR DEFENSE ANALYSES, 1958

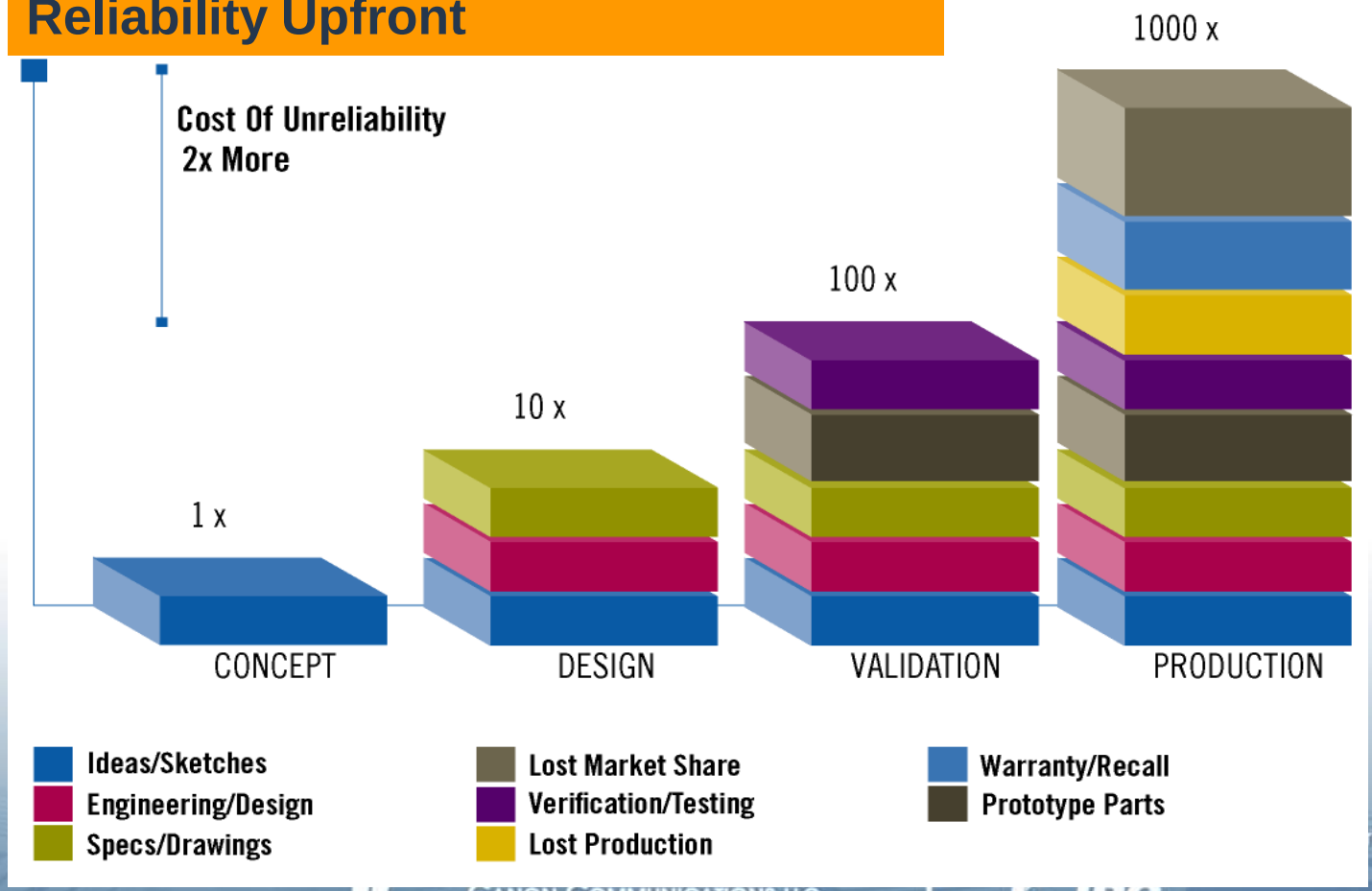
Why DfR?



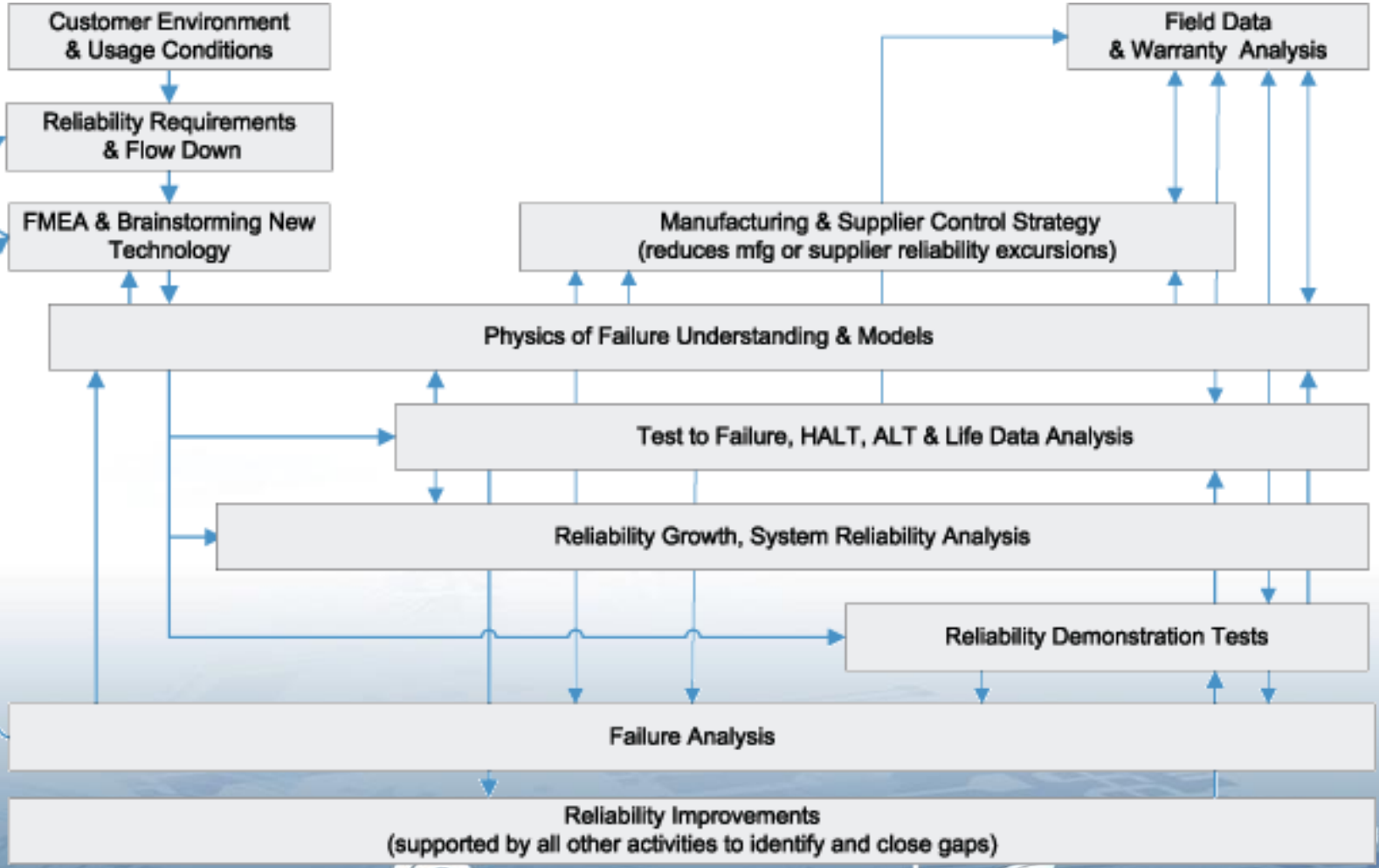
Architectural Design for Reliability, R. Cranwell and R. Hunter, Sandia Labs, 1997

Why DfR? (cont.)

Reduce Costs by Improving Reliability Upfront



Process of DfR (example)



http://www.reliasoft.com/newsletter/v8i2/reliability.htm

Limitations of Current DfR

- Too broad in focus (not electronics focused)
- Too much emphasis on techniques (e.g., FMEA and FTA) and not answers
  - FMEA/FTA rarely identify DfR issues because of limited focus on the failure mechanism
- Overreliance on MTBF calculations and standardized product testing
- Incorporation of HALT and failure analysis (HALT is test, not DfR; failure analysis is too late)
  - Frustration with ‘test-in reliability’, even HALT, has been part of the recent focus on DfR

DfR and Physics of Failure (PoF)

- Due to some of the limitations of classic DfR, there has been an increasing interest in PoF (aka, Reliability Physics)

- PoF Definition: The use of science (physics, chemistry, etc.) to capture an understanding of failure mechanisms and evaluate useful life under actual operating conditions

PoF (cont.)

- Originally instituted by Rome Air Development Center (RADC) in 1961
  - Over time, original broad focus (resistors, transistors, capacitors, etc.) replaced by emphasis on integrated circuits
- Movement to circuit card and higher level integration initially limited by complexity, lack of wearout mechanisms

G. Ebel, Reliability Physics in Electronics: A Historical View, IEEE Trans. Rel., Vol. 47, NO. 3-SP Sept 1998 SP-379

PoF Examples

$$\tau_{HCI} \propto \exp[\frac{b_{HCI}}{V_D}] \cdot \exp[\frac{E_{aHCI}}{kT}]$$

$$L = L_r\left(\frac{V_r}{V_0}\right) \times 2^{\left(\frac{T_r - T_A}{10}\right)}$$

$$T_f \propto \exp\left(\frac{\sim 0.51eV}{kT}\right) \times \exp(\sim -0.063\%RH)$$

$$\tau_{TDDB} \propto \exp[-b_{TDDB} \cdot V_G] \cdot \exp[\frac{E_{aTDDB}}{kT}]$$

$$N_f^{-0.6} D_f^{0.75} + 0.9 \frac{S_u}{E}\left[\frac{\exp(D_f)}{0.36}\right]^{0.1785 \log \frac{10^5}{N_f}} - \Delta\varepsilon = 0$$

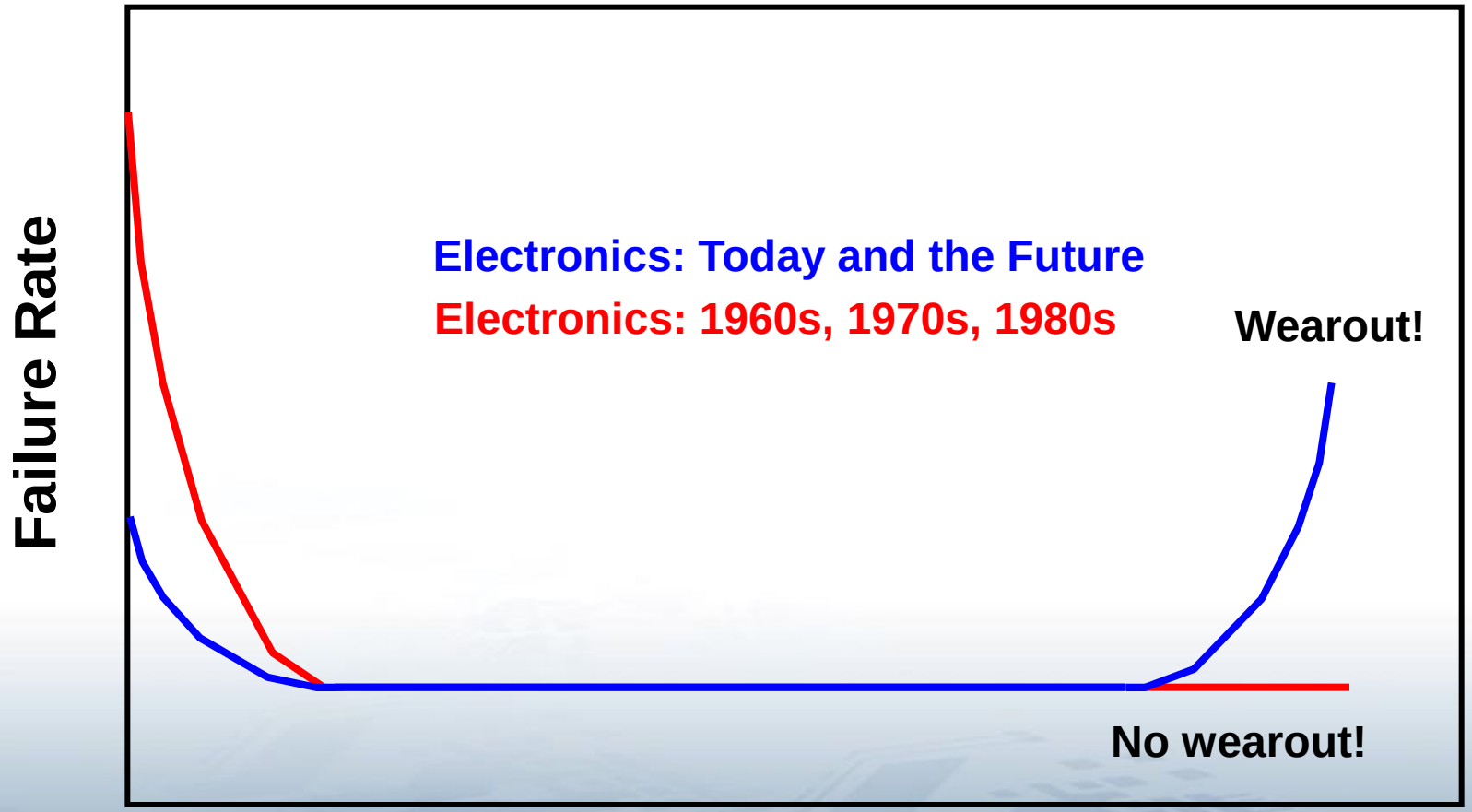
$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n \exp \frac{E_a}{K_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)$$

$$\tau_{EM} \propto (J)^{-n} \cdot \exp[\frac{E_{aEM}}{kT}]$$

$$\tau_{NBTI} \propto \exp[-b_{NBTI} \cdot V_G] \cdot \exp[\frac{E_{aNBTI}}{kT}]$$

$$(\alpha_2 - \alpha_1) \cdot \Delta T \cdot L = F \cdot \left(\frac{L}{E_1 A_1} + \frac{L}{E_2 A_2} + \frac{h_s}{A_s G_s} + \frac{h_c}{A_c G_c} + \left(\frac{2-\nu}{9 \cdot G_b a}\right)\right)$$

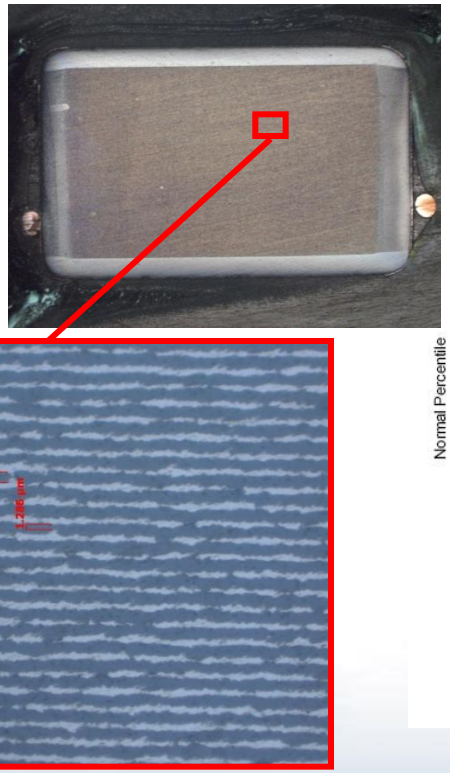
Why PoF is Now Important

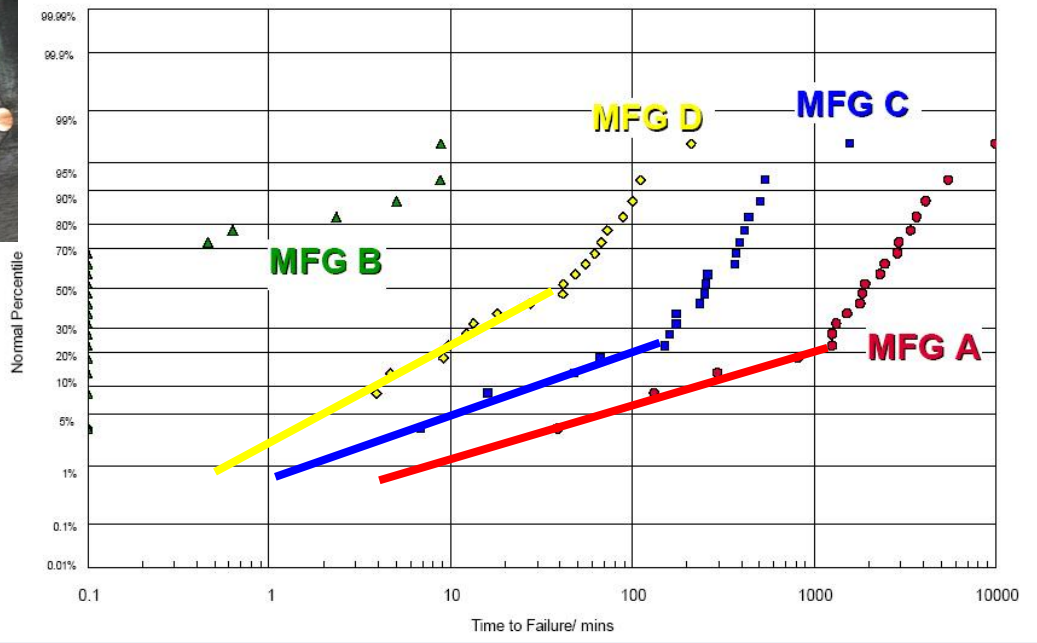


PoF and Wearout

- What is susceptible to wearout in electronic designs?
  - Ceramic Capacitors (oxygen vacancy migration)
  - Memory Devices (limited write cycles, read times)
  - Electrolytic Capacitors (electrolyte evaporation, dielectric dissolution)
  - Resistors (if improperly derated)
  - Silver-Based Platings (if exposed to corrosive environments)
  - Relays and other Electromechanical Components
  - Light Emitting Diodes (LEDs) and Laser Diodes
  - Connectors (if improperly specified and designed)
  - Tin Whiskers
  - Integrated Circuits (EM, TDDB, HCI, NBTI)
  - Interconnects (Creep, Fatigue)
    - Plated through holes
    - Solder joints

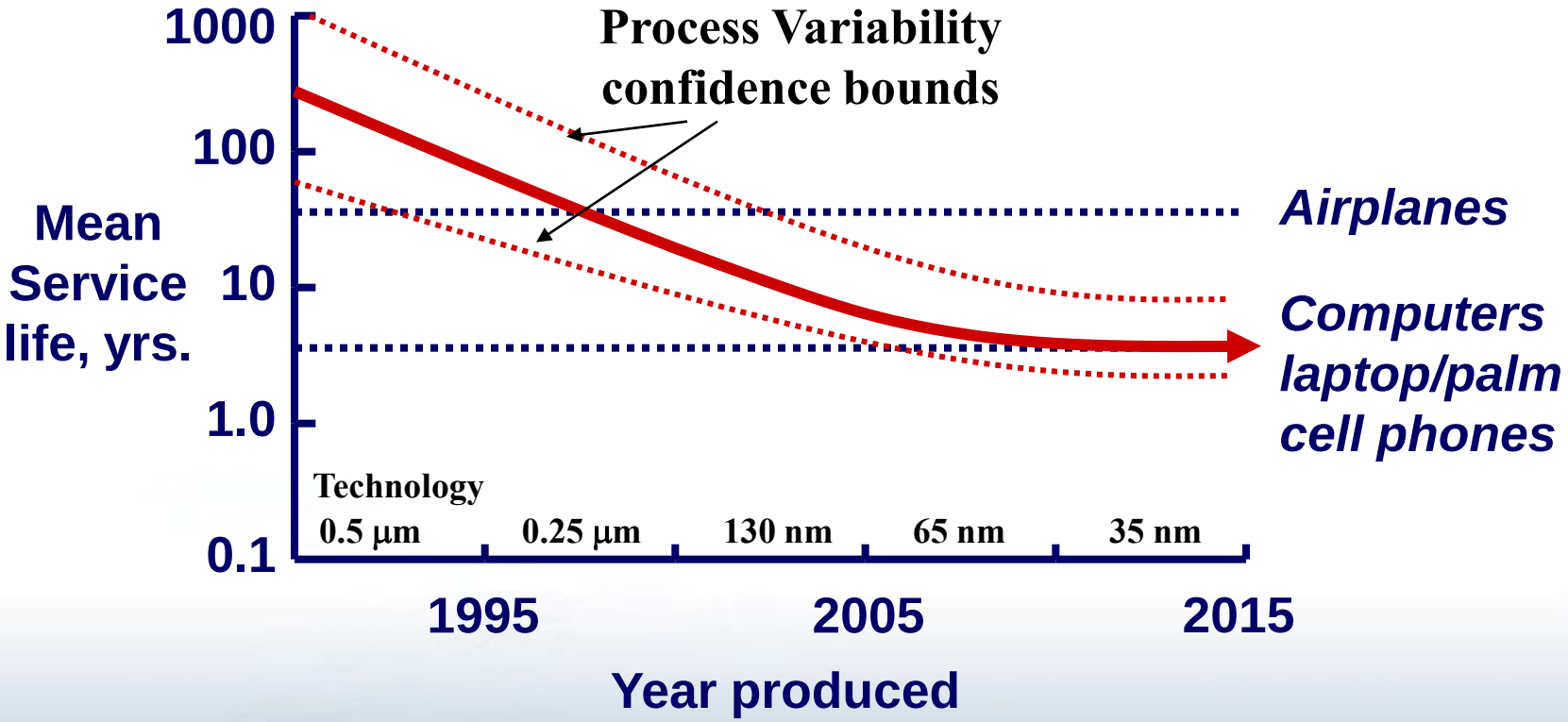
Wearout (Ceramic Capacitors)





- Ceramic chip capacitors with high capacitance / volume (C/V) ratios
  - Can fail in **less than one year** when operated at rated voltage and temperature

Wearout (Integrated Circuits)



Known trends for TDDB, EM and HCI degradation

(ref: extrapolated from ITRS roadmap)

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IC Wearout: Background

Guaranteeing the conventional 10-year life of ICs is going to become increasingly difficult….the progressive degradation of the electrical characteristics of transistors and wires will start dominating over abrupt functional failures. Furthermore, the mean-time-to-first-soft-break will significantly diminish."

Antonis Papanikolaou, IMEC, Leuven, Belgium, 2007

…the progress of Moore's Law means that transistor wear-out and statistical performance issues are beginning to cross over from the realm of academic and hypothetical discussion to real-world R&D engineering.

EE Times Europe, 2007

"The notion that a transistor ages is a new concept for circuit designers," says Chris Kim (U of Minnesota). Transistor aging has traditionally been the bailiwick of engineers who design the processes that make transistors; they also formulate recipes that guarantee the transistors will operate within a certain frequency and other parameters typically for 10 years or so…But as transistors are scaled down further and operated with thinner voltage margins, it's becoming harder to make those guarantees… transistor aging is emerging as a circuit designer's problem.

IEEE Spectrum, June 2009

IC Wearout (cont.)

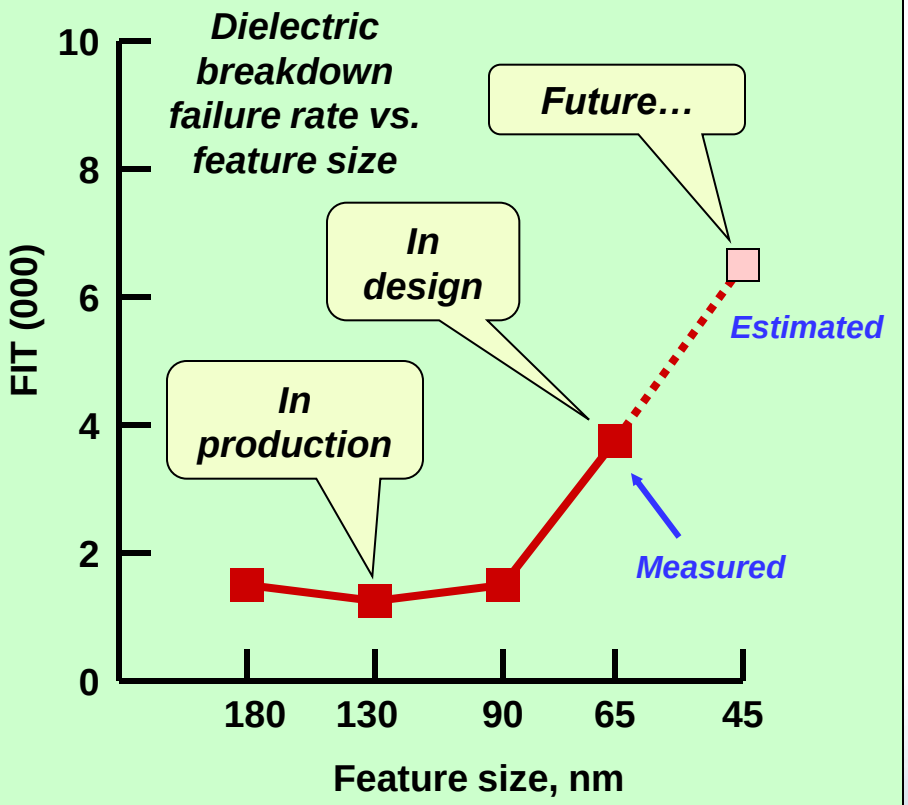


Figure adapted from industry published data, 2008

It is becoming more challenging to achieve very high reliability for products made with advanced technologies (90nm and smaller)

Phil Nigh, IBM Microelectronics

"failure rate increases as we scale to smaller technologies…hard failures will present a significant and increasing challenge in future technology generations."

Pradip Bose, Jude A. Rivers, et al., IBM T.J. Watson Research Center

Increasing need to predict failure behavior before incorporating new technology in long-life systems

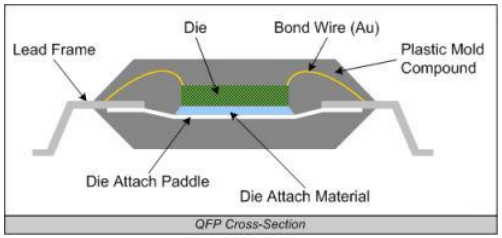
IC Testing Falls Short

- Limited degree of mechanism-appropriate testing
  - Only at transition to new technology nodes
  - Mechanism-specific coupons (not real devices)
  - Test data is hidden from end-users
- Questionable JEDEC tests are promoted to OEMs
  - Limited duration (1000 hrs) hides wearout behavior
  - Use of simple activation energy, with incorrect assumption that all mechanisms are thermally activated, can result in overestimation of FIT by 100X or more

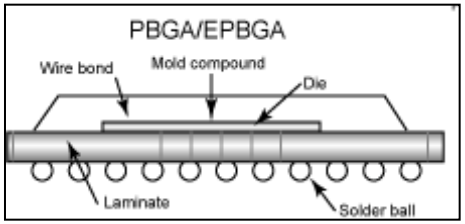
Solder Joint (SJ) Wearout

- Elimination of leaded devices
  - Provides lower RC and higher package densities
  - Reduces compliance

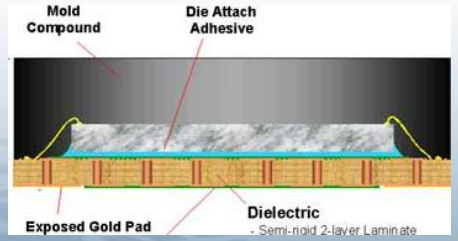
Cycles to failure
-40 to 125C



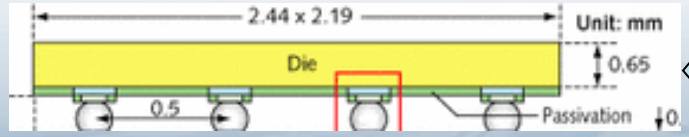
QFP: >10,000



BGA: 3,000 to 8,000



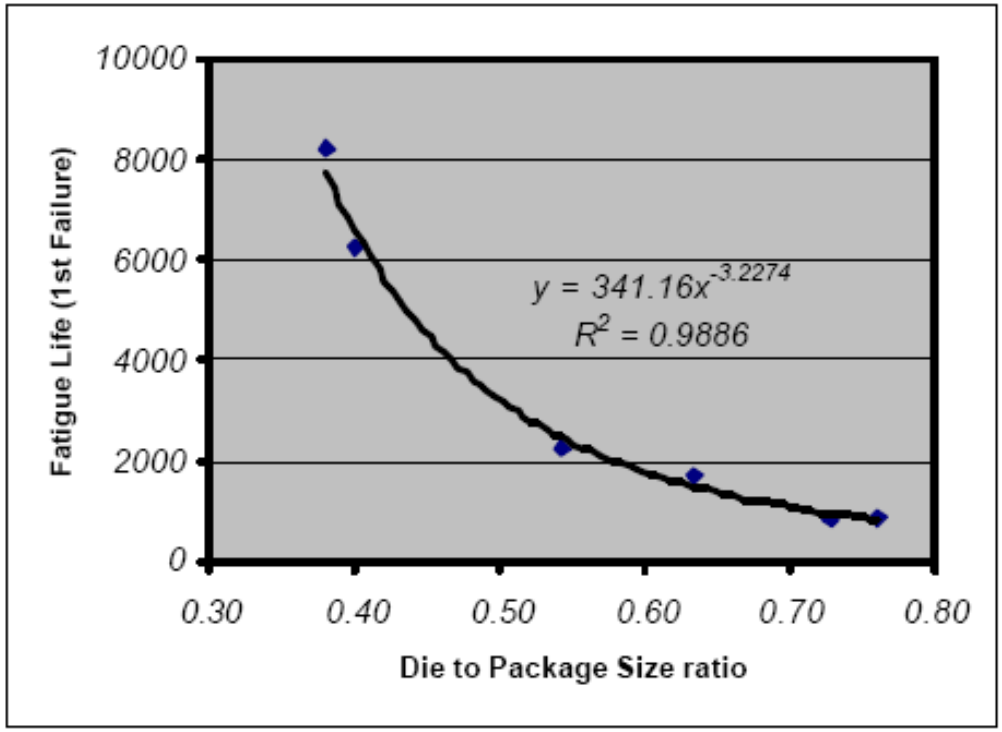
QFN: 1,000 to 3,000



CSP / Flip Chip: <1,000

SJ Wearout (cont.)

- Design change: More silicon, less plastic
- Increases mismatch in coefficient of thermal expansion (CTE)



BOARD LEVEL ASSEMBLY AND RELIABILITY CONSIDERATIONS FOR QFN TYPE PACKAGES, Ahmer Syed and WonJoon Kang, Amkor Technology.

Industry Testing of SJ Wearout

- JEDEC
  - Specification body for component manufacturers
- JEDEC JESD47
  - Guidelines for new component qualification
  - Requires **2300** cycles of 0 to 100C
  - Testing is often done on **thin** boards
- IPC
  - Specification body for electronic OEMs
- IPC 9701
  - Recommends **6000** cycles of 0 to 100C
  - Test boards should be **similar thickness** as actual design

Industry Testing (cont.)

JEDEC requirements are 60% less than IPC

+

Testing on a thin board can extend lifetimes by 2X to 4X

- What does this mean?
  - The components you buy may only survive 500 cycles of 0 to 100C
- What must you do?
  - Components at risk must be subjected to PoF-based reliability analysis

Industry Response

- Increasing concern with wearout and lack of appropriate response at design stage leading to implementation of PoF requirements
  - Especially within the DoD and avionics communities

DoD and PoF

- Army Reliability Policy (2007) and Weapon Systems Acquisition Reform Act (2009)
  - Designed to improve the consideration of reliability into the acquisition process
  - Current Army Scorecard emphasizes PoF-based modeling
- Drove the adoption of GEIA-STD-0009 Reliability Program Standard for System Design, Development and Manufacturing

Industry and PoF

- VITA 51.2: Physics of Failure Reliability Predictions (est. 2011)
  - Established by the standard bodies responsible for VME technology (open system architecture of real-time, modular embedded computing)
- IEC-TS-62239 2nd edition: Process management for avionics
- FAA and Boeing expected to require PoF for IC wearout

Implementing DfR / PoF

- Many organizations have developed DfR Teams to speed implementation
  - Success is dependent upon team composition and gating functions
- Challenges: Classic design teams consist of electrical and mechanical engineers trained in the 'science of success'
  - PoF requires the right elements of personnel and tools

DfR / PoF Team

- Component engineer
- Mechanical / Materials engineer
- Electrical engineer
- Thermal engineer
  - Depending upon power requirements
- Reliability engineer?
  - Depends. Many classic reliability engineers provide **NO** value in the DfR / PoF process due to over-emphasis on statistical techniques and environmental testing

Conclusion

- Design for Reliability is a valuable process for lowering cost, reducing time-to-market, and improving customer satisfaction
- PoF is a powerful tool that can leverage the value of DfR activities
- Successful DfR / PoF implementation requires the right combination of personnel and tools and time limitations
  - Changes in the supply chain will soon require its use in multiple industries