Design Considerations for High Reliability PCB

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History & Importance of PCB

PCB's literally form the backbone of electronic devices and became commonplace in consumer electronics over a half century ago and over the last decade the complexity and density of interconnect requirement has been increasing due to consumer demand for higher functionality within a smaller format. The transition of density has been driven by smaller lines and space, for example about fifty years ago line widths that were 0.040" were supposedly high tech and as time elapsed they successfully became 0.010" and 0.006", and 0.004" & 0.003" is the standard of today. And similarly the mechanical drilled holes have been shrinking to keep up with the increased densities from 0.040" in the past down to 0.012", 0.010" and 0.008" or less for plated through holes (**PTH**) or commonly referred as thru vias today

PCB is the communication **link** between semiconductor devices

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Environmental Initiatives
European Union Directives

WEEE Directive

- Waste from Electrical & Electronic Equipment
- “Re-cycling” and recovery
- Private sector manages and funds program
- Applies to all products except military

RoHS Directive

- Restriction of Hazardous Substances
- July 2006 or 2010 depending on product
- “Lead Free initiative”

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www.RoHS.gov.uk

Environmental Initiatives
What's Driving it?

Primary Drivers

- Environmental laws
- Marketing considerations.
  - Increased market share by carrying the environmental friendly initiatives
  - Possible barrier to EU markets
- Material
  - Lead Free plastic BGA is not compatible with a Tin-Lead assembly process
  - IC manufactures are already switching to Lead Free only BGA's
- Manufacturing
  - CM would like to focus on one soldering process

Environmental Initiatives
European Union Directives Definition

Definition of WEEE

Waste Electrical and Electronic Equipment (WEEE)

The WEEE directive sets collection, recycling and recovery targets for various categories of electrical products

Definition of RoHS

The Restriction of Hazardous Substances in Electrical and Electronic Equipment (RoHS)

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Environmental Initiatives
European Union Directives: WEEE

Ten categories of products covered:

1. Large household appliances (refrigerators, washing machines, stoves, etc.)
2. Small house hold appliances (vacuum cleaners, toasters, hair dryers, etc.)
3. Information and telecommunications equipment (computers and peripherals, cell phones, calculators, etc.)
4. Consumer equipment (radios, TVs, stereos, etc)
5. Lighting (fluorescent lamps, sodium lamps, etc.)
6. Electrical and electronic tools (drills, saws, sewing machines, etc.)
7. Toys, leisure, and sports equipment (electric trains, video games, etc.)
8. Medical devices (ventilators, cardiology and radiology equipment, etc)
9. Monitoring instruments (smoke detectors, thermostats, control panels,)
10. Automatic dispensers (appliances that deliver products such as hot drinks)

Environmental Initiatives
European Union Directives: RoHS

Definition of RoHS Compliance for Materials

Material	Allowable Amount by weight
Lead (Pb)	0.1% by weight
Cadmium (Cd)	<0.01% by weight
Mercury (Hg)	0.1% by weight
Hexavalent Chromium (Hex-Cr)	<0.1% by weight
Polybrominated Biphenyls (PBB – fire retardant)	0.1% by weight
Polybrominated Diphenyl Ethers (PBDE- fire retardant)	0.1% by weight

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Environmental Initiatives
Exemptions to RoHS

Exemptions

- Network infrastructure (Solder joints)
- Equipment deemed for national security (but not all military equipment)
- Service and storage arrays (solder joints until 2010)
- Leaded glass, Electronic ceramic parts, Applications that specifically require high Pb solder
- Equipment with rated operating voltages of 1000 Vac or 1500 Vdc
- Equipment related to Nuclear or Biological containment

Environmental Initiatives
RoHS AND PWB's

How Will RoHS Impact Printed Circuit Design and Long Term Reliability ?

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Environmental Initiatives
Eutectic Tin Lead Based Solder

Tin Lead Solder

63% tin 37% lead

183˚C

Reflow Peaks at approximately 206˚ C

The time above reflow is from 60-90 seconds

for eutectic tin-lead solder

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Environmental Initiatives
Lead Free Solders

SN-Ag-Cu (SAC) Alloys (Current leaders)

Tin-Silver-Copper (Sn96.5-Ag3.0-Cu0.5)	217° C -218° C
Tin-Silver-Copper (Sn95.5-Ag3.9-Cu0.6)	217 ° C
Tin-Silver-Copper (95.5-Sn-3.8Ag – 0.7Cu)	216° C

Some Of The Other Lead Free Alloys !		Comment !
Tin-Copper eutectic (Sn99.3-Cu0.7)	227° C	High temp
Tin-Silver eutectic (Sn96.5-Ag3.5)	221° C	High temp
CASTIN® (Sn96.2-Ag2.5-Cu0.8-Sb0.5)	217° C	
Tin-Zinc (Sn91-Zn9)	199° C	Oxide concern
Tin-Bismuth-Silver (Sn57-Bi42-Ag1)	139° C	Recycling issue

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Environmental Initiatives
Assembly Impact: High Temp. Soldering

- **Higher Process Temperatures**
  - Bare Printed Circuit Boards
    - Laminate
    - Solder Mask
    - Epoxy Legend
  - SMT Components
  - Through Hole Components
  - Press Pin
  - Labels (bar codes, assembly #)
  - SMT Adhesive
  - Optical Components (Plastic)

- **Process Impact**
  - Reflow ovens
  - Wave solder
  - Solder fountain
  - BGA rework platforms
  - Hand solder / Rework

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Environmental Initiatives
Typical Soldering Process Temperatures

Process Temperatures			
	Tin-Lead	Lead-Free	Δ° C
Solder Paste Range	183 ° C	216°C-221°C	33-38°C
Re-flow Oven	217°C	240° C - 260°C	23-43°C
Wave Solder	260°C	260°C - 280°C	0-20°C
Wave Contact time	3-5 sec	5-8 sec	
BGA Rework (BGA case)	230C	260C	30°C

- Tin Lead Solder: Sn63, Pb37
- Lead Free Alloy Sn95.5, Ag3.9,Cu0.6 (SAC)

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Reliability Consideration With High Temp Processing

- Interconnect Stress Test (IST); electrically heats the barrel from ambient to 150ºC, about 3 minutes per cycle, looking for a 10% resistance change
- Highly Accelerated Thermal Shock (HATS); temperature cycling in a chamber from -40ºC to 145ºC, roughly 14 minutes per cycle, looking for a 10% resistance change
- Via Reliability After Lead Free Cycling
  - Plated hole diameter
  - Board thickness
  - Multiple lamination cycles
- Peel Strength a Factor, Particularly for Rework
- De-lamination of base substrate
- Will There Be a Change in CAF Resistance?

Reliability Considerations for Materials to withstand Lead Free Assembly

Laminate must be compatible with the Pb Free Assembly process (higher temperatures)

Determining Factors:

- Z axis Coefficient of Thermal Expansion (CTE)
- Glass Transition Temperature (Tg)
- Modulus of elasticity of the composite laminate
- Thermal Decomposition Temperature (Td)
- T260 & T288 Time to de-lamination
- CAF Resistance

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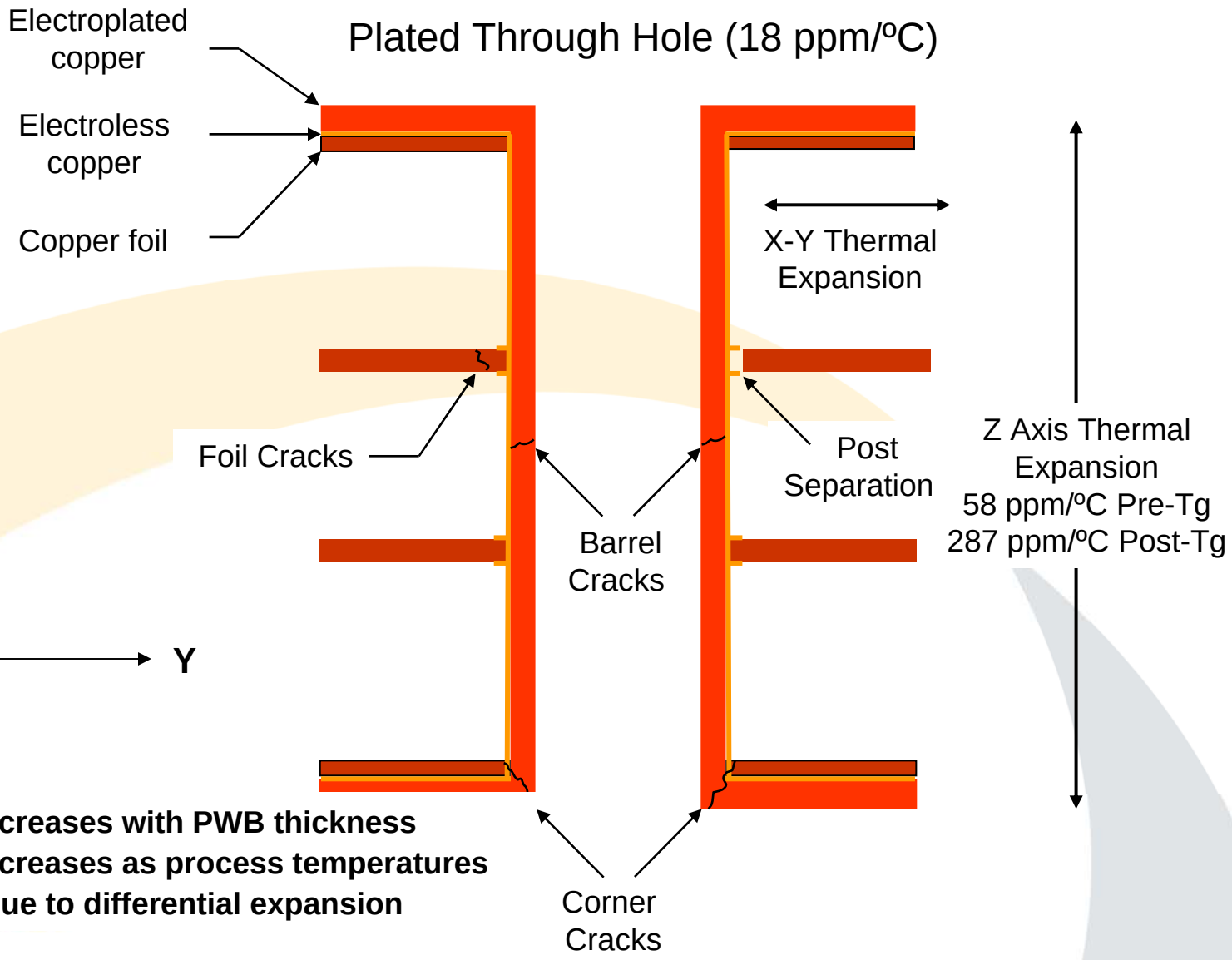
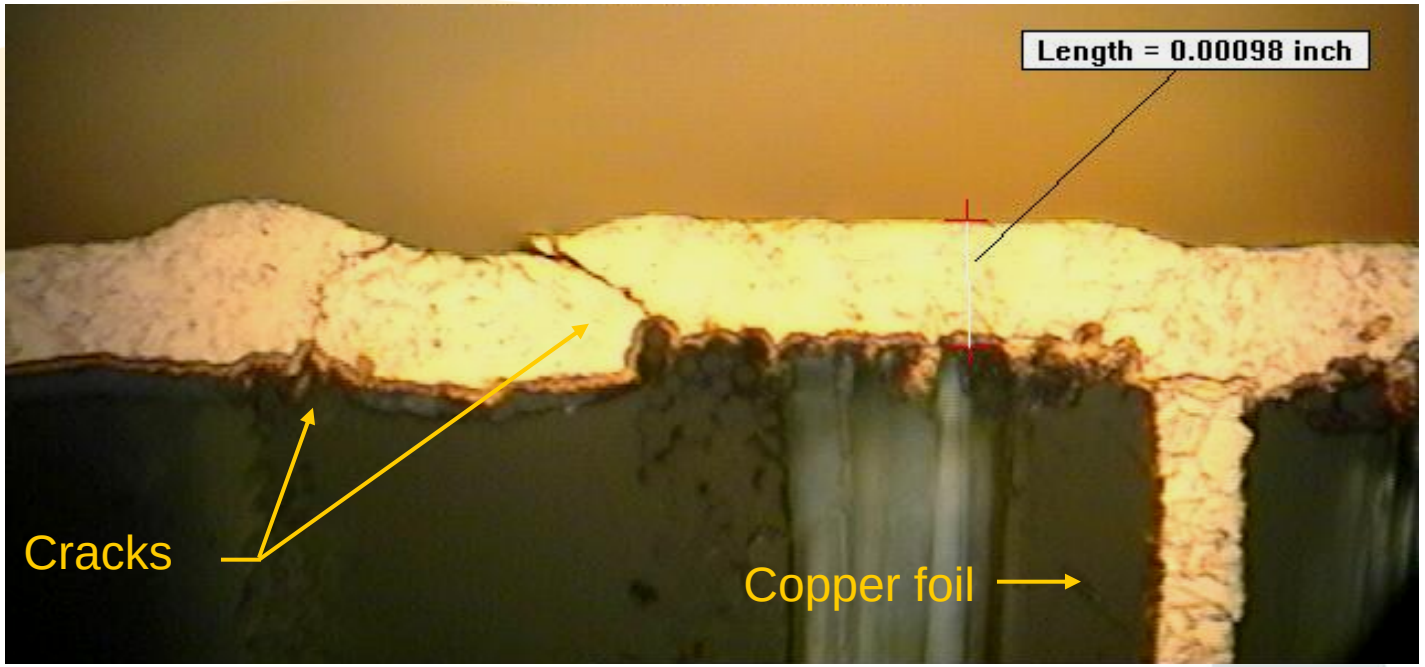
Plated Through Hole Failure Modes



- **Stress increases with PWB thickness**
- **Stress increases as process temperatures increase due to differential expansion**

Plated Through Hole Failure: Barrel Cracking

Hole barrel Z axis



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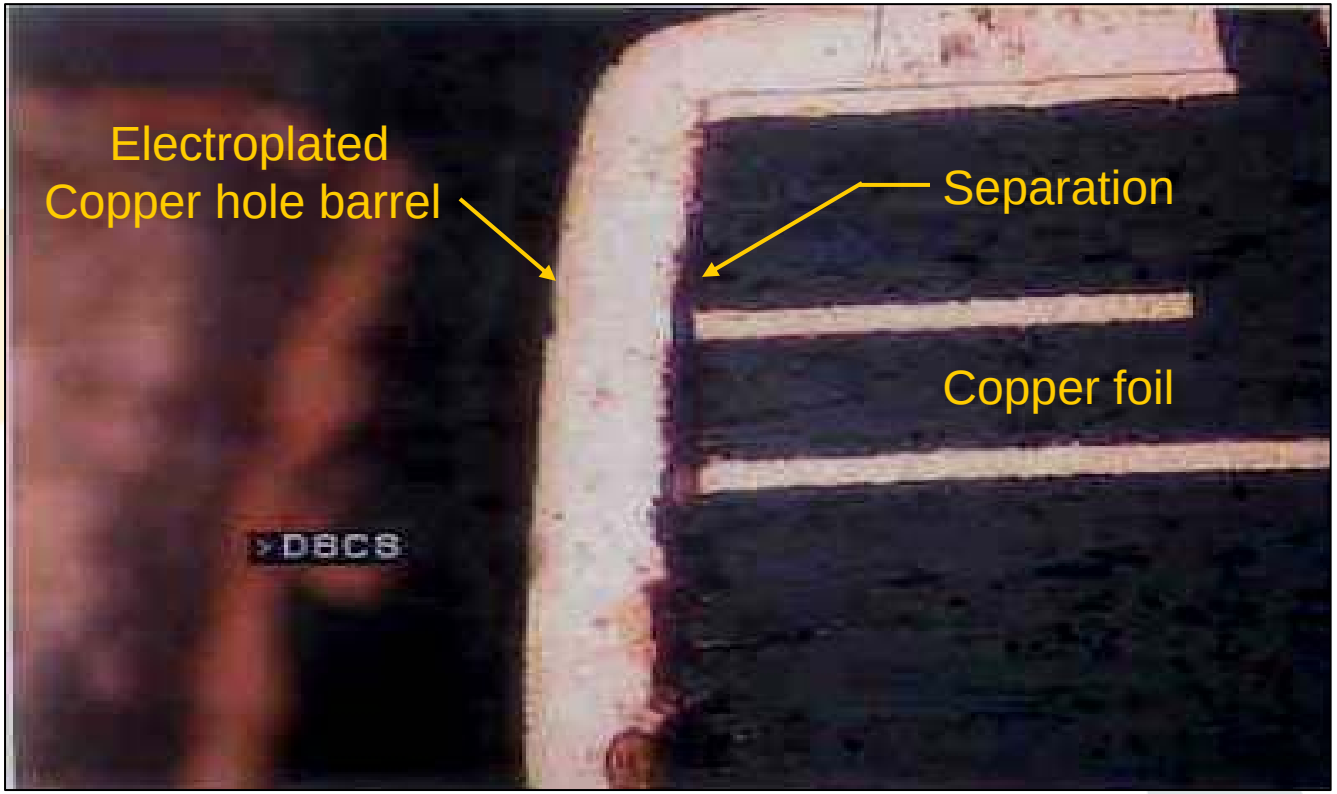
Plated Through Hole Failure: Post Separation



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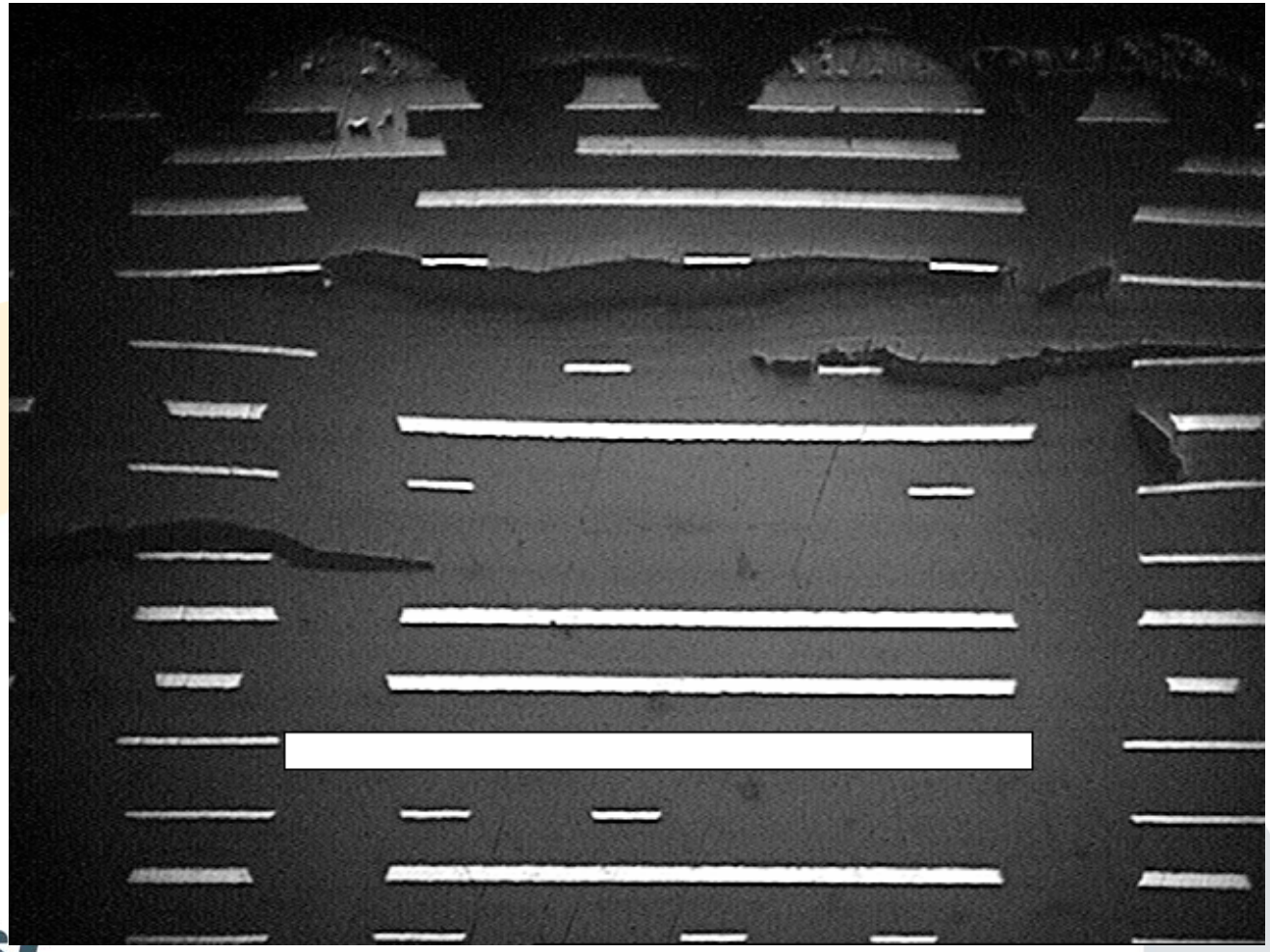
PWB Laminate Failure: De-Lamination



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Take Away

- **Current FR4 materials are RoHS compliant**

  (Surface Finish, Solder Mask and Legend)
- **Not all FR4 materials can survive Lead Free Assembly**
- **Lead-Free Assembly maintains temperatures**

  ranging from 238° C to 288° C
- **RoHS does not state Halogen - Free as a requirement**
- **Halogen – Free means “no bromines” (non standard FR4)**

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Considerations for PCB laminate materials

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Printed Circuit Materials Overview

Overview

What is FR-4?
- Laminate construction
- Basic electrical properties

Advanced Materials
- Special purpose & low loss
- Industry specifications

Hybrid Constructions

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PCB Material Properties

Material properties are playing an increasingly important role in advanced system designs as speed, power dissipation and process temperatures increase

Factors that influence material selection

- Electrical Design:
  - Dielectric constant
  - Loss tangent
- Reliability:
  - Lead free assembly
  - Long term life
- Thermal Mechanical:
  - X,Y,Z CTE
  - Conduction cooling

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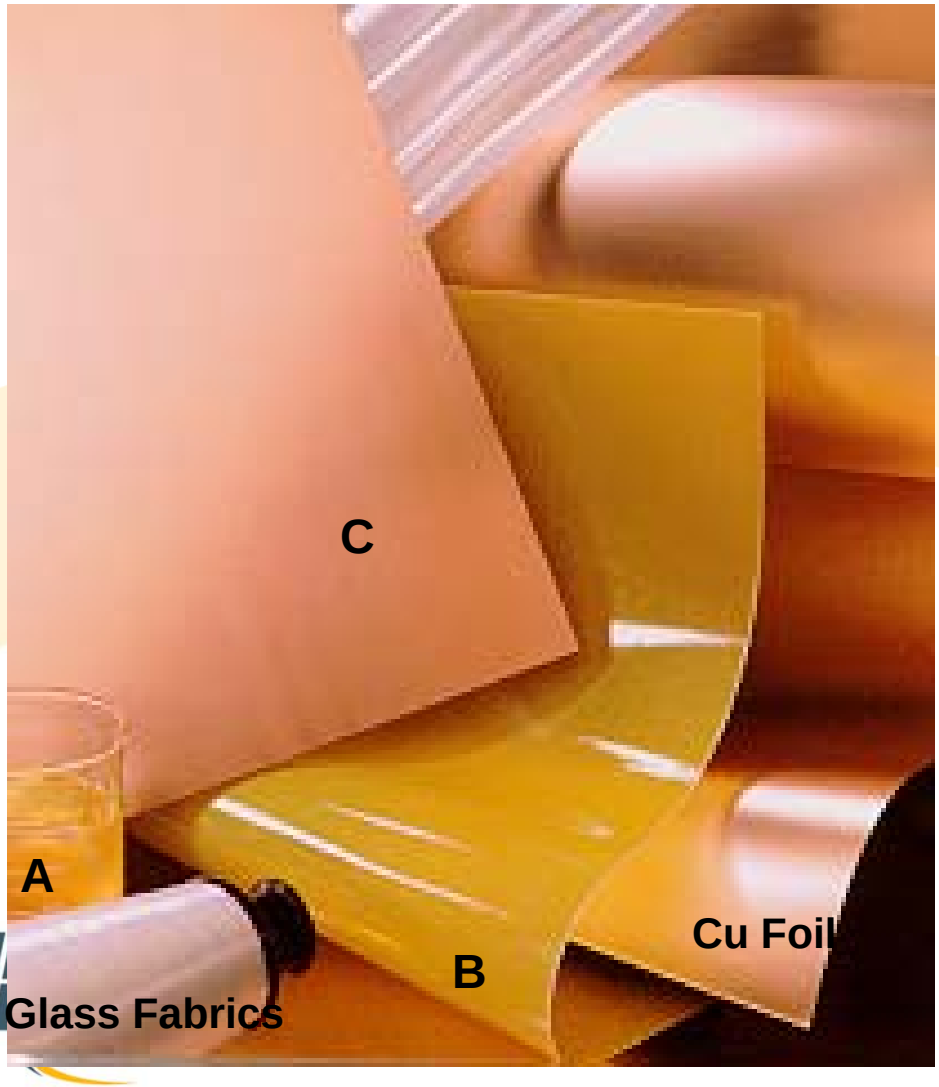
What is “FR4”, Laminate Composition



Laminate Components

- *Copper Foil*
- *Glass Fibers*
- *Woven Glass Fabrics*
- *Resin*

Resin Stages

A Stage = Liquid Form

B Stage = Partially Cured Resin

C Stage = Fully Cured Resin

“FR4” Standard Resin Systems

- Tetrafunctional Resin
  - Tg =130° - 140° C
  - ε_r = 4.4
  - Tan δ = 0.024
- Multifunctional Resin
  - Tg = 140° to 160° C
  - ε_r = 4.3
  - Tan δ = 0.022
- High Temperature Multifunctional Resin
  - Tg 170° - 175° C
  - E_r = 4.1
  - Tan δ = 0.019
- Enhanced Multifunctional Resin (Low loss)
  - Tg 180° - 210° C
  - ε_r = 3.7
  - Tan δ = 0.010

- Lead Free Solder Compatible Resins
  - Tg = 170° - 185° C
  - ε_r = 4.1 – 4.4
  - Tan δ = 0.015 - 0.02
  - Td = ≥ 340° C
  - CTE (z) = 2.7% - 3.2%

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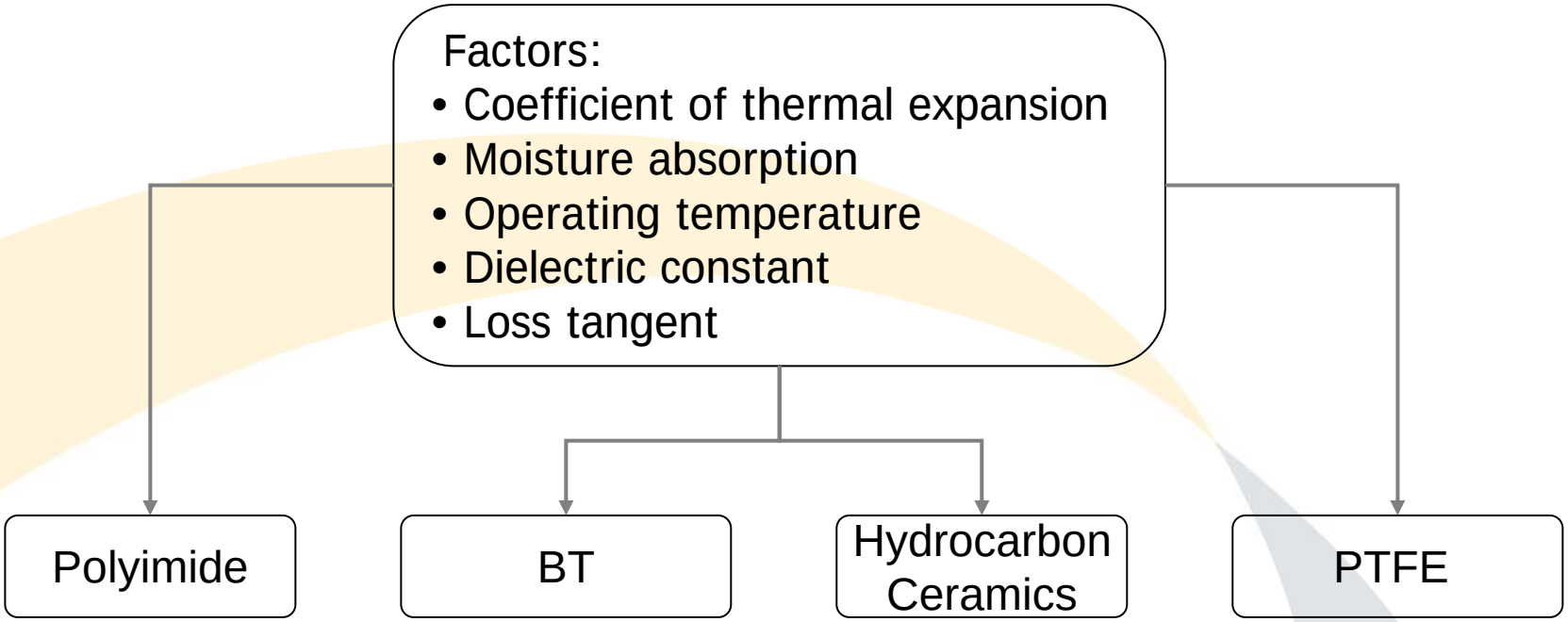
Special Purpose Laminate Materials

Often times unique design requirements dictate the use of special purpose laminate:



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Polyimide Laminates

Polyimide resin reinforced with
woven E-glass, Typical properties

• Tg	260C
• Td	382C
• ZCTE	1.5%
• T260	60 Min.
• T-288	60 Min.
• Dk @ 2.0GHz	3.85
• Dk @ 10 GHz	3.83
• Df @ 2.0 GHz	0.018
• Df @ 10 GHz	0.024
• Moisture Abs.	0.4%

Applications

- High temperature applications
- IC Burn-in boards
- Engine controls
- Down hole instruments
- Extreme chemical resistance
- Severe assembly applications

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Bismaleimide-Triazine (BT) Laminates

BT resin reinforced with woven E-glass, Typical properties

• Tg	180C
• Td	325C
• ZCTE	3.3%
• T260	12 Min.
• Dk @ 2.0GHz	3.70
• Dk @ 10 GHz	3.65
• Df @ 2.0 GHz	0.013
• Df @ 10 GHz	0.015
• Moisture Abs.	0.2%

Applications

- Multiple thermal excursions
- Low moisture absorption
- IC substrates
- High voltage applications
- Chemical and thermal resistance

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Hydrocarbon Ceramic Laminates

Hydrocarbon resin with ceramic filler reinforced woven glass
- Precise dielectric constant
- Low loss tangent

Applications

- RF Microstrip circuits
- RF Multilayer Stripline
- RF filters and power dividers

Hydrocarbon resin with ceramic filler
- Precise dielectric constant
- Homogeneous dielectric
- Electrical properties stable over temperature
- Low loss tangent

Applications

- Microwave Microstrip circuits
- Microwave power circuits
- Microwave filters & power dividers
- Antenna applications

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PTFE Based Laminates

PTFE with ceramic filler
- Precise dielectric constant
- Low loss tangent
- Homogeneous dielectric
- Stable mechanical properties

allowing mixed dielectric constants

Applications

- Microwave Microstrip circuits
- Microwave Multilayer Stripline
- Microwave filters & power dividers
- Antenna applications

PTFE with glass random glass microfiber reinforcement
- Precise dielectric constant
- Very low dielectric constant
- Homogeneous dielectric
- Electrical properties stable over temperature
- Low loss tangent into the Ku band

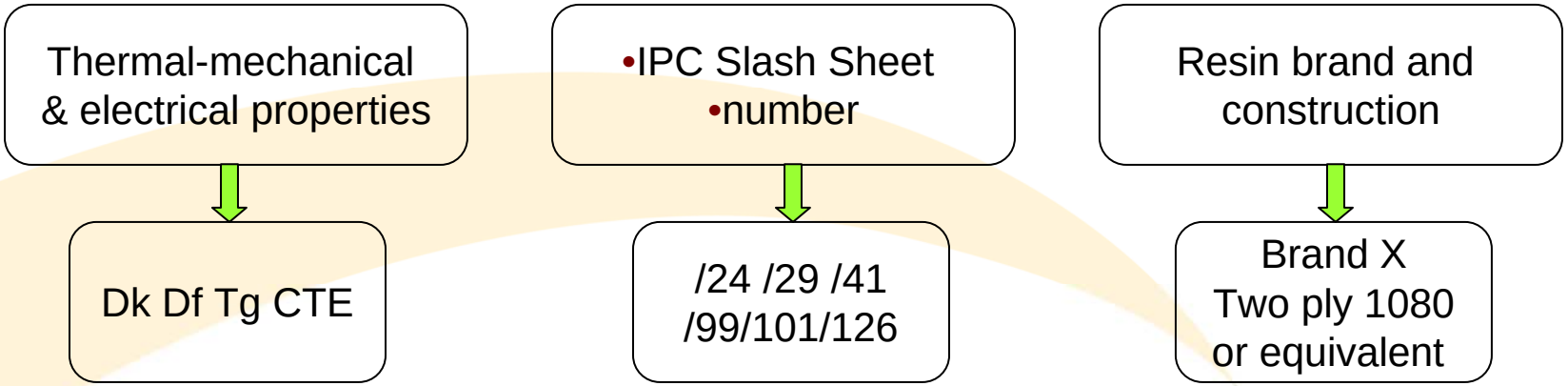
(12 to 18 GHz)

Applications

- Microwave Microstrip circuits
- Microwave power circuits
- Microwave filters & power dividers
- Antenna applications

Specifying Laminate Materials

There are three methods to specify laminate materials:



Issues: Difficult to interpret and trade-offs are almost always encountered in engineering and planning

Issues: IPC slash numbers are generic categories and on critical designs, properties may vary too much within a given slash sheet number

Issues: The best method to specify laminates however, when using multiple vendors they may not all support the specific materials

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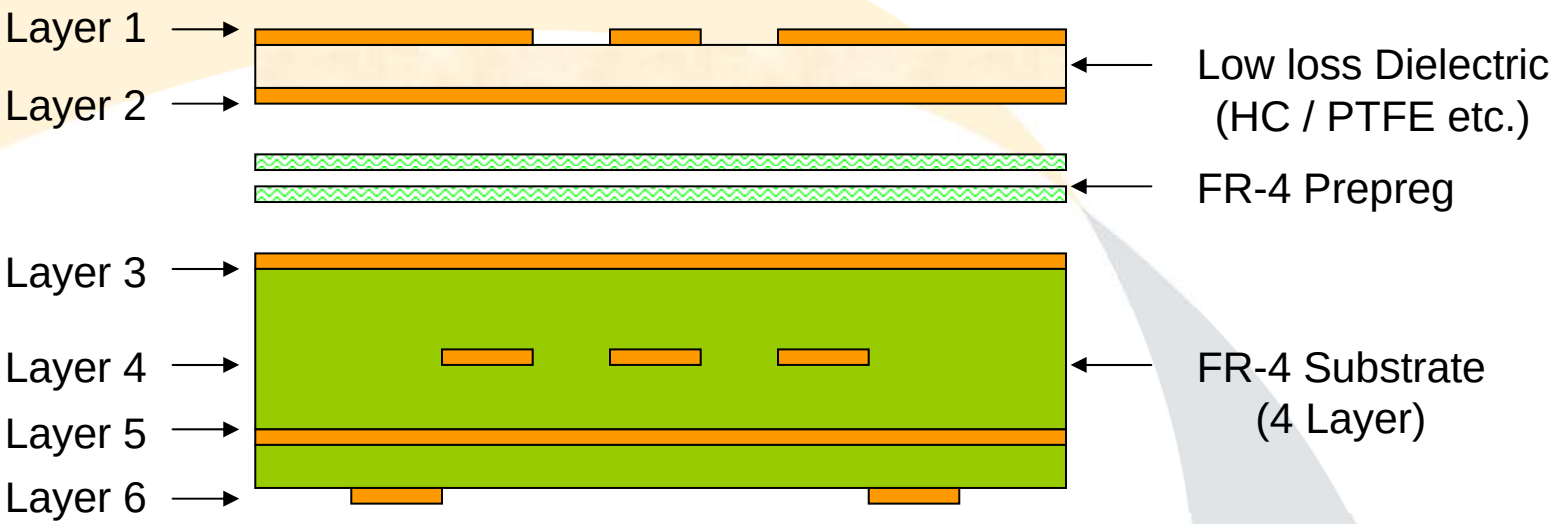
Mixed Dielectric Substrates

- Mixed dielectric constructions reduce cost by only using more expensive low loss materials where needed
- FR-4 Epoxy-Glass Sub-Cores provide structural support when using PTFE based laminates



Typical mixed dielectric construction with low loss cap layer

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Summary

Laminate materials play an important role in PCB performance:

- Laminates consist of a resin system and reinforcement material, depending upon the laminate they are woven glass, ceramic or glass microfibers

- Dielectric properties are highly dependant on the ratio of resin to the reinforcing material

- Specialty laminates are often required when thermal-mechanical or high frequency requirements exceed the properties of standard multifunctional epoxy based laminates

- Care should be taken when specifying laminate materials so boards can be produced consistently from lot to lot

- Specialty or “exotic” laminates come at a significant cost premium and hybrid constructions can offer significant cost reduction

Design Considerations for Mechanical Via-In-Pad

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Plated Through Hole PCB Technology Constraints

As density increases one needs to explore options beyond the standard plated through hole (PTH) technology

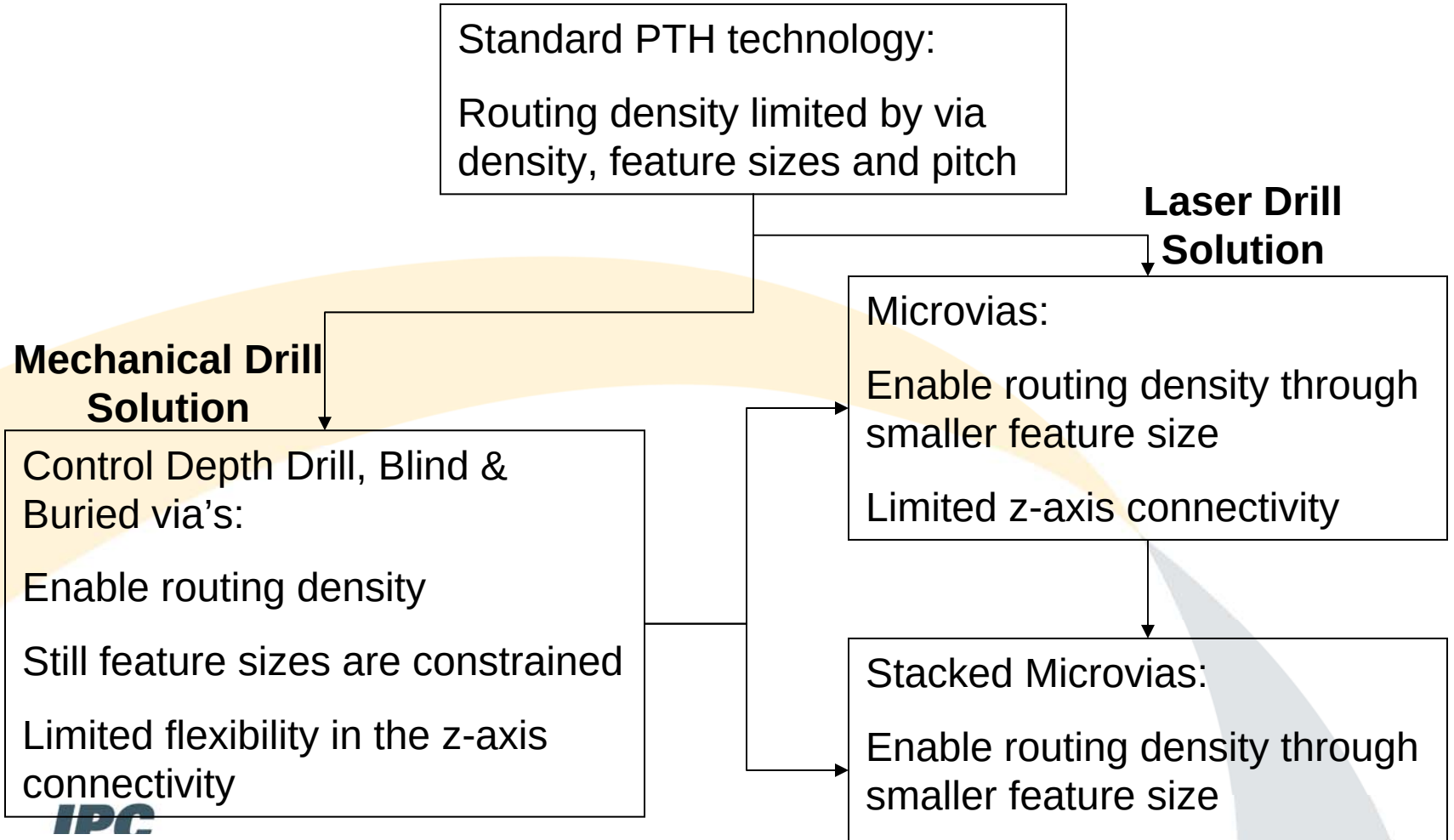
- Standard PTH PCB technology constraints
  - Mechanical drilled hole size
  - Plating aspect ratio (Thickness : Hole size)
  - PTH reliability / Lead Free
  - Minimum line width
  - Layer count
  - High speed via transitions

Technology options for high density features

There are many technology options that will enable high density features. In order to successfully provide these options a PCB fabricator needs to be well invested in highly sophisticated equipment for tooling, imaging, mechanical drilling, laser drilling, registration systems, and will also need significant copper plating capabilities

- Technology options to enable high density features
  - Via-In-Pad technologies
  - Blind via (sequential lamination)
  - Blind and Buried via (sequential lamination)
  - Control depth drilling
  - Laser Microvia
  - Stacked Microvia
  - All of the above (highly complex boards)

Engineering considerations for via structures



Once you leave through hole designs the goal is to find the via combination that maximizes trace routing density at the lowest cost

Mechanical Via-In-Pad (VIP)

Via is the essence of connectivity in a multi-layer PCB which connects one layer to any and all of the other layers. And with the advent of shrinking devices with smaller footprint comes the challenge of routing circuits as available real estate is limited. In order to overcome this challenge the PCB designer started introducing plated through hole Via-In-Pad (VIP) technology, which requires the fabricator to wrap plate followed by selective barrel plate, via fill process (conductive or non-conductive via fill material), planarization to remove excess via fill material from the surface, and finally followed by plating over the vias to define the pads (or land) of the PCB during final plating process

HDI (high density interconnect) is the evolution to next level of density; a transition to sub 0.4mm pitch devices that will utilize microvias and stacked microvias to fan-out fine pitch array pattern as is the case in a **BGA and other Chip Scale Package requirements**

Advantages of Via-In-Pad Construction

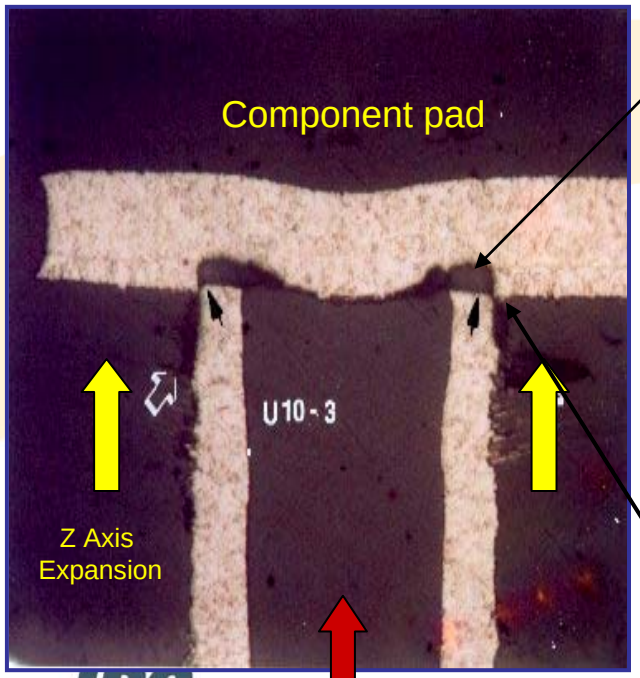
- Solution for high pin count devices because it gives the designer flexibility of increased routing density on surface layers by eliminating the need for dog-bone
- Pads only structure possible on outer layers for high reliability (minimizes issues related to surface etch)
- Reduced inductance on power and ground connections
- Increased pad adhesion for high mass components
- Increased surface area on thermal pads and prevent solder from wicking down the vias during assembly
- Provides a planar surface over the vias for ease of component placement during PCBA

First Generation Via-In-Pad Prior To Copper Wrap Plating Failure Mechanisms

First generation Via-In-Pad process:

- Drill panel after lamination, Electroless Cu, Barrel plate
- Fill via with conductive or non-conductive filler
- Planarize surface
- Electroless copper plate
- Electrolytic copper over plate (Pattern Plate)

Planarization = resulted in a **butt-joint** between barrel plate and surface copper foil



Failure result from differential expansion between the high expansion dielectric and the low expansion copper. Fractures generally occur at the copper grain boundary (electroless) Between the plated hole wall and the copper foil And the Cu over plate and top of the hole barrel

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Low Tg high expansion via filler material

Revised IPC 6012B Specification For Wrap Plating Thickness

3.6.2.11.1 Copper Wrap Plating Copper wrap plating minimum as specified in Table 3-2 **shall** be continuous from the filled plated hole onto the external surface of any plated structure and extend by a minimum of 25 µm [984 µin] where an annular ring is required (see Figures 3-13 and 3-14). Reduction of wrap-plating by processing (sanding, etching, planarization, etc.) resulting in insufficient wrap plating is not allowed (see Figure 3-15).

Add new Figure 3-13 as follows:

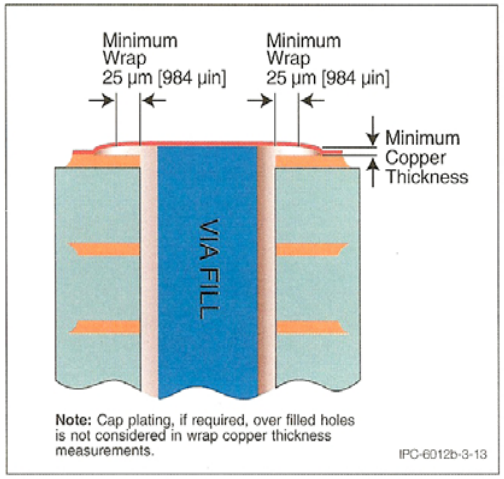

Figure 3-13 Surface Copper Wrap Measurement (Applicable to all filled plated-through holes)

Add new Figure 3-14 as follows:

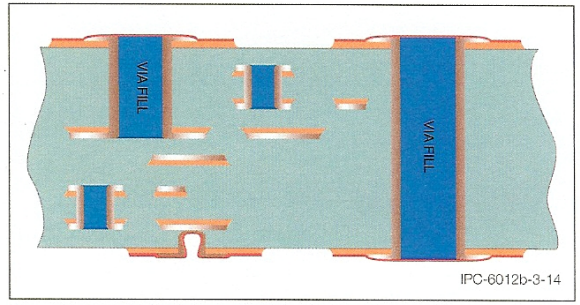

Figure 3-14 Wrap Copper in Type 4 PCB (Acceptable)

Add new Figure 3-15 as follows:

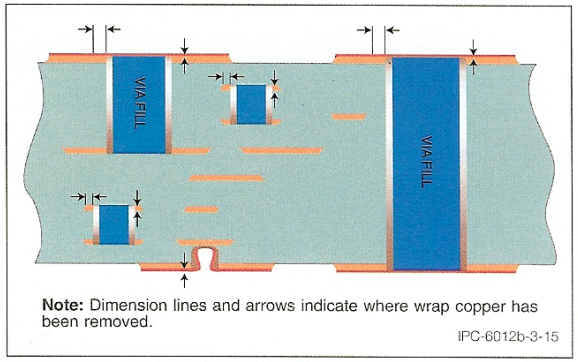

Figure 3-15 Wrap Copper Removed by Excessive Sanding/Planarization (Not Acceptable)

3.6.2.13 Minimum Surface Conductor Thickness The minimum total (copper foil plus copper plating) conductor thickness after processing **shall** be in accordance with Table 3-8. When the procurement documentation specifies a minimum copper thickness for external conductors, the test coupon or production board **shall** meet or exceed that minimum thickness. The minimum surface conductor thickness after processing values given in Table 3-8 are determined by the following equation:

Minimum Surface Conductor Thickness = a + b - c

Where:

a = Absolute copper foil minimum (IPC-4562 nominal less 10% reduction).

b = Minimum copper plating thickness (20 µm [787 µin] for Class 1 and 2; 25 µm [984 µin] for Class 3).

c = A maximum variable processing allowance reduction.

3.2.6.2 Additive Copper Depositions Additive/electroless copper platings applied as the main conductor metal **shall** meet the requirements of this specification.

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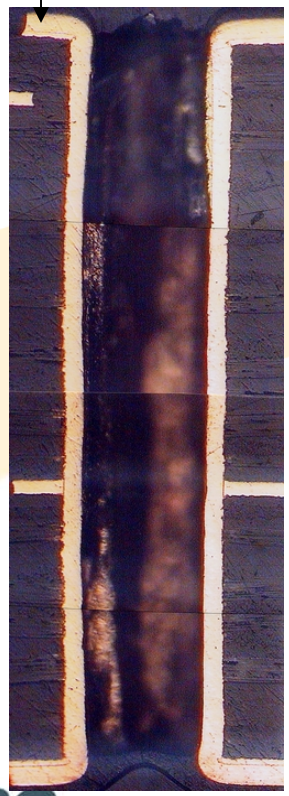
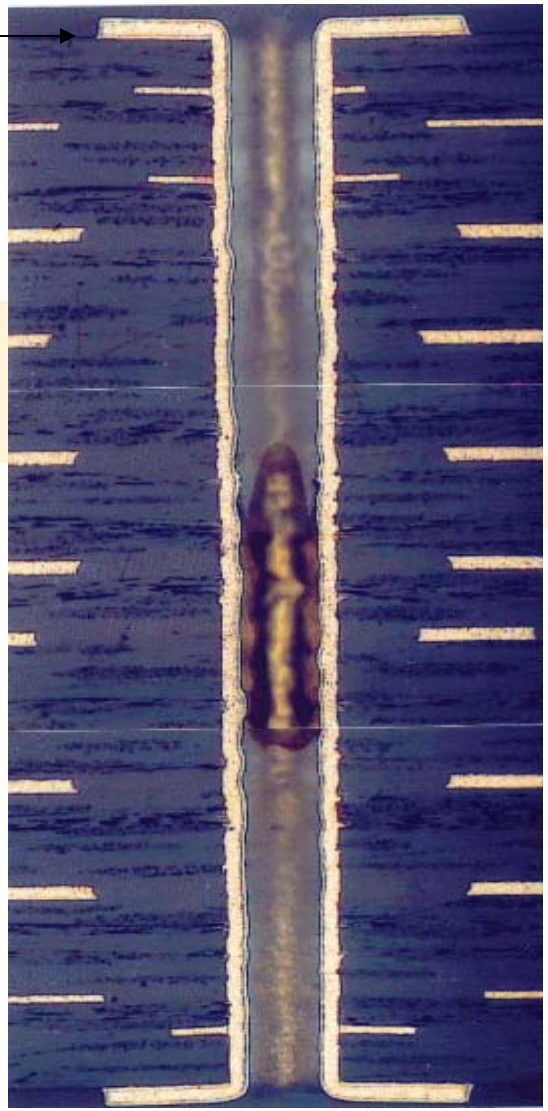
Copper Wrap Plate - Background Review

- Reliability concerns led to the implementation of wrap plating requirements for via filled plated holes (ref. IPC 6012B Amendment 1 p. 3.6.2.11.1)
  - Class 2 - 0.000197” (5 micron) min. wrap plating
  - Class 3 - 0.000472” (12 micron) min. wrap plating
- Conventional processing methods to satisfy Class 2 and 3 wrap plating requirements limit the FAB suppliers capability for producing surface feature packaging density (LWS)
- The LWS limitations are magnified with designs requiring multiple wrap plating/sequential lamination steps
- As packaging requirements become more dense, the need for sequential laminations and denser LWS is growing
- Constant dialog between design and fab regarding process capabilities to maintain minimum wrap plating thicknesses often lead to design compromises and/or deviations

Standard through holes maintain a “wrap plate (by default)

“wrap plate”





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Through Hole Via Filling Process & Materials

- Via filling materials come in two forms:
  - Electrically and thermally conductive, they are generally filled with silver particles or a combination of silver and copper
  - Non-conductive fillers are epoxy or polymer based materials
- Application method to apply via fill material in via holes is generally accomplished by a manual or semi-automated squeegee process with vacuum assist
- After via fill process, excess material is removed using automated planarizing equipment

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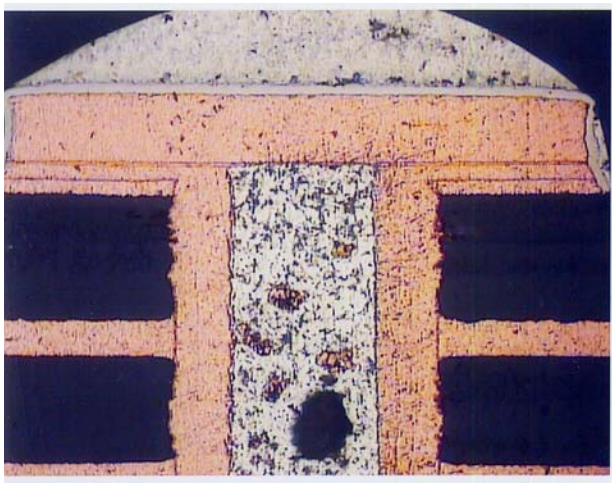
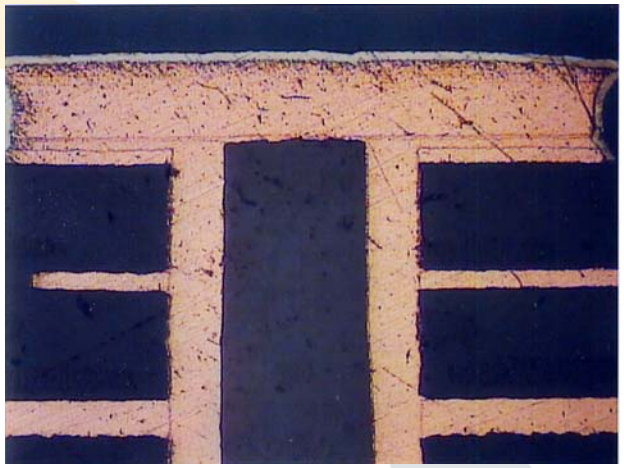
Conventional Process – Industry Standard

1 mm BGA
Mechanical Via-in-Pad

With Wrap-Around Plating



Conductive Via fill



Non-conductive Via fill

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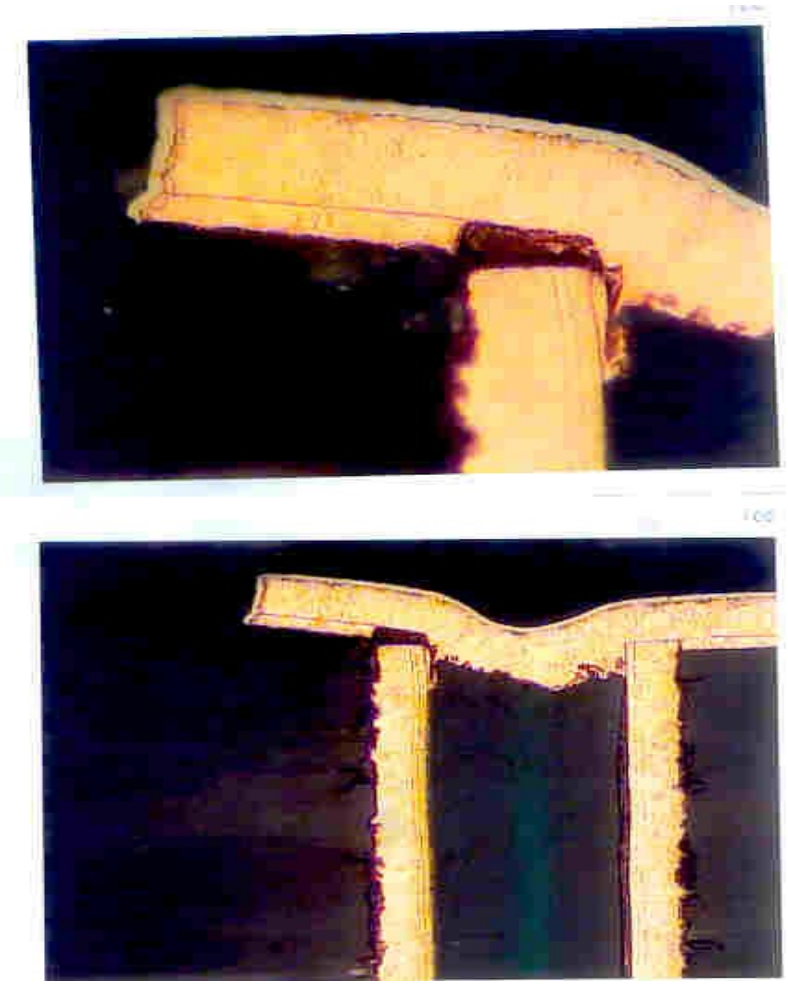
Common Problems with Conventional Wrap Plating Processing

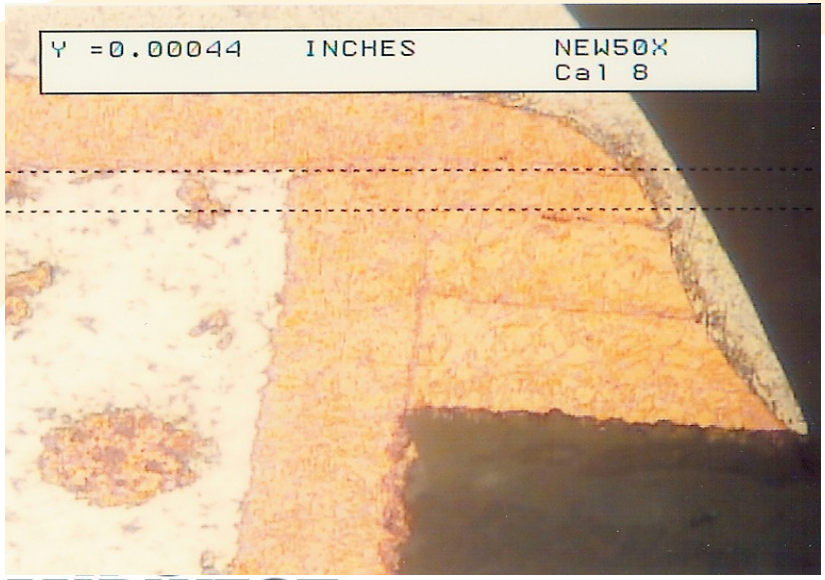
- Example of plating separation following thermal stress
- Wrap plating was removed due to excessive sanding / planarization
- Process control techniques are costly and time consuming
- Current process control techniques are not 100% representative of the entire panel

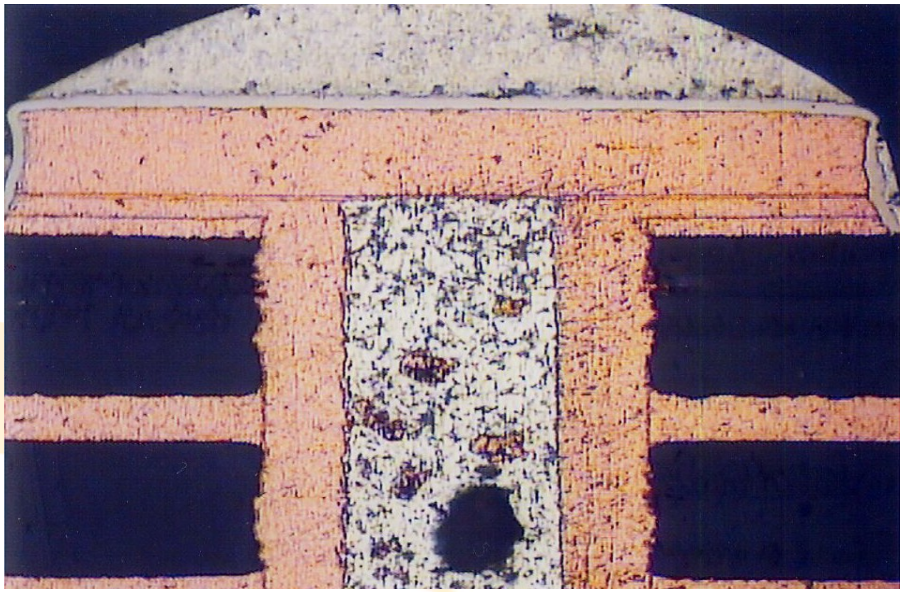


MIDWEST CONFERENCE & EXHIBITION

Common Problems with Conventional Wrap Plating Processing

- Wrap plating onto the surface increases panel copper thickness
- Increased etch factors / process allowances are required due to thicker finished surface copper

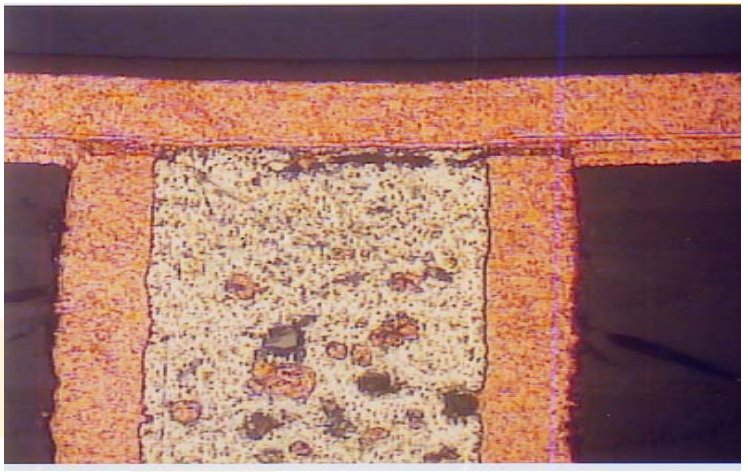


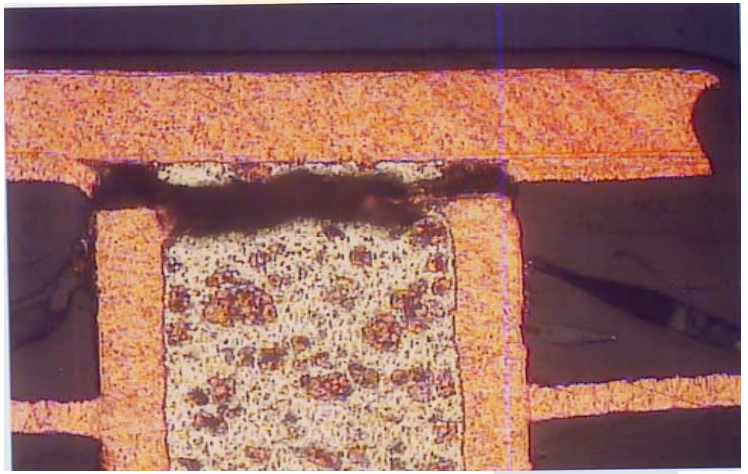


- Issue is magnified on products requiring multiple lamination steps
- Third wrap plating thickness is below .0005” min. class 3 requirement

Common Problems with Conventional Wrap Plating Processing

- Even with wrap plating – evidence of starter cracks and full separation have been observed
- Experience has shown that choice of via fill material and wrap plating thickness are key factors in ability to withstand thermal stress
- Due to surface density requirements often times design compromises are implemented
  - Reduced wrap thickness, class 2 vs. class 3
  - Alternate packaging with wider LWS
  - Reduced starting foil thickness

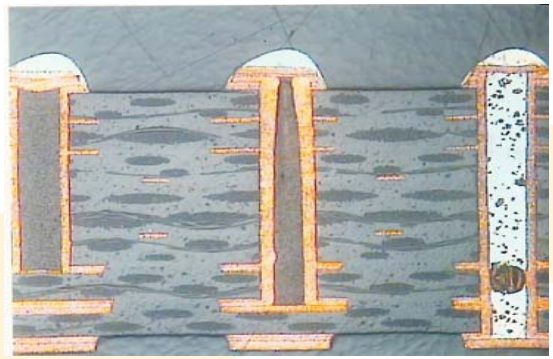




IPC MIDWEST CONFERENCE & EXHIBITION

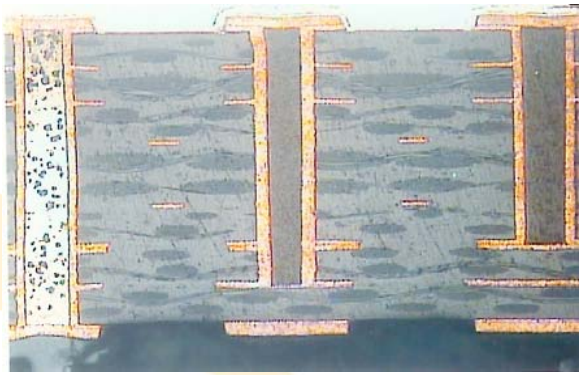
Conventional vs. New Technology Surface Copper Comparison

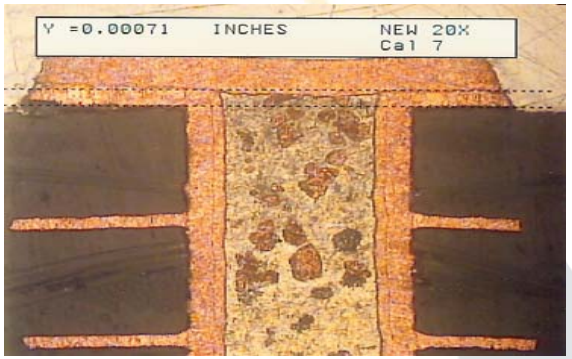
Conventional Wrap Plating
(3x wrap on a common layer)



.012” finished pad dia.

New Technology
(3x wrap on a common layer)

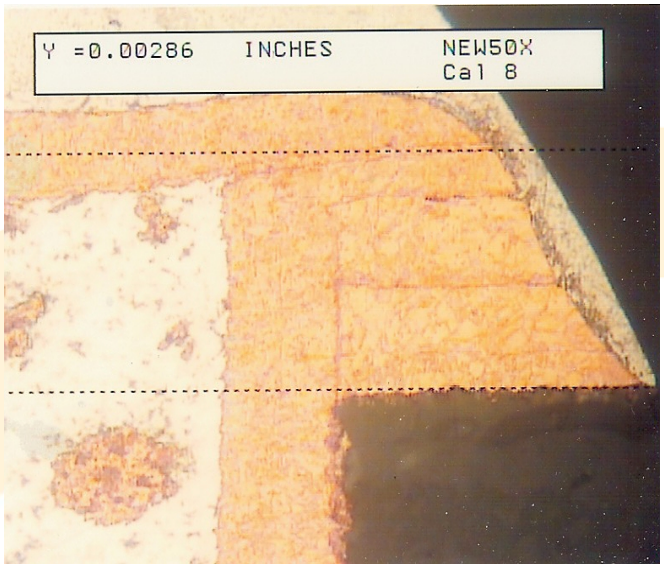




.018” finished pad dia.

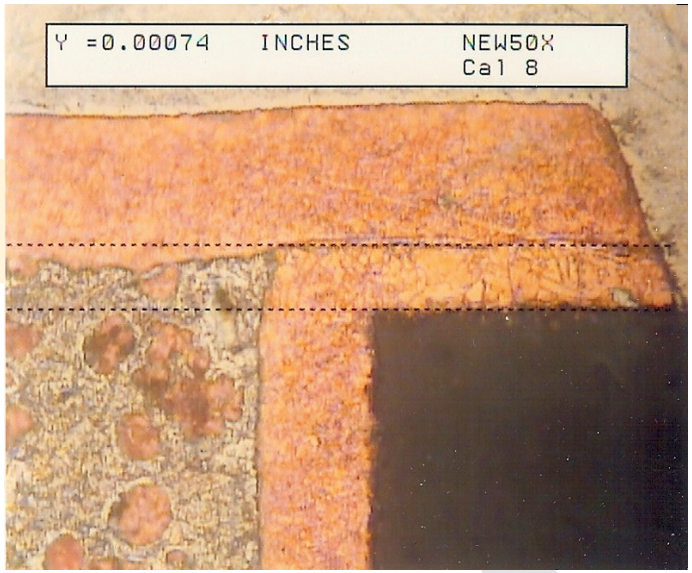
Conventional vs. New Technology Surface Copper Comparison

Conventional Wrap Plating
(3x wrap on a common layer)



Surface Copper Thickness
~ .0022” minimum
~ .003” - .004” typical

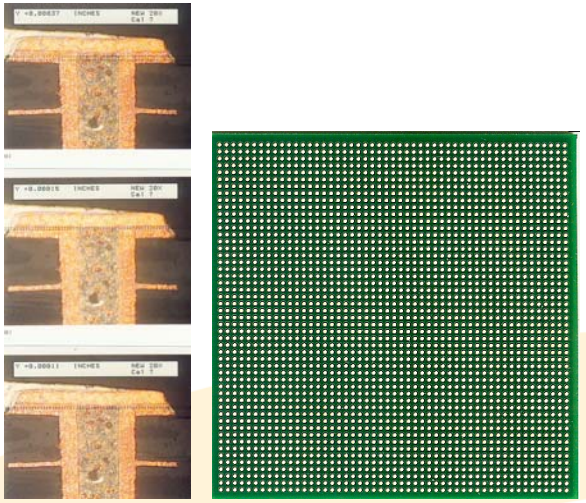
New Technology
(3x wrap on a common layer)

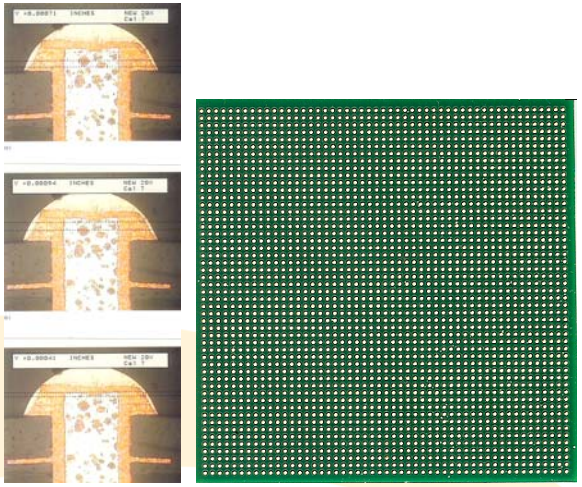


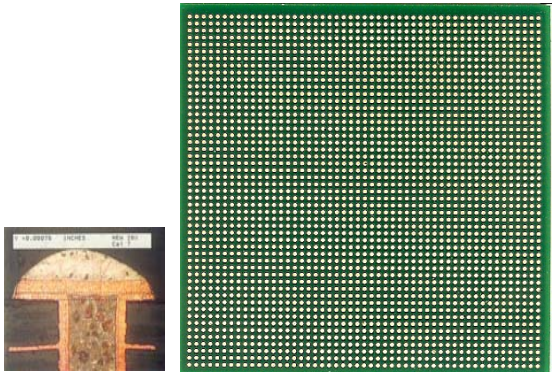
Surface Copper Thickness
~ .0007” typical

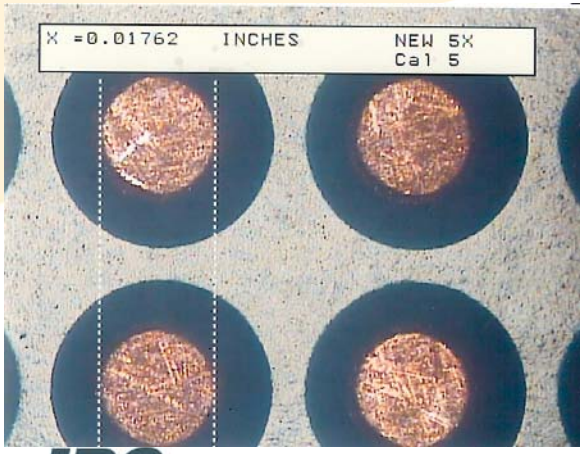
IPC MIDWEST CONFERENCE & EXHIBITION

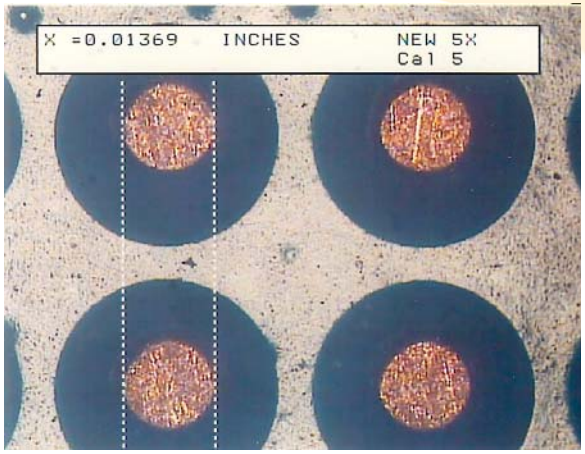
Conventional vs. New Technology Pad Size & Pad Height Comparison

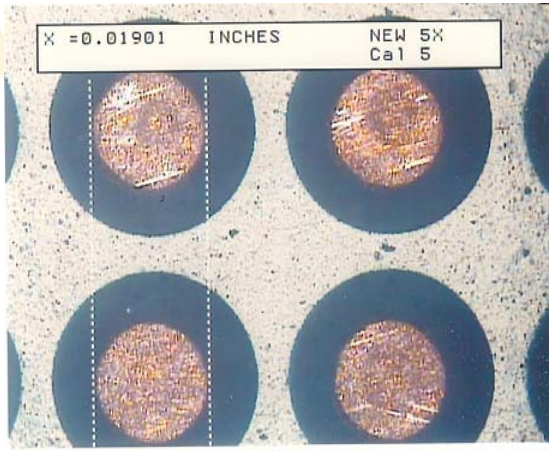












CONVENTIONALCLASS 2 WRAP
Pad dia.: 0.01762” (447 microns)

CONVENTIONALCLASS 3 WRAP
Pad dia.: 0.01369” (347 microns)

NEW TECHNOLOGY CLASS 3 WRAP
Pad dia.: 0.01901” (482 microns)

Wrap Plating design Guideline Comparison

Conventional Wrap Plate Design Guidelines

Design Rule	IPC 6012B Class 2 - assume a starting copper foil of 3/8 oz				IPC 6012B Class 3 - assume a starting copper foil of 3/8 oz			
	No Wrap	1 X Wrap	2 X Wrap	3 X Wrap or greater	No Wrap	1 X Wrap	2 X Wrap	3 X Wrap or greater
Preferred	0.003" Line	0.005" Line	0.006" Line	0.006" Line	0.003" Line	0.005" Line	0.006" Line	Call
	0.0035" Space	0.005" Space	0.007" Space	0.009" Space	0.0035" Space	0.00575" Space	0.0085" Space	
Advanced capability = reduced yield (call engineering prior to quote)	0.003" Line	0.004" Line	0.005" Line	0.006" Line	0.003" Line	0.005" Line	0.006" Line	Call
	0.003" Space	0.005" Space	0.006" Space	0.008" Space	0.003" Space	0.0055" Space	0.0075" Space	

Note: Due to the overhang (caused by undercut during etch) all Gold body jobs or designs that utilize Gold as an etch resist and require wrap plating to meet IPC 6012B, Class 2 or 3 specification, will need engineering approval prior to quote……no exceptions

DDi *FLAT-WRAP*™ Technology Design Guidelines

Design Rule	IPC 6012B Class 2 - Starting copper weight 3/8 oz				IPC 6012B Class 3 - Starting copper weight 1/2 oz			
	No Wrap	1 X Wrap	2 X Wrap	3 X Wrap or greater	No Wrap	1 X Wrap	2 X Wrap	3 X Wrap or greater
Preferred	0.003" Line	0.003" Line	0.003" Line	0.003" Line	0.0035" Line	0.0035" Line	0.0035" Line	0.0035" Line
	0.0035" Space	0.0035" Space	0.0035" Space	0.0035" Space	0.004" Space	0.004" Space	0.004" Space	0.004" Space
Advanced capability = reduced yield (call engineering prior to quote)	0.003" Line	0.003" Line	0.003" Line	0.003" Line	0.003" Line	0.003" Line	0.003" Line	0.003" Line
	0.003" Space	0.003" Space	0.003" Space	0.003" Space	0.0035" Space	0.0035" Space	0.0035" Space	0.0035" Space

Note: Gold body jobs or designs that utilize Gold as an etch resist and require wrap plating to meet IPC 6012B, Class 2 or 3 specification, will not need engineering approval if PCB's are fabricated with **this new t**echnology

New Technology Reliability Test Matrix

Description of Tests					Remarks	Test Status	Test Results
Manufacturability Tests	As received - Microsection PTH Quality	Plated Barrel Copper Thickness	Record Avg Plating Thickness		Microsection analysis performed by DDi	Completed	Passed
Pb-Free Assy Process Compatibility	Solder Float Test - Microsection PTH Quality	Temperature Deg C (Deg F)	260 (500)	3X	BGA coupons - DDi	Completed	Passed
				6X	BGA coupons - DDi	Completed	Passed
			288 (550)	3X	BGA coupons - DDi	Completed	Passed
				6X	BGA coupons - DDi	Completed	Passed
	Pb Free Reflow Assembly Simulation	Temperature Deg C (Deg F)	260 (500)	4X	Microtek Labs to process BGA coupons through Pb Free profile through IR Reflow oven and DDi to do microsection analysis	Completed	Passed
				6X			Passed
Reliability Tests	IST - Interconnect Stress Test	IST Pre-conditioning cycles at 260 C	4X		3 coupons / preconditioning (Total of 18 coupons). Dual sense test performed by DDi VA. Two different test conditions with San-Ei & CB100 via fill materials	Completed & Reported by Avg Cycles	Blind Vias No Failure & Thru Vias Pass 864 @ 6X & 1176 @ 4X
			6X				
		Pb Free Assembly Profile Pre-conditioning, peak temp 260 C	4X		IST testing to be perfromed by PWB Corp, Dual Sense to 1000 cycles	Completed & Reported by Avg Cycles	Blind Vias No Failure & Thru Vias Pass 731 @ 6X & No Failure @ 4X
			6X				
	HATS - Highly Accelerated Thermal Shock	Pb Free Assembly Profile Pre-conditioning, peak temp 260 C	0		12 coupons tested. Test performed by Microtek Labs. Two different test conditions with San-Ei & CB100 via fill materials	Coupons tested by MicroTek to 1000 cycles	Passed
			4X				Passed
			6X				987 average cycles

New Technology - Benefits

- Consistent wrap plate thickness matching the thickness of the initial surface foil. Minimum wrap and copper thickness in accordance with IPC6012 B
- Increased reliability due to wrap plate uniformity over the entire panel surface
- Eliminates copper thickness build-up during multiple wrap plating cycles on a common layer
- Consistent impedance values on the plated layers with copper filled holes due to improved surface plating distribution
- Improved dielectric thickness on all sub-laminations between the sub-outer plated layer and the subsequent laminated layer.
- Reduced surface copper thickness enhances the fabrication process for designs with fine lines and tighter geometries
- Improved solder mask thickness uniformity due to reduced copper feature height

Thank You

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