Pb-Free Reflow, PCB Degradation, and the Influence of Moisture Absorption

Kerin O'Toole, Bob Esser, Seth Binfield,
Craig Hillman, Cheryl Tulkoff and Joe Beers
DfR Solutions / Gold Circuits

IPC Midwest 2009

Executive Summary

Cracking and delamination defects in printed circuit boards (PCBs) during elevated thermal exposure have always been a concern for the electronics industry. However, with the increasing spread of Pb-free assembly into industries with lower volume and higher complexity, these events are occurring more frequently. Several telecom and enterprise original equipment manufacturers (OEMs) have reported that the robustness of their PCBs is their number one concern during the transition from SnPb to Pb-free. Cracking and delamination within PCBs can be cohesive or adhesive in nature and can occur within the weave, along the weave, or at the copper/epoxy interface. The role of moisture absorption and other PCB material properties on this phenomenon is still being debated.

This presentation details research initiated to better understand the influence of moisture on delamination using capacitance measurements. Measurable changes in capacitance were recorded in the PCBs after each reflow. Discrimination between different test structures and MSL exposures strongly suggests the capacitance approach measures true material degradation rather than an increase in resistance at contact pads due to oxidation. However, contact resistance should be quantified in a next round of testing. Strong differences in shield-over-shield capacitance between test structures are interesting and should also be further characterized.

Pb-Free Reflow, PCB Degradation, and the Influence of Moisture Absorption

Kerin O'Toole, Bob Esser, Seth Binfield,
Craig Hillman, Cheryl Tulkoff and Joe Beers
DfR Solutions / Gold Circuits

IPC MIDWEST
CONFERENCE & EXHIBITION

Introduction

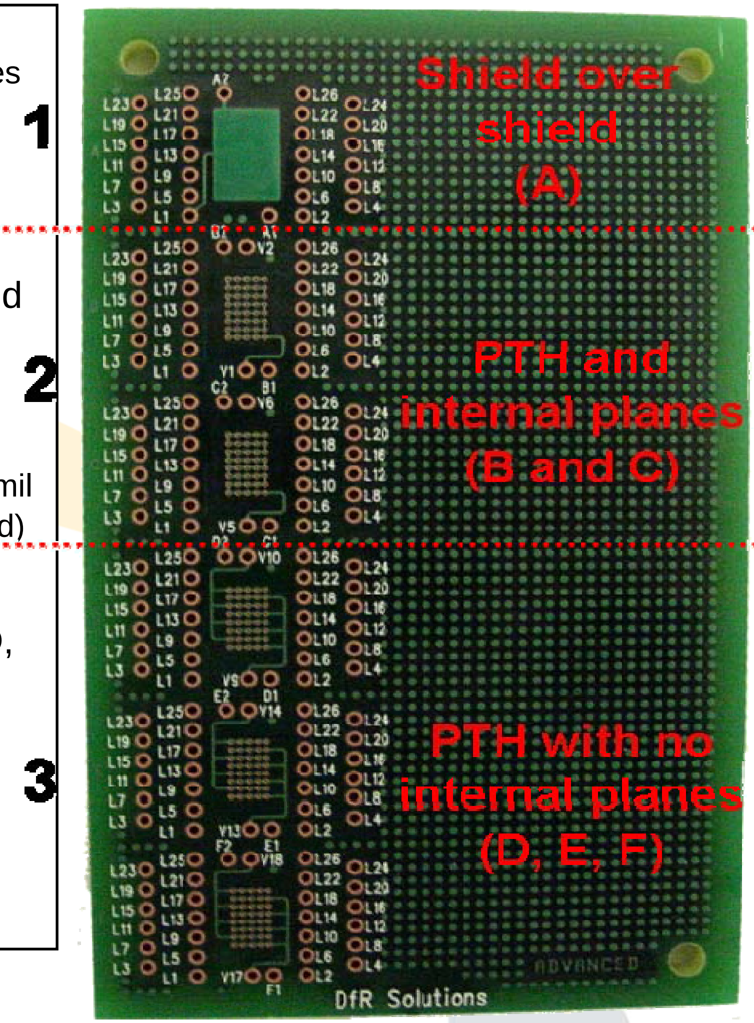
- An increasing number of clients of DfR Solutions are reporting cracking and delamination of printed circuit boards
  - Predominantly under Pb-free reflow but some under SnPb reflow conditions
- Several telecom and enterprise OEMs are reporting PCB robustness is their primary concern regarding Pb-free reliability
- Cracking or delamination during reflow is a stress vs. strength phenomenon
  - Either the environmental stress was higher than expected or the material strength was lower than expected

Research Study

- An earlier customer case study showed:
  - Initial reduction in PCB cracking / delam after baking for 48 hours at 125C
    - Could suggest de-absorption of moisture
    - May also suggest sublimation of volatiles or a cure process that is improving adhesion
  - Final elimination of cracking / delam after baking for 48 hours at 125C and reducing maximum reflow temperature to 245C
- To better assess the root cause of delamination of printed circuit boards, an internal study on the influence of moisture absorption was initiated.

Coupon Design

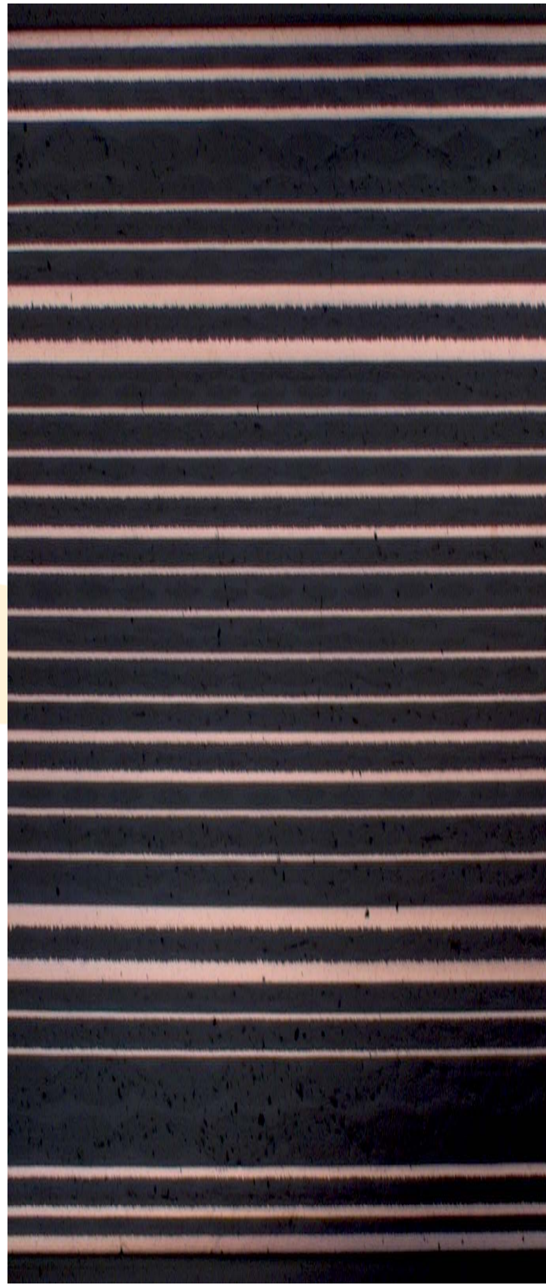
- Two coupon designs (Standard / Advanced)
  - Each coupon design has three sections and six test structures
- Section 1: 'Shield over shield' (Test Structure A)
  - Plane-to-plane spacing: See slide 4 (same for both standard and advanced designs)
- Section 2: PTH with internal planes (Test Structures B and C)
  - Plane-to-plane spacing: See slide 4 (same for both standard and advanced designs)
  - Drill diameter: Standard: 15 mil; Advanced: 12 mil
  - Clearance: Standard: Drill + 10 mil; Advanced: Drill + 7 mil
  - Pitch: 78 mil (same for both standard and advanced)
  - Pad diameter: 27 mil
- Section 3: PTH with no internal planes (Test Structures D, E, & F)
  - Drill diameter: Standard: 15 mil; Advanced: 12 mil
  - Pitch: Standard: 40 mil; Advanced: 32 mil
  - Pad diameter: 27 mil



IPC MIDWEST CONFERENCE & EXHIBITION

Coupon Stackup

- Board thickness
  - 150 mil (3.75 mm)
- Number of layers
  - 26
- Dielectric thickness
  - 3 mil (75 µm), 4 mil (100 µm), and 5 mil (125 µm)
- Glass fabric
  - 106, 1080, 7628, and 2116
- Copper foil thickness
  - 0.5 oz (17.5 µm), 1 oz (35 µm), and 2 oz (70 µm)



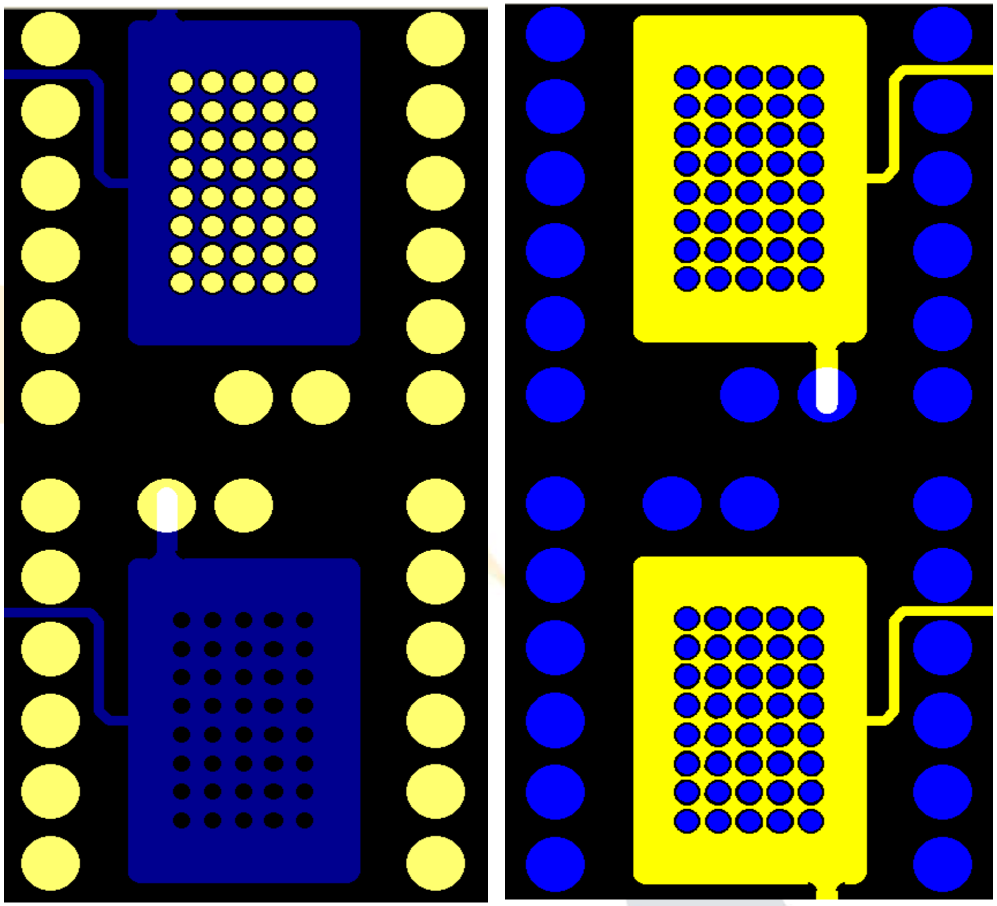
1	0.65	foil 1/2 oz	
	3	prepreg	1 x 1080
2	0.65	1 oz	
	4	core	
3	0.65	1 oz	
	14	prepreg	2 x 7628
4	0.65	1/2 oz	
	4	core	
5	0.65	1/2 oz	
	5	prepreg	2 x 1080
6	2.4	2 oz	
	4	core	2 x 106
7	2.4	2oz	
	5	prepreg	1080 + 211
8	0.65	1/2 oz	
	5	core	1 x 2116 H
9	0.65	1/2 oz	
	3	prepreg	1 x 1080
10	1.4	1 oz	
	4	core	2 x 106
11	1.4	1 oz	
	3	prepreg	1 x 1080
12	0.65	1/2 oz	
	5	core	1 x 2116 H
13	0.65	1/2 oz	
	5	prepreg	1080 + 211
14	0.65	1/2 oz	
	5	core	1 x 2116 H
15	0.65	1/2 oz	
	3	prepreg	1 x 1080
16	1.4	1 oz	
	4	core	2 x 106
17	1.4	1 oz	
	3	prepreg	1 x 1080
18	0.65	1/2 oz	
	5	core	1 x 2116 H
19	0.65	1/2 oz	
	5	prepreg	1080 + 211
20	2.4	2 oz	
	4	core	2 x 106
21	2.4	2oz	
	5	prepreg	2 x 1080
22	0.65	1/2 oz	
	4	core	
23	0.65	1/2 oz	
	14	prepreg	2 x 7628
24	0.54	1 oz	
	4	core	
25	0.65	1 oz	
	3	prepreg	1 x 1080
26	0.65	foil 1/2 oz	

Test Structures

- The current design had 6 test structures (A-F), with multiple nets per test structure
- Test Structure A: shield over shield (copper planes with no PTHs)
  - Alternating planes are tied to power (node A1) and ground (node A2)
- Test Structure B: shield over shield (copper planes with PTHs)
  - Non-functional pads on every layer
  - Alternating planes are tied to power1 (node B1) and ground (node B2)
  - PTHs are daisy chained and are tied to power2 (node V1)
- Test Structure C: shield over shield (copper planes with PTHs)
  - Non-functional pads on every other layer
  - Alternating planes are tied to power1 (node C1) and ground (node C2)
  - PTHs are daisy chained and are tied to power2 (node V5)

Test Structures B and C (Example)

- Test structures B (top) and C (bottom)
  - Layer 19 (left)
  - Layer 20 (right)
- Note how non-functional pads are present in both layers for test structure B, but are absent in layer 19 for test structure C



Nets

- Nets A1-A2, B1-B2, and C1-C2 allow measurement of capacitance between layers
- Nets V1-B1, V1-B2, V5-C1, and V5-C2 allow measurement of capacitance between PTHs and layers

Coupon Material

- Manufacturer: ITEQ
  - Product: IT-180
  - High T_g phenolic resin
- Material characteristics
  - Glass transition temperature (T_g): 180^{o}C +/- 5^{o}C (DSC) [1]
  - Decomposition temperature (T_d): 350^{o}C +/- 5% (TMA) [2]
  - No available data on time to delamination
- Astec Power reported that ITEQ IT-180 survived 4 reflow cycles (245^{o}C peak) at MSL3, MSL4, and MSL5 [3]
  - Testing ceased after 4 reflow cycles.

[1] http://www.iteq.com.cn/product.html

[2] "2006 status & 2007 outlook." *Global SMT & Packaging*, January 2007. <http://www.trafalgar2.com/documents/Columns-Custer/7.1-custer.pdf>.

[3] John Kippen. "A Test Coupon Approach to Qualification of Lead-Free PCB Laminates for DC/DC Converters." DCDC Technical White Paper from Astec Power, December 2004. <http://www.astecpower.com/whitepaper/dcdc/Done%20A%20WP-Test%20Coupon%20Approach%20to%20Qualification%20of%20Lead.pdf>.

Phase 1: Simulated Reflow

- 260^{o}C reflow, test 1:
  - 5 advanced coupons*
  - 30 reflow cycles at 260^{o}C peak
  - Monitored shield over shield capacitance (test structure A) out of package and after each reflow cycle
  - All capacitance measurements taken at room temperature (26^{o}C +/-2^{o}C.)
- 280^{o}C reflow:
  - 5 advanced coupons*
  - 12-13 reflow cycles at 280^{o}C peak
  - Monitored shield over shield capacitance (test structure A) out of package and after each reflow cycle
  - All capacitance measurements taken at room temperature (26^{o}C +/-2^{o}C.)

* Note: standard and advanced designs are identical for test structure A (shield-over-shield)

Phase 1: Simulated Reflow, Part 2

- 260^{o}C reflow, test 2:
  - 5 standard coupons
  - 15 reflow cycles at 260^{o}C peak
  - Monitored shield over shield capacitance (test structures A, B, and C) out of package and after each reflow cycle
  - Monitored shield-PTH capacitance (test structures B and C) out of package and after each reflow cycle
  - All capacitance measurements were taken at room temperature (26^{o}C +/-2^{o}C)

IPC MIDWEST CONFERENCE & EXHIBITION

Phase 2: Moisture Sensitivity

Note: GCE noted concerns with long-term exposure to elevated temperature inducing degradation. Future pre-bakes may need to be performed at lower temperatures (~105C)

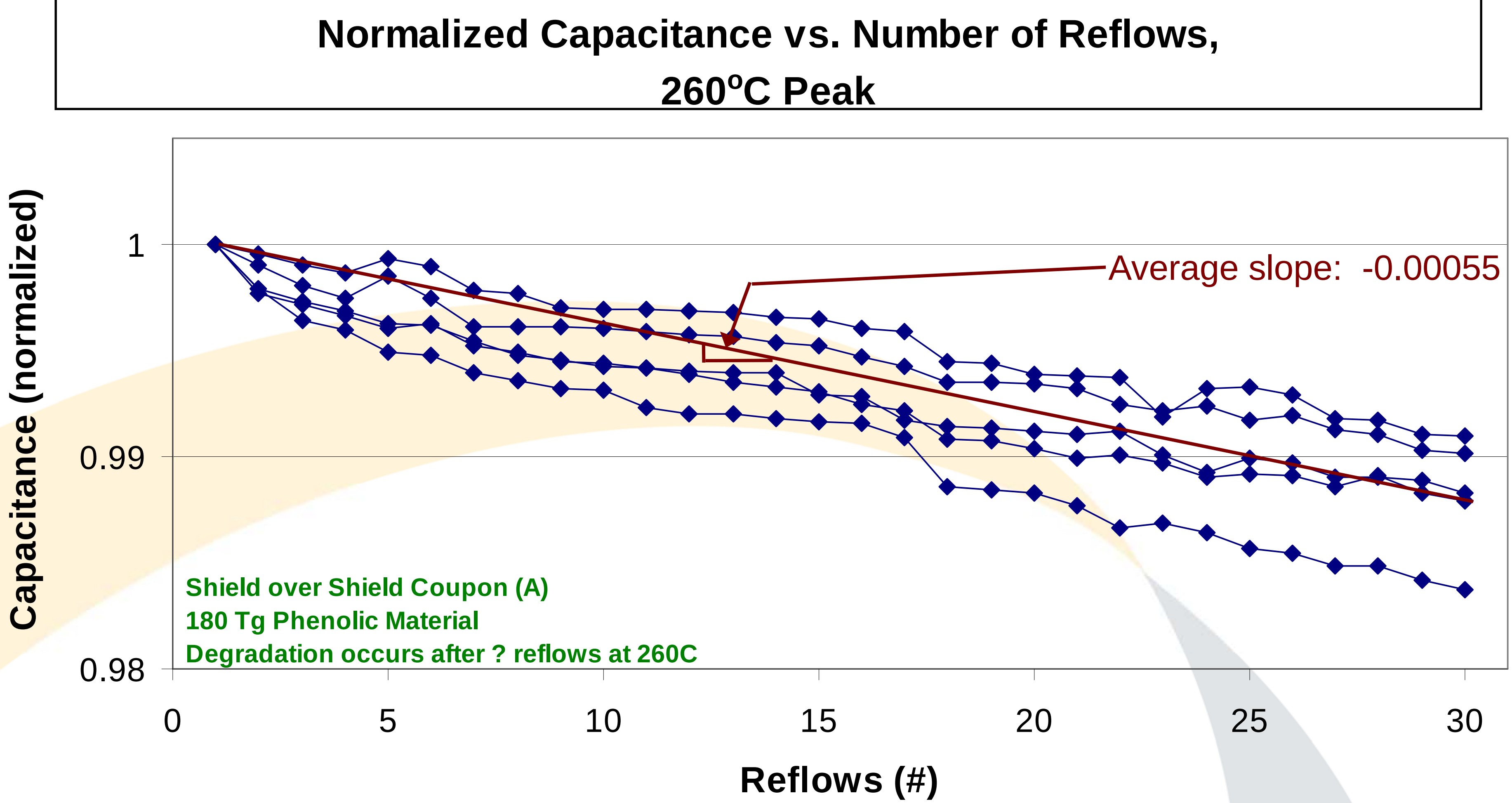
- Protocol:
  - 3 boards per condition
  - 3 conditions: MSL1, MSL2, and MSL2a
  - Boards were dried at 125^{o}C for 72 to 88 hours immediately before humidity testing
  - Humidity testing protocol followed the standards outlined in J-STD-020C
  - All boards were subjected to 3 reflow cycles, starting 15 minutes after removal from humidity chamber
  - Monitored weight gain and capacitance throughout the testing periods

IPC MIDWEST CONFERENCE & EXHIBITION

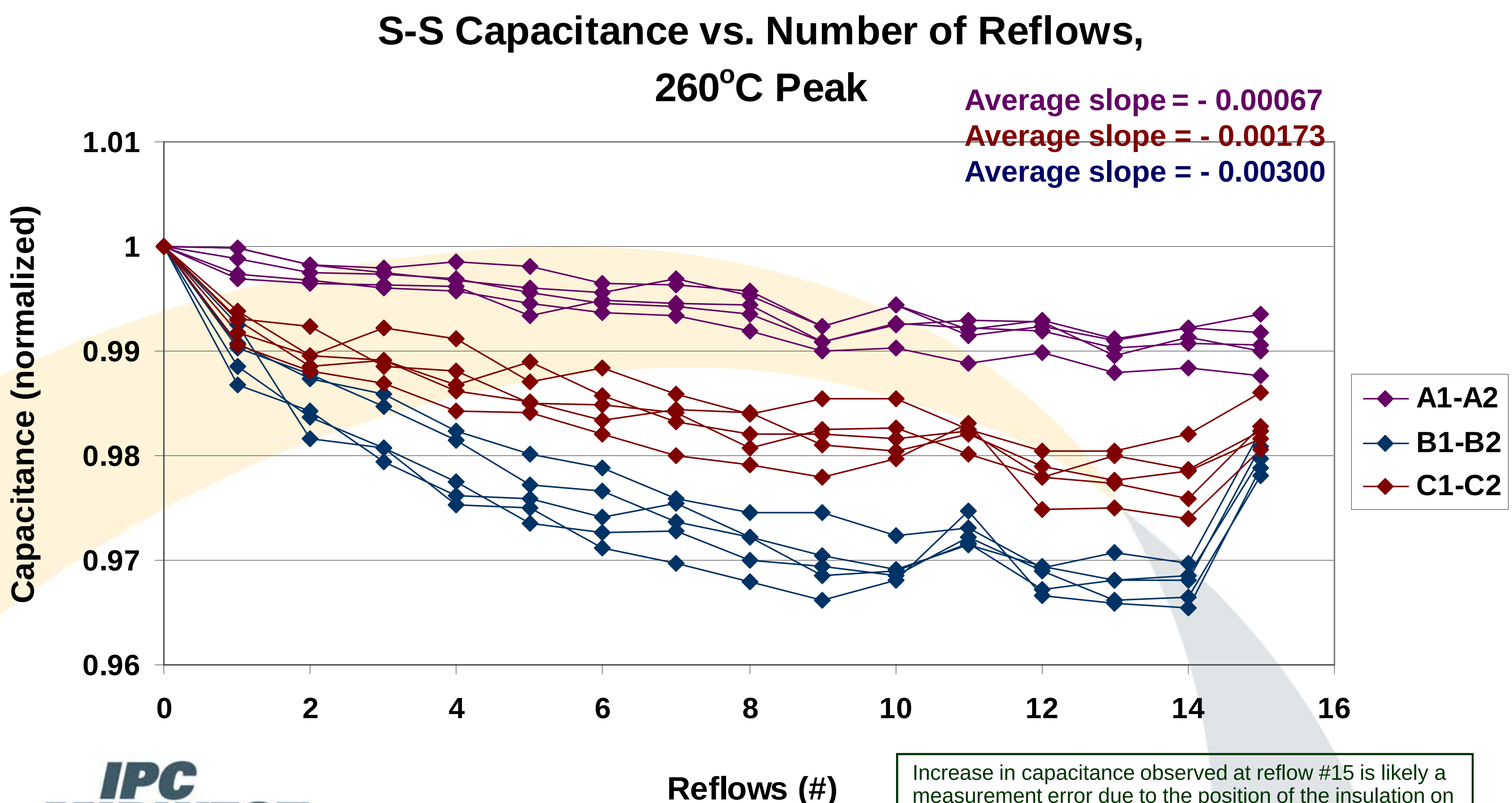
Phase 2: Moisture Sensitivity

- Protocol continued:
  - MSL 1:
    - 88-hour prebake at 125^{o}C
    - 85^{o}C/85%RH, 168 hours
    - Monitored weight gain and shield-shield capacitance on test structure A
  - MSL 2:
    - 88-hour prebake at 125^{o}C
    - 85^{o}C/60%RH, 168 hours
    - Monitored weight gain and shield-shield capacitance on test structure A
  - MSL 2a:
    - 72-hour prebake at 125^{o}C
    - 60^{o}C/60%RH, 120 hours
    - Monitored weight gain and shield-shield capacitance on test structures A-C, as well as shield-PTH capacitance on test structures B and C

Phase 1: 260^{o}C Reflow Results, Test 1

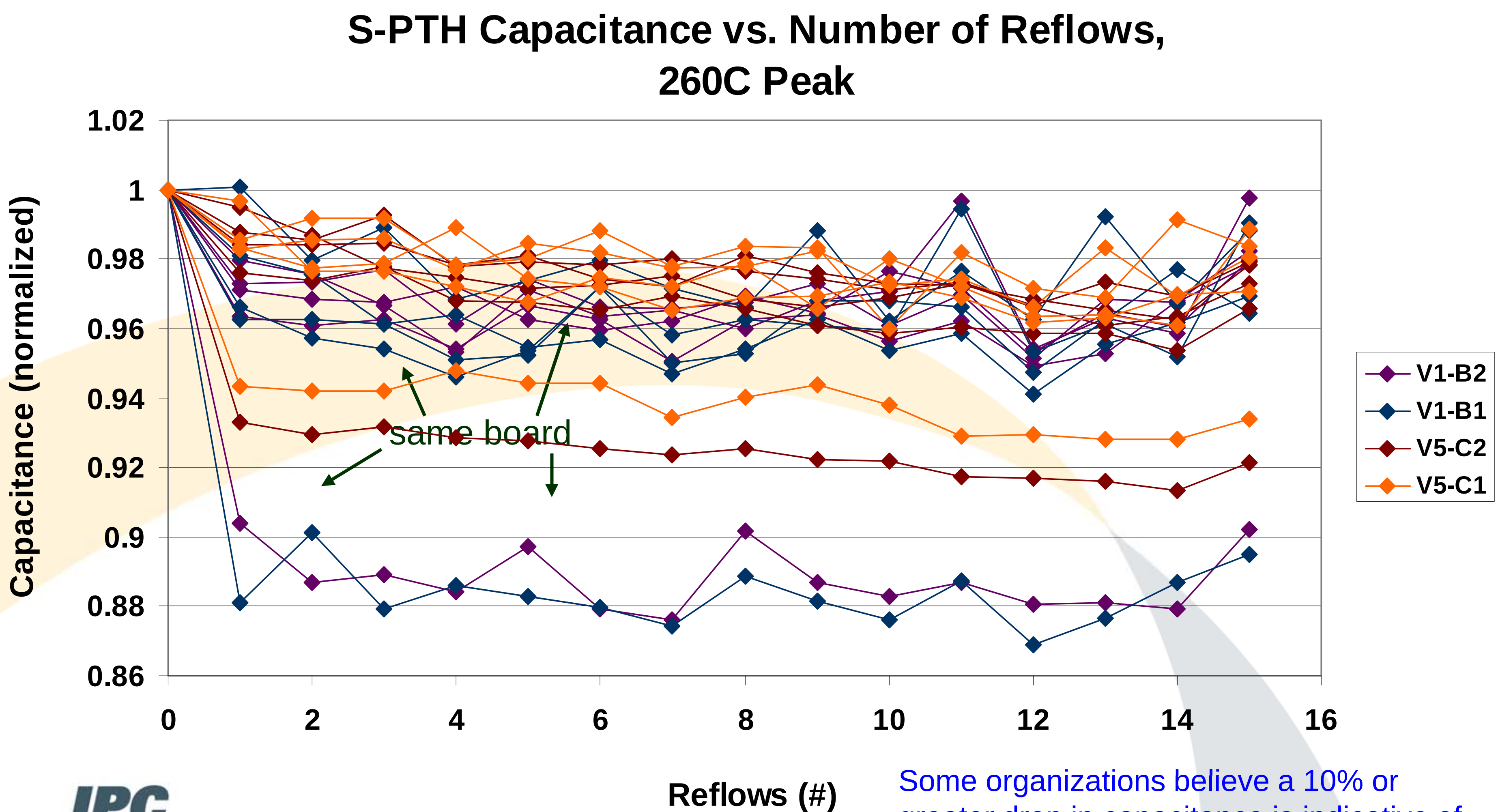


Phase 1: 260°C Reflow Results, Test 2



Increase in capacitance observed at reflow #15 is likely a measurement error due to the position of the insulation on the leads of the measuring device.

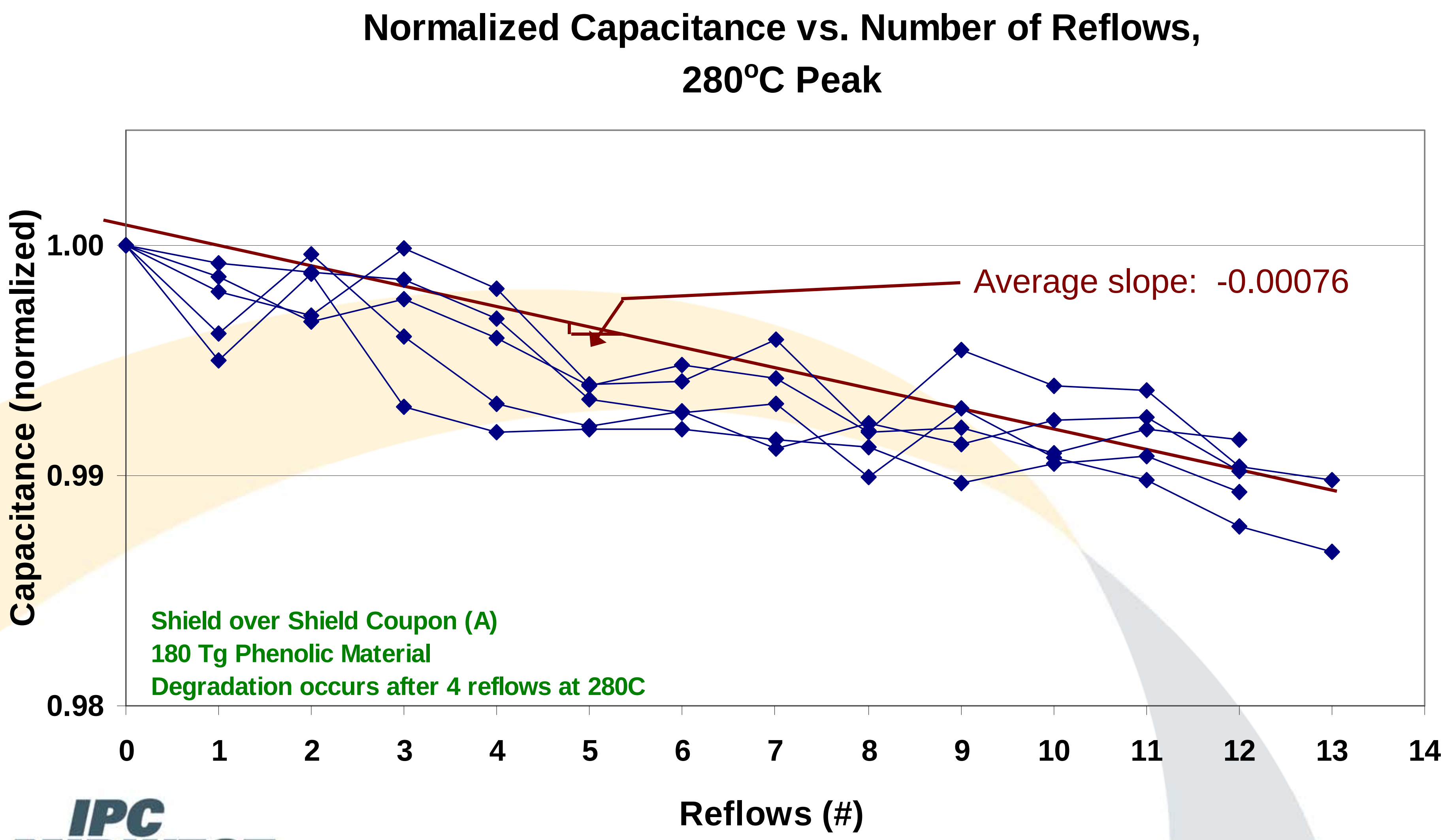
Phase 1: 260^{o}C Reflow Results, Test 2



Some organizations believe a 10% or greater drop in capacitance is indicative of cracking or delamination

IPC MIDWEST CONFERENCE & EXHIBITION

Phase 1: 280^{o}C Reflow Results



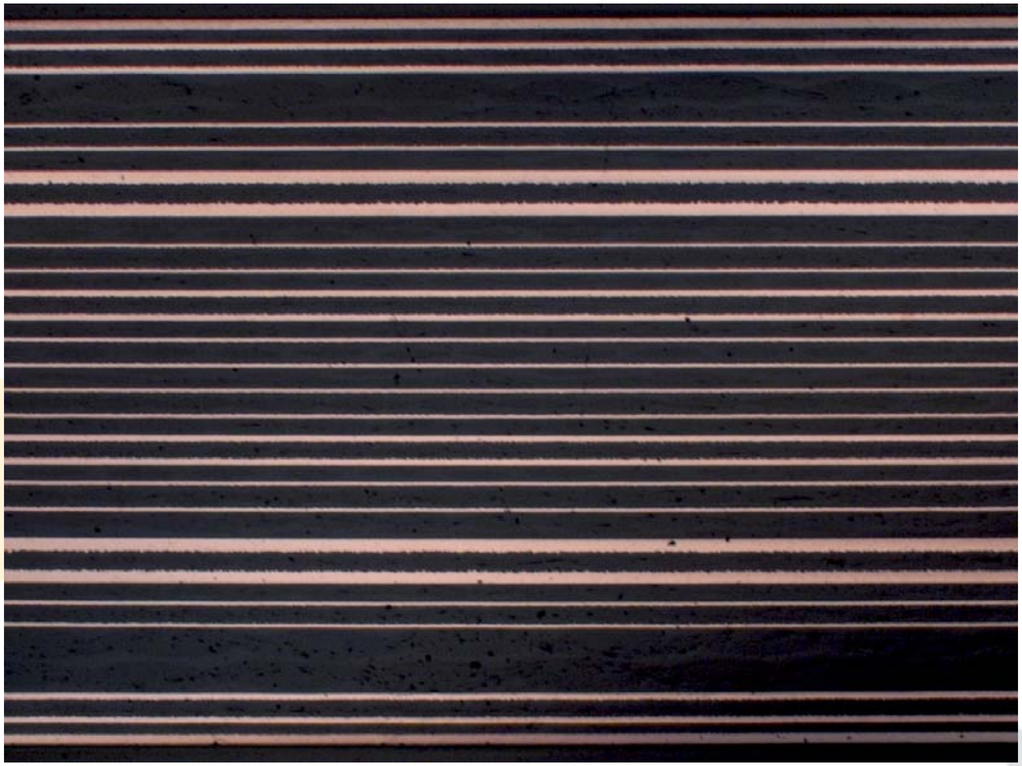
Phase 1: Shield over Shield Observations

- Steady decrease in shield over shield (S-S) capacitance at 260ºC, but no clear roll-off point
- Test structures A, B, and C degrade at different rates, with B showing the greatest change in capacitance
  - Test structure B has an average degradation rate almost 5X greater than that of test structure A
  - Test structure C has an average degradation rate almost 3X greater than that of test structure A
- 280ºC samples show a stronger (~0.5% average) decrease in shield over shield capacitance after 4 reflows, but gradual degradation continues with each subsequent reflow cycle
  - Average degradation rate of the 280ºC samples was approximately 50% greater that of the 260ºC samples

Phase 1: Shield - PTH Observations

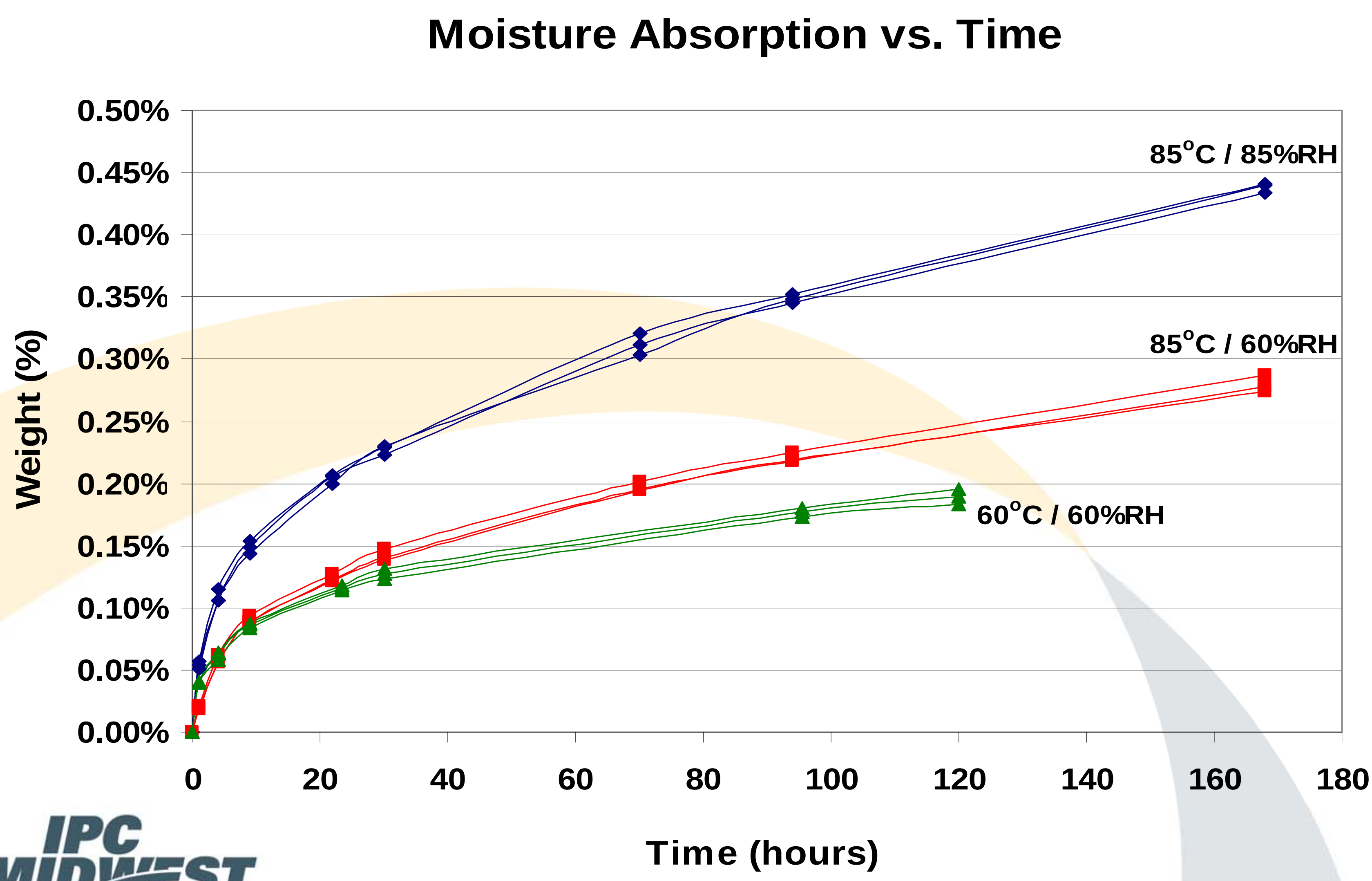
- Shield to PTH (S-PTH) capacitance:
  - A higher degree of degradation compared to shield over shield
    - After just one reflow cycle, the degradation in S-PTH capacitance is comparable to that of the S-S capacitance after 15 reflow cycles.
  - Very significant decrease in capacitance after 4 reflow cycles, followed by very gradual degradation with an extensive degree of variation
  - One board had a much larger decrease in capacitance on all S-PTH nets

Phase 1, Part 1: Cross Section

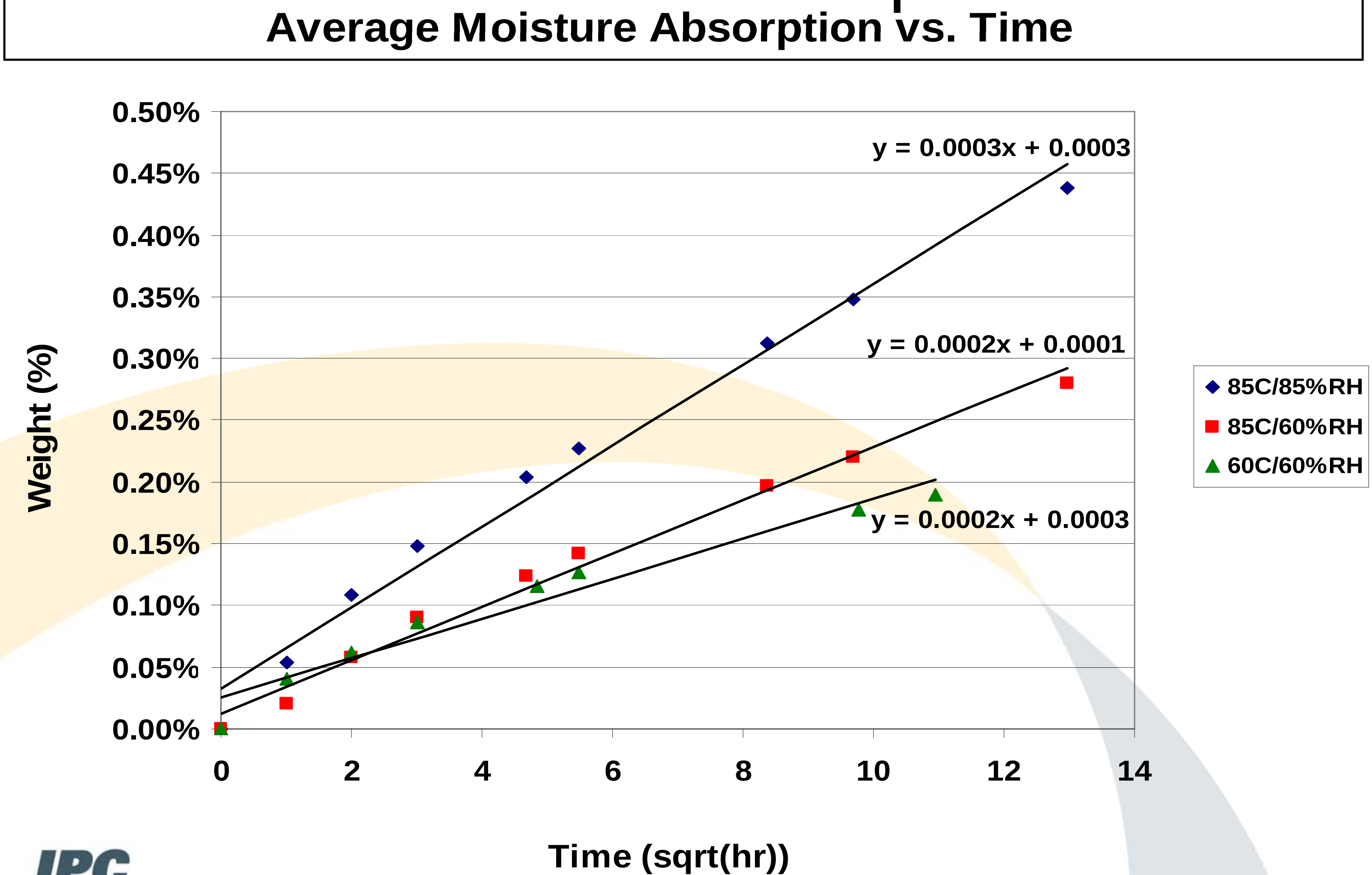


- Cross section of sample after 33 reflows at 260^{o}C peak
- Low magnification: no cracking observed

Phase 2: Moisture Absorption Results



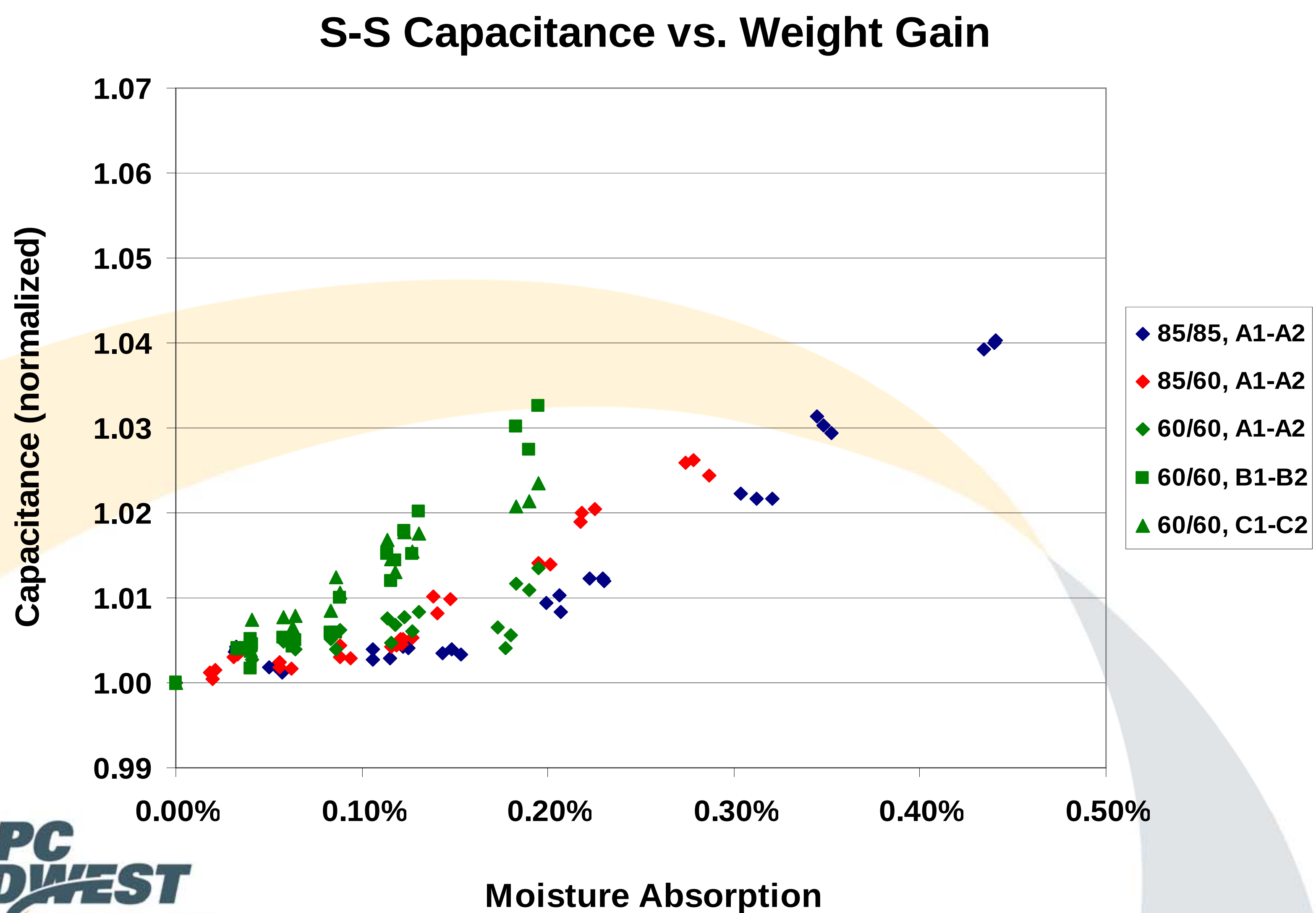
Phase 2: Moisture Absorption Results



Phase 2: Moisture Absorption Observations

- The 85^{o}C/85%RH samples showed the largest weight gain due to moisture absorption
- The 60^{o}C/60%RH samples showed the smallest weight gain due to moisture absorption
- Higher temperature results in increased moisture absorption at 60%RH
- Moisture absorption is proportional to the square root of time in hours, as per Fick's law of diffusion
  - Deviation is observed as moisture saturation is approached
  - Saturation seems to initiate around 64 (8^2) hours

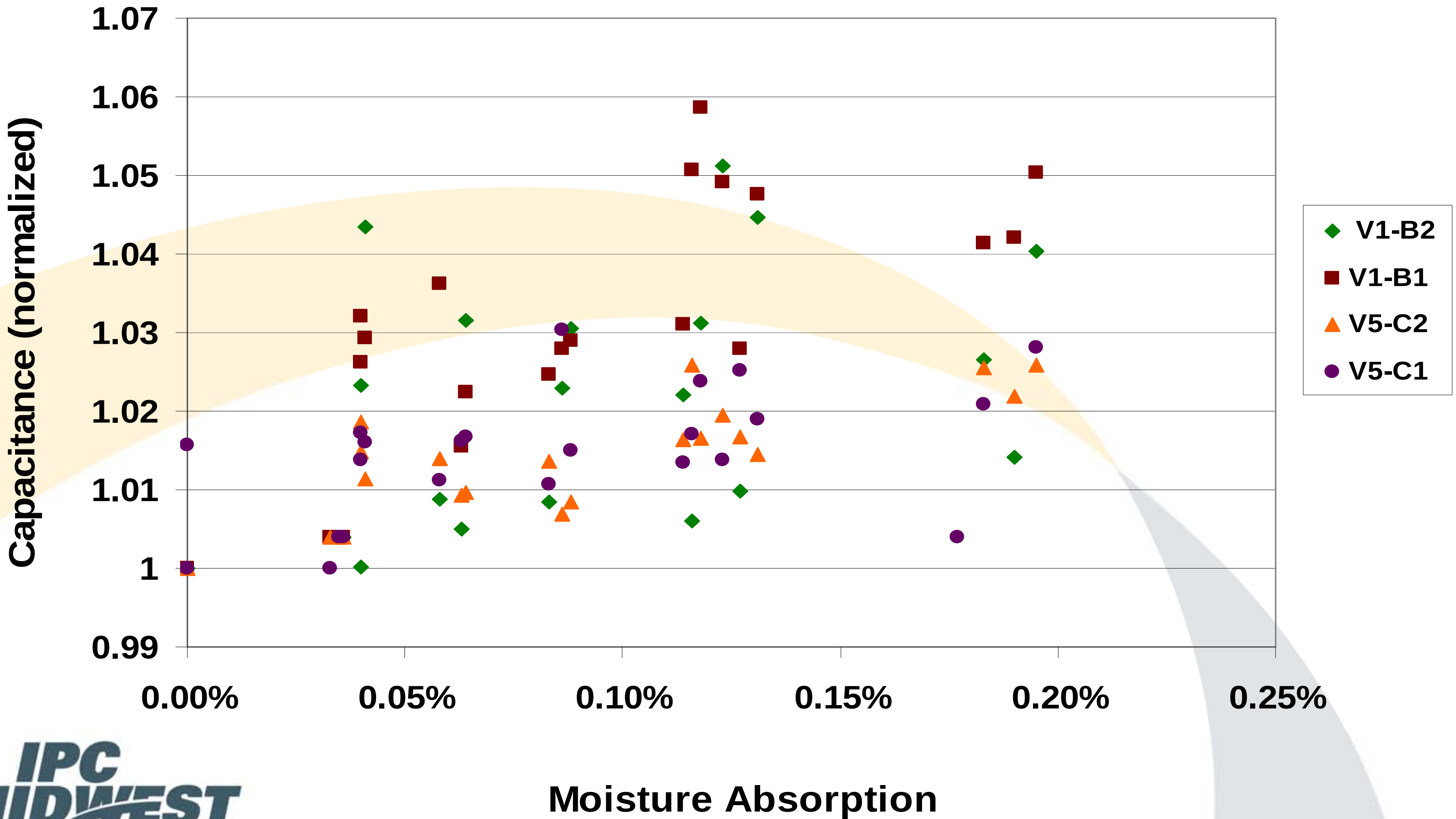
Phase 2: Moisture Capacitance Results



IPC MIDWEST CONFERENCE & EXHIBITION

Phase 2: Moisture Sensitivity Results

S-PTH Capacitance vs. Weight Gain, 60C/60%RH

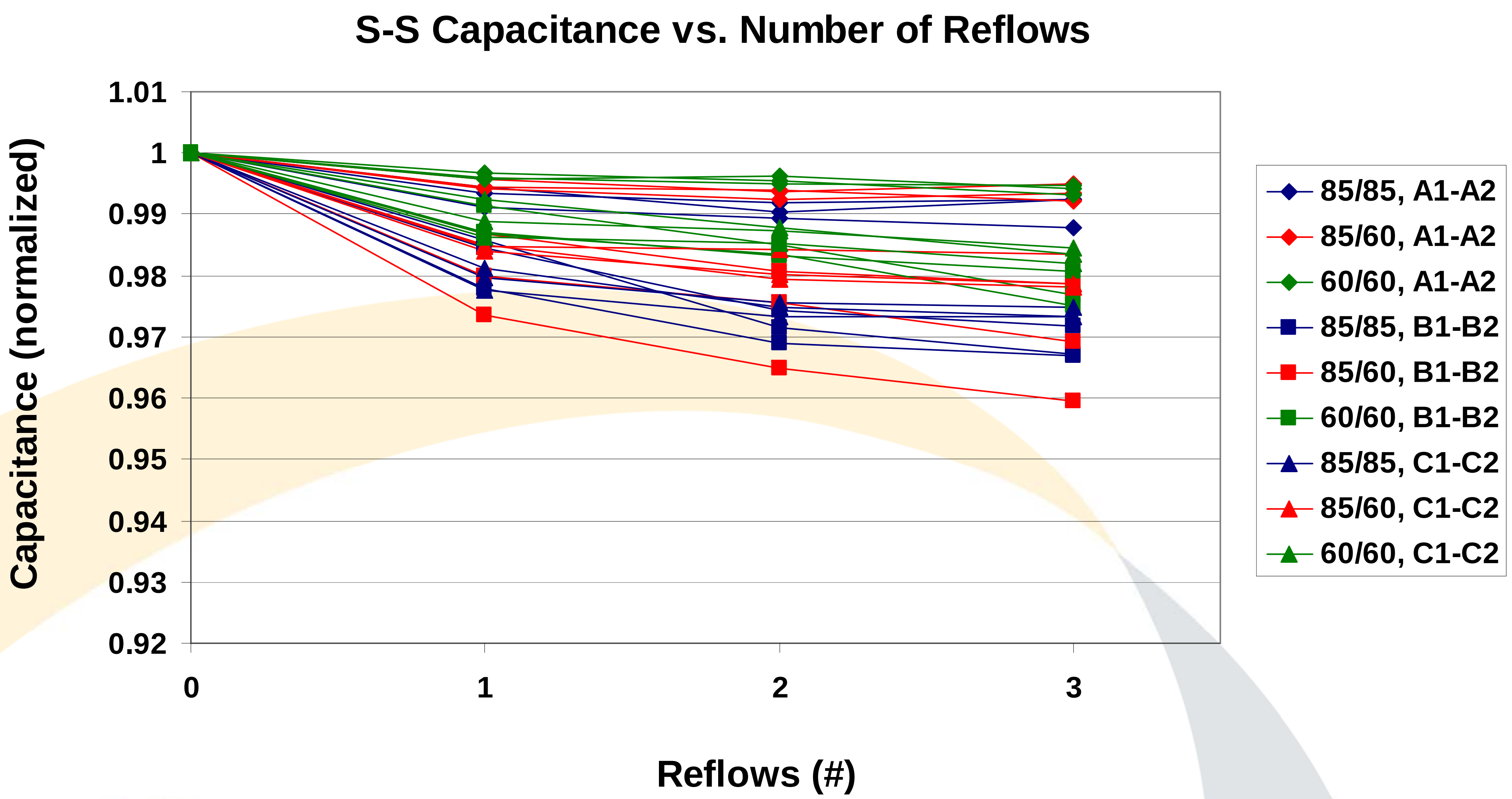


IPC MIDWEST CONFERENCE & EXHIBITION

Phase 2: Moisture Capacitance Observations

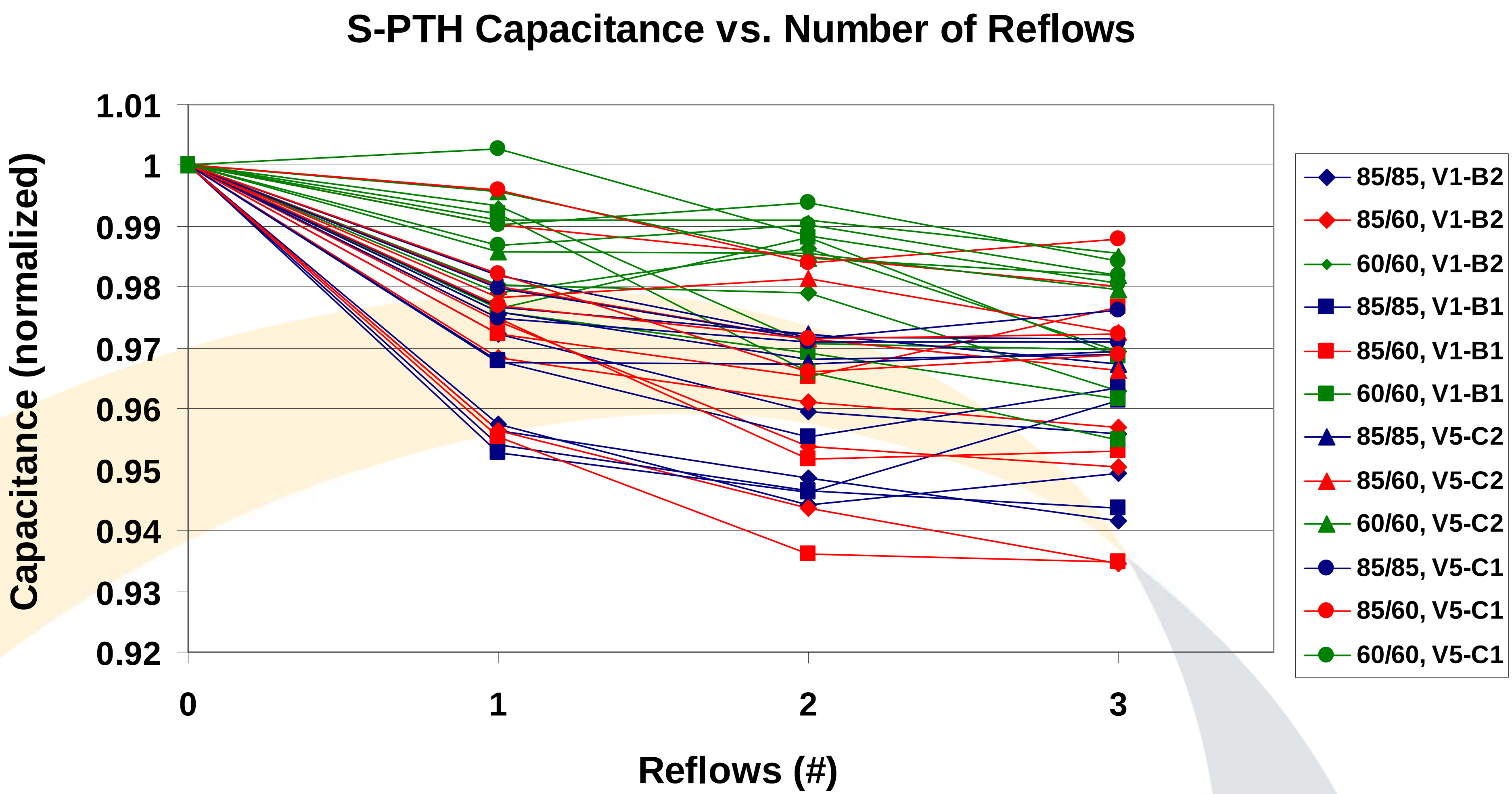
- Capacitance as a function of moisture absorption shows similar trends for all three environmental conditions
- Shield-over-shield with no PTHs showed minimal change up to 0.15%, followed by approximately linear behavior
- The shield-over-shield with PTHs showed a larger increase in capacitance relative to the amount of moisture absorbed
- Shield-to-PTH capacitance showed a larger increase in capacitance relative to amount of moisture absorbed, but no clear trend

Phase 2: Moisture Sensitivity Reflow Results



IPC MIDWEST CONFERENCE & EXHIBITION

Phase 2: Moisture Sensitivity Reflow Results



Phase 2: Moisture Sensitivity (S-S Results)

- Capacitance degradation
  - Test structure B degrades more than test structure C, which degrades more than test structure A
    - Same as reflow without moisture preconditioning
  - 60ºC/60%RH degrades the least, while 85ºC/60%RH and 85ºC/85%RH seem to show similar behavior
- Was capacitance degradation due to moisture desorption or damage accumulation within the coupon?
  - After 85ºC/85%RH, 4% <u>increase</u> in capacitance
  - After 3 reflows, 4% <u>decrease</u> in capacitance
  - Is there moisture remaining after the first reflow?

Phase 2: Moisture Sensitivity (S-PTH Results)

- S-PTH degrades more than S-S
  - Maximum 6% reduction vs. maximum 4% reduction
- 60ºC/60%RH degrades less than the other two conditions
- Test structure B generally degrades more than test structure C

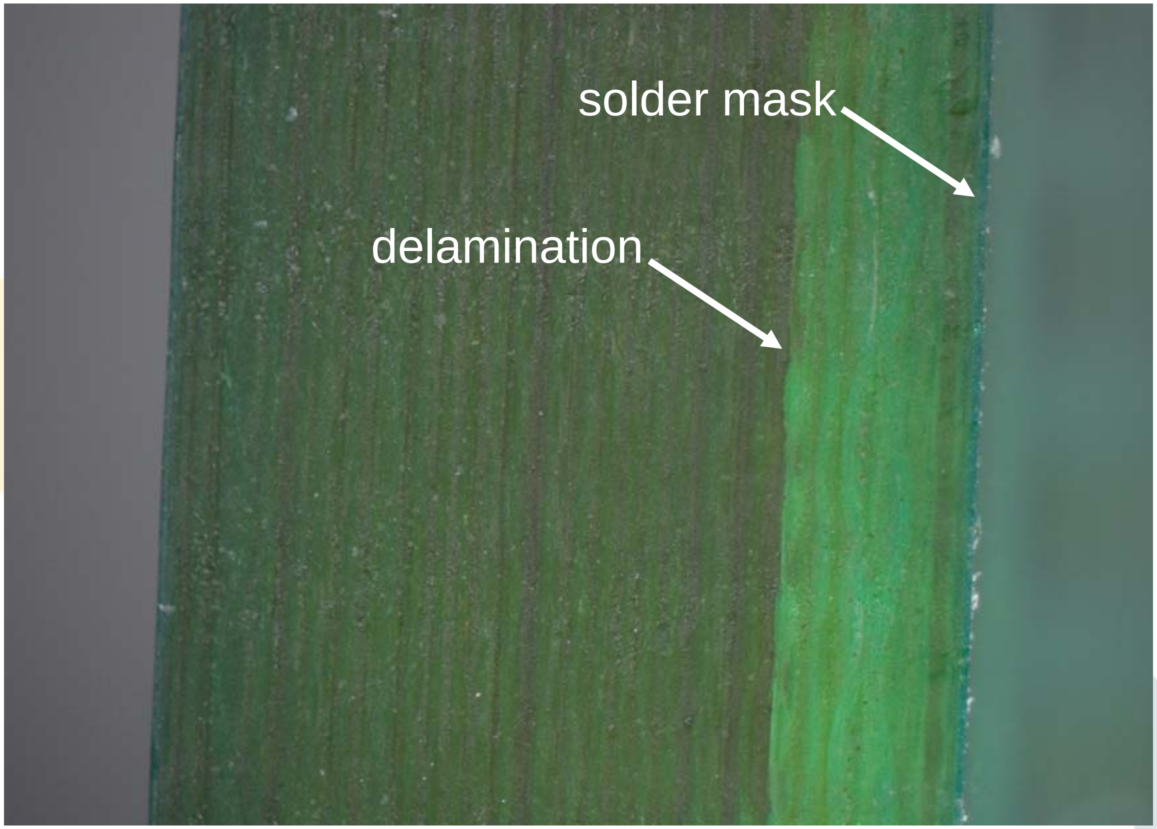
Delamination

- Delamination occurred primarily in featureless areas
- Evidence of failures only in specimens tested as per MSL1 (85^{o}C/85%RH, 168 hours)
  - These samples had the highest % weight gain
- No visible delamination in MSL2 (85^{o}C/60%RH, 168 hours) and MSL2a (60^{o}C/60%RH, 120 hours) samples
- No observable delamination in any "dry samples" from phase 1

IPC MIDWEST CONFERENCE & EXHIBITION

Phase 2: Moisture Sensitivity Results

Delamination observed in 85^{o}C/85%RH test boards

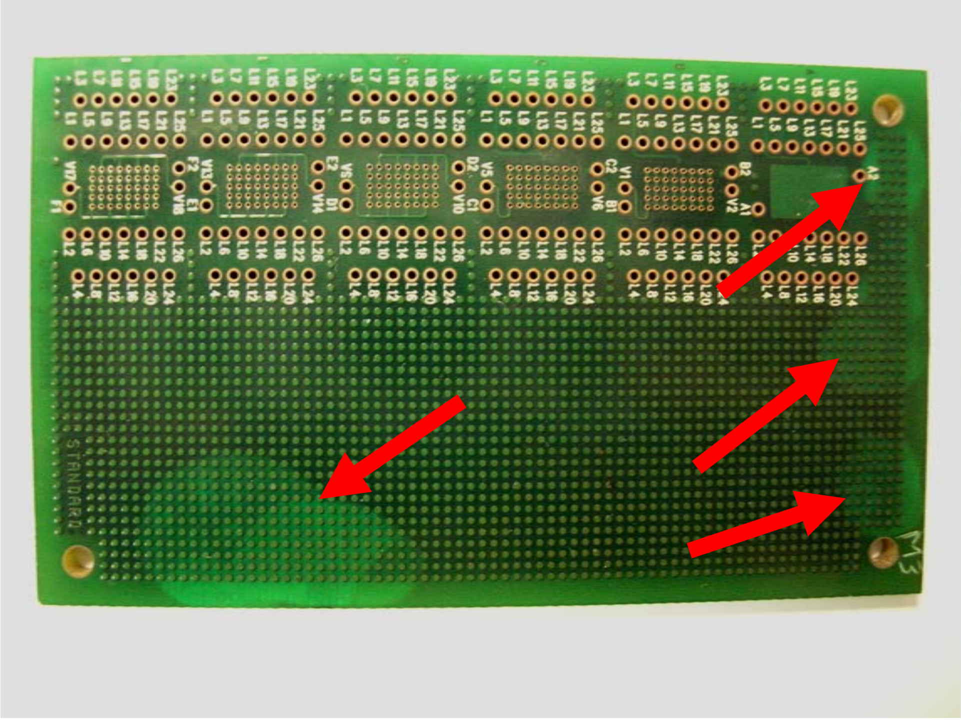


2.5X side view of 85^{o}C/85%RH board after 3 reflows at 260^{o}C peak

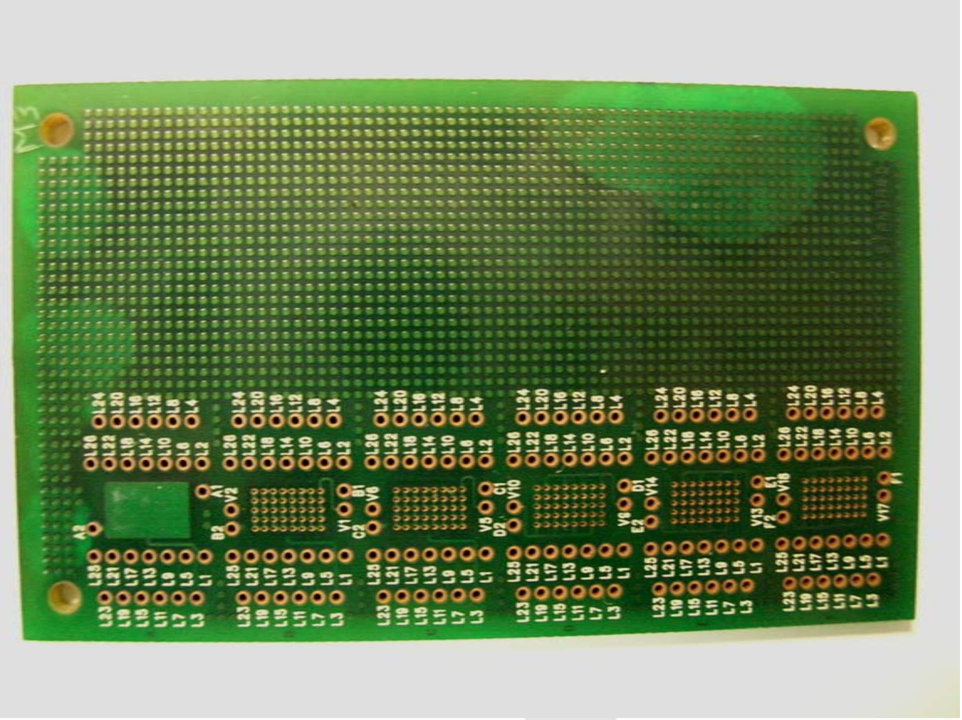
IPC MIDWEST CONFERENCE & EXHIBITION

Coupons after 85C/85%RH + 3 Reflows

Top



Bottom



Red arrows mark internal delamination

Phase 1: Observations

- Variation in degradation rates on different test structures may be evidence of microcracking in the PCB
  - Microcracking seems to be exacerbated by the presence of PTHs
  - Microcracking also seems to be exacerbated by the presence of non-functional pads

Phase 1 (cont.)

- One board had a significant decrease in capacitance on all S-PTH nets
  - On two supposedly isolated test structures (B and C)
- Potential root-cause (#1): Measurement error due to measurement at elevated temperature
  - Unlikely because 'normal' S-S measurements were taken at the same time as the anomalous S-PTH measurements
- Potential root-cause (#2): Possibility of a plane-PTH short
  - Unlikely to affect both test structures B and C
- Potential root-cause (#3): Extensive microcracking
  - A similar decrease in S-S capacitance was not observed

Phase 2

- The 85ºC/60%RH seem to show a larger increase in capacitance for a given amount of moisture absorption
  - Uncertain as to the driver for this behavior
- Shield-over-shield test structures with PTHs showed a greater increase in capacitance for a given amount of moisture absorption
  - Damages caused during drilling could enable more localized moisture absorption (tiny cracks or delamination can absorb more water)

Phase 2 (cont.)

- Shield-PTH capacitance vs. moisture absorption:
  - No clear trend
  - For the same level of moisture absorption, test structure B generally showed a larger increase in capacitance than test structure C
  - Test structure B then displayed a larger degradation in capacitance than test structure C after reflow

Phase 1 vs. Phase 2 Observations

- Moisture sensitivity samples display more extensive degradation after reflow
  - 260°C samples from phase 1 show approximately 1% degradation in test structure A after 15 reflows
  - Phase 2 samples show an average of nearly 1% degradation for all conditions on test structure A after 3 reflows
  - This trend holds true for all S-S and S-PTH nets

Conclusions

- Measurable change of capacitance after each reflow
  - Discrimination between different test structures and MSL exposures strongly suggests approach captures material degradation, as opposed to an increase in resistance at contact pads due to oxidation
  - However, contact resistance should be quantified in next round of testing through ESR measurements
- Strong difference in shield-over-shield capacitance between test structures B and C, due to the presence of non-functional pads, is very interesting and should be further characterized
  - Future focus on clearance and pad dimensions

IPC MIDWEST CONFERENCE & EXHIBITION