Microvia Reliability Failure Modes

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Recent increases in assembly temperatures in response to removing lead from solder used in printed circuit boards (PCBs) assembly has increase the strain and stress on interconnect structures. The elevated assembly temperature has reduced the reliability of interconnect structures including microvias. This paper addresses how microvias may fail in response to the thermal excursion associated with assembly and the end use environment. The logic of different elevated temperature testing on FR4 (G10) and polyimide materials is reviewed. The paper compares and contrasts the implications of testing the microvia passively and under an electrical load. Also addressed are microsectioning techniques to improve the acuity of microscopic analysis. The failure modes addressed include separation between the base of the microvia and capture pad, microvia barrel cracks, and corner cracks, circumferential cracks around the base of the microvia in the capture pad and microvia misregistration to the base of the capture pad. This paper addresses the reliability implications of microvia constructions including stand alone, staggered, stacked microvias, copper and epoxy filled microvias and the failure modes unique to these structures.

Test Method – Microvia testing was performed as per IPC Test Methods Manual 650, 2.6.26 DC Current Induced Thermal Cycle Test also referred to as Interconnect Stress Testing (IST). The test method was modified from the default temperature of 150°C maximum to 190°C for testing FR4 materials and 230°C for testing PWBs fabricated with polyimide. Testing at 190°C was demonstrated to be effective in enunciating microvia failure without producing artifact failure modes within 500 thermal cycles. Testing at the lower default temperature of 150°C did not accurately find failures in 1000 cycles on coupons associated with printed circuit boards that had a 30% failure rate in assembly (Anderson, Parry, and Reid 2005). As of august 2009 testing of microvias fabricated with polyimide at 230°C is being evaluated in certain high density applications with promising results and testing continues.

The test coupons used for IPC test method 2.6.26 have a power circuit that is used for thermal cycling and one or two sense circuits that have interconnect structures that are representative of the printed wire board design. Changes in resistance above that induced by heating reflect damage to the circuits. Both power and sense circuits are monitored for damage accumulation during the test. The power circuit is tested under an electrical load while the sense circuits are tested passively. Microvias can be tested by powering the microvia directly. Testing by powering on the microvia allows testing under an electrical load. It is common for microvias to fail in a manor where the interconnection is intermittent for a number of cycles until the accumulating damage produces a catastrophic failure. Powering on the microvia has the additional benefit of sensing an instantaneous open circuit and stopping the test immediately. This test modification accelerates damage accumulation and at the same time improves sensitivity. Weak microvia fail readily when powering on microvia circuits while robust microvia survive to end of test at 500 cycles.

In this test method testing stops at a 10% increase in resistance, and in doing so, prevents catastrophic failures that could be a challenge to interpret by microscopic examination. Since the increase in resistance is an objective reflection of damage accumulating in the circuit one can related the resistance increase to the physical damage observed in microscopic examination. This method bridges the gap between objective evidence (resistance change) to the subjective observations associated with microscopic evaluations. This feed back loop of objective evidence and subjective interpretation hones the skill and accuracy of the examiner improving the interpretation of damage in the interconnection and its' reliability implications. At a 10% increase in resistance cracks in the microvia are beginning to develop but have not progressed to a point of an open. That the microvia has failed is established objectively by electrical test which allows the observer to learn what is significant in microscopic examination. It turns out that what may be considered as subtle damage by microscopic examination previously, may be found to have a significant impact on reliability.

Failure Location and Microsection Preparation – Microsections were processed as per IPC Test Methods Manual TM 650 2.1.1 Microsection, Manual Method. It should be noted that a mild microetch after polishing was applied to allow the improved visualization of microvia structures. Microscopic examinations were conducted up to a magnification of 1250X. Micrographs were digitally captured using a Nikon Cool Pix.

Microvia Overview - For the purposes of this paper a microvia is defined as a blind interconnection with a diameter of .15 mm (.006") or less. A microvia is often used to form a conductive interconnection between adjacent layers although two and three layer interconnections have been produced. Microvias are typically produced by the use of laser ablating through the dielectric material between two conductive layers. Drilling and dielectric etching has also been used to produce microvias.

References

Microvia – Paul Anderson, Gareth Parry, Paul Reid 2005
IPC Test Methods Manual 650, 2.6.26 DC Current Induced Thermal Cycle Test
IPC Test Methods Manual TM 650 2.1.1 Microsection, Manual Method.
IPC T50 Terms and Definitions
Review of Micro-via Processing, Gray Hoeppel, Coretec

Paul Reid's' career in printed circuit board fabrication and reliability testing spans 28 years. Paul received a Bachelor in Science degree in 1975 and a Master in Science in 1980 from Rivier College, Nashua, New Hampshire. Paul has worked in Quality and Engineering in Managerial roles in New England and Canada. He has created technical animations of PCB fabrication, and recently, failure modes induced by thermal excursions in support of reliability testing. His animations have been used for education, technical reports and promotions internationally. Paul is a Program Coordinator at PWB Interconnect Solutions Inc., Ottawa, where his duties include reliability testing, failure analysis and material analysis. He is currently investigating the reliability of microvias in lead/free applications.

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Microvia – Paul Anderson, Gareth Parry, Paul Reid 2005
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Introduction

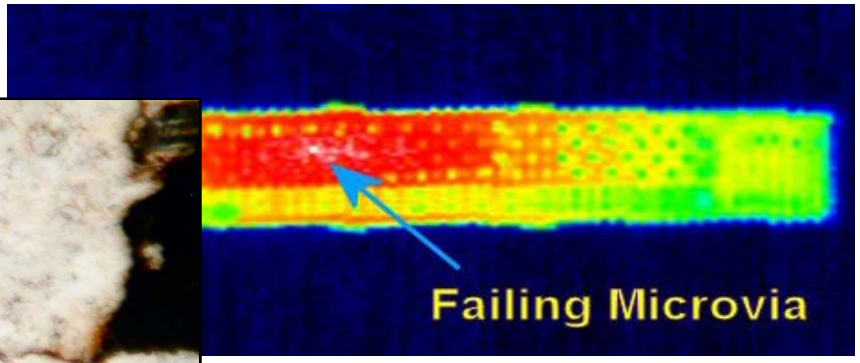
- Microvia are becoming more common in HDI applications
- Microvia are typically the most robust interconnect structure
- Test Method IPC TM 650 2.6.26
- The temperatures used in lead free application can degrade MV
- Effect MV testing is at elevated temperatures
- Different microvia configuration have different stresses
- Effective microscopic evaluation requires a microetch
- Failure mode to isolated microvias
  - Microvia to target pad separation, barrel cracks, corner cracks, target pad pull out and misregistration of ablation to target pads
- Failure Mode of Stacked Microvias
  - Copper voids, copper cap separation

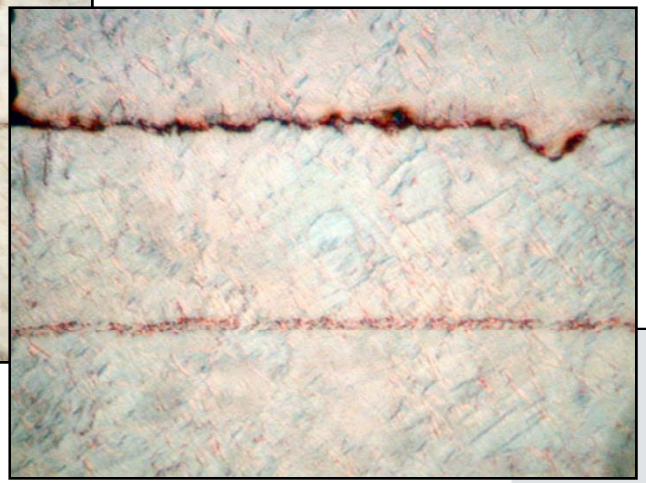
Test Method – IPC TM 650 2.6.26

- Microvia testing IPC Test Methods Manual 650, 2.6.26 DC Current Induced Thermal Cycle Test also called Interconnect Stress Testing (IST).
- Microvia Testing at 190° C in FR4
  - *Paper Microvia Reliability Concerns in the Lead Free Assembly Environment*, Paul Anderson, Gareth Parry, Paul Reid 2005
- Microvia testing in ridged polyimide is proposed at 230° C
  - Preliminary results are positive, Testing continues
- Coupons have power and sense circuits
  - Testing stops at 10% increase in resistance
  - Testing microvias by powering on the microvia
    - Event detector
    - Testing under load to accelerate failures without artifacts

Microscopic Examination

- Testing stop at 10% increase in resistance
  - Allow failure location with a thermal camera
  - Allows evaluation of a failing microvia not a catastrophic failure

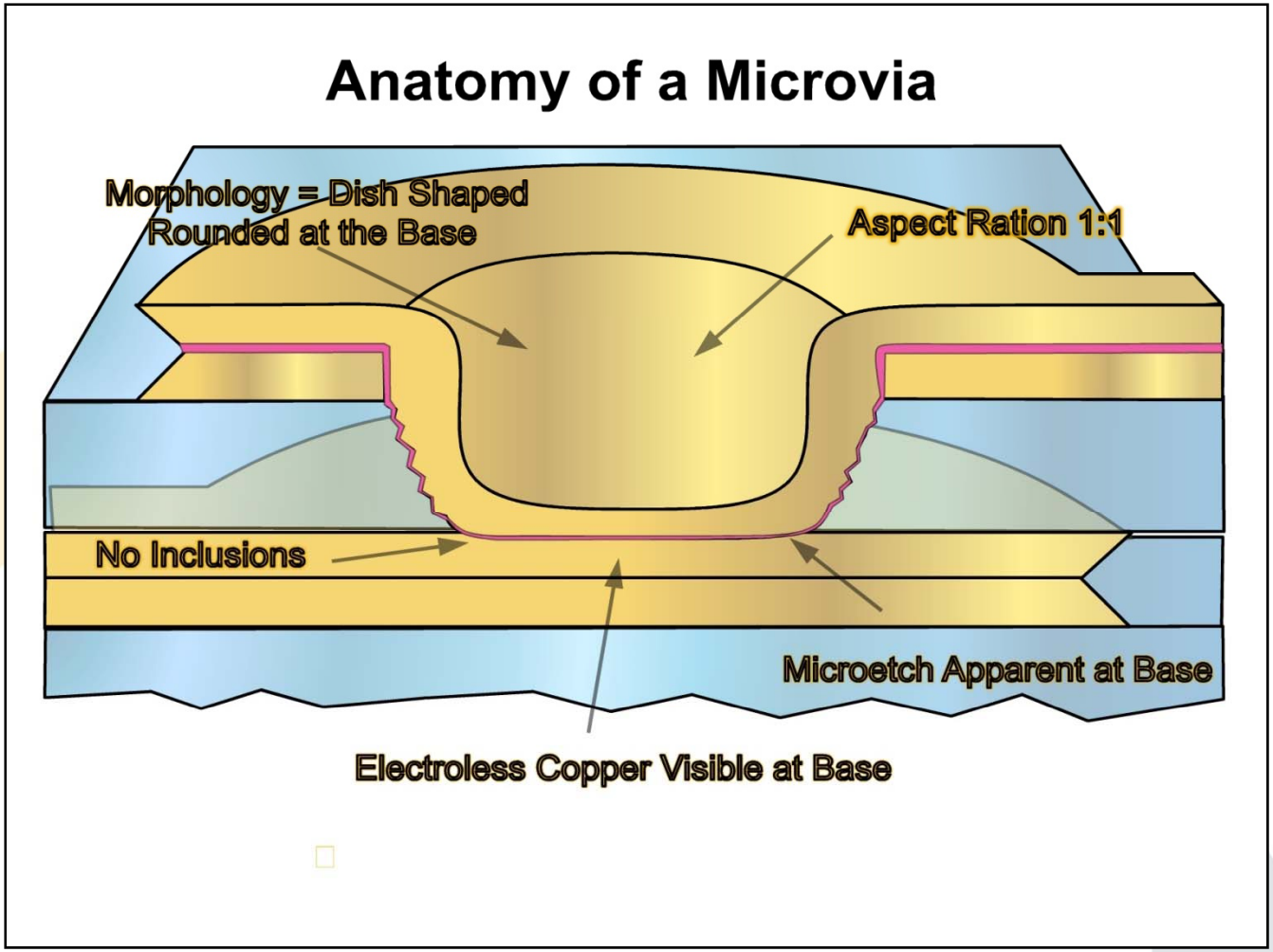




Anatomy of a Microvia

- The anatomy of a well fabricated microvia is a blind hole that has a dish shaped profile
- Distribution of electroless and electrolytic copper is uniform
- The side wall are smooth with few glass fibers protruding
- The top layer the capture pad
- The bottom layer target pad.
- Aspect ratios greater than 1:1 are a challenge

Anatomy of a Microvia



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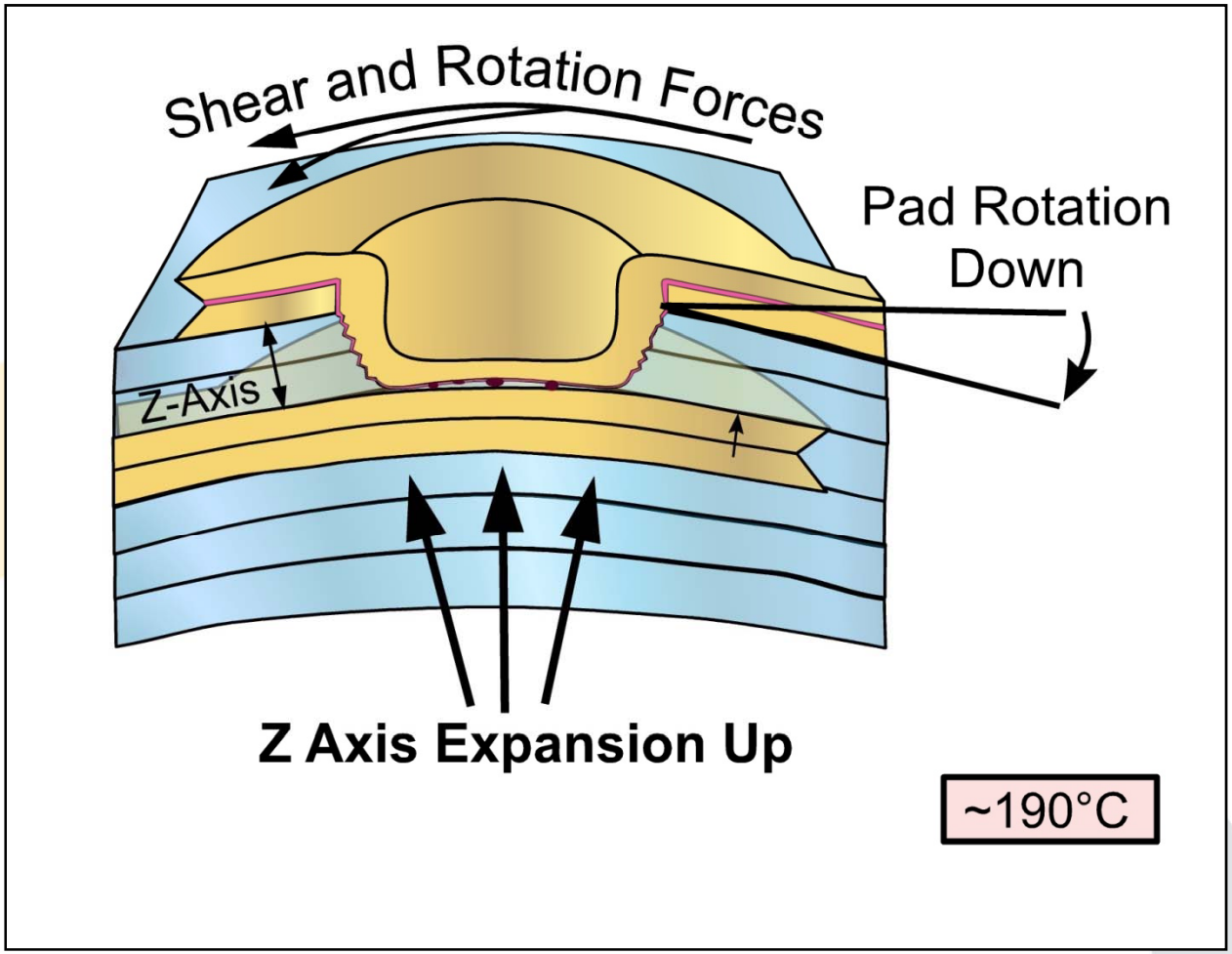
Microscopic Examination of MV

- A microvia that has been polished only is a challenge
- MV failure by testing and a Hx of microscopic evaluation demonstrate a mild microetch is required to discern
  - Subtle microvia damage,
  - Review crystalline structures
  - Identify micro-inclusions at the base of the microvia.
- The microetch needs to be controlled and applied appropriately
- Aggressive etching produces artifact conditions
- Highest magnifications are used 800X to 1200X
- Experience shows fine micro-cracks at the base of the microvia that have caused a 10% increase in resistance may not be visible optically without an appropriate microetch and examination at high magnification

Thermal Expansion – Isolated MV

- Isolated MV are not influenced interconnect structures
- Pad rotation response to z-axis expansion is down
- In a micro section elastic material shows not pad rotation
- I observe pad rotation the material must be plastically deformed
- The pads are rotated inward as the dielectric expands pushing up on the microvia.
- The further the microvia is from the center of the PWB the greater the displacement

Thermal Expansion – Isolated MV



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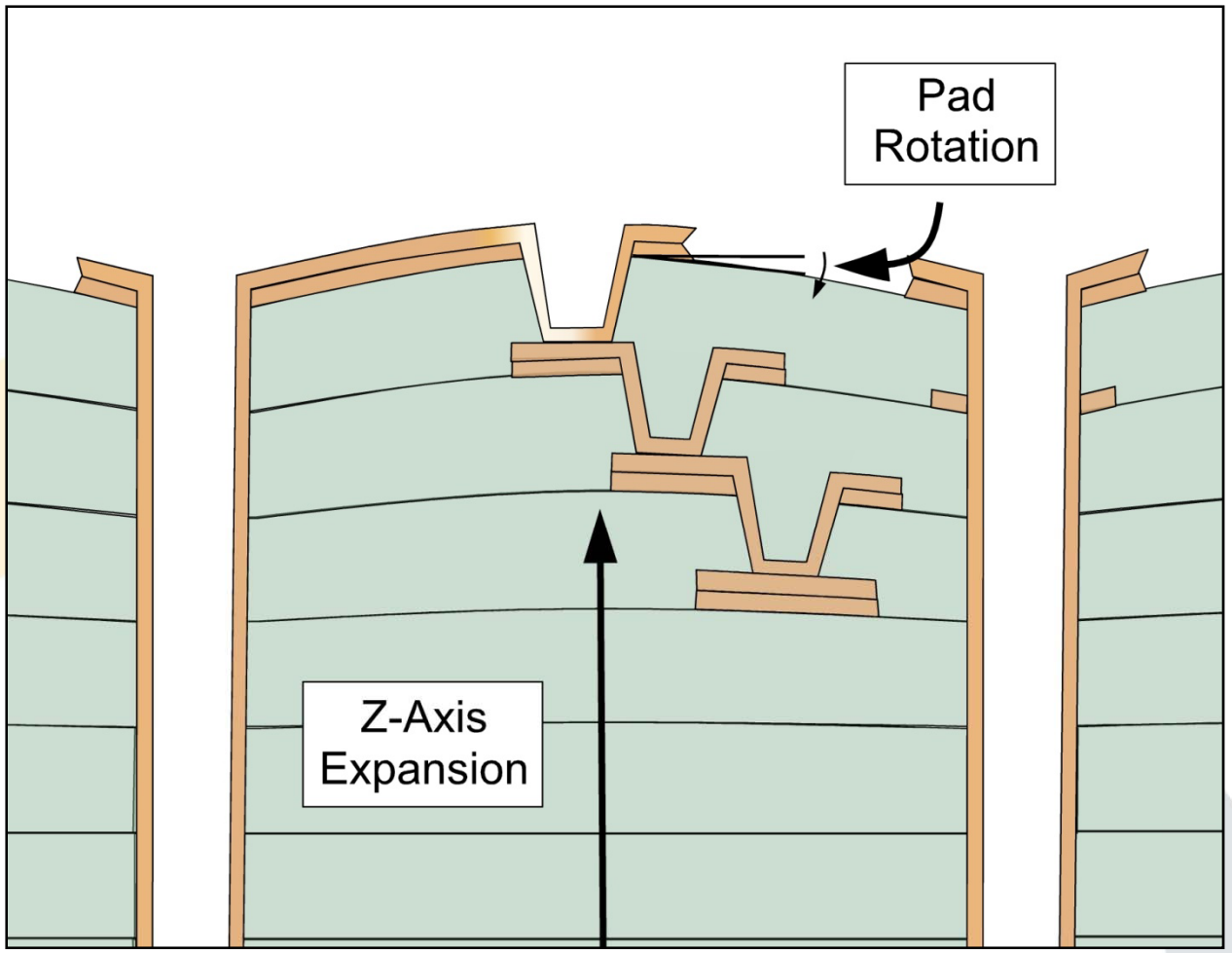
Thermal Expansion – Staggered MV

- Staggered microvias are offset from each in a manor that allows interconnections between layers without requiring a microvia fill or copper cap.

- Generally pad rotation will be downward in staggered microvias. The forces acting on staggered microvias are similar to those acting on isolated microvias.

Thermal Expansion – Staggered MV



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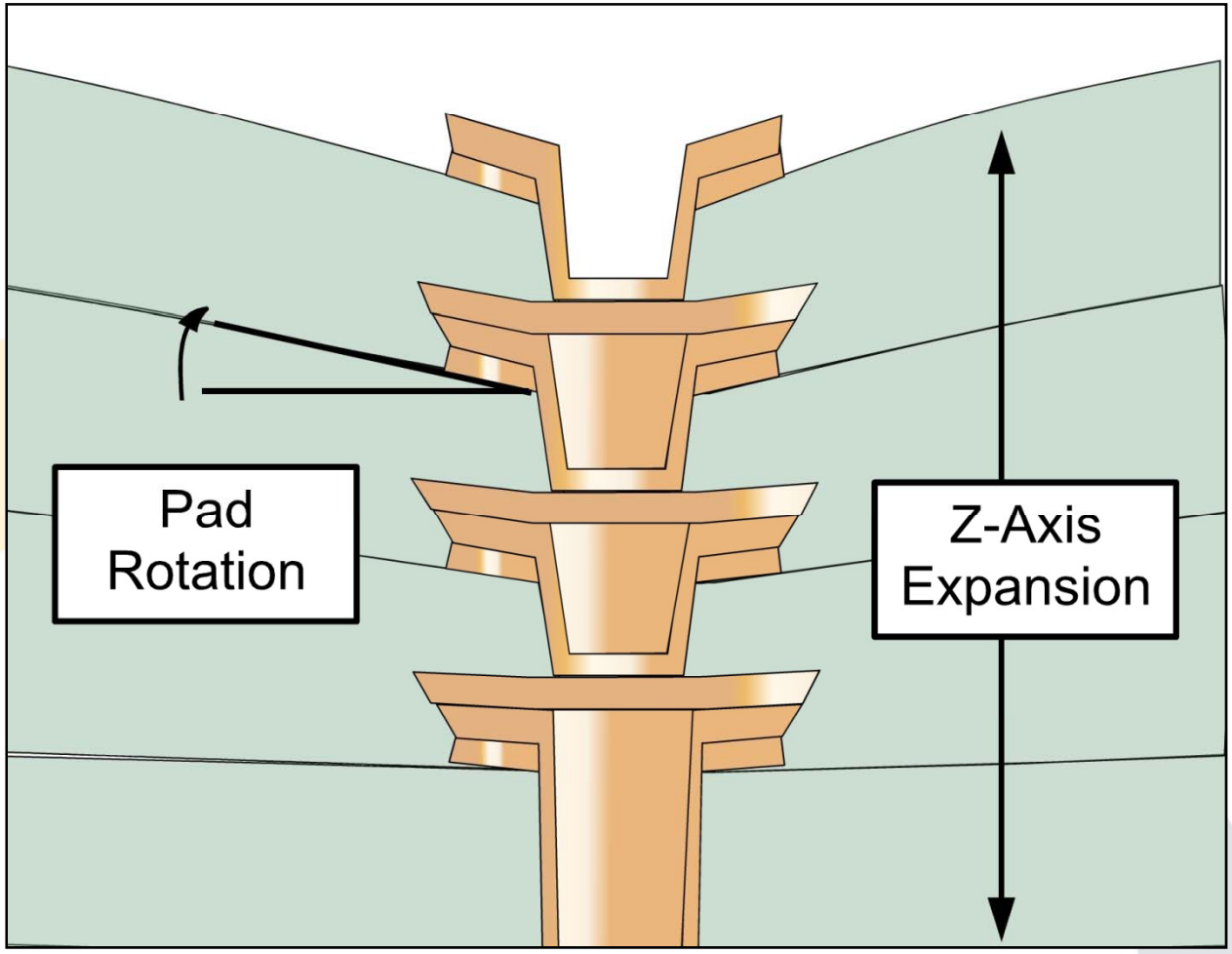
Thermal Expansion – Stacked MV

- Stacked microvias are arranged on top of each other.
- This requires that internal microvias within the stack are filled and capped.
- Stacked microvias on the outer layers may be connected to buried vias to produce a continuous structure that spans the full thickness of the printed wire board.
- Multiple stacked microvias can produce a long enough structure to resist the z-axis expansion resulting in an outward (upward) pad rotation.
- The microvias lower in the stack tend to failure due earlier to interface separation than microvia on outer layers.
- Outer layer microvias have greater pad rotation than the microvia lower in the stack.

Thermal Expansion – Stacked MV



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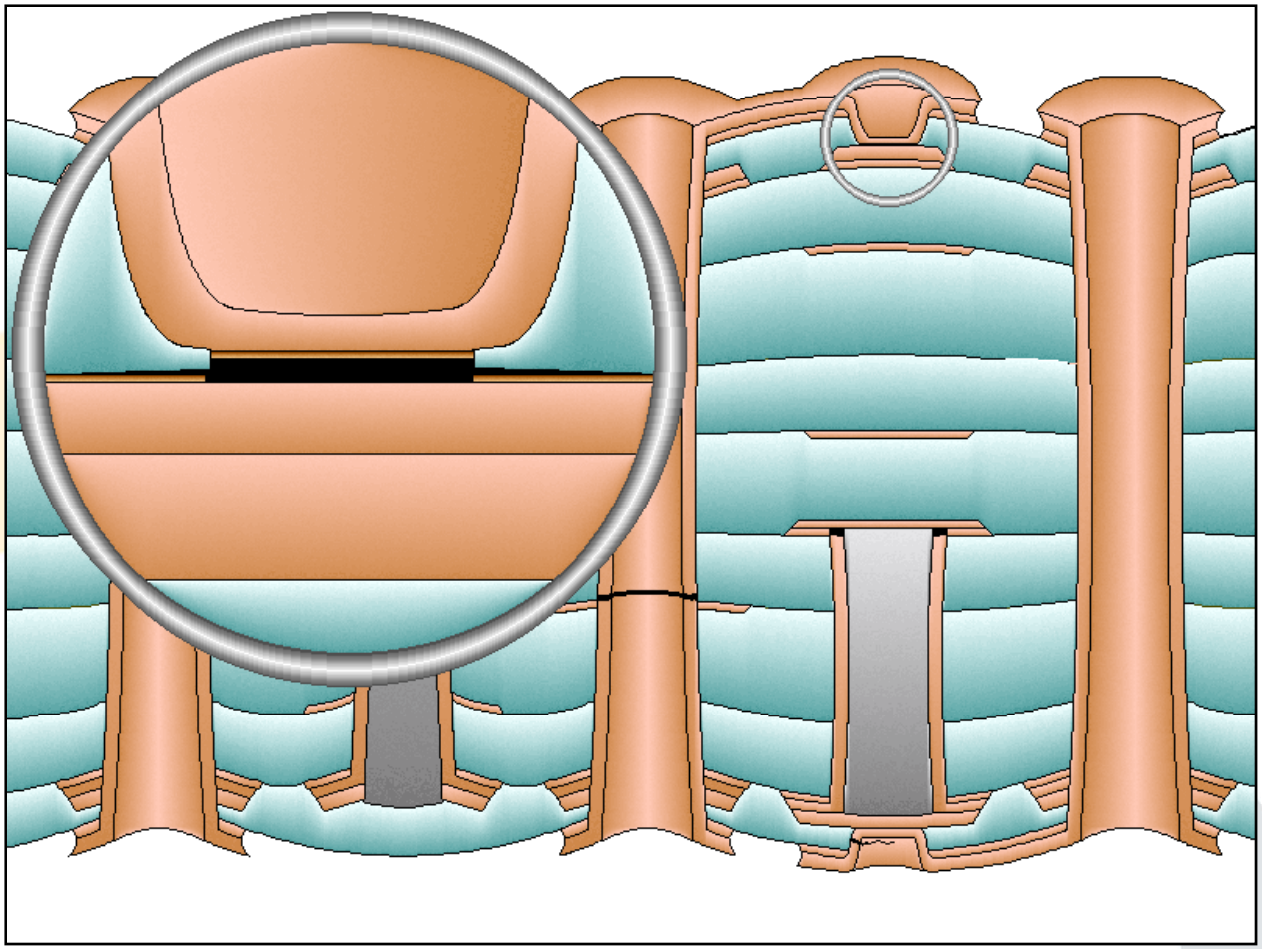
Failure Mode – Interface Separation

- The most common microvia failure mode
- The crack is between the base of the microvia - target pad
- This failure mode presents as a catastrophic failure
- The failure is usually expressed in the cooling cycle
- The cracks may initiate from inclusions at the base of the MV
- Small cracks will coalesce into a larger crack
- Cracks can initiate at the dielectric “foot” at the base of the MV
- Determine if the crack is above or below the electroless copper
- Frequently direct metallization is too thin to be observed
- Given that an electroless copper layer is visible, cracks below the electroless copper reflect inadequate hole preparation and cleaning before metallization.
- Cracks above the electroless copper suggest that investigation should be directed after hole preparation and metallization.

Failure Mode – Interface Separation



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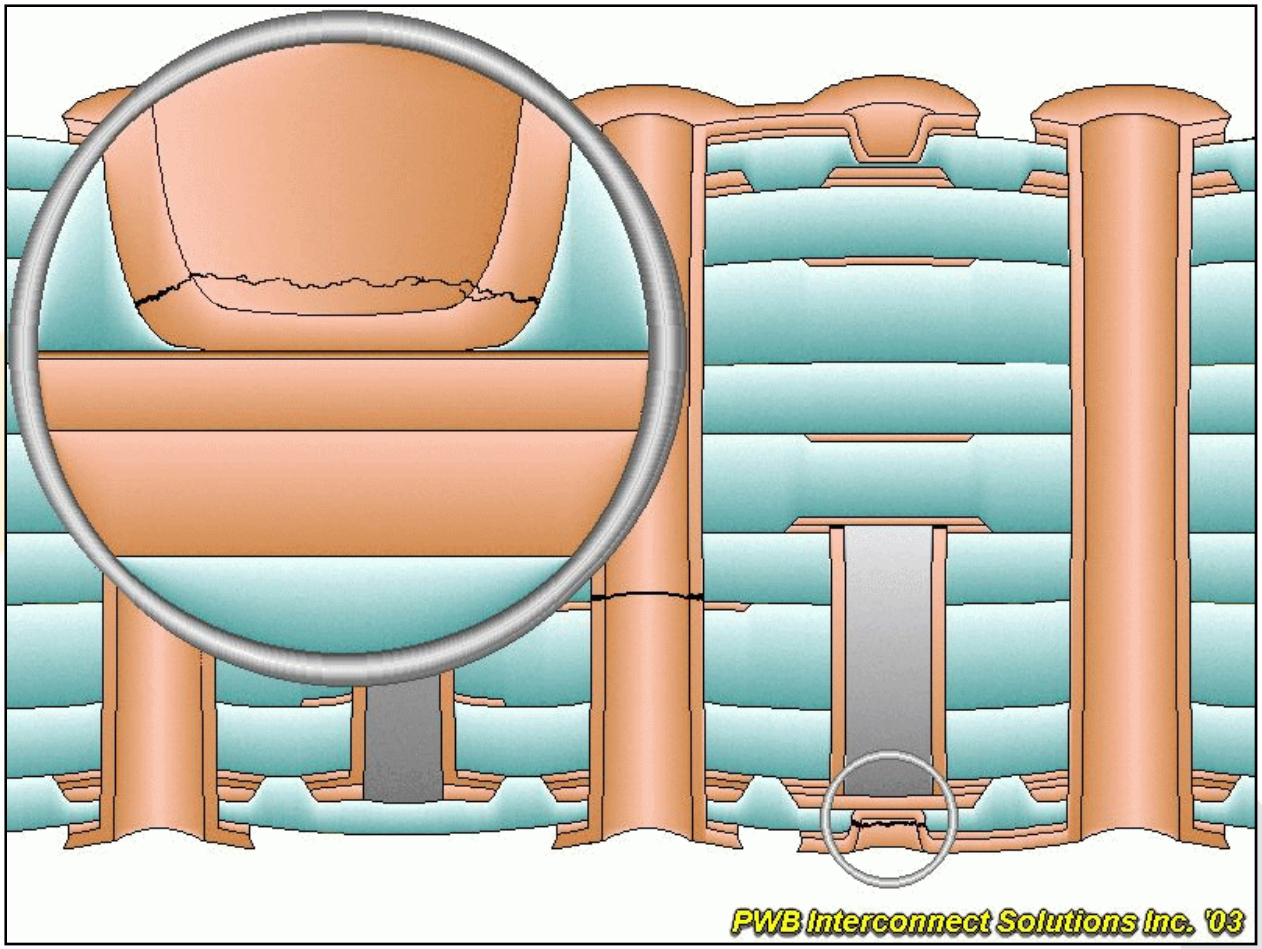
Failure Mode – MV Barrel Crack

- A MV barrel may be a wear out or catastrophic failure
- Failure often occurs during the heating cycle.
- Frequently the barrel crack is associated with thin copper plating in the lower section of the microvia.
- Wedge and step plating may be associated with thin metallization in the barrel of the microvia.
- Macro-throw or “leveling” electrolytic copper baths frequently create exaggerated “dog bone” distribution in the barrel of the microvia.
- Rough MV with glass fibers in the microvia hole wall can exhibit wedge voids, inclusions and copper folds that may contribute to barrel cracks.
- On occasion a crack will traverse a copper flash and proceed down the interface between a flash and full thickness copper plating.

Failure Mode – MV Barrel Crack



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Failure Mode – Corner Crack

- A microvia corner crack is initiated by the z-axis expansion of the dielectric between the capture pad and the target pad.

- Since the dielectric between the two layers is between .05 mm (.002”) and .15 mm (.006”) it is not likely to produce enough expansion to initiate a crack.

- This is an uncommon failure mode. A microvia corner crack frequently presents a wear out type failure.

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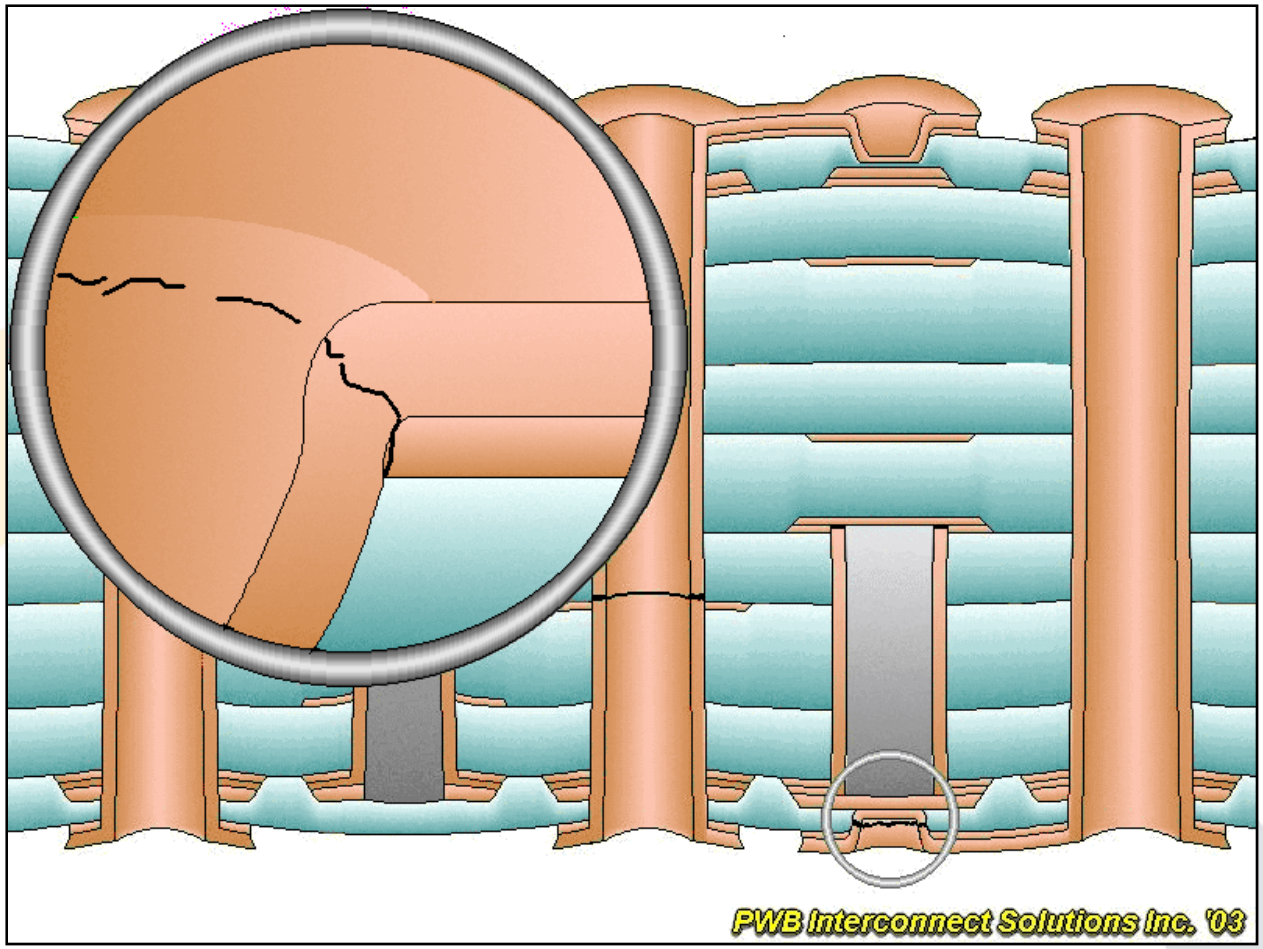
Failure Mode – Corner Crack



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Failure Mode – Target Pad Pull Out

- Like corner cracks microvia pad cracks, sometimes referred to as microvia “pull out” occurs in response to the z-axis expansion of the dielectric between the capture pad and the target pad.

- The crack propagates vertically through the target pad and circumferentially around the base of the microvia.

- This failure mode is more often observed in flex circuits with an acrylic adhesive which has a high CTE and low glass transition temperature (Tg).

- In printed wire board columnar crystalline in the target pad may contribute to this failure mode

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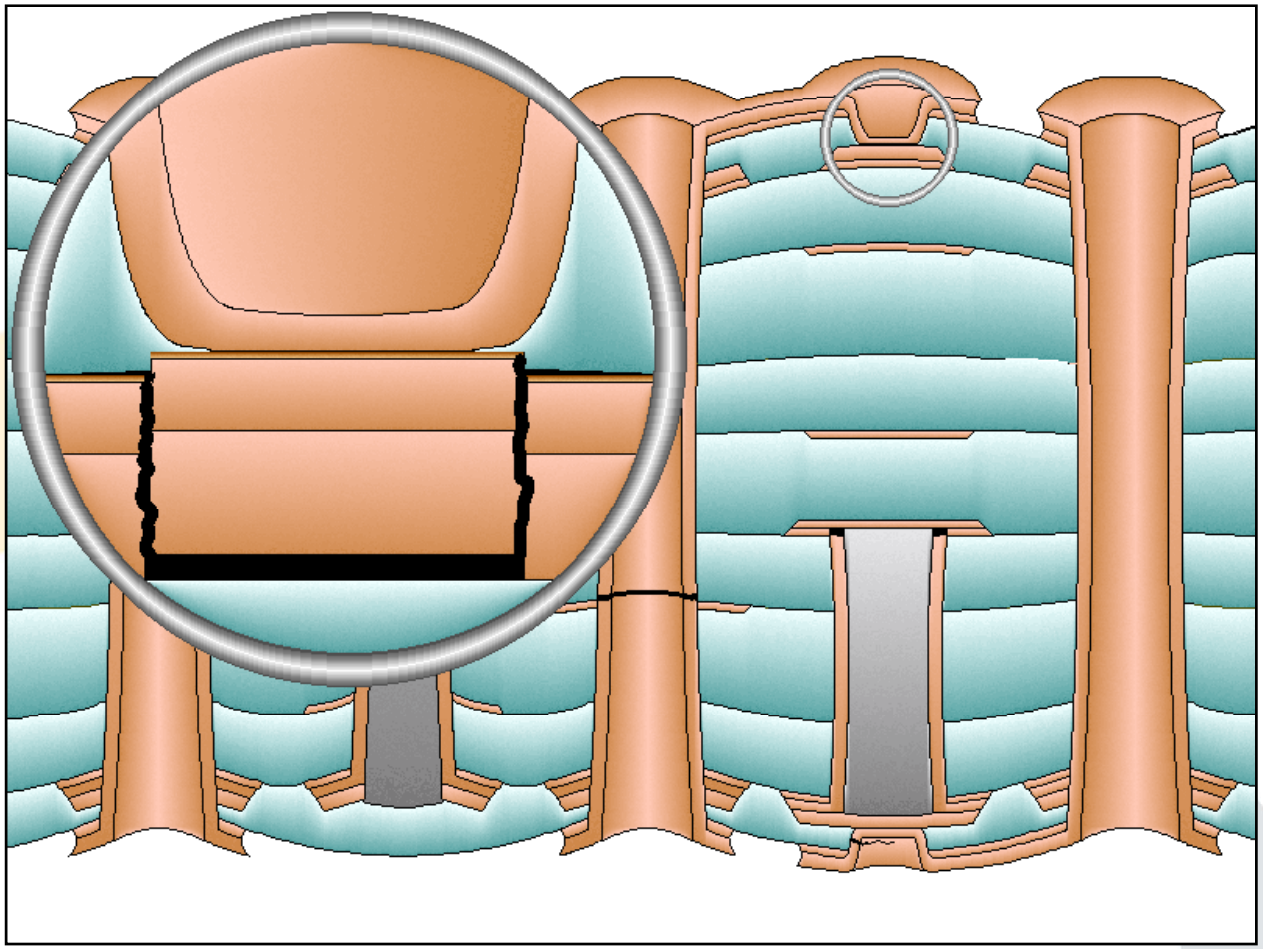

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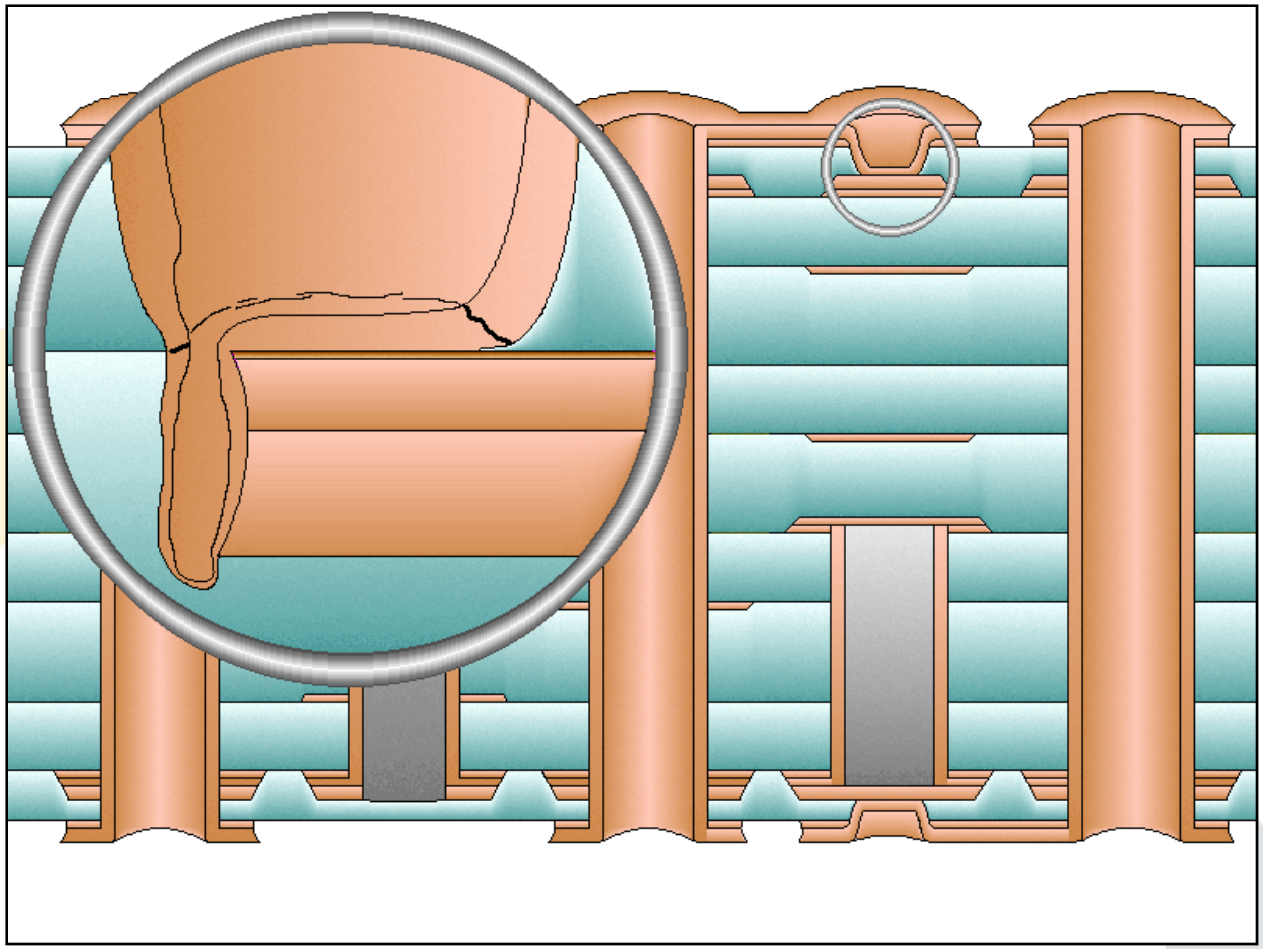
Failure Mode – Misregistration



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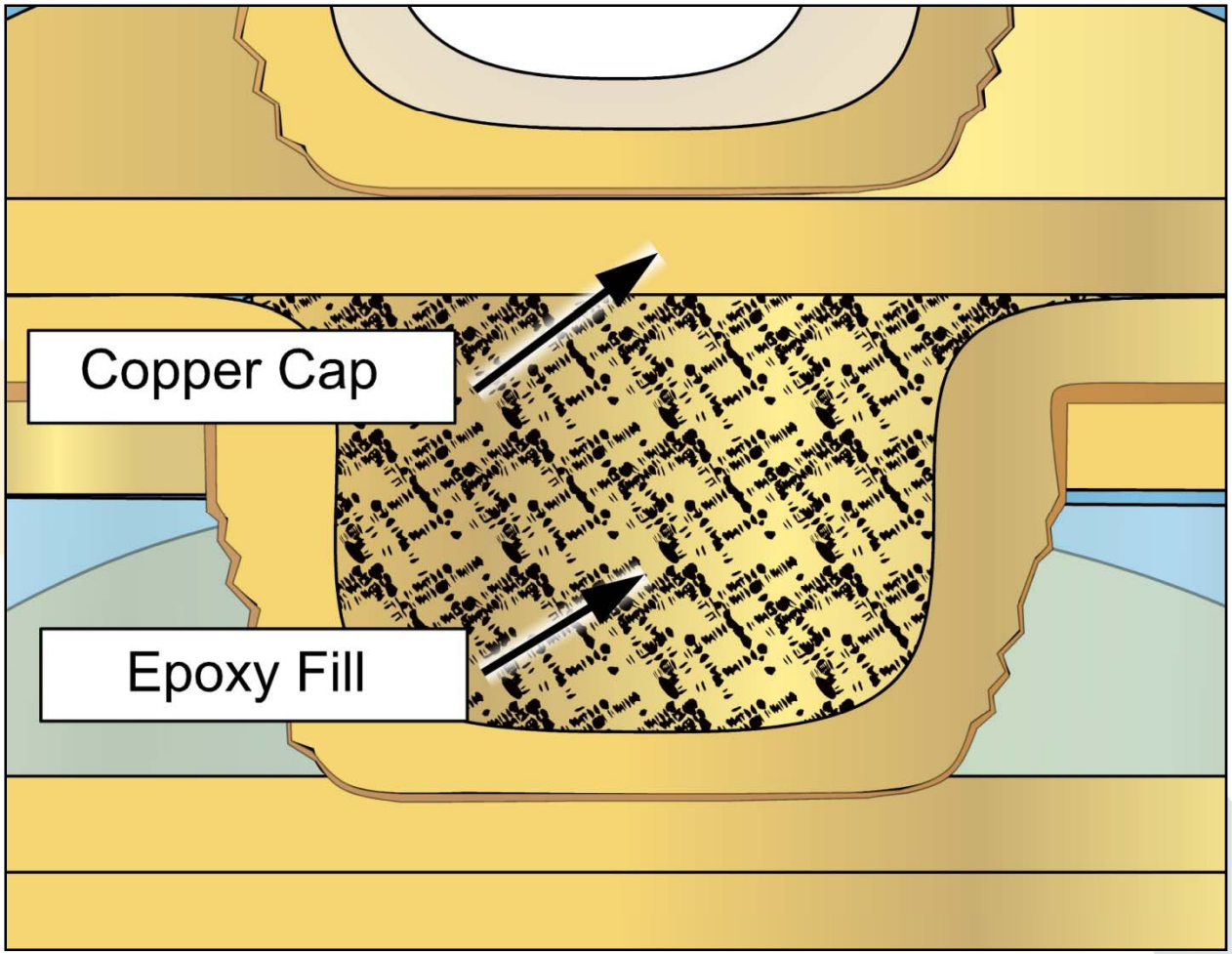
Failure Mode – Misregistration

- There are two types of microvia misregistration; misregistration of the ablated hole to the capture pad and misregistration of the ablated hole to the target pad.

- In both cases this failure mode tends to produce opens or short that is indentified by electrical test.

- An associated condition is where ablation pierces the full thickness of the target pad and penetrates the dielectric or interconnects structures below.

Filled Capped Microvias



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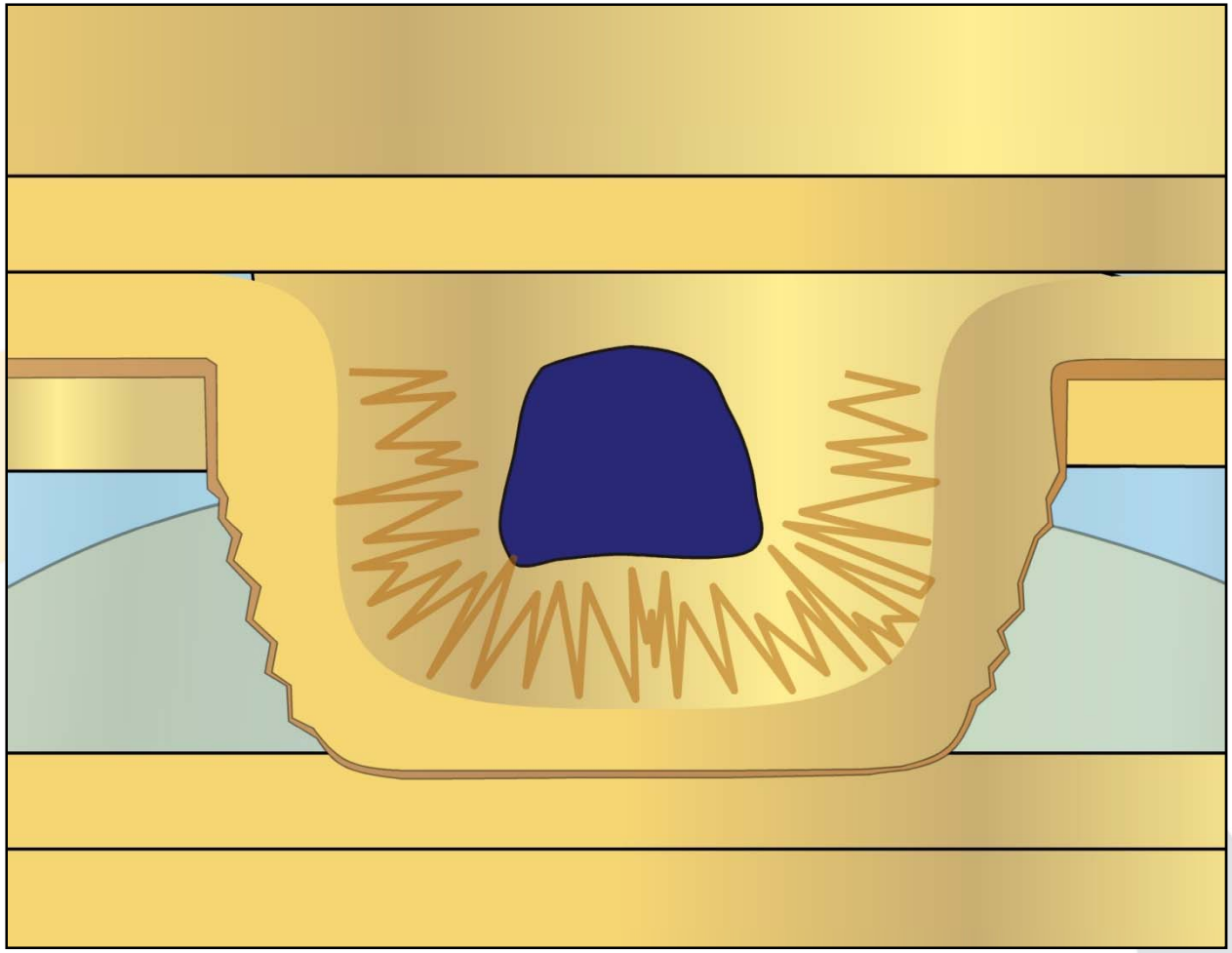
Filled Capped Microvias

- When a copper cap is used in a stacked MV the cap it is part of the conductive path and, can fail.
- If there is no interconnect structure above the copper cap, then the cap is not part of the conductive path and cannot fail
- Frequently the fill used in microvia has a different coefficient of thermal expansion (CTE) and glass transition temperature (Tg) than the surrounding dielectric materials.
- These mismatches in thermal properties are expressed as stress in the microvia. During thermal cycling an epoxy fill will become less viscous and distribute pressure equally throughout the microvia structure.
- This pressure can result in cracks developing in the interfaced between the bottom of the target pad and the top of the microvia wrap. The result is failure due to a lifted copper cap.

Filled Microvia – Copper Void



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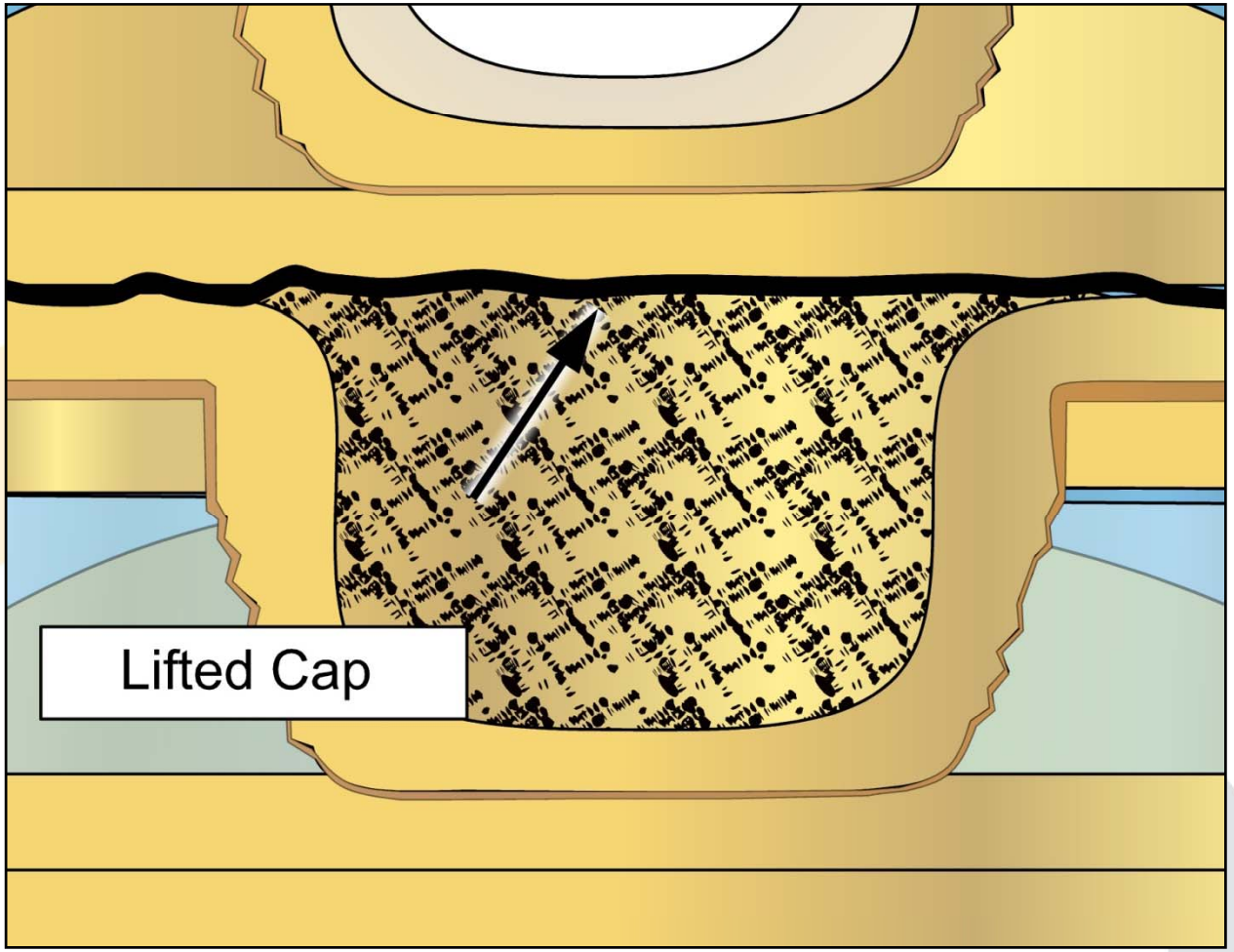
Filled Microvia – Copper Void

- A common condition of concern with copper filled microvias is voids in the electrolytic copper.
- The voids are usually plated closed. If the void was plated closed then there must be trapped acid copper plating solution.
- The solution appears to corrode the barrel of the copper until the solution is saturated.
- Micro sectioning usually removes the contaminates trapped in the voids. On occasion bizarre crystalline structures are formed as the void is plated closed.
- Copper void may reduce cycles to failure if the copper in the barrel of the hole compromises the hole wall thickness.
- Voids in the middle of the microvia where the copper in the barrel of the microvia is relatively thick may not influence thermal cycles to failure.

Filled Microvia – Lifted Copper Cap



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Conclusions/Observations

- The use of microvia interconnection structures in HDI applications is expanding
- The formation and fabrication of microvias is a challenge to fabricators due to their small size.
- Effective Microvia Testing - Higher Test temperature, 190C for FR4.
- Testing at 230C is being investigated for rigid polyimide constructions
- Using TM 2.6.26 DC Current Induced Thermal Cycle Test Power on MV
- Powering on microvia allows the power supply stop test in real time.
- A robust MV, dish shape, good microetch at the target pad, uniform distribution of the electroless and electrolytic copper, and typically has an aspect ratio of 1:1 or less.
- Microsections of microvias require a mild etch and a review at high power
- MV Failure modes target pad separation, barrel cracks, corner cracks, pull out failures and laser misregistration.
- Stacked, and filled include voids in copper filled microvia cap separation.

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