IPC Get Interconnected.™ MIDWEST CONFERENCE & EXHIBITION

Grounding to Control Noise and EMI

IPC Midwest Conference & Expo
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Rick Hartley

L-3 Avionics Systems

richard.hartley@L-3com.com

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Read - Understand Truth

Those who never retract their opinions love themselves more than they love truth. - Joseph Joubert, essayist (1754-1824)

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Read Books Not IC App Notes

Circuit Application notes produced by IC manufac-turers should be assumed Wrong until Proven Right!

Lee W. Ritchey

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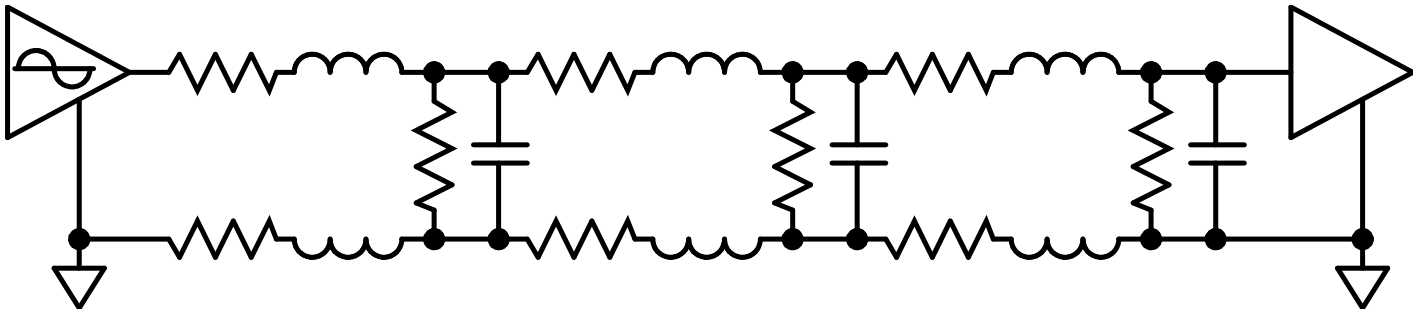
Signal Return Paths

- Transmission Line -
  - Any Pair or Wires or Conductors used to Move Energy From point A to point B
  - Usually of Controlled Size and in a Controlled Dielectric to create a Controlled Impedance (Zo).

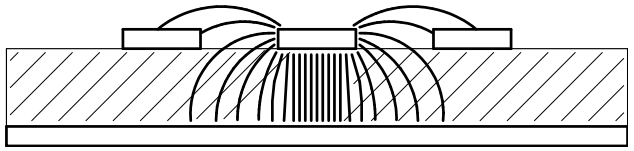


Evenly Distributed R, L, G & C – $Zo=\sqrt{\frac{R+j\omega L}{G+j\omega C}}$

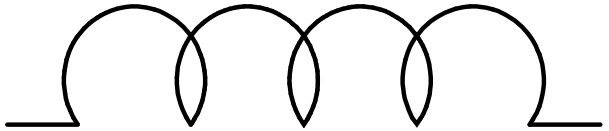
Signal Return Paths

Capacitance is formed by 2 conductive surfaces separated by an insulator.

Control Electric Field in Transmission Line by maintaining tight coupling between the Trace and Return Path.



Inductance is property of a circuit which allows Energy Storage in a Field Induced by Current Flow.



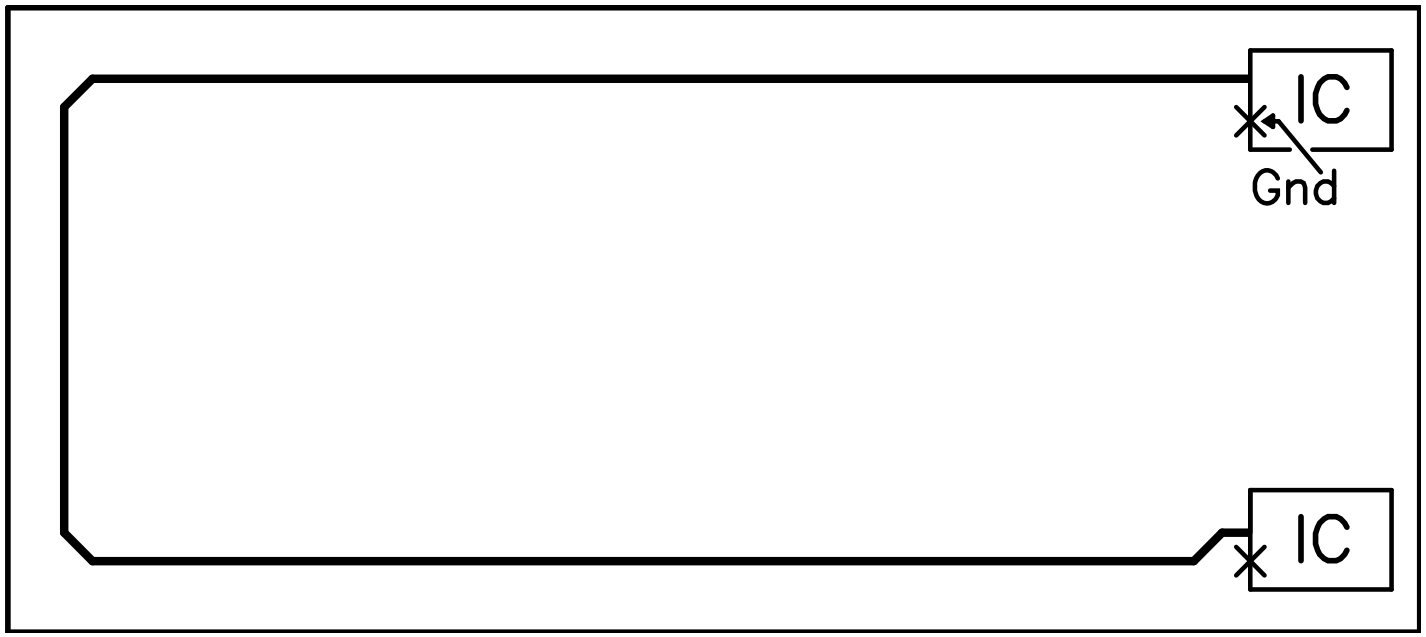
Tight coupling between forward and return path are secret to lowering Inductance in Circuit.

Signal Return Paths

- 2 Layer Microwave Style PC Board -

L1- Routed Signal, routed Power and poured Ground copper.

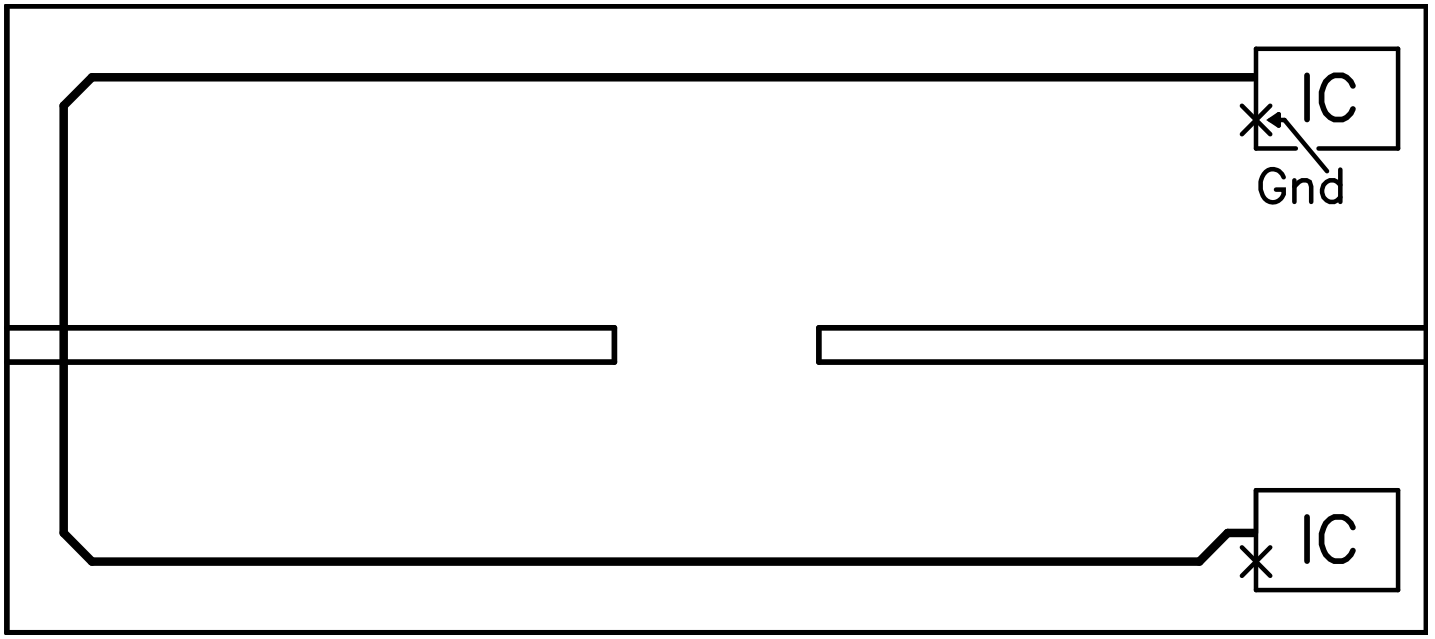
L2- Ground.



Where does signal's return current flow?

Signal Return Paths

- What happens if Return Plane is Split???

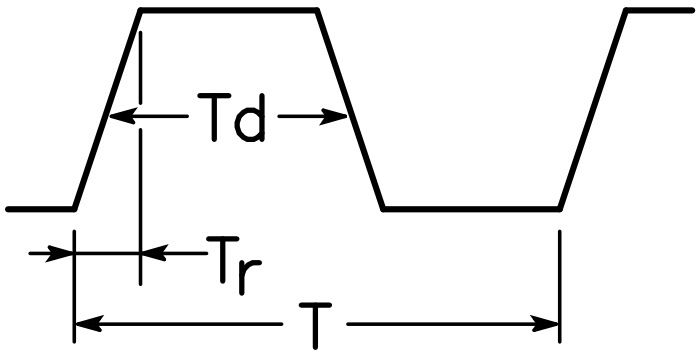


Now where does signal's return current flow?

Signal Return Paths

Digital Square Wave -

Time Domain

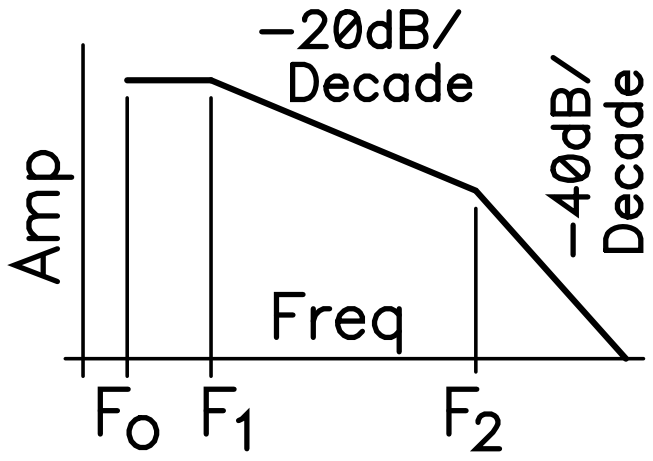


$F_o = 1/T$

$F_1 = 1/(\pi Td)$

$F_2 = 1/(\pi Tr)$

Frequency Domain



Signal Return Paths

- Highest Frequency of Dig Sig IS NOT the Clock.
- IS Frequency of the High Harmonics necessary to create the Fast Rising Edges of the Signal.
- Called Maximum Pulse Frequency.

F(freq-GHz)= .50 / Tr(rise/fall time-nSec*)

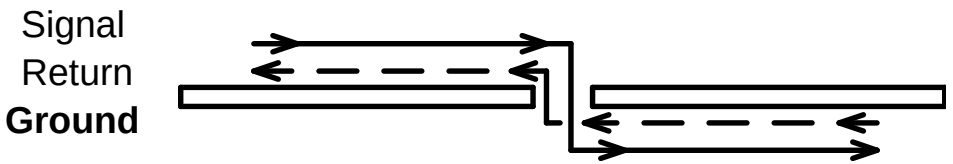
* (Tr = 10-90% (Typical))

* (Tf = 10-90% (Typical))

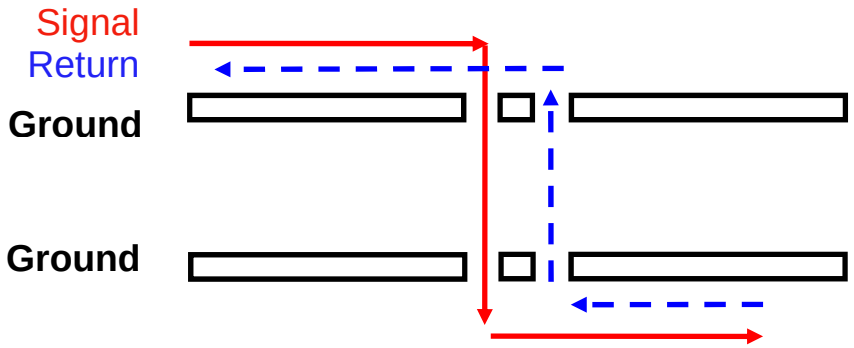
- Digital Frequency Bandwidth is from Clock to Maximum Pulse Frequency.

Signal Return Paths

- When moving signals between layers, route on either side of the same plane, as much as possible!!!

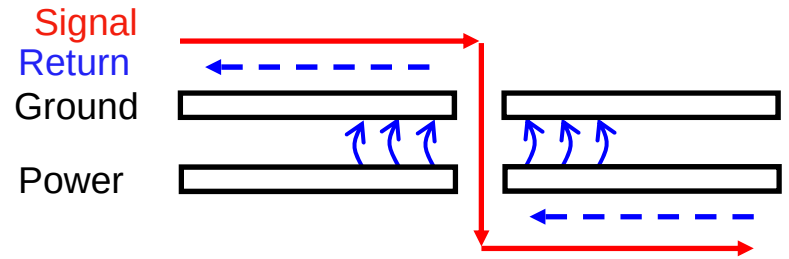


- When moving signals between 2 Gnd planes, use a transfer (stitching) via VERY near the signal via.

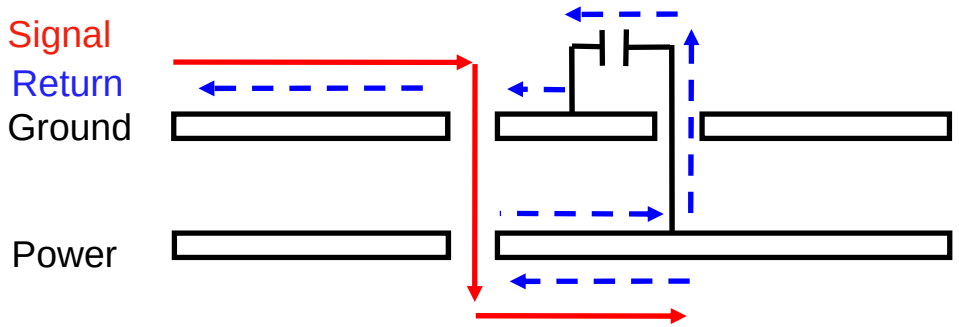


Signal Return Paths

- When routing signals from Power to Ground, Return energy will transfer as follows -

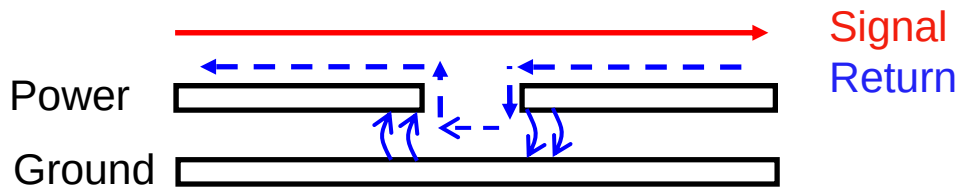


Tightly Coupled Planes



Loosely Coupled Planes w/ Cap. Cap has limited Freq Response and is Poor Path

Signal Return Paths



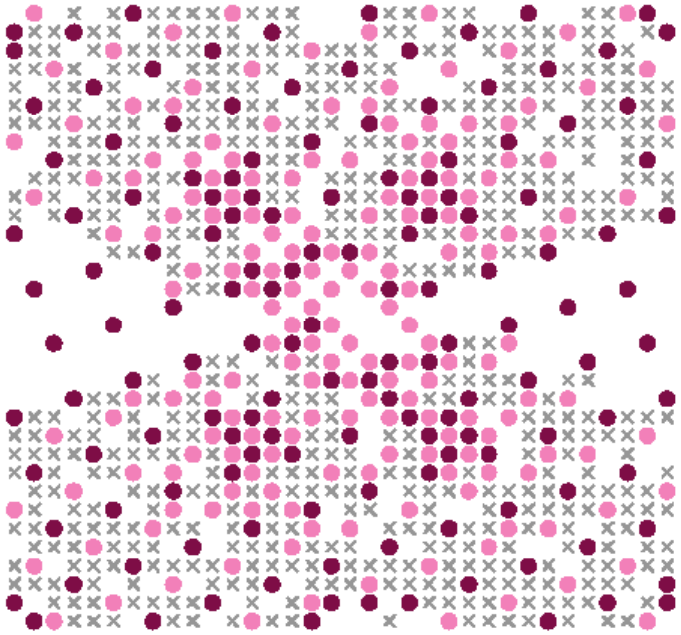
- With a second, un-split plane TIGHTLY coupled (<.008”) to the split plane, the return energy can capacitvely couple from the split plane to the whole plane and back again.
- If both planes of a pair are split, don’t cross at ANY frequency.

Signal Return Paths

Return Path equally important in IC Package.

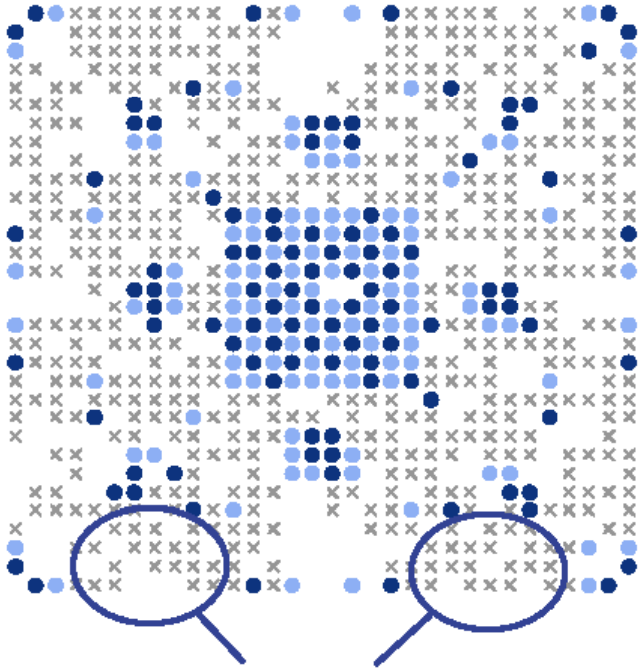
F1120 had 5X greater noise level than FF148 -

Xilinx Virtex-4 FF148



Returns spread evenly

Altera Stratix II F1120



Many regions devoid of returns

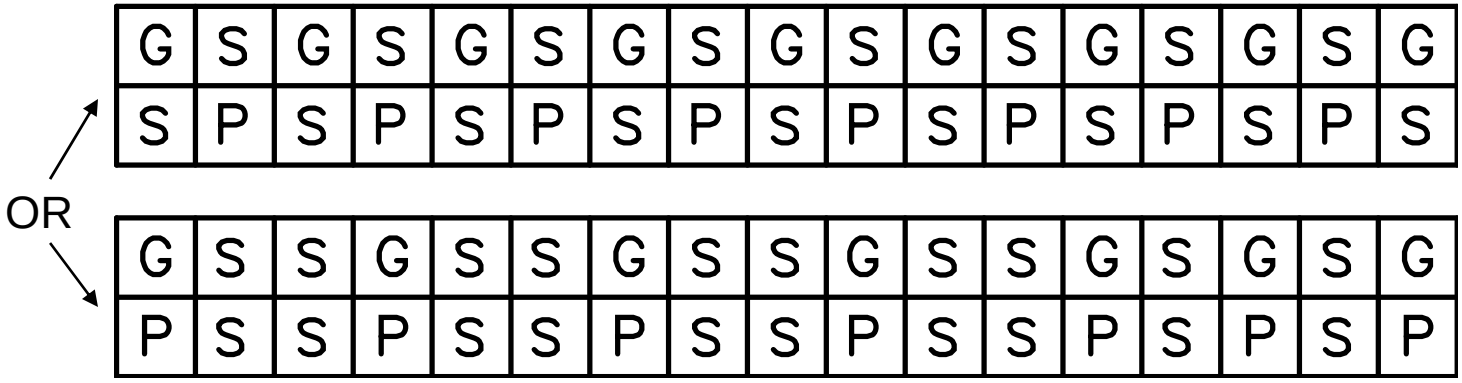
(Source: BGA Crosstalk - Dr. Howard Johnson)

Signal Return Paths

Return Path equally important in Connectors.

Conventional Connectors w/Digital Signals-

- Proper Pin Assignment to prevent Cross Coupling and Common Mode Noise:



Signal Return Paths

At this point it should be apparent that -

1) We MUST control the forward and return path of all Transmission Lines (Trace and Return Plane).
2) We MUST create as much Interplane Capacitance in PCBs as reasonably Possible.

How do we do this???

Signal Return Paths

Four(4) Layer Digital Designs

(A) ----Ground-----

----Sig/Pwr----

----Sig/Pwr----

----Ground-----

(B) ----Sig/Poured Pwr-----

---------Ground----------

---------Ground----------

----Sig/Poured Pwr-----

Signal Return Paths

Six(6) Layer Digital Designs

-Short Sig/Pwr-	----Sig/Pwr-----
----Sig/Gnd-----	----Ground-----
-----Power------	----Sig/Pwr-----
----Ground------	----Sig/Gnd-----
----Sig/Pwr-----	-----Power------
-Short Sig/Gnd-	----Sig/Gnd-----

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Signal Return Paths

Six(6) Layer Designs to AVOID

-----Signal------	-----Signal-----
-----Signal------	-----Power-----
----Ground------	-----Signal------
-----Power------	-----Signal------
-----Signal------	----Ground-----
-----Signal------	-----Signal------

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Signal Return Paths

Eight(8) Layer Digital Designs

----Signal-----	---Sig/Pwr----
---Ground-----	---Ground-----
----Signal-----	---Sig/Pwr----
----Power-----	---Ground-----
---Ground-----	----Power-----
----Signal-----	---Sig/Gnd----
---Ground-----	----Power-----
----Signal-----	---Sig/Gnd----

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Signal Return Paths

Eight(8) Layer Digital Designs

---Sig/Gnd----	---Sig/Gnd----	---Ground----
----Power-----	----Power-----	----Signal-----
---Ground-----	---Ground-----	----Signal-----
----Signal-----	---Sig/Pwr----	----Power-----
		---Ground----
----Signal-----	---Sig/Pwr----	----Signal-----
---Ground-----	---Ground-----	----Signal-----
----Power-----	----Power-----	---Ground----
---Sig/Gnd----	---Sig/Gnd ----	

Signal Return Paths

Eight(8) Layer Designs to AVOID

----Signal-----	----Signal-----	----Signal-----
----Signal-----	----Signal-----	----Power-----
----Signal-----	----Power-----	----Signal-----
----Power-----	----Signal-----	----Signal-----
---Ground----	----Signal-----	----Signal-----
----Signal-----	---Ground-----	----Signal-----
----Signal-----	----Signal------	---Ground-----
----Signal-----	----Signal------	----Signal-----

Signal Return Paths

- Board Stack Basics:
  - Signal Layers MUST be placed One Dielectric Layer away from Plane for Best Control of Impedance and Noise.
  - Outer Layers have Poorest Impedance Control and Poorest Cross Talk Control.
  - Plane Pairs give Highest Interplane Capacitance (Critical for EMI).
  - Copper Pours on all Layers (assign as Alternating Power and Ground) increase Interplane Capacitance.
  - Copper Pours help to Balance Board for lower fabrication cost.

Signal Return Paths

- IC Selection:
  - Paired Power/Ground Pins (Avoid ICs with Corner Power Pins).
  - Lowest Vcc Level that Satisfies Circuit Needs (i.e- 3.3v vs 5v, 1.8v vs 3.3v).
  - Dedicated Return Pins for Critical Signals.
  - Power & Ground Plane Pairs on Internal PCB.
  - Internal Decoupling Capacitors.
  - Direct Chip Attachment, Not Bond Wire (Limited Availability).