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Solving the Metric Pitch BGA & Micro BGA Dilemma

The following presentation provides Via fanout and trace routing solutions for various metric pitch Ball Grid Array Packages

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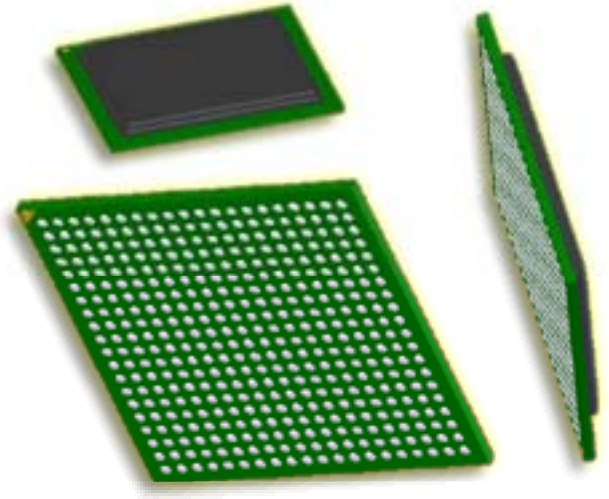
Presented By:

Tom Hausherr



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METRIC BGA FEATURE SIZES

- The starting point to solve the metric pitch BGA dilemma is a basic understanding of the metric feature sizes for –
  - BGA ball sizes
  - BGA land pattern pad construction
  - BGA Via anatomy
  - Trace / Space
  - Trace and via routing grid
  - HDI hole size / annular ring

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BGA BALL & PAD SIZES

Table 14-5 Land Approximation (mm) for Collapsible Solder Balls

Nominal Ball Diameter	Reduction	Land Pattern Density Level	Nominal Land Diameter	Land Variation
0.75	25%	A	0.55	0.60 - 0.50
0.65	25%	A	0.50	0.55 - 0.45
0.60	25%	A	0.45	0.50 - 0.40
0.55	25%	A	0.40	0.45 - 0.35
0.50	20%	B	0.40	0.45 - 0.35
0.45	20%	B	0.35	0.40 - 0.30
0.40	20%	B	0.30	0.35 - 0.25
0.35	20%	B	0.30	0.35 - 0.25
0.30	20%	B	0.25	0.25 - 0.20
0.25	20%	B	0.20	0.20 - 0.17
0.20	15%	C	0.17	0.20 - 0.14
0.17	15%	C	0.15	0.18 - 0.12
0.15	15%	C	0.13	0.15 - 0.10

Note: The IPC-7351A LP Calculator Uses this chart for calculations

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BGA 3-TIER BALL SIZE

Table 3-18 Ball Grid Array Components (Unit: mm)

Lead Part	Minimum (Least) Density Level C	Median (Nominal) Density Level B	Maximum (Most) Density Level A
Periphery Collapsing Ball	15% reduction below nominal ball diameter	20% reduction below nominal ball diameter	25% reduction below nominal ball diameter
Periphery Noncollapsing Ball or Column	5% increase above the nominal ball or column diameter	10% increase above the nominal ball or column diameter	15% increase above the nominal ball or column diameter
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.50	1.00	2.00
Ball Grid Array **(BGA)** Construction and land pattern development are described in 14.1 & 14.4			
Column Grid Array **(CGA)** Construction and land pattern development are described in 14.1.3 & 14.4			

ANATOMY OF THE METRIC VIA

- The base value round-off for metric via features are in 0.05mm increments. This includes –
  - Pad Size
  - Hole Size
  - Solder Mask Size
  - Plane Clearance (Anti-pad) Size
  - Plane Thermal Relief Size or None

METRIC BGA VIA SIZES FOR DOGBONE VIA FANOUT

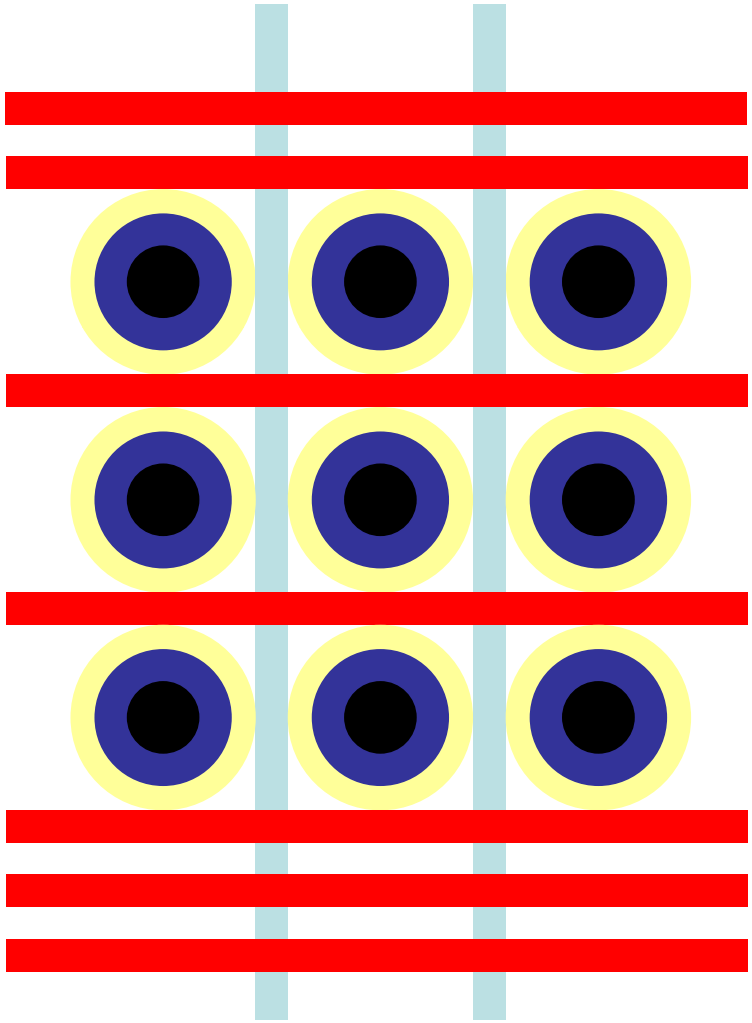
BGA Pin Pitch	VIA Name	Pad	Hole	Plane Anti-Pad	Solder Mask	Thermal ID	Thermal OD	Thermal Spoke Width
1.50mm	VIA60-25-80	0.60	0.25	0.80	0.00	0.55	0.80	0.25 or None
1.50mm	VIA55-25-75	0.55	0.25	0.75	0.00	0.55	0.75	0.25 or None
1.27mm	VIA63-30-85	0.635	0.30	0.85	0.00	0.65	0.85	0.25 or None
1.00mm	VIA55-25-75	0.55	0.25	0.75	0.00	0.55	0.75	0.25 or None
1.00mm	VIA50-25-70	0.50	0.25	0.70	0.00	0.55	0.70	0.25 or None
0.80mm	VIA45-20-65	0.45	0.20	0.65	0.00	0.50	0.65	0.20 or None
0.75mm	VIA40-20-65	0.40	0.20	0.65	0.00	0.50	0.65	0.20 or None

Show via calculator

METRIC TRACE/SPACE SIZES

- Metric trace widths are in 0.025mm (1 mil) increments
- Common metric BGA trace widths
  - 0.075mm (3 mils)
  - 0.1mm (4 mils)
  - 0.125mm (5 mils)
  - 0.15mm (6 mils)
  - 0.2mm (8 mils)

0.5mm PITCH BGA



Via-in-Pad Technology

BGA Ball Size: 0.30 (12)
BGA Pad Dia: 0.275 (11)
Hole Size: 0.15 (6)
Thermal Relief Required
Anti-Pad: 0.425 (17)
Solder Mask: 1:1 scale

Trace/Space Data

Trace Width: 0.075 (3)
Trace/Trace Space: 0.075
Trace/Via Space: 0.075 (3)
Trace/BGA Pad: 0.75 (3)
Routing Grid: 0.05 (2)
Via Grid: 0.5 (20)
Part Place Grid: 1 (40)

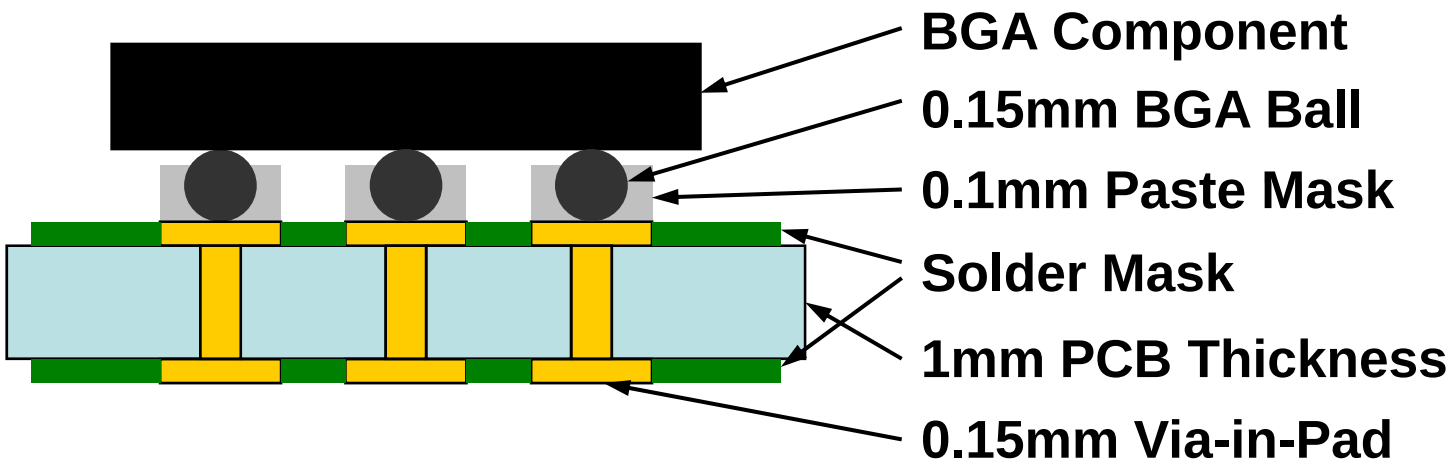
0.5mm PITCH BGA WITH NON-COLLAPSING BALLS

Via-in-Pad Technology

BGA Ball Size: 0.15 (6)
BGA Pad Dia: 0.275 (11)
Hole Size: 0.15 (6)
Anti-Pad: 0.425 (17)
Solder Mask: 1:1 scale

Trace/Space Data

Trace Width: 0.075 (3)
Trace/Trace Space: 0.075
Trace/Via Space: 0.075 (3)
Trace/BGA Pad: 0.75 (3)
Routing Grid: 0.05 (2)



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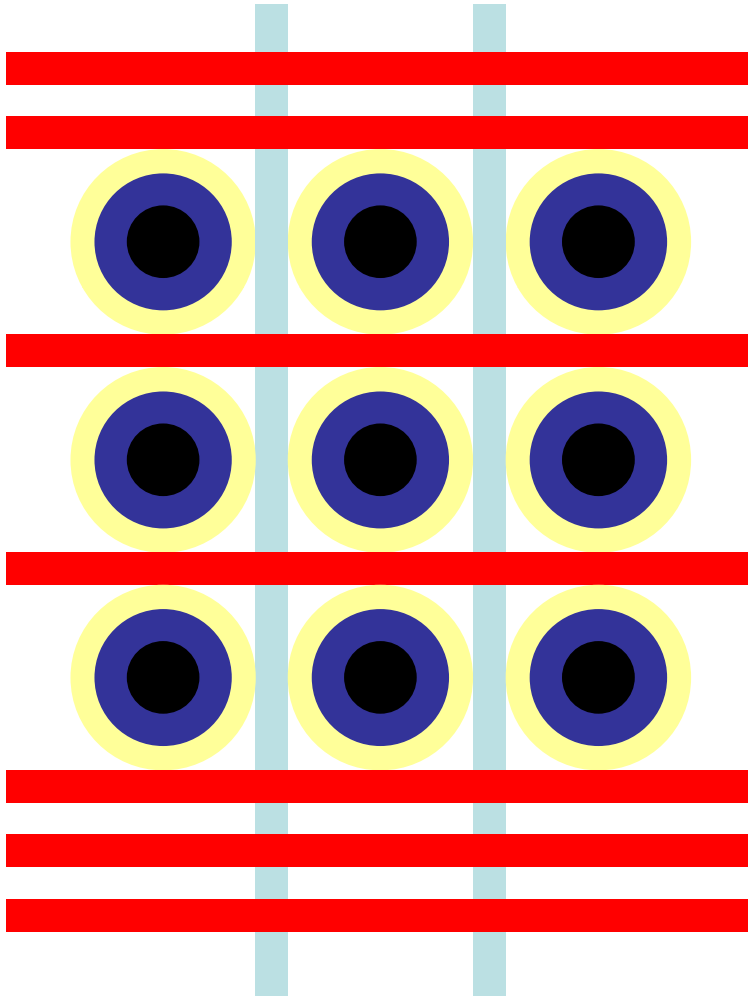
0.65mm PITCH BGA



Via-in-Pad Technology

BGA Ball Size: 0.4 (16)
BGA Pad Dia: 0.4 (16)
Hole Size: 0.15 (6)
Anti-Pad: 0.5 (20)
Solder Mask: 1:1 scale

Trace/Space Data

Trace Width: 0.1 (4)
Trace/Trace Space: 0.1 (4)
Trace/Via Space: 0.1 (4)
Trace/BGA Pad: 0.75 (3)
Routing Grid: 0.05 (2)
Via Grid: 0.65 (26)
Part Place Grid: 1 (40)

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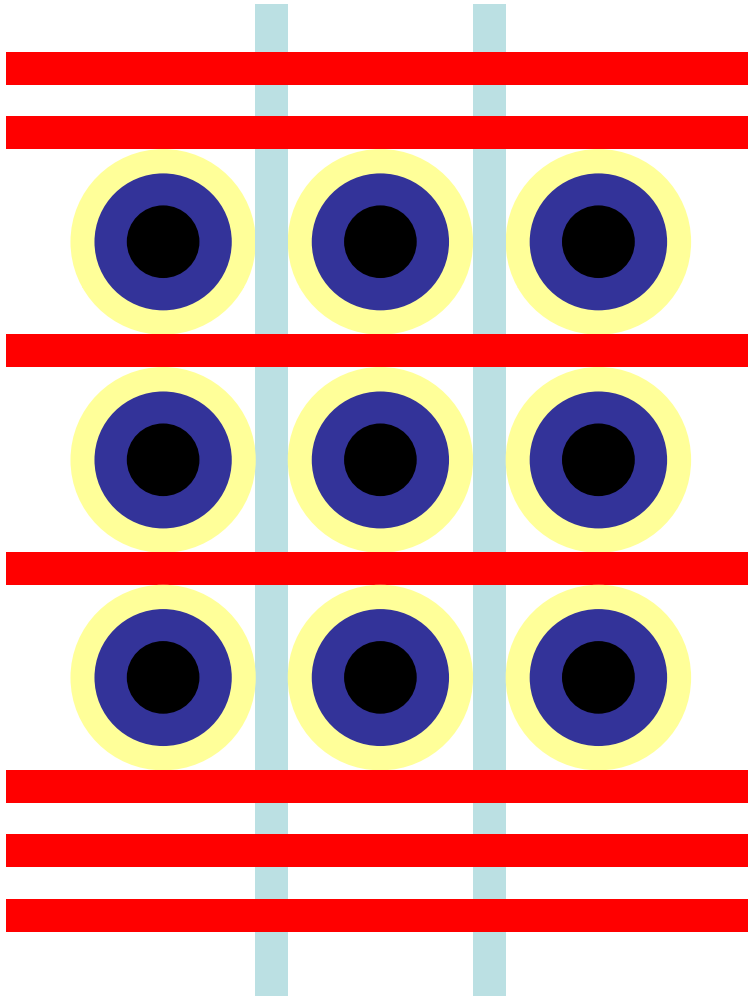
0.65mm PITCH BGA



Via-in-Pad Technology

BGA Ball Size: 0.4 (16)
BGA Pad Dia: 0.425 (17)
Hole Size: 0.2 (8)
Anti-Pad: 0.575 (23)
Solder Mask: 1:1 scale

Trace/Space Data

Trace Width: 0.075 (3)
Trace/Trace Space: 0.075
Trace/Via Space: 0.075 (3)
Routing Grid: 0.05 (2)
Via Grid: 0.65 (26)
Part Place Grid: 1 (40)

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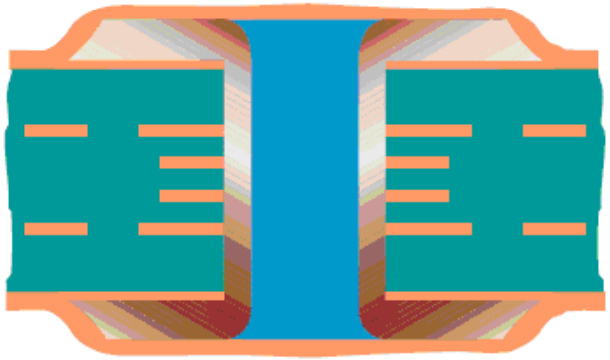
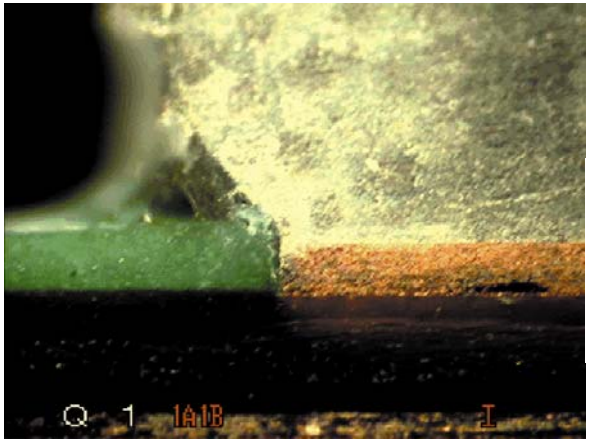
FILLED AND CAPPED VIA

Filled and Capped Via (Type VII Via) - A Type V via with a secondary metallized coating covering the via. The metallization is on both sides.

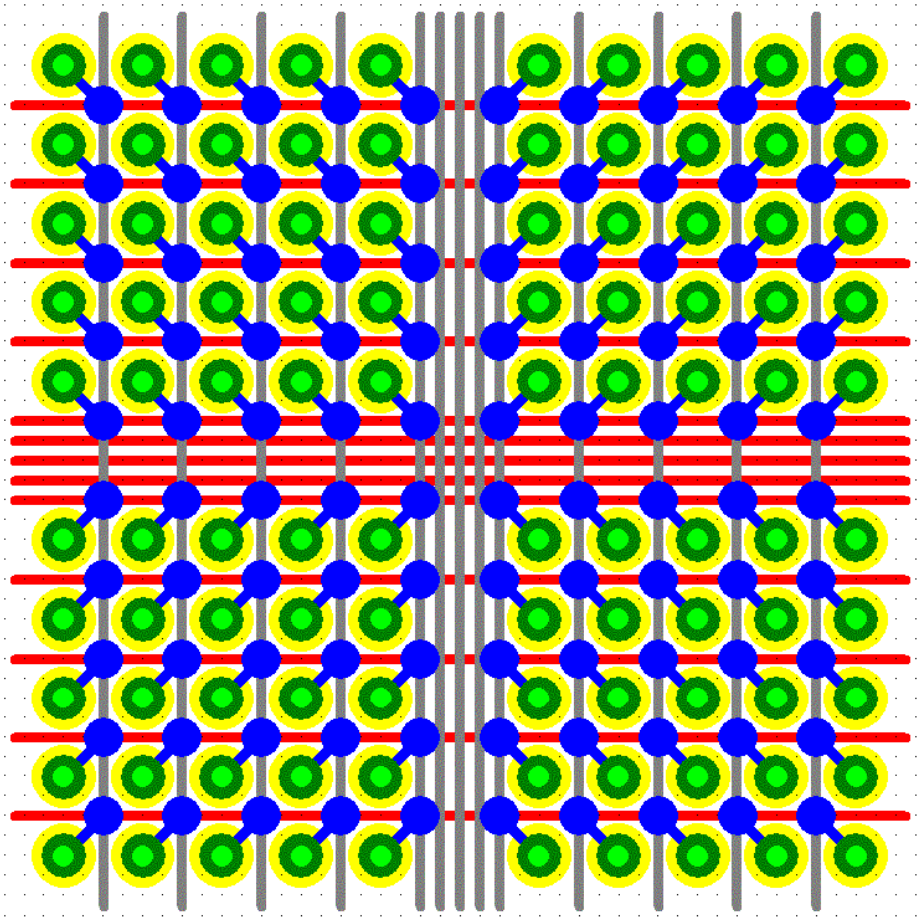
This technique is used for Via-in-pad technology for 0.65mm and 0.5mm BGA pitch devices.

Solder mask is 1:1 scale on the BGA side of PCB and Tented on the opposite side to protect the routed trace.





0.8mm PITCH BGA



BGA Data

BGA Ball Dia: 0.5 (20)
BGA Pad Size: 0.4 (16)
Solder Mask: 1:1 scale

Via Data

Pad Size: 0.5 (20)
Hole Size: 0.25 (10)
Anti-Pad: 0.7 (28)

Trace/Space Data

Trace Width: 0.1 (4)
Trace/Trace Space: .1
Trace/Via Space: .125
Routing Grid: 0.1 (4)
Via Grid: 0.2 (8)
Part Place Grid: 1 (40)

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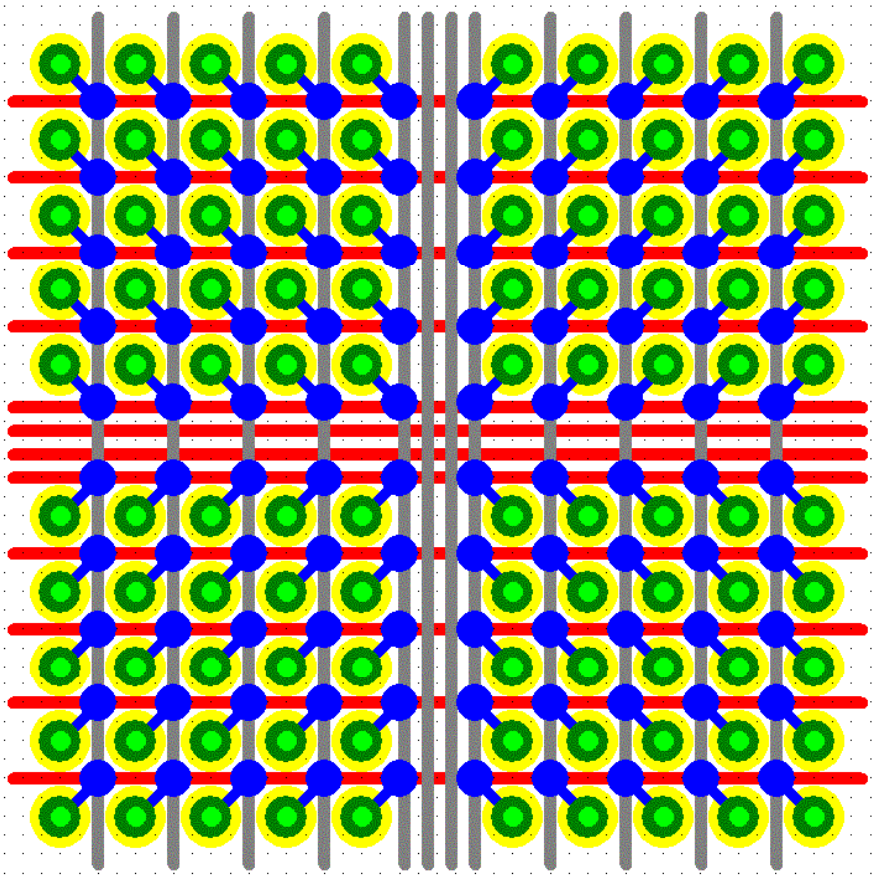
0.8mm PITCH BGA



BGA Data

BGA Ball Dia: 0.5 (20)
BGA Pad Size: 0.4 (16)
Solder Mask: 1:1 scale

Via Data

Pad: 0.45 (18)
Hole: 0.2 (8)
Anti-Pad: 0.65 (26)

Trace/Space Data

Trace Width: 0.125 (5)
Trace/Trace Space: .125
Trace/Via Space: 0.1 (4)
Routing Grid: 0.05 (2)
Via Grid: 0.2 (8)
Part Place Grid: 1 (40)

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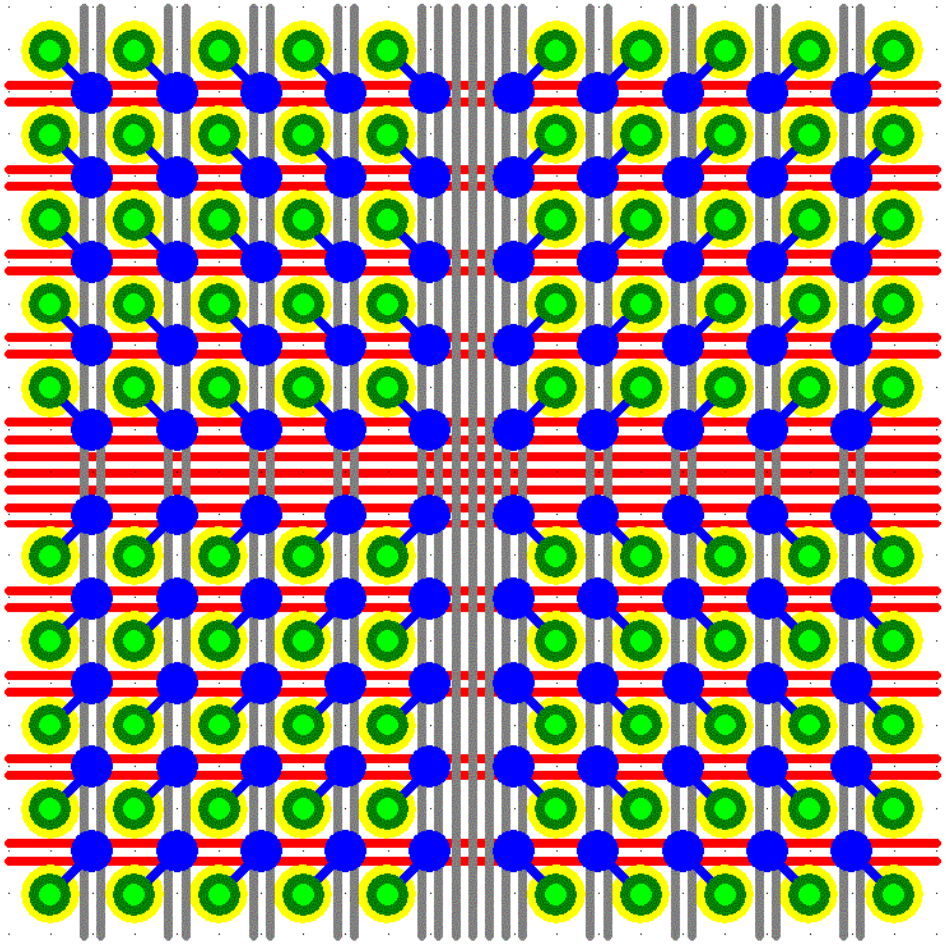
1mm PITCH BGA



Via Data

Pad: 0.50 (20)
Hole: 0.25 (10)
Anti-Pad: 0.70 (28)

BGA Pad Size: 0.5 (20)

Trace/Space Data

Trace Width: 0.1 (4)
Trace/Trace Space: 0.1
Trace/Via Space: 0.1
Routing Grid: 0.1 (4)
Via Grid: 1 (40)
Part Place Grid: 0.5 (20)

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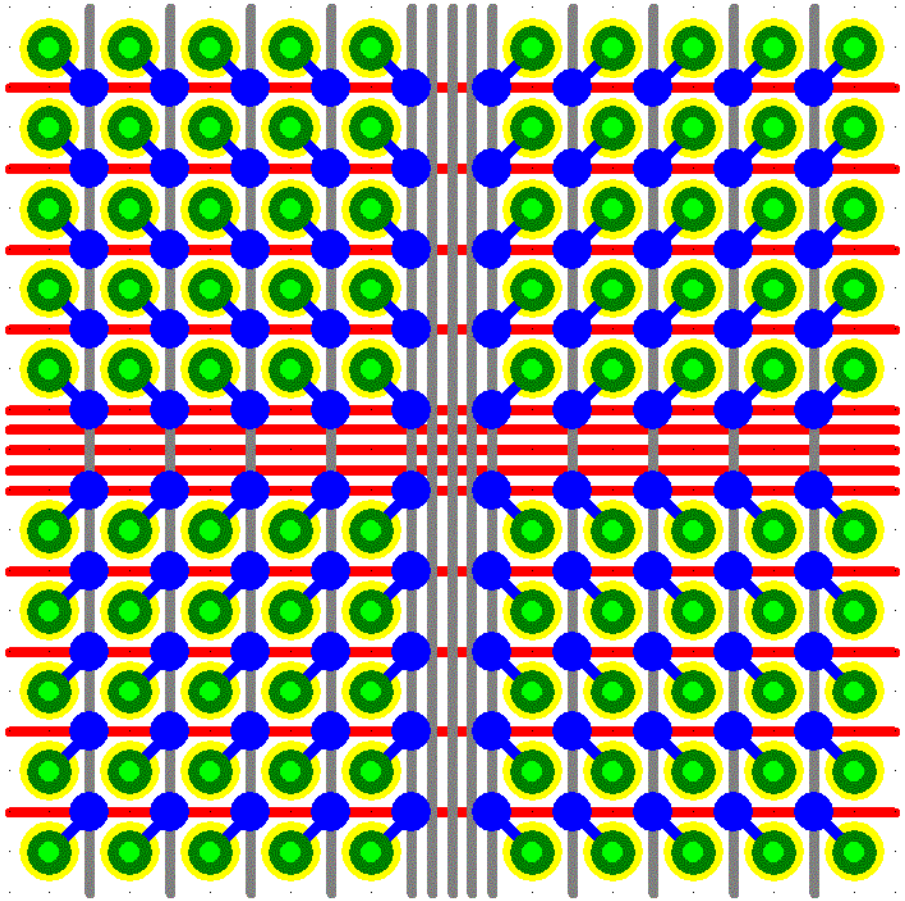
1mm PITCH BGA



Via Data

Pad: 0.55 (22)

Hole: 0.25 (10)

Anti-Pad: 0.75 (30)

BGA Pad Size: 0.5 (20)

Trace/Space Data

Trace Width: 0.125 (5)

Trace/Trace Space: 0.125

Trace/Via Space: 0.16 (6)

Routing Grid: 0.05 (2)

Via Grid: 1 (40)

Part Place Grid: 0.5 (20)

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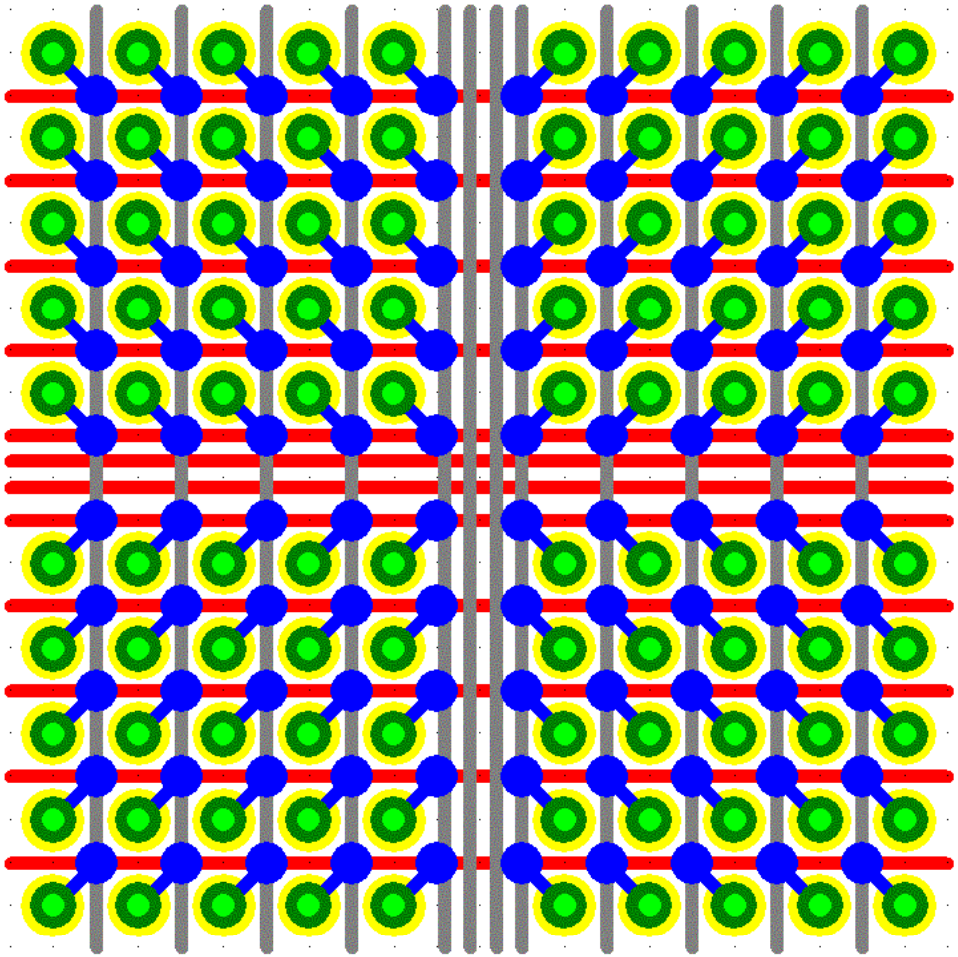
1mm PITCH BGA



Via Data

Pad: 0.55 (22)

Hole: 0.25 (10)

Anti-Pad: 0.75 (28)

BGA Pad Size: 0.5 (20)

Trace/Space Data

Trace Width: 0.15 (6)

Trace/Trace Space:0.15

Trace/Via Space: 0.15

Routing Grid: 0.1 (4)

Via Grid: 1 (40)

Part Place Grid: 0.5 (20)

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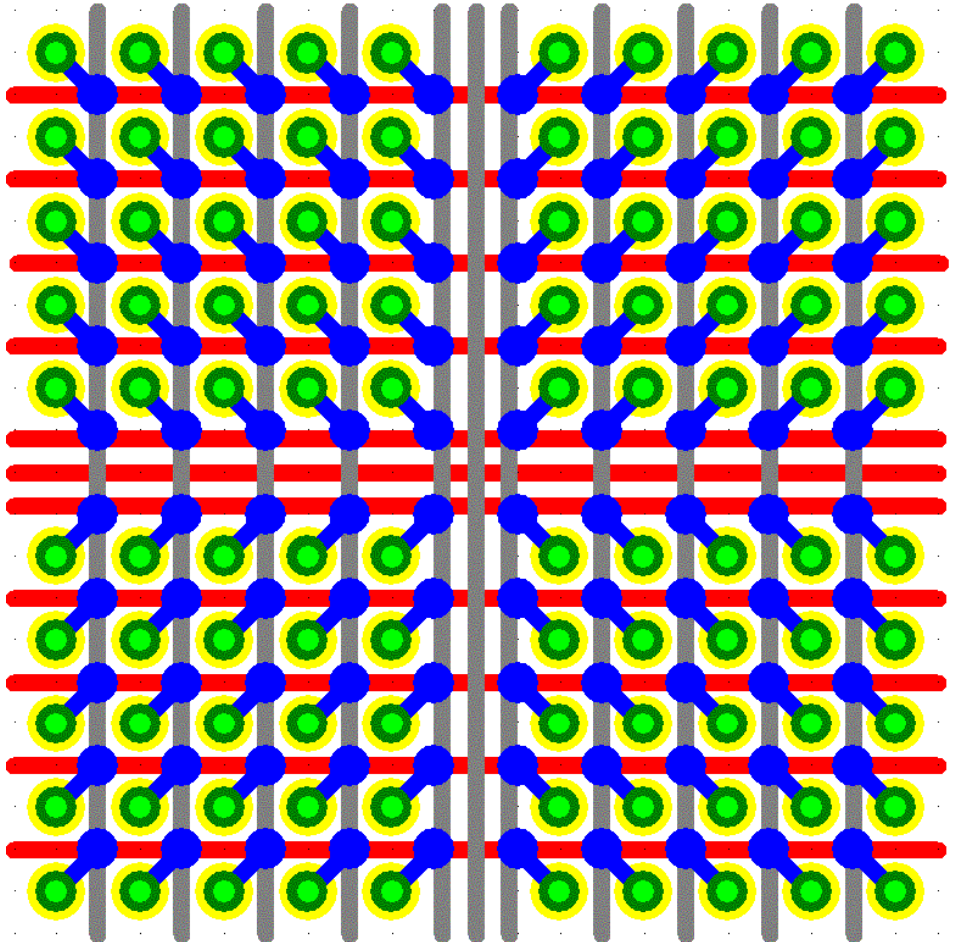
1mm PITCH BGA



Via Data

Pad: 0.50 (20)
Hole: 0.25 (10)
Anti-Pad: 0.70 (28)

BGA Pad Size: 0.5 (20)

Trace/Space Data

Trace Width: 0.2 (8)
Trace/Trace Space: 0.2
Trace/Via Space: 0.15
Routing Grid: 0.1 (4)
Via Grid: 1 (40)
Part Place Grid: 0.5 (20)

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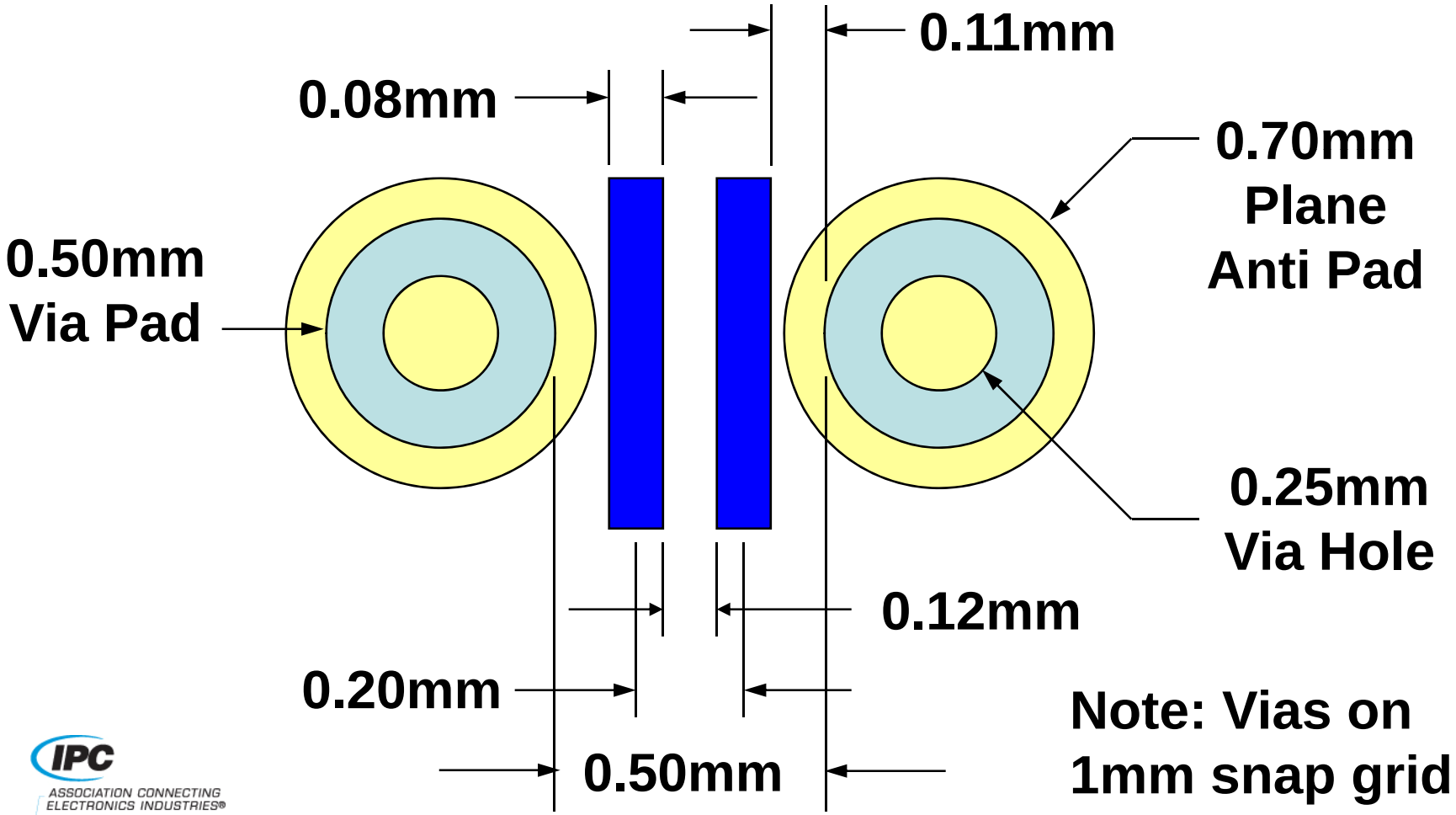
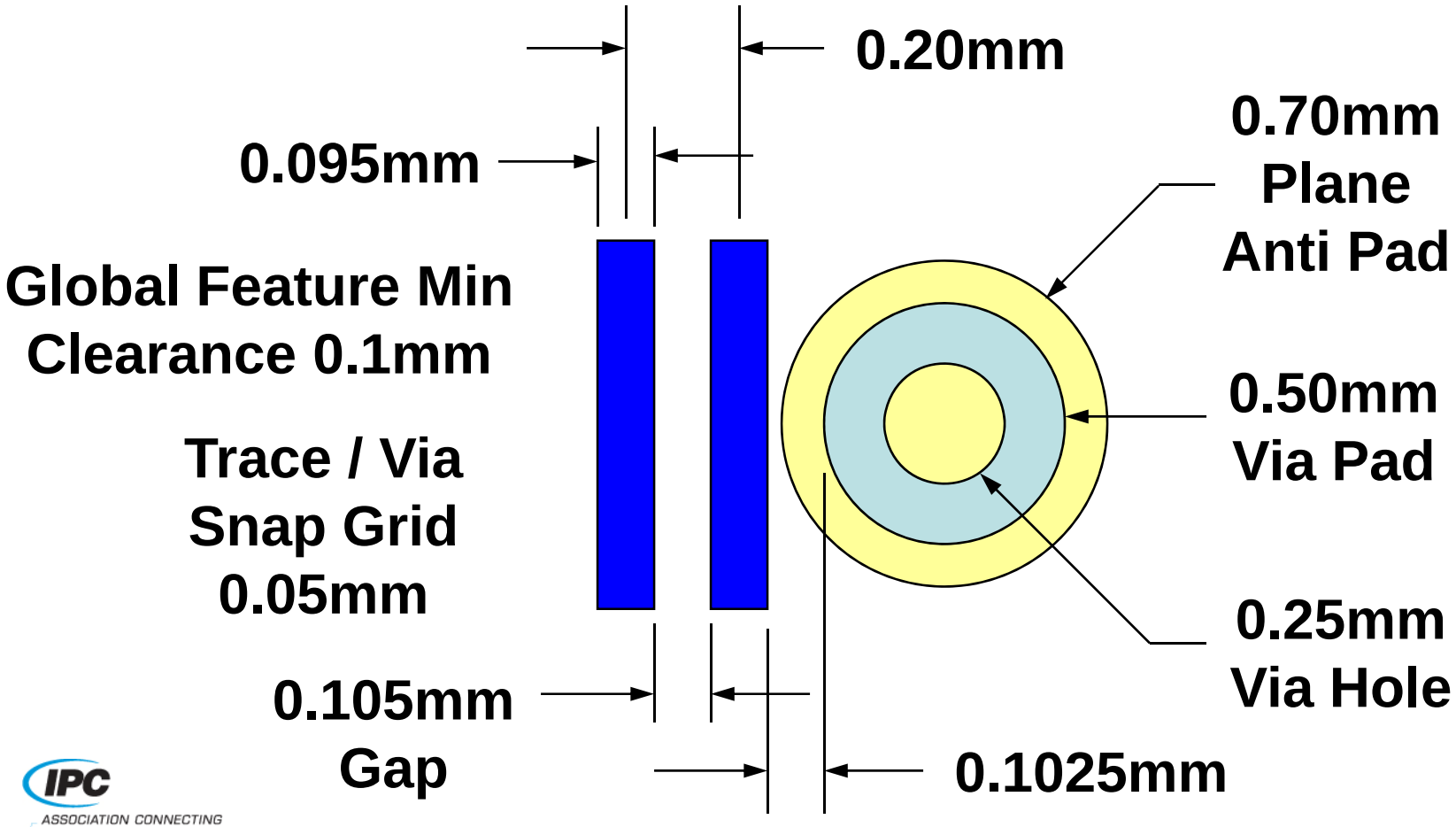
1mm PITCH BGA

100 Ohm Differential Pairs
Internal Layers (20 layer Bd)



1mm PITCH BGA

50 Ohm Single Ended Traces
Internal Layers (20 layer Bd)



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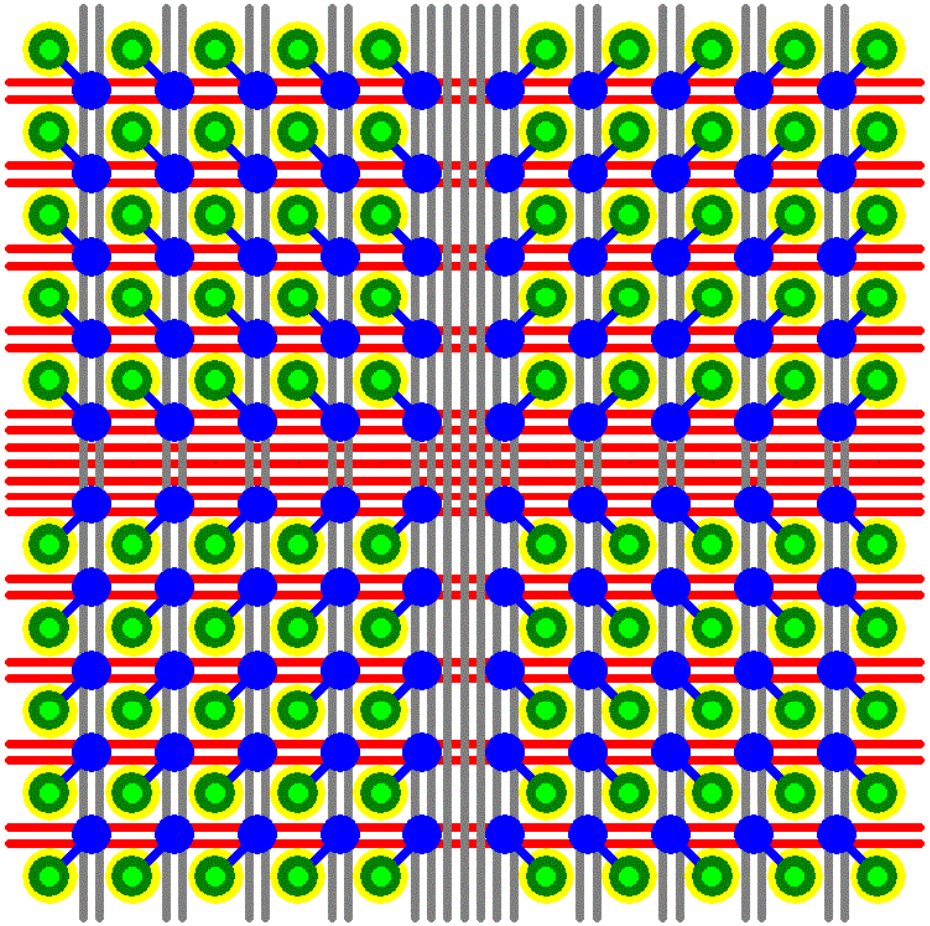
1.27mm PITCH BGA



Via Data

Pad: 0.635 (25)

Hole: 0.30 (12)

Anti-Pad: 0.85 (33)

BGA Pad Size: 0.6 (24)

Trace/Space Data

Trace Width: 0.127 (5)

Trace/Trace Space:.127

Trace/Via Space: 0.127

Routing Grid: 0.127 (5)

Via Grid: 0.635 (25)

Part Place Grid 1: 1.27

Part Place Grid 2: 0.635

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METRIC BGA SNAP GRIDS

Part Placement, Via Fanout and Routing grids should be evenly divisible into 1mm

Metric Working Grids	Metric Non-Working Grids
1	0.9
0.5	0.8
0.25	0.7
0.2	0.6
0.125	0.4
0.1	0.3
0.05	0.15

PLACEMENT & VIA FANOUT

- When placing components on a PCB Design, always have your Via Display Grid turned on.
- When you place the parts, place the part pins evenly in-between your Via Display Grid to optimize the via fanout lengths and maximize your available routing channels.
- You may have to use various placement grids to accomplish this, but you will enhance the routing phase of the PCB Design layout.

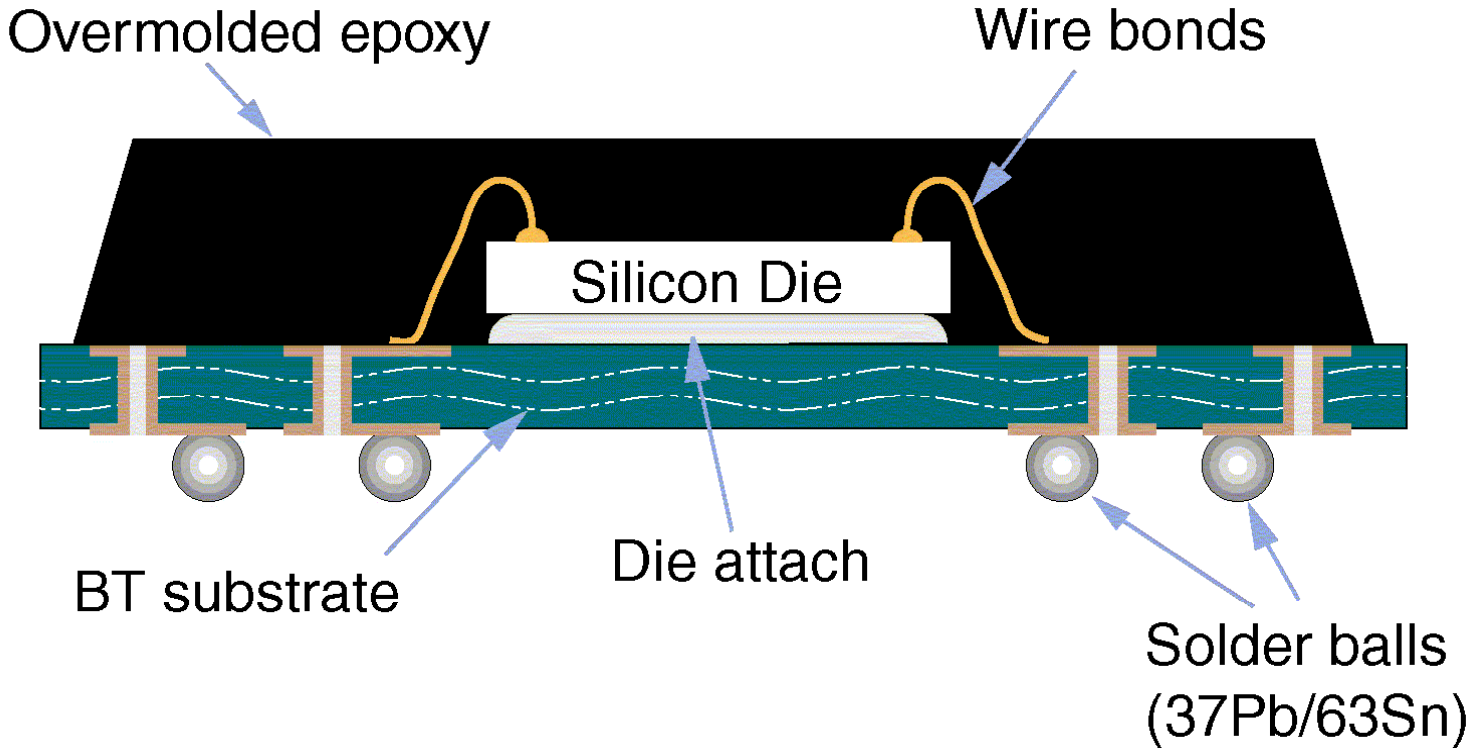
OPTIMAL VIA PADSTACKS

- **0.1 Trace Width / 0.1 Route Grid**
  - **Pad Size: 0.5**
  - **Hole Size: 0.25**
  - **Anti-pad: 0.7 – Avoid Trace / Anti-pad Overlap**
- **0.125 Trace Width / 0.05 Route Grid**
  - **Pad Size: 0.65**
  - **Hole Size: 0.3**
  - **Anti-pad: 0.8 – Avoid Trace / Anti-pad Overlap**
- **0.15 Trace Width / 0.05 Route Grid**
  - **Pad Size: 0.55**
  - **Hole Size: 0.25**
  - **Anti-pad: 0.75 – Avoid Trace / Anti-pad Overlap**

MAXIMIZE ROUTING CHANNELS

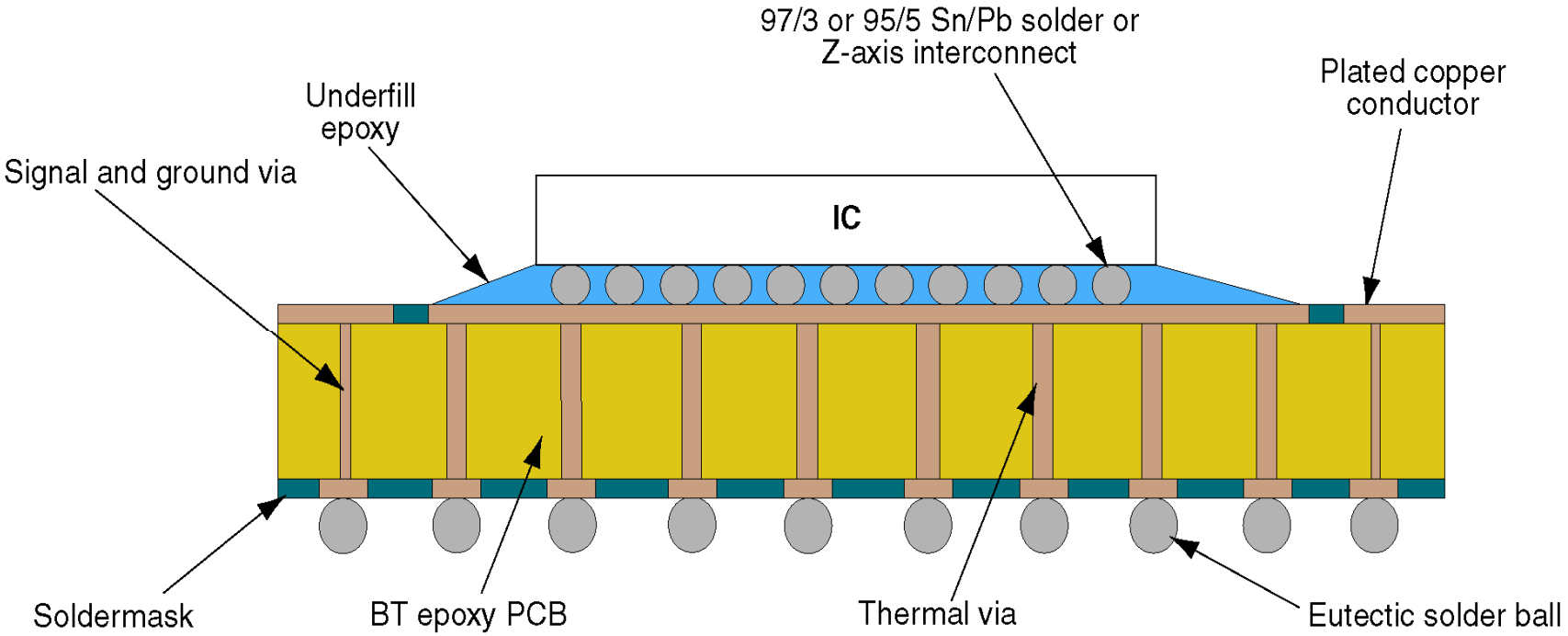
- Design your PCB like you are planning a housing development
- First establish where all the freeways are going to go – Buss Routes and Main Arteries
- Then establish the local road map – Trace Routes that don't have to bend
- Then build the houses along each side of the local roads – Via Sites

PLASTIC BALL GRID ARRAY, CHIP WIRE BONDED



Note: Interposer land area is solder mask defined

BALL GRID ARRAY, FLIP CHIP BONDED



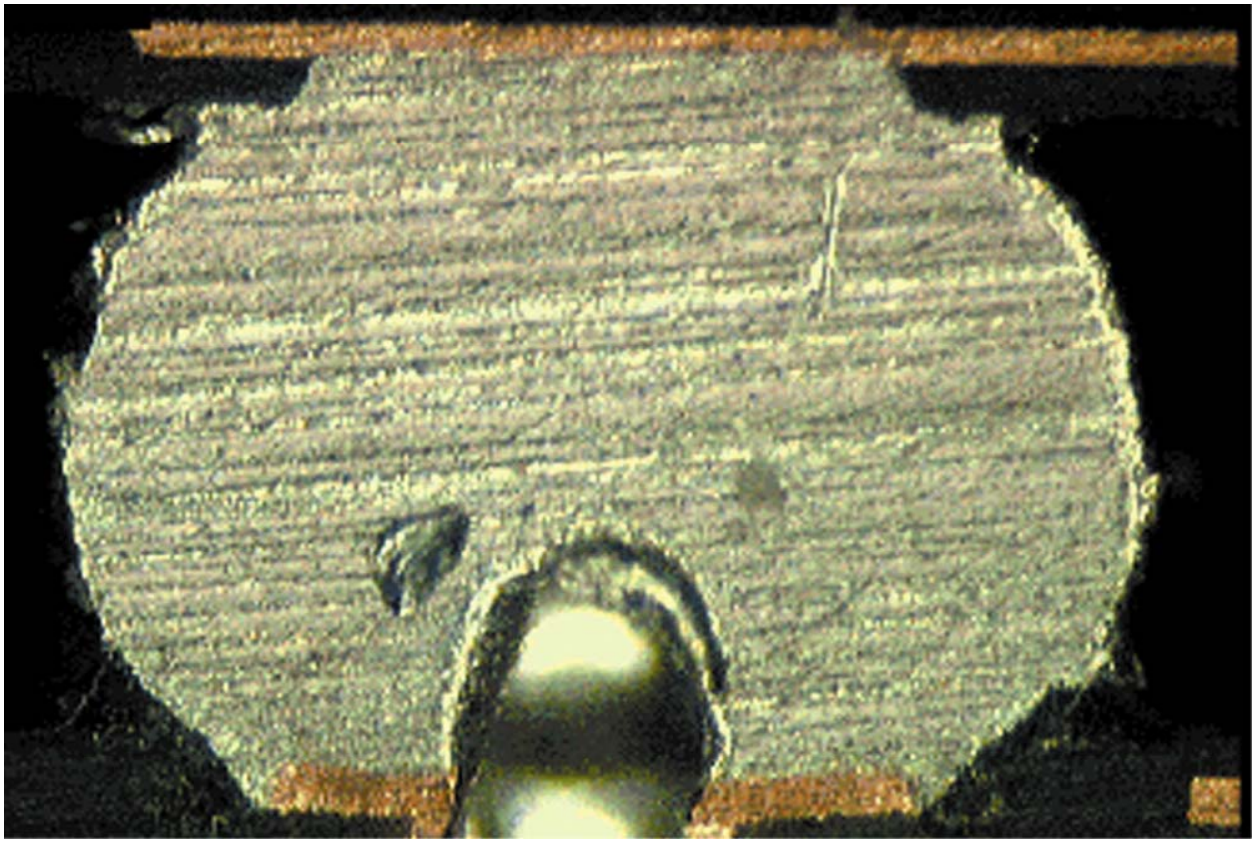
Note: Interposer land area is solder mask defined

VIA-IN-PAD AND IMPACT ON RELIABIITY

Via-in-Pad (through-hole via, capped on bottom of the board) for BGA Lands cause voids in the BGA solder joints, which may impact reliability.

Current data indicates that, for the standard 25 - 35 mm package body with 0.75 mm balls, there is no reliability risk from voids. Accelerated aging tests have been performed and the failure rate was statistically equivalent to standard dog bone designs. It appears that void consistency is more important than void size with respect to joint reliability.

CROSS SECTION OF 0.75mm BALL WITH VIA-IN-PAD STRUCTURE



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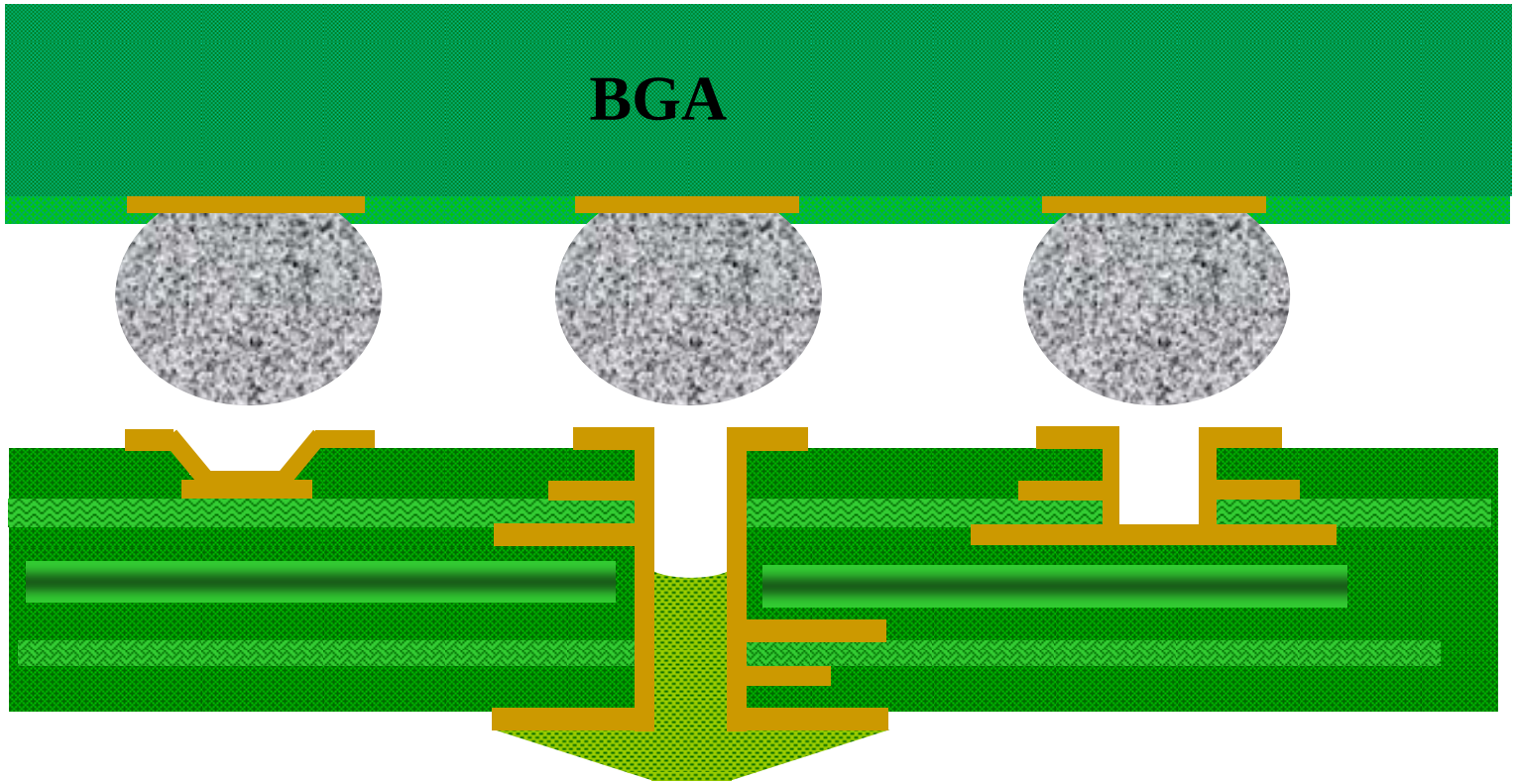
BEFORE ASSEMBLY PROCESS



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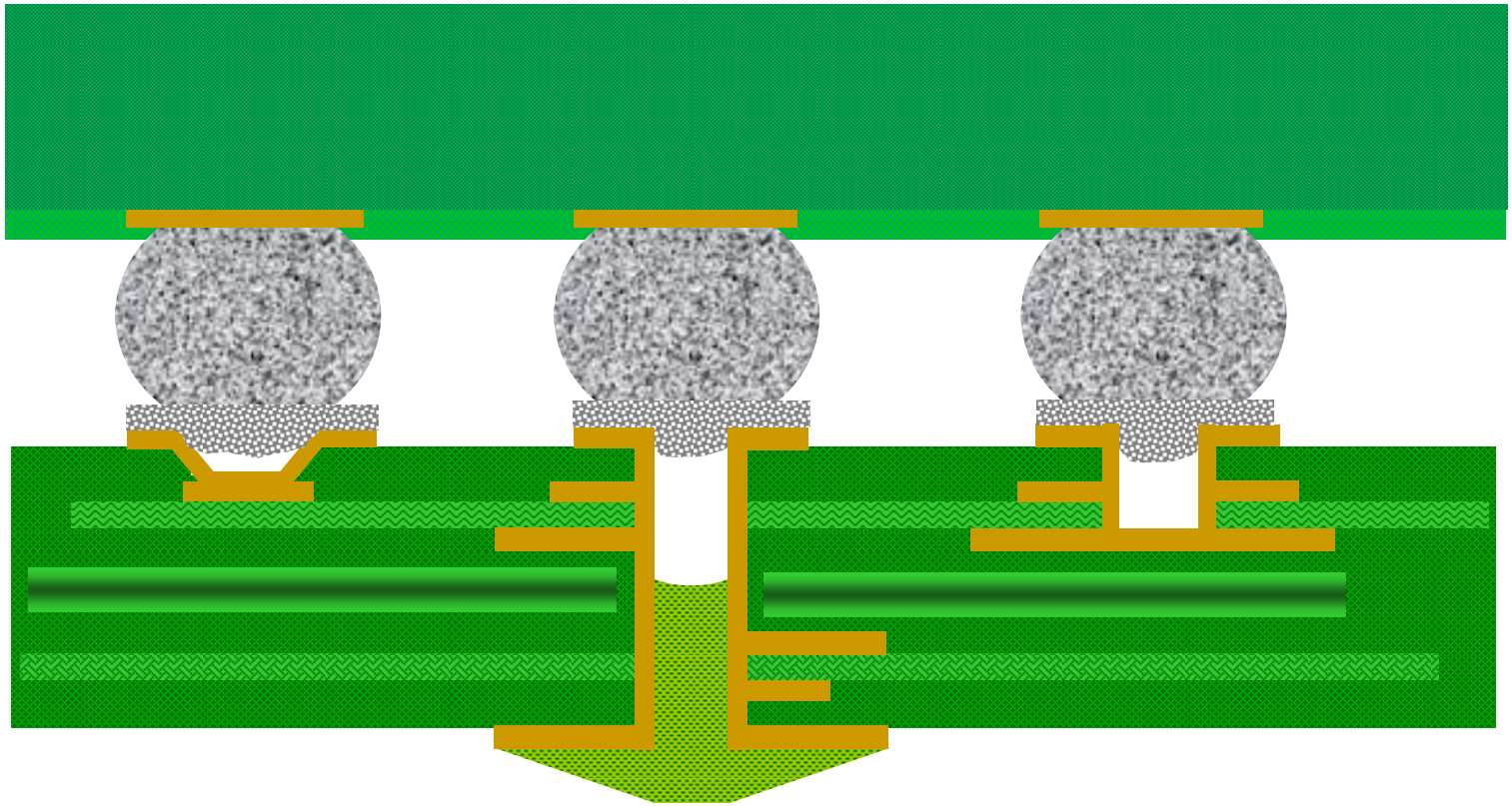
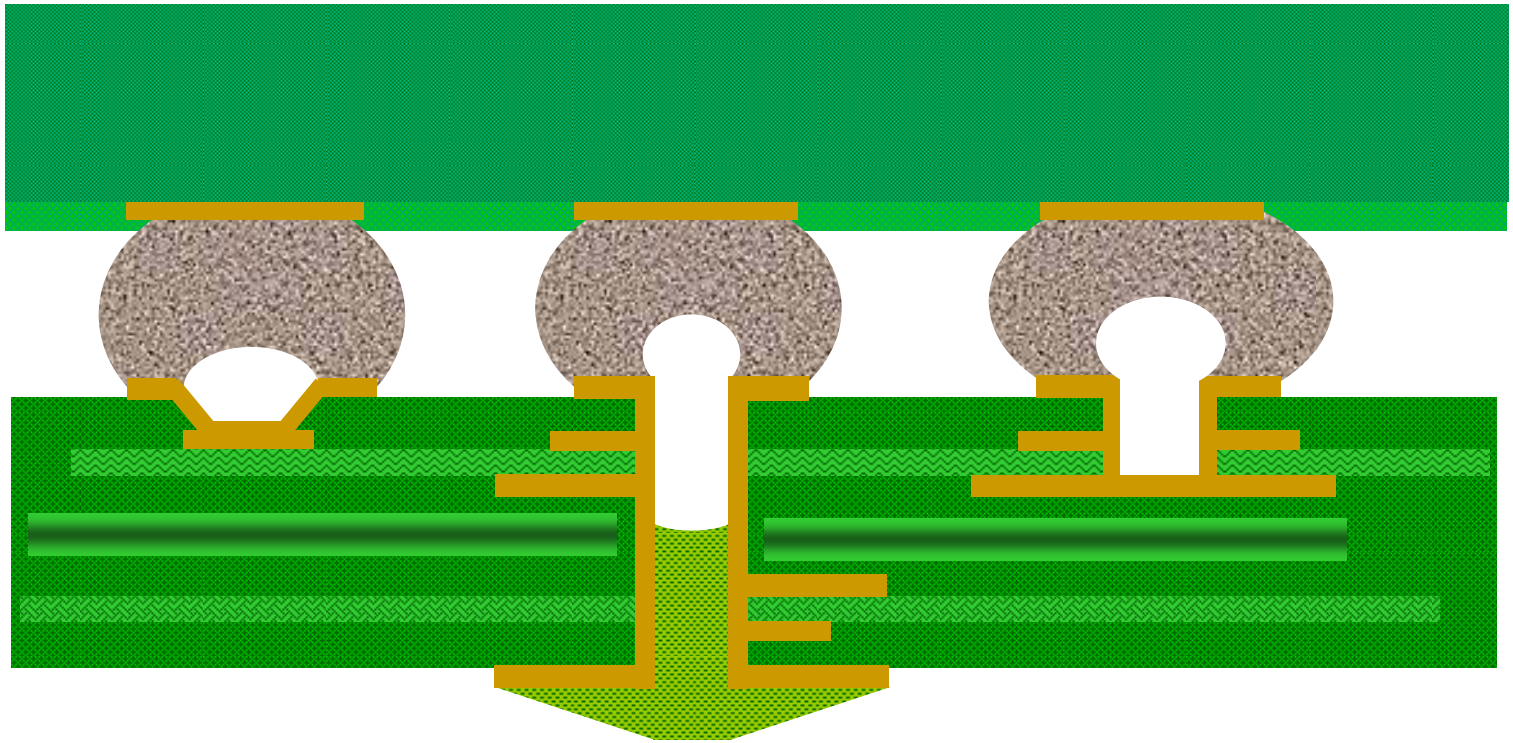
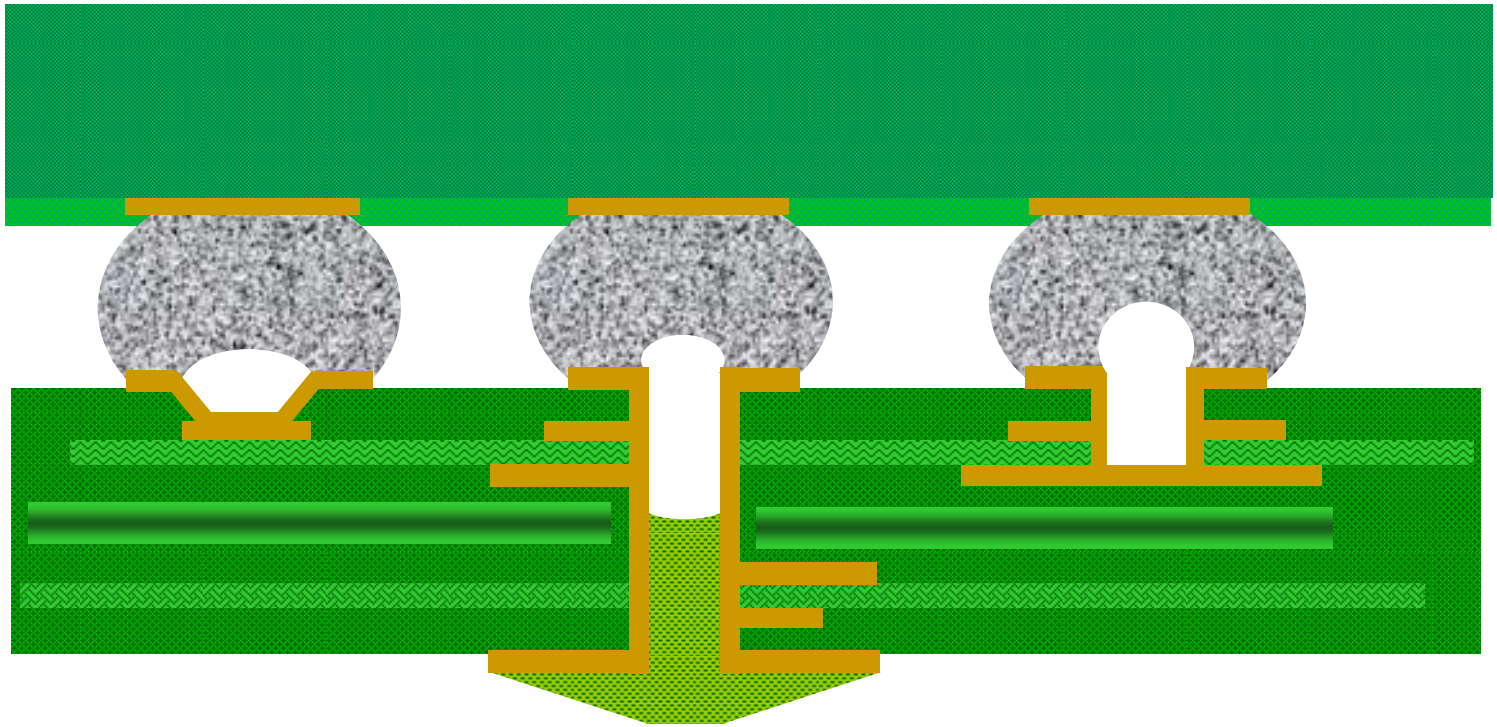
AFTER PRINTING PASTE, AND BGA PLACEMENT



DURING REFLOW SOLDERING



POST REFLOW SOLDERING



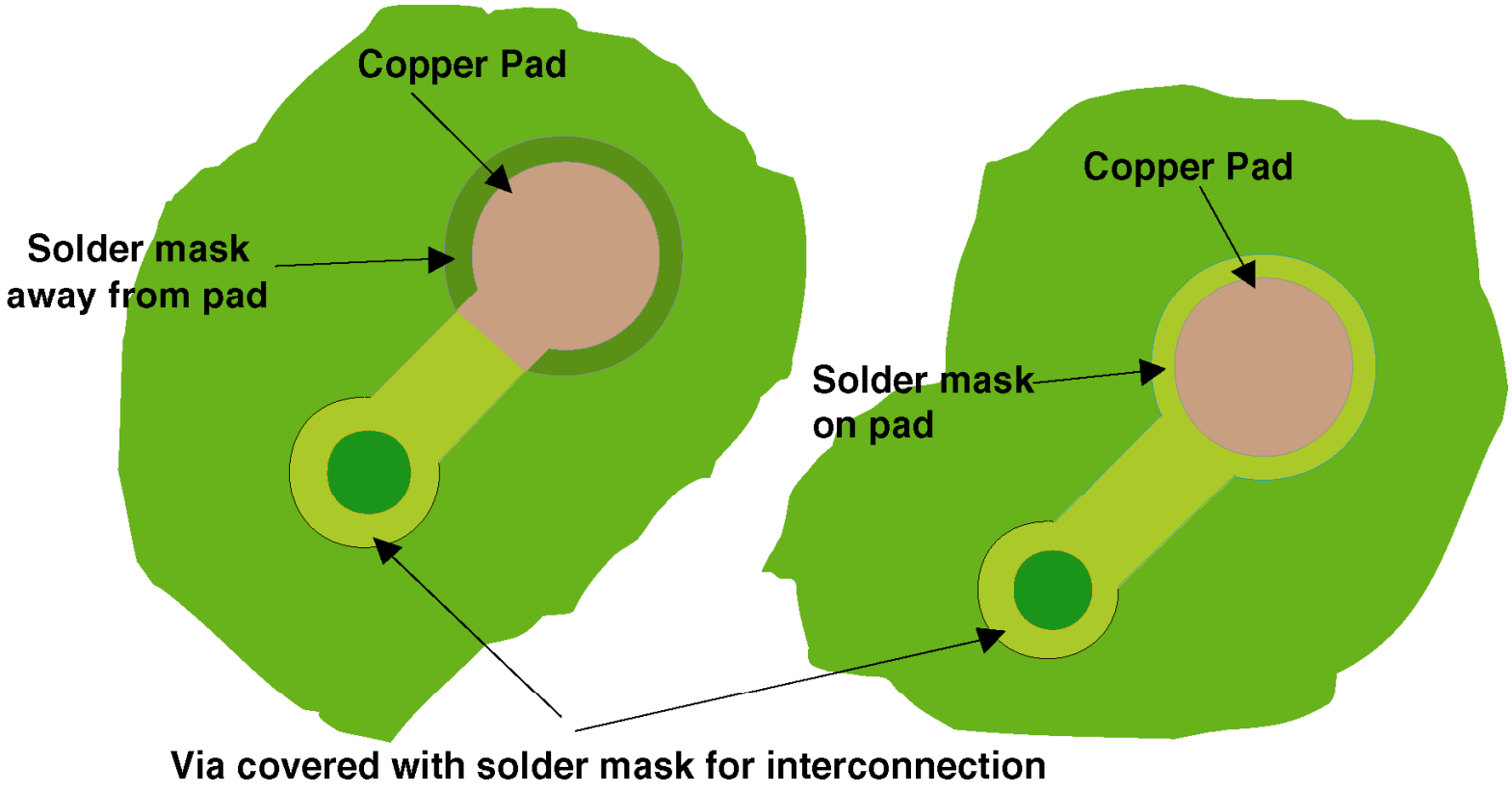
SOLDER MASK VS. METAL DEFINED LAND DESIGN

- Two basic types of solder lands used for BGA packages
  - Non-solder mask defined (NSMD)
  - Solder mask defined (SMD)
- NSMD lands are copper defined - solder mask clearance around land
- SMD lands have solder mask overlapping the copper land

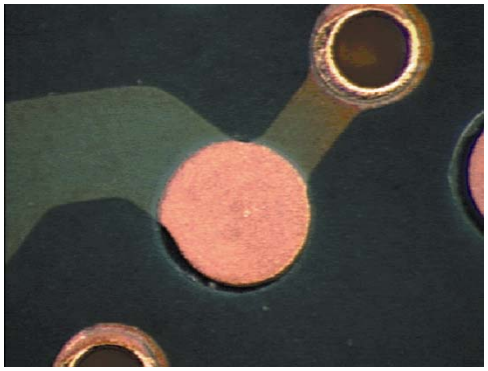
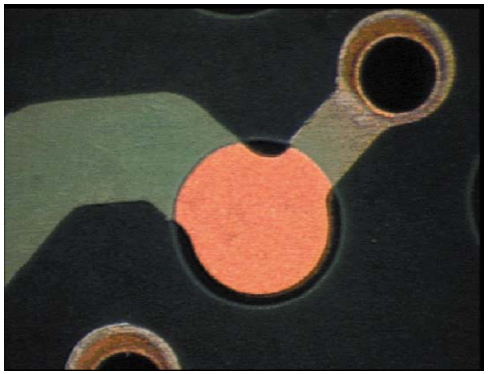
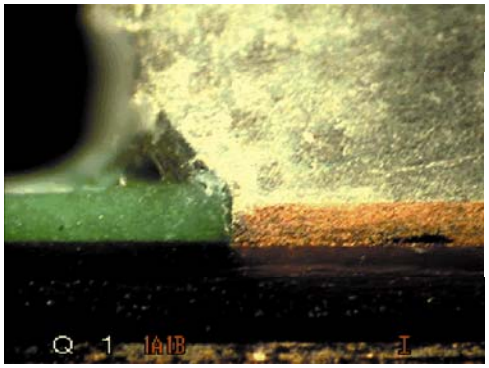
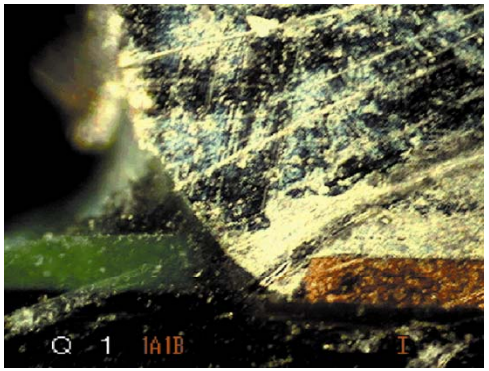
SOLDER LANDS FOR BGA COMPONENTS

Non-Solder Mask Defined Land

Solder Mask Defined Land



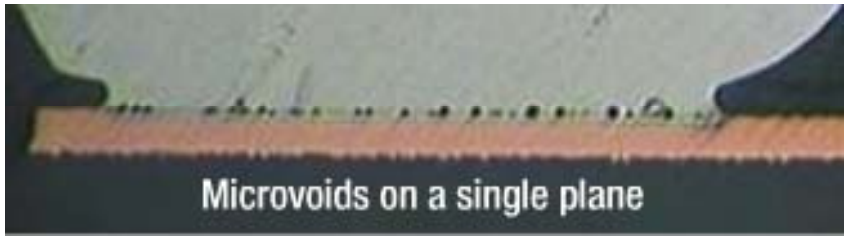
EFFECT OF HAVING SOLDER MASK RELIEF AROUND THE BGA LANDS OF THE BOARD

Solder Mask Relief Around Land	~0 mm	0.15 mm
Top view of land illustrating increase of effective land diameter due to trace connections		
Cross-sectional view of land with solder ball joint illustrating the solder wetting down the edge of the land when there is solder mask relief away from the land edge		

BGA PLANAR MICROVOIDS

Microvoids are:

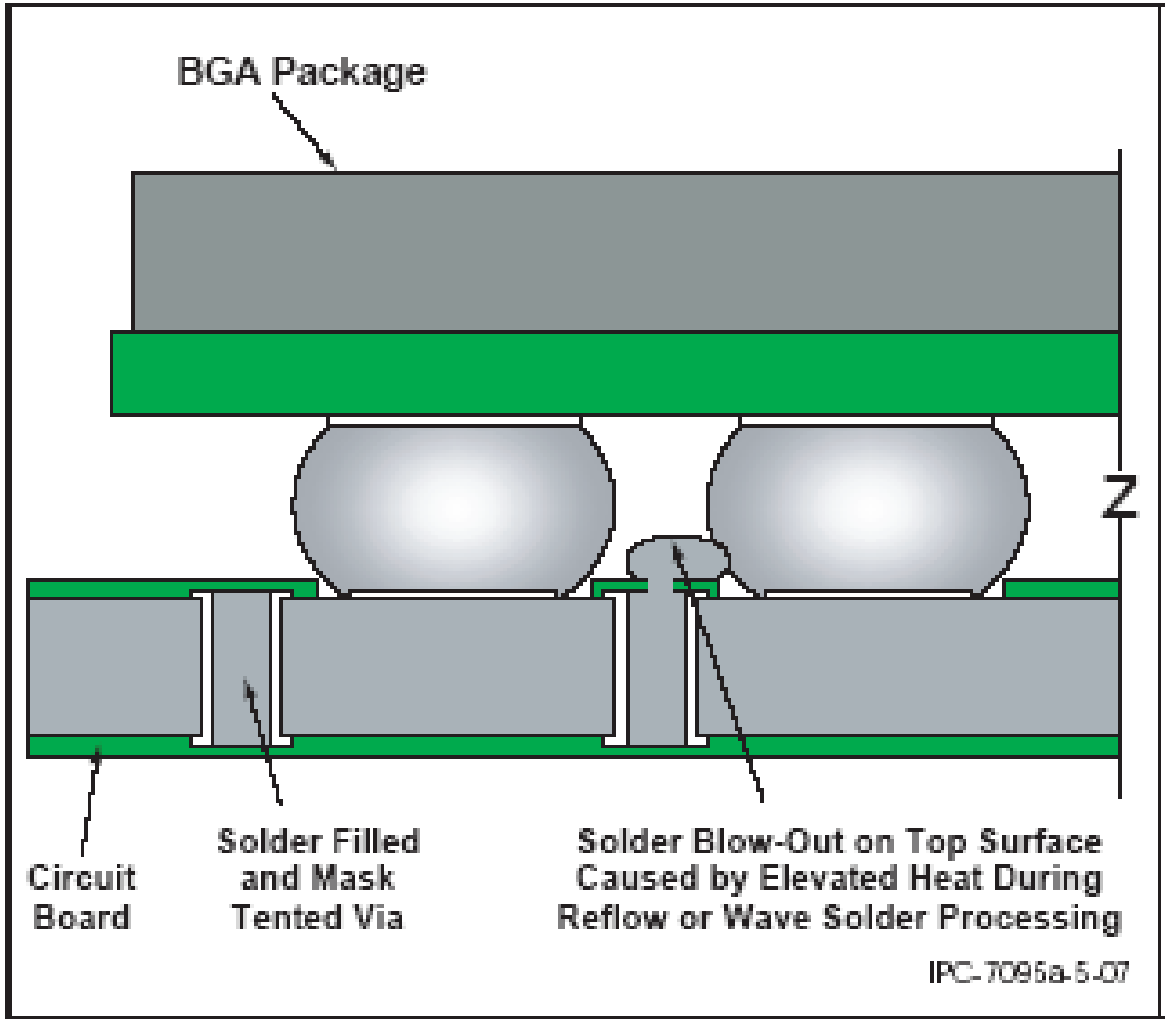
1. A layer of voids in the Ball to Board interface
2. Located immediately above the intermetallic compound
3. Less than 25um (1 mil) in diameter
4. More prevalent in solder mask defined pads



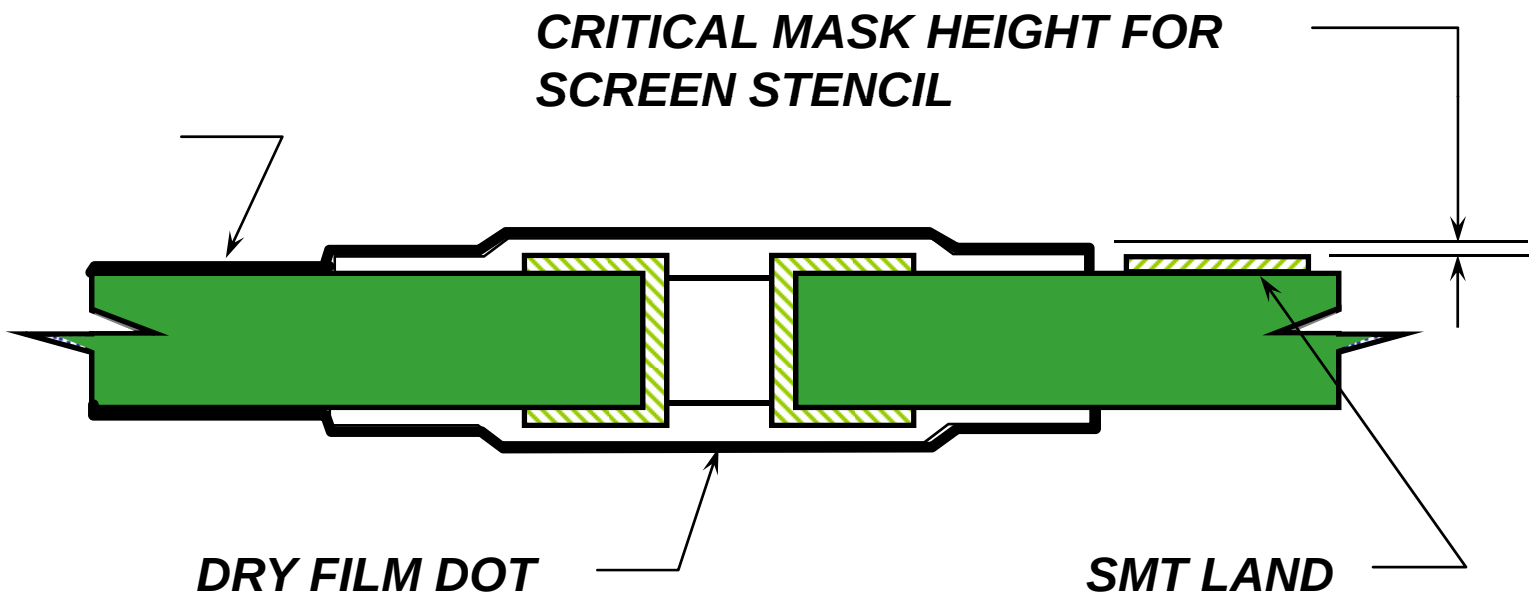
Microvoid Prevention:

1. Use Immersion Silver Plating with a low thickness
2. Avoid using solder mask defined BGA pads
3. For additional information see - http://www.microvoids.org/

VIA'S AND BGA's

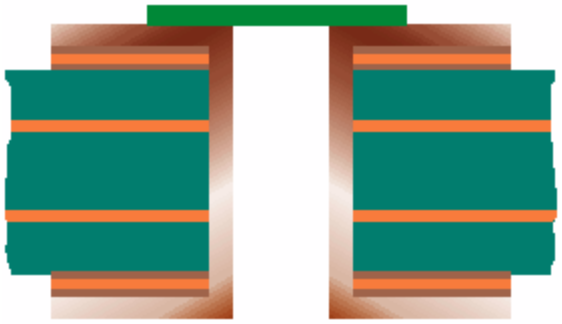


SOLDER MASK TENTING

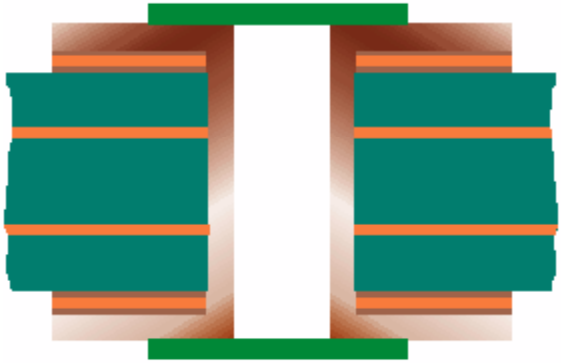


TYPE I - TENTED

Tented Via (Type 1 Via) - A via with a mask material (typically dry film) applied bridging over the via wherein no additional materials are in the hole. It may be applied to one side or both

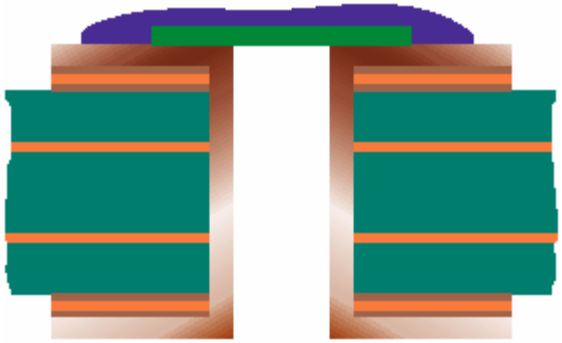


A via covered with dry film solder mask; the via is not filled. When tenting from both sides there may be issues with trapped air that expands during mass soldering.

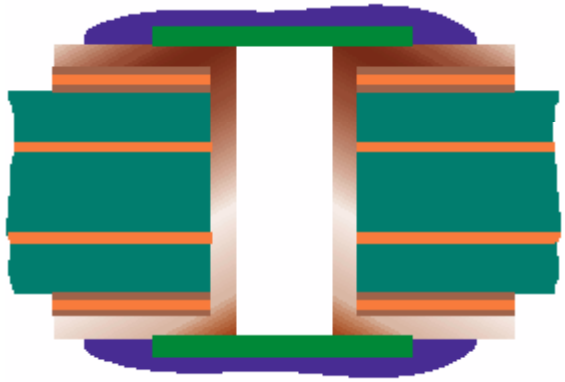


TYPE II – TENTED AND COVERED

Tented and Covered Via (Type II Via) - A Type I via with a secondary covering of mask material applied over the tented via.



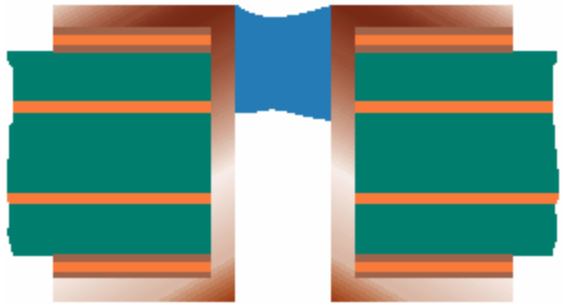
A via covered with dry film and the LPI solder mask; the via is not filled. Just like Type 1 when tenting from both sides there may be issues with trapped air that expands during mass soldering.



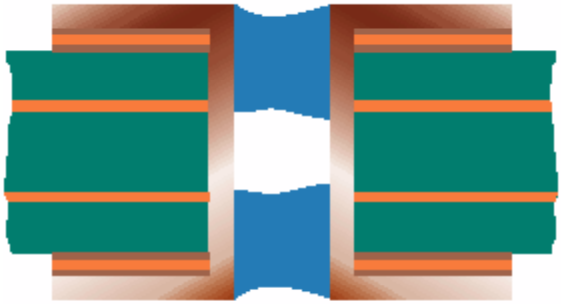
TYPE III - PLUGGED

Plugged Via (Type III Via) - A via with material applied allowing partial penetration into the via.

It may be applied from either one side or both sides

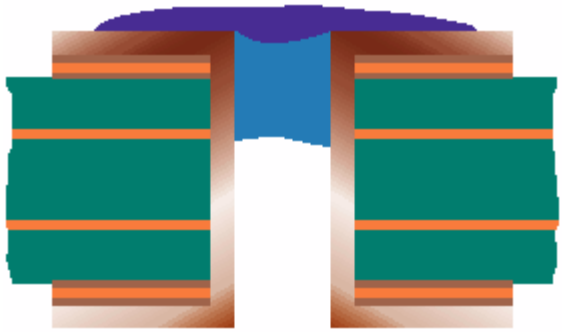


During solder mask application the via is flooded with solder mask. The via is partially filled. Chemical entrapment is a major concern.

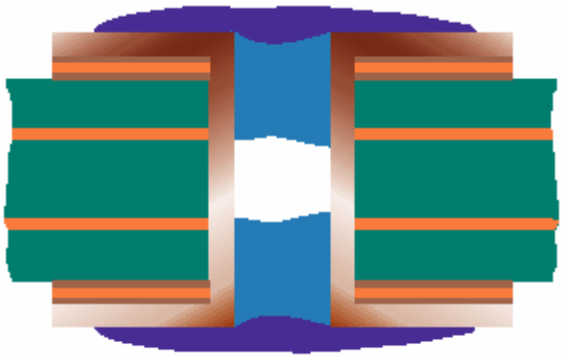


TYPE IV – PLUGGED AND COVERED

Plugged and Covered Via (Type IV Via) - A Type III via with a secondary covering of material applied over the via.

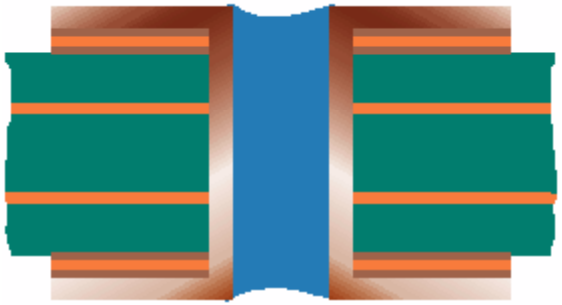


An additional operation which is done independent of solder mask application on one or both sides of the via. The via is partially filled. When capping from both sides there may be issues with trapped air that expands during mass soldering.



TYPE V - FILLED

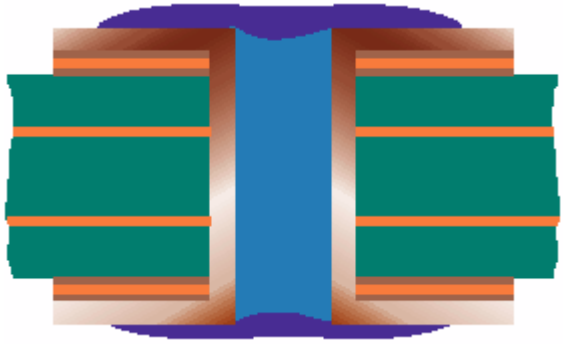
Filled Via (Type V Via) - A via with material applied into the via targeting a full penetration and encapsulation of the hole

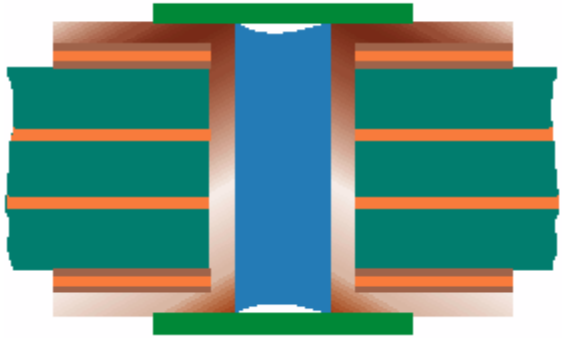


An additional operation which is done independent of solder mask application. The via is filled with a non-conductive material.

TYPE VI – FILLED AND COVERED

Filled and Covered Via (Type VI Via) - A Type V via with a secondary covering of material (liquid or dry film solder mask) applied over the via. It may be applied from either one side or both sides.

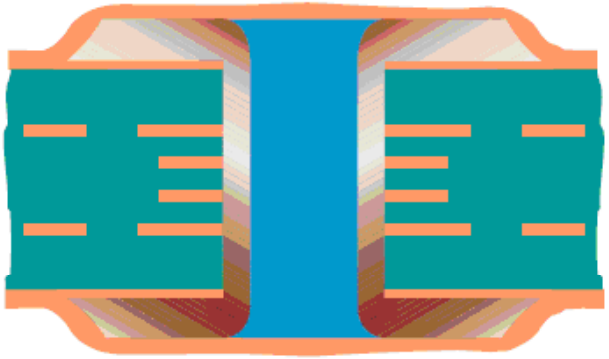




TYPE VII – FILLED AND CAPPED

Filled and Capped Via (Type VII Via) - A Type V via with a secondary metallized coating covering the via. The metallization is on both sides.

This technique is used for Via-in-pad technology for 0.8mm, 0.075mm, 0.65mm and 0.5mm BGA pitch devices.



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Questions?

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