Impact Evaluation of Solder Transfer Peak Temperatures on C4NP Lead Free Solder Bumps

Jayshree Shah
IBM Microelectronics, 2070 Route 52, Hopewell Junction, NY 12533
Hai P. Longworth
IBM Microelectronics, 2070 Route 52, Hopewell Junction, NY 12533
David Hawken
IBM Microelectronics, 1701 North St., Endicott NY 13760

ABSTRACT
C4NP (Controlled Collapsed Chip Connection-New Process) is a novel solder bumping technology developed by IBM and commercialized by Suss MicroTec. C4NP is a solder transfer technology where molten solder is injected into pre-fabricated and reusable glass templates (molds). Mold and wafer are brought into close proximity and solder bumps are transferred onto the entire wafer in a single processing step. The technology is capable of fine pitch bumping while offering the same alloy selection flexibility as solder paste printing. The simplicity of the C4NP process makes it a low cost solution for both, fine-pitch FC in package as well as large pitch / large ball WLCSP (wafer level chip scale package) bumping applications.

Solder Transfer is the key process step in C4NP technology. Wafer with capture pad and mold with filled solder is heated and brought together at a specific temperature. This paper provides a summary of impact evaluation of wafer and mold peak temperatures during solder transfer process. We discuss intermetallic structure of UBM and solder as well as chip pull strength and fracture mode. We will also show the reliability results of C4NP Lead Free bumps transferred at several different transfer temperatures and compare it with the Electroplated High Lead solder bumped high-end logic devices. The data in this paper is provided by IBM's packaging operation at the Hudson Valley Research Park in East Fishkill, NY

INTRODUCTION
The use of Flip chip packages has become more common for integrated circuits. Flip chip technology offers many advantages that drive the current and anticipated large increase in their volumes: superior electrical and thermal performance, high pin count at small form factor and direct power distribution to the chip. Bump reliability is of paramount importance to assure product lifetime, especially as the most advanced high performance integrated circuits often come as flip chips. Reliability challenge multiplied for Lead free solders in fine pitch applications. In Lead free solder, reliability of the bump is driven by several factors: less known reliability of Lead free solder material under harsh operating conditions, UBM and package surface finish metal. At different temperatures, when Lead free solder such as SnAg comes in contact with UBM, the intermetallic structure varies. Subsequent wafer finishing processes, such as reflowing to reshape solder ball, and chip assembly thermal excursion further changes the solder joint metal crystal structure. This paper reports interaction and impact on reliability of UBM intermetallic and Solder bump material when solder is transferred [1] at multiple wafer and mold peak temperatures using C4NP process.

SOLDER TRANSFER IN C4NP
The solder used for wafer bumping do not wet the glass mold, so upon heating, the solder alloys form spherical balls in the cavities. The filled mold is aligned with wafer as shown in Figure 2. After alignment, for this evaluation, wafer and mold are heated to six different temperatures: 235, 243, 250, 260, 280 and 300 C to prepare six wafer samples. Heated wafer and mold are brought into close proximity/contact, allowing molten solder balls to wet the appropriate UBM pads where they preferentially remain when the wafer and mold are separated.

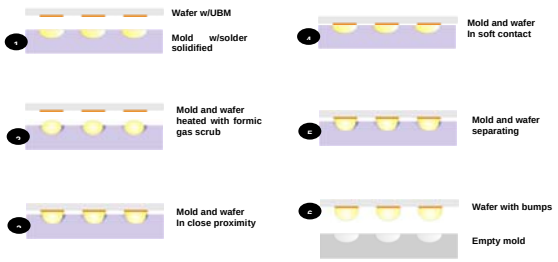


Figure 1 - Solder Transfer Process Sequence

The solder transfer process took place in a reducing gas environment which assured clean, oxide free, solder and UBM surfaces. This process does not need liquid flux and subsequent cleaning. In this experiment, wafer and mold were diced before solder transfer for a single chip solder transfer. Finished chips with SnAg C4 got assembled to organic laminate package with SAC surface finish.

Test Vehicle Description

We use a specially designed test chip to evaluate C4 reliability. There are 3 main test features for C4 evaluation. To monitor C4 fatigue behavior, we use a ring connection of signal C4s to enable the testing of C4 failures at different DNP (distance to neutral point). Migration ring consists of 3 parallel C4-stitch pattern is used to evaluate C4 migration/corrosion by biasing the center ring against the two neighbor rings. There are 4 electromigration (EM) test sites The EM design allows 4-point C4 resistance measurement of the stressed C4 along with a thermal sense and short monitor.

- Chip size: 14.67 x 14.76 mm
- Pitch: 200um
- Wafer size: 300mm
- # of Chips in wafers: 271
- # of C4's in chip: 4,699
- Total C4s in wafer: 1.27 million
- Chip technology: 90 nm
- Package: FC-PBGA
- Solders: Sn1.8% Ag
- UBM Sputtered TiW / Cu, Plated Ni / Cu

Figure 2 - Assembled module cross section

LEAD FREE C4NP RELIABILITY

Extensive reliability evaluation of Lead Free solders bumps manufactured by C4NP process have been performed (ref 1 & 2). For this study of solder transfer peak temperatures, we selected four evaluations to best characterize the effect of temperatures on solder bump integrity and reliability: wettability (tensile strength & fracture mode), construction analysis, electromigration and high temperature storage.

Figure 3 depicts the chip test vehicle used to collect 200um C4 pitch manufacturing and reliability data.

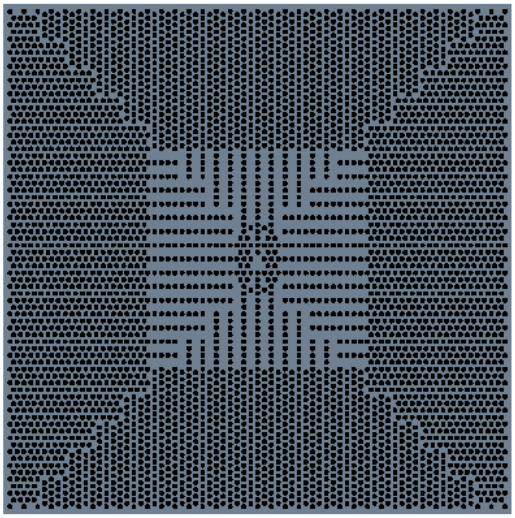


Figure 3 - 200 um pitch test vehicle C4 pattern

1.) Tensile Strength and Fracture mode

To evaluate the solder joint strength of SnAg C4NP transferred at different temperatures, a series of bump tensile tests have been performed. A stud is glued on back side of the assembled chip on FCPBGA package. Chip is pulled away from the package at constant speed at room temperature until joint is separated. Measured pull strength is 2X to 3X higher than the Leaded 97Pb3Sn solder and has no correlation with transfer temperature.

UBM rupture at intermetallic level changes with transfer temperature. Higher transfer temperature gave more rupture in poly pull out or Aluminum pad lifting, changing from 5% at 235 C to 59% at 300 C. Figure 4. Grain structure for UBM intermetallic rupture changed from equal axial – hexagonal to fine tetragonal at higher temperature.

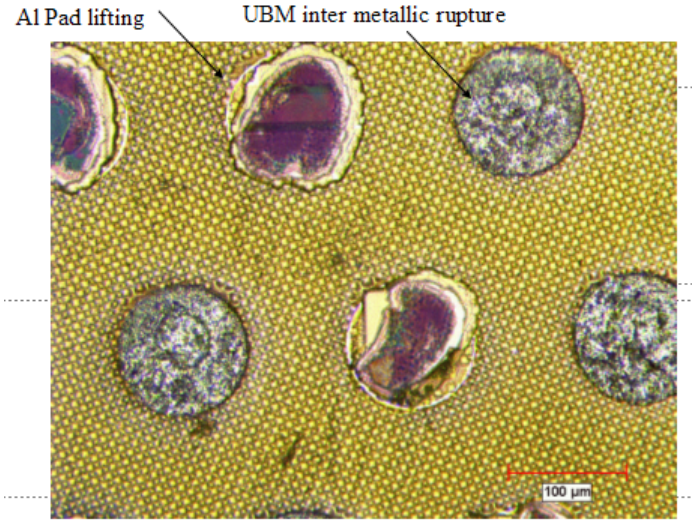


Figure 4 - Fracture mode

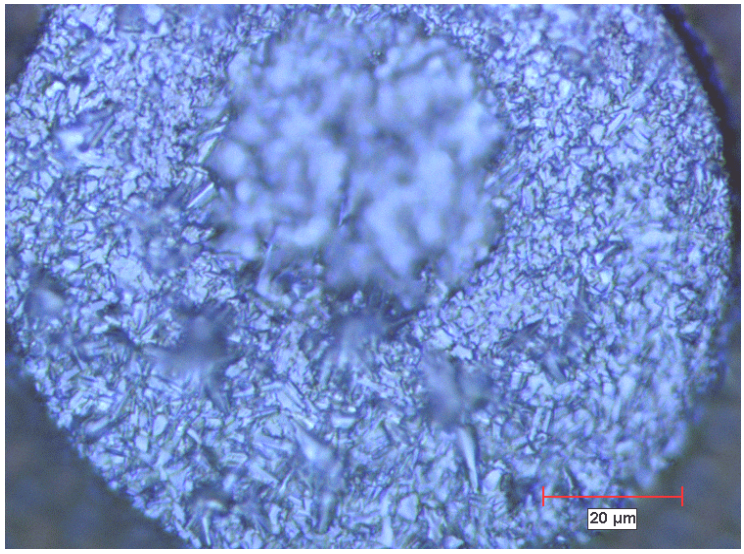


Figure 5 - Grains structure 1000X with blue filter

2.) Construction Analysis

To examine SnAg solder reaction with Plated Ni /Cu UBM, SEM (Scanned Electron Microscopy) pictures were taken after cross sectioning C4 ball for each transfer temperature sample chip. More than 2 um of Ni barrier remain unreacted post transfer regardless of transfer temperature. However, the Cu under the Ni started reacting more as the transfer temperature increased. This thermal undercut created a stress concentration point, causing rupture in UBM and Aluminum pad.

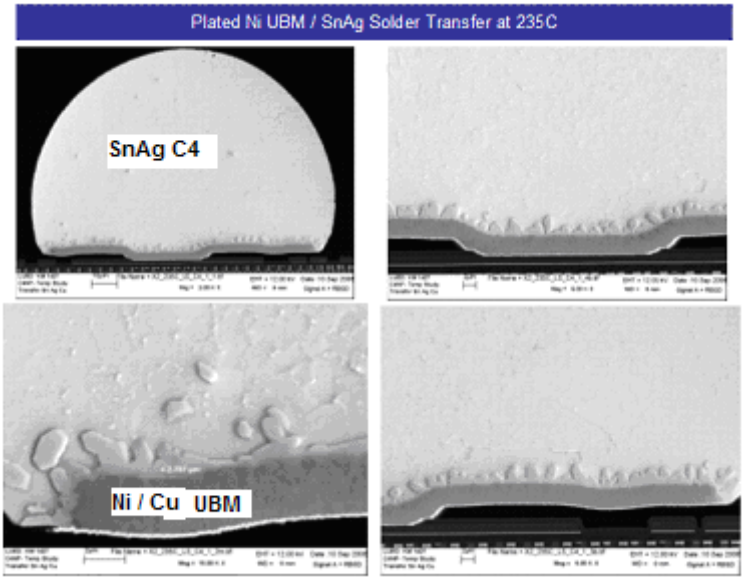


Figure 6 - SEM at Solder Transfer temp 235C

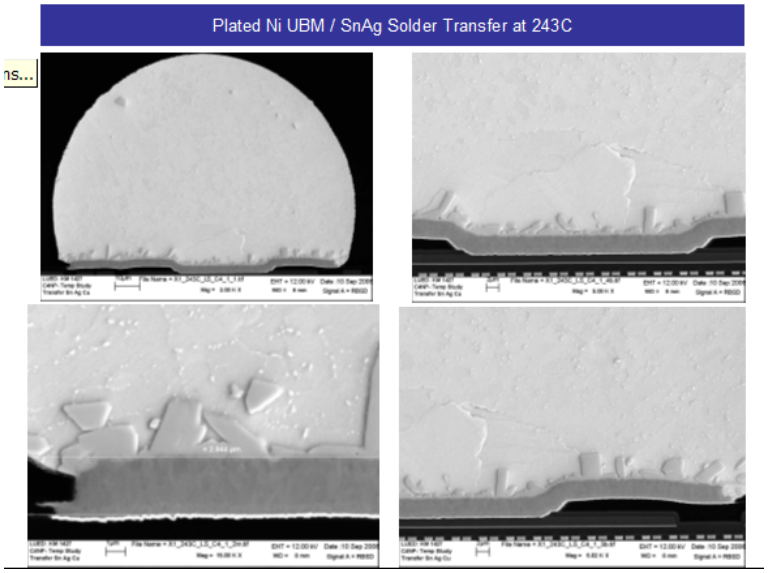


Figure 7 - SEM at Solder Transfer temp 243C

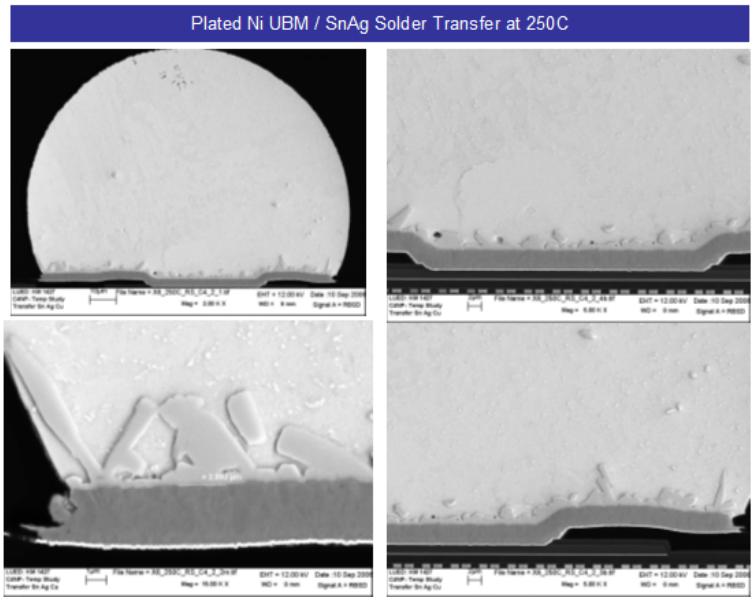


Figure 8 - SEM at Solder Transfer temp 250C

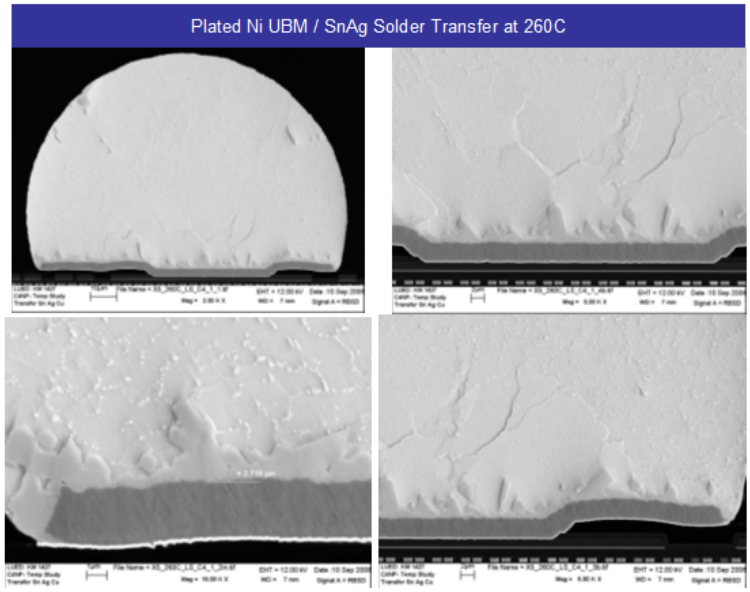


Figure 9 - SEM at Solder Transfer temp 260C

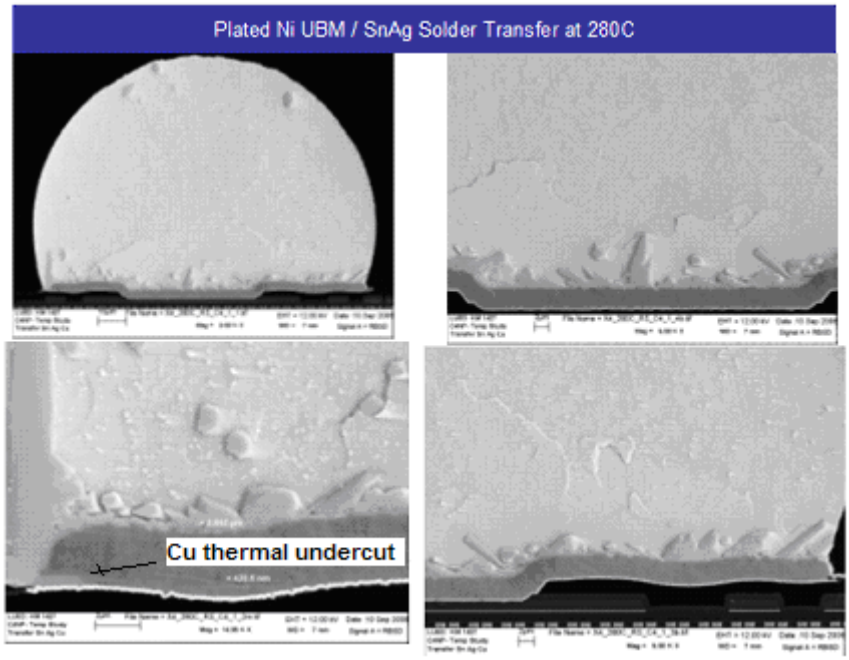


Figure 10 - SEM at Solder Transfer temp 280C

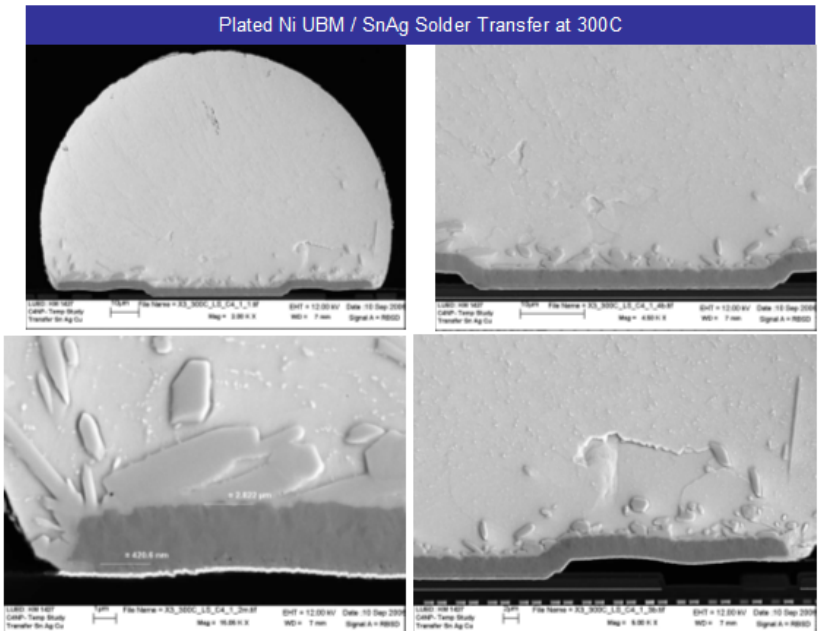


Figure 11 - SEM at Solder Transfer temp 300C

3.) High Temperature Storage

High temperature storage (HTS) or solid-state aging has been reported to induce void formation in Lead free C4s. The most common voiding mechanism is Kirkendall voids which are formed at the interface of two dissimilar materials, such as intermetallic layers, because of different diffusion rates. Accelerated aging at high constant temperature can aggravate Kirkendall void growth leading to reduction in strength of solder joints (ref 3). Non-equilibrium state of void formation different from the classical Kirkendall void formation has also been reported in lead-free solder joints during solid-state aging (ref 4).

It is expected that the reaction of Sn and Cu in the BLM during solder transfer process can be strongly influenced by the transfer temperature hence HTS test was used to evaluate any potential effect of transfer temperature on void formation.

For this study, we selected a more aggressive aging temperature of 170C over the standard 150C. 4-point measurements of C4 resistances were performed at Tzero (as joined state), post Jedec Level 3 preconditioning and at every 250hrs stress intervals. No changes in C4 resistances were observed post 1000hrs of stressing.

4.) Electromigration

C4 electromigration was performed to evaluate whether the current carrying capability of the C4 was affected by the higher solder transfer temperatures. Twelve test vehicle modules were built using chips that experienced the maximum solder transfer temperature. All of the modules were exposed to JEDEC level 3 preconditioning using 2X module reflow at 245C and 1X module to card join reflow at 245C. The modules/cards were then put into C4 electromigration testing at 140C and 0.7Amps. Six of the modules had electron flow from the chip to the substrate and six had electron flow from the substrate to the chip. All 12 modules successfully completed 2000 hours of electromigration stress with no fails. After the 2000 hour stress was completed, modules were cross sectioned to evaluate the UBM and Cu, Ni, and Sn intermetallics. No difference was seen between modules assembled with chips that experienced nominal solder transfer temperatures that had previously been stressed in C4 electromigration and these chips that experienced maximum solder transfer temperature.

CONCLUSION

Solder transfer temperatures were found to have an impact on UBM rupture at intermetallic level. Grain structure for UBM intermetallic rupture changed from equal axial – hexagonal to fine tetragonal at higher temperature. The high solder pull strengths showed robust bump integrity for the entire range of studied temperatures. The apparent difference in intermetallic structure as function of transfer temperature was not found to have any impact on solder reliability as demonstrated in high-temperature storage and electromigration tests.

Acknowledgments

The authors would like to thank several colleagues at IBM for their contributions – Luc Ouellet, Clement Fortin and Bill Bernier for Bond, Assembly & Test, Eric Kastberg and Joe Ross for reliability stressing, Eric Perfecto for technical contribution, and Chuck Goldsmith for F/A coordination and analysis.

REFERENCES

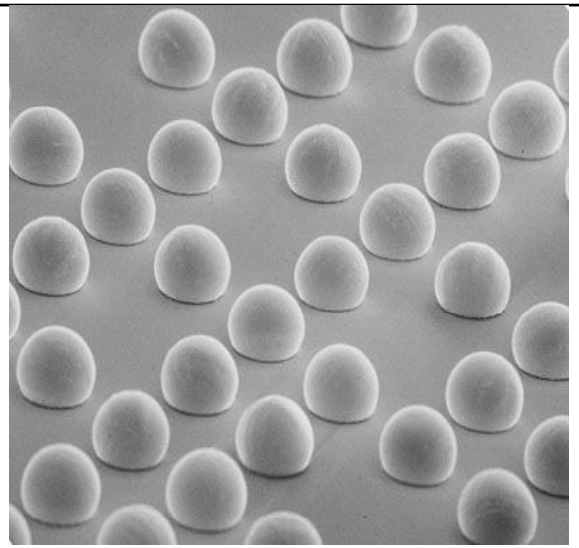
1. E. Laine, K. Ruhmer, E. Perfecto, H. Longworth, D. Hawken "C4NP as a high-volume manufacturing method for fine-pitch and lead-free Flip Chip Solder Bumping" *Proceedings of ECST, IEEE, Dresden, Germany,* September, 2006.
2. J. Shah, D. Hawken, H. Longworth *et al*. "C4NP Lead free versus Electroplated High Lead Bumps" *Proc. of IPC Works 2006*, Dallas, Sept 14, 2006
3. Tz-Cheng Chiu, et.al., "Effect of Thermal Aging on Board Level Drop Reliability of Pb-Free BGA Packages," Proc. 2004 ECTC,pp.1256-1262
4. J.W. Wang, J. K. Lin, D.R. Frear, T. Y. Lee, and K. N. Tu: Ripening-assisted void formation in the matrix of lead-free solder joints during solid-state aging", J. Mater. Res. 22, 826 (2007)

IPC Get Interconnected.™ MIDWEST CONFERENCE & EXHIBITION

Impact Evaluation of Solder Transfer Peak Temperatures on C4NP Pb Free Solder Bumps

Jayshree Shah, Hai Longworth, Dave Hawken

IBM Systems and Technology Group



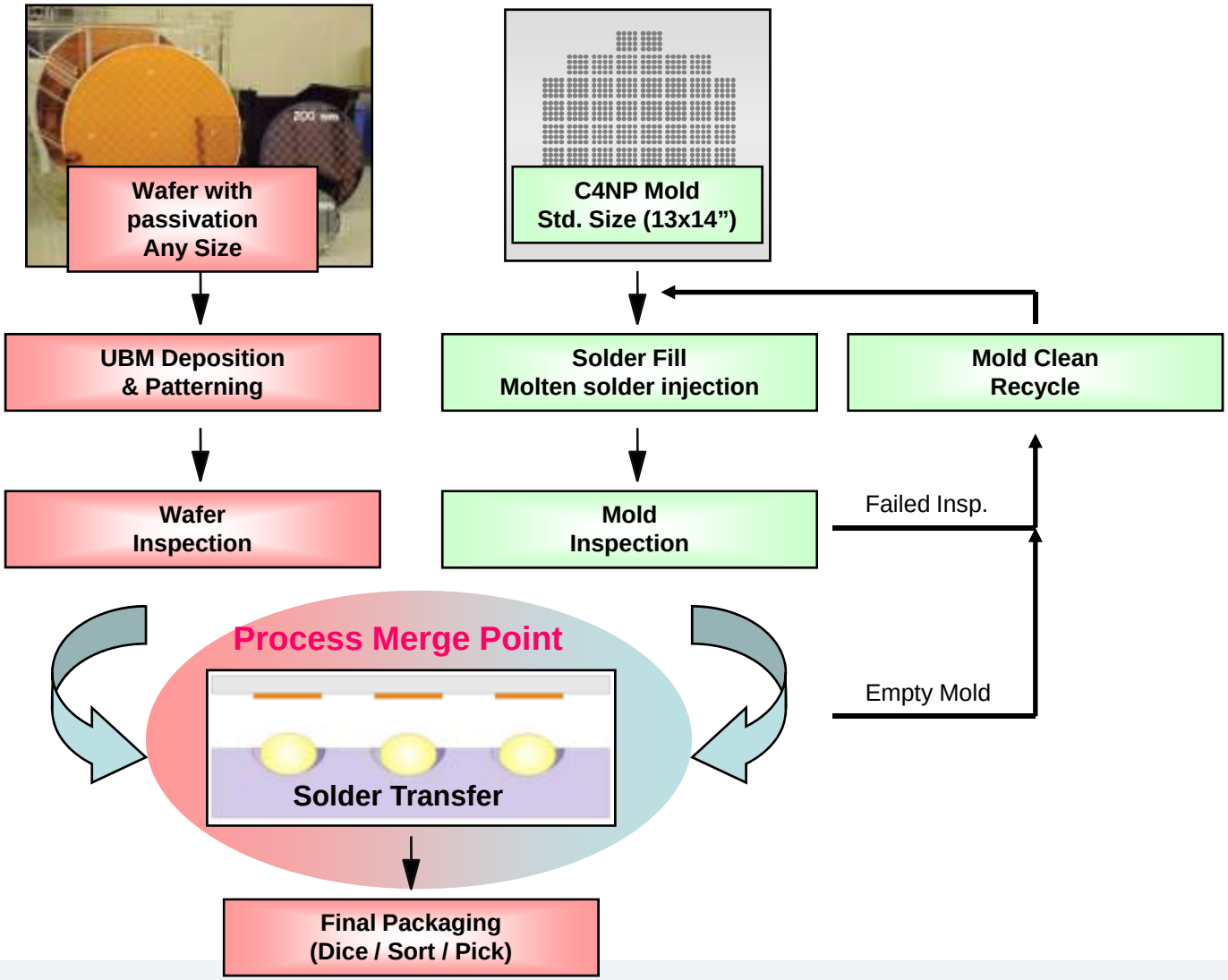
IPC ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES®

Outline

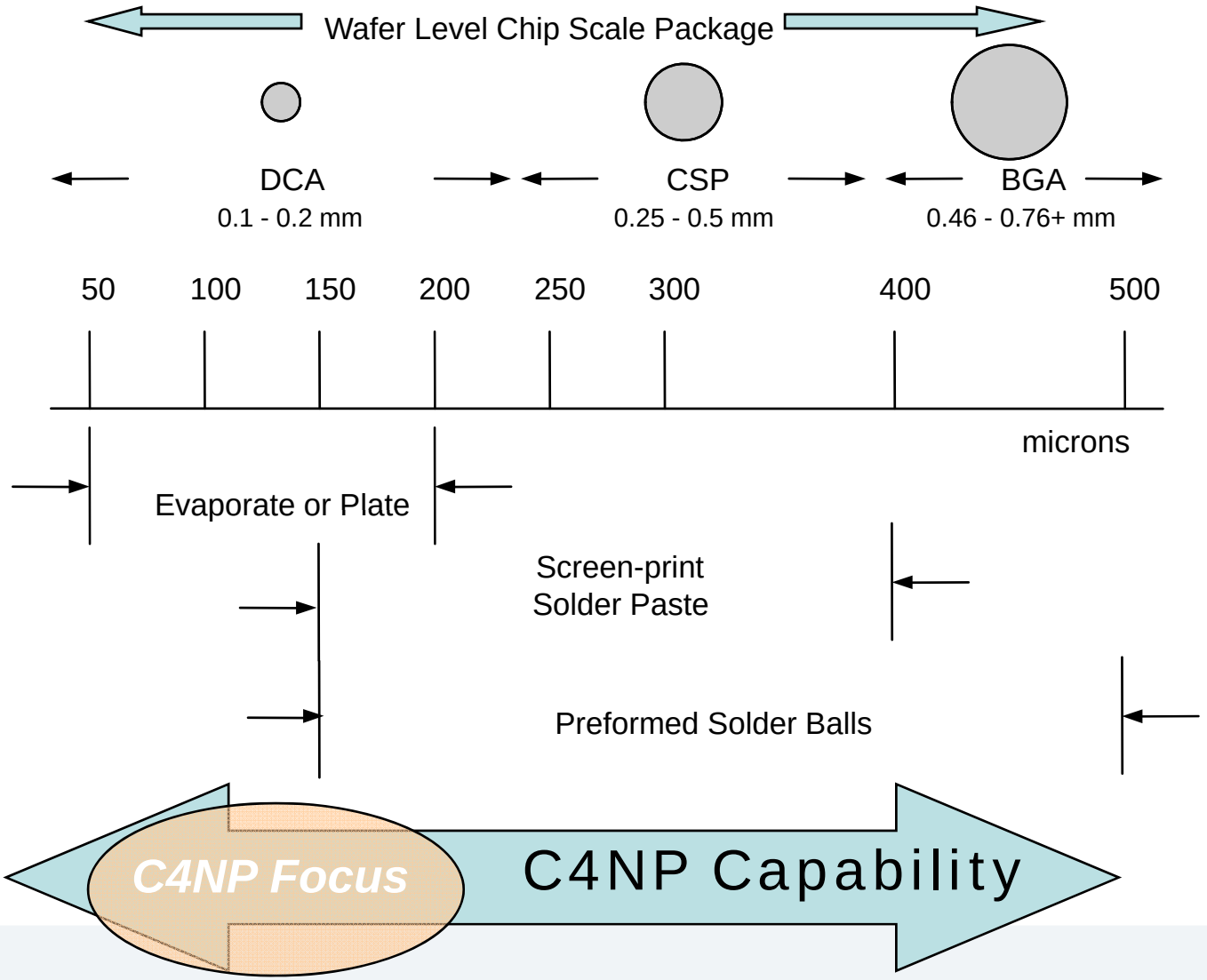
- C4NP Technology Overview
- 200um Reliability Test Vehicle
- Lead Free C4NP Reliability
- Conclusion

❖ C4NP = Controlled Collapsed Chip Connection- New Process

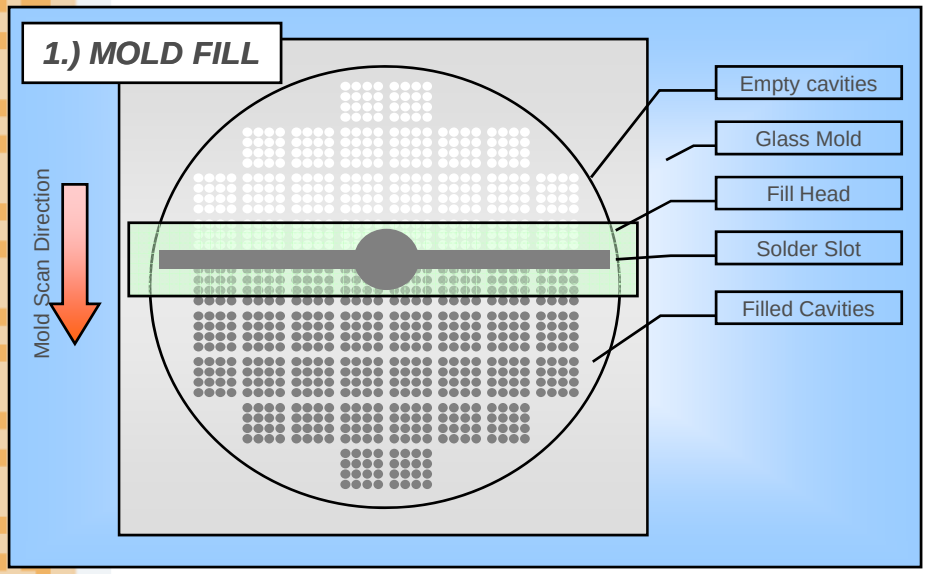
C4NP Technology Overview; Bumping Process Flow

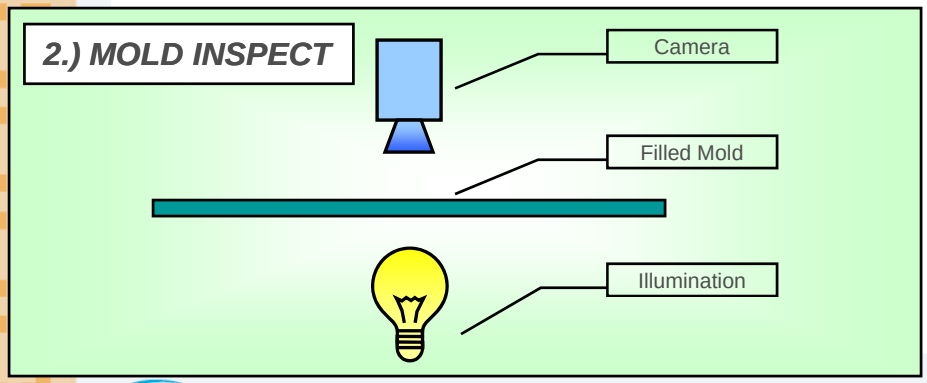


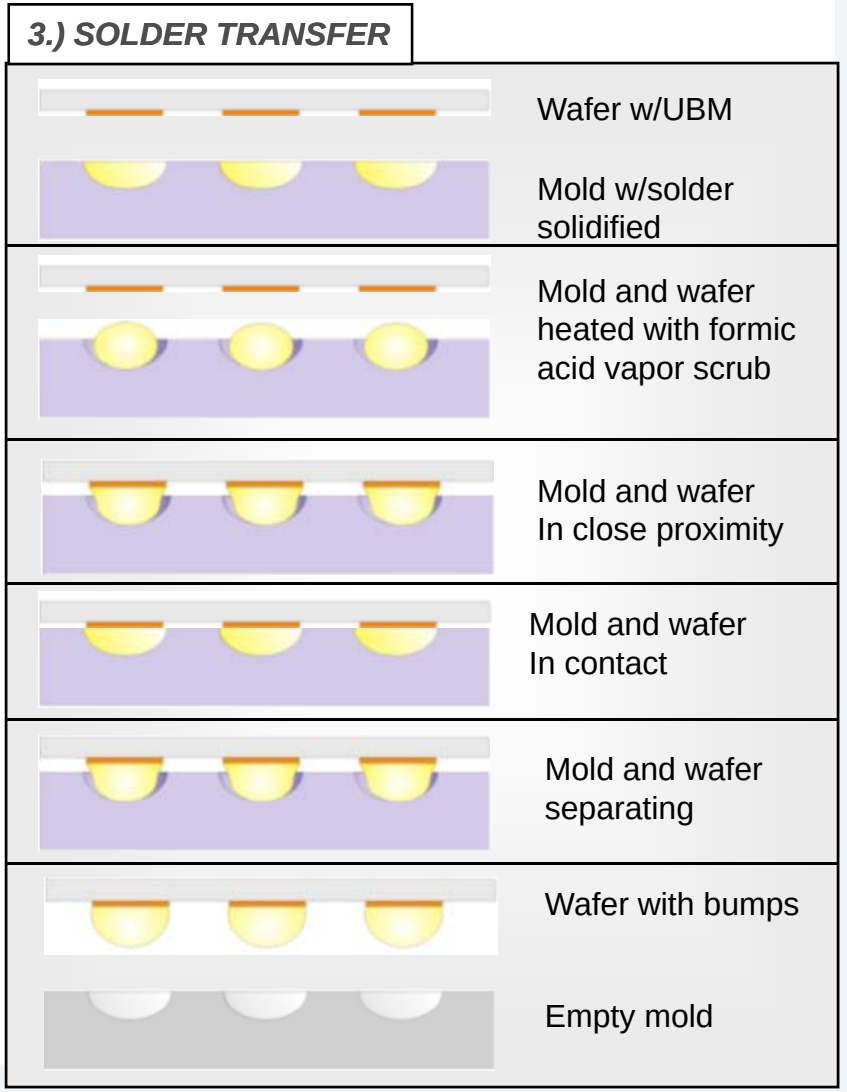
C4NP Technology Overview; Application Space



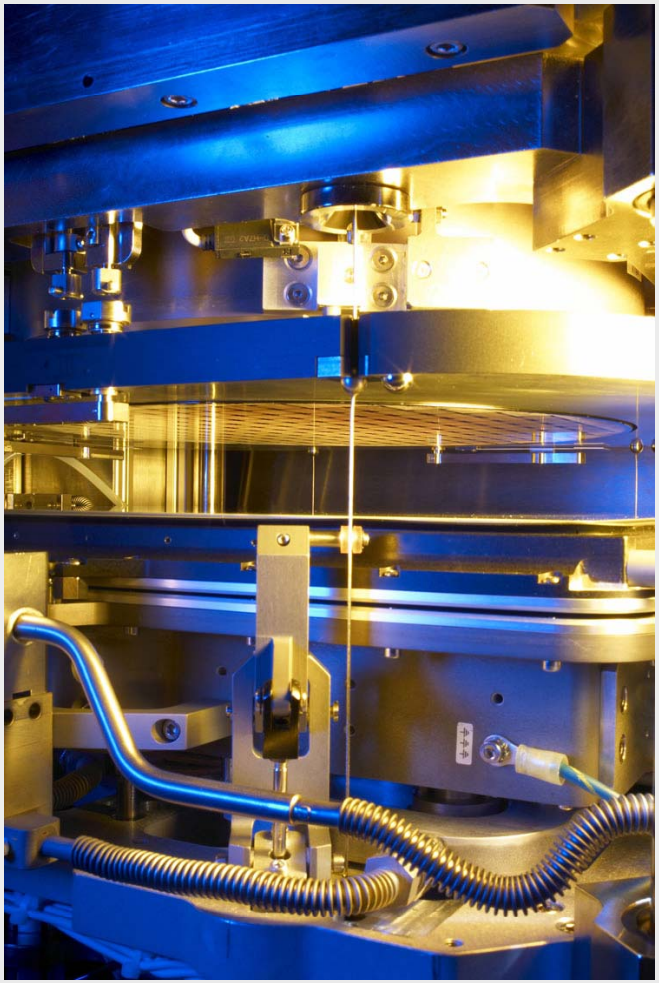
C4NP Technology Overview; Process







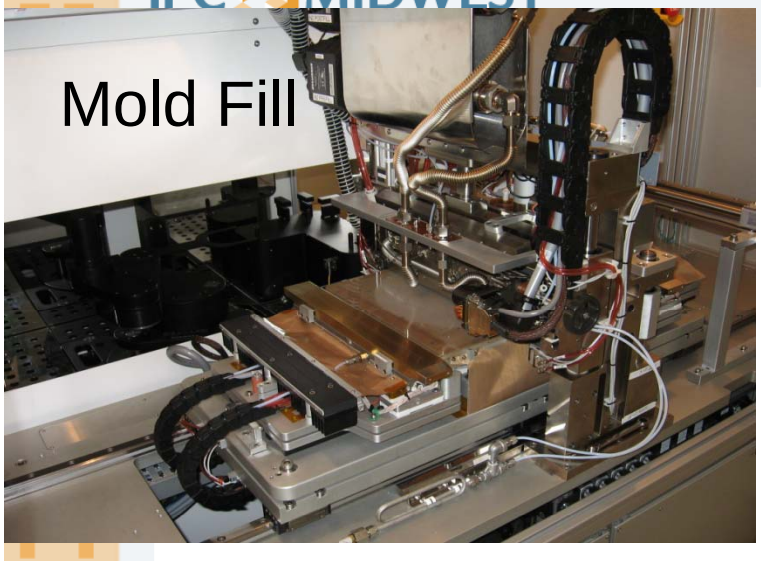
SUSS HVM Tooling; Solder Transfer

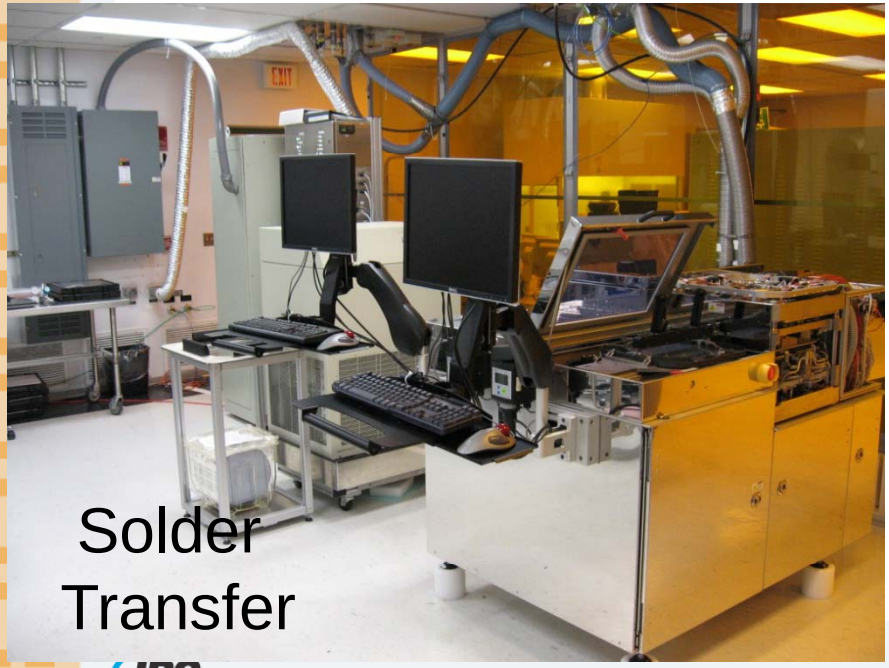


- 50 WPD solder transfer
- Qualified & in production

IPC MIDWEST Get Interconnected.™

HVM Tool Installation at IBM



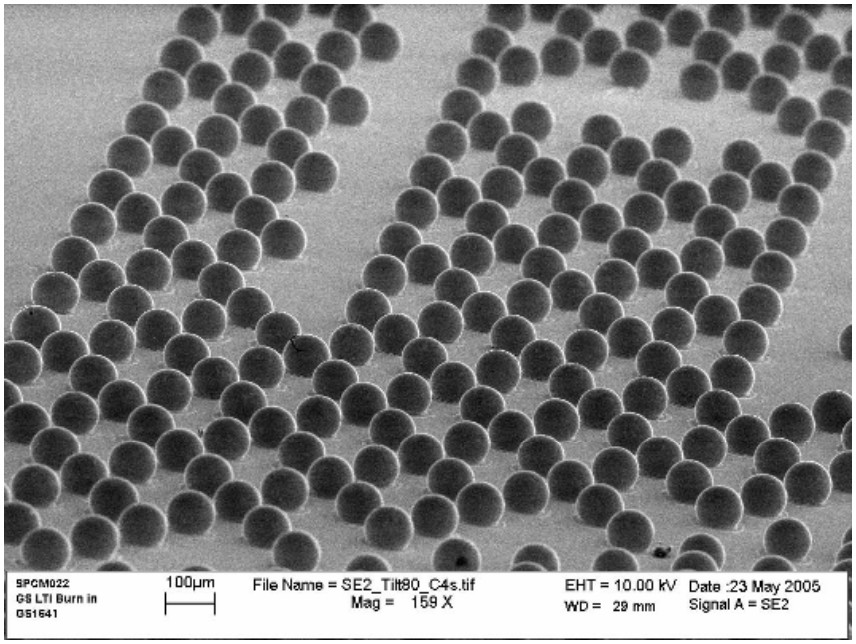


IPC
ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES®

C4NP Technology Overview; Process Dev- Solder Transfer

Solder Transfer Variables

- Alignment (x-y)
- Planarization
- Pressure
- Temperature
- Formic acid clean



Solder Transfer Response

- Quality (missing / bridged C4s)
- C4 bump Reliability
- C4 Metrology

Outline

- C4NP Technology Overview
- 200um Reliability Test Vehicle
- Lead Free C4NP Reliability
- Conclusion

200 μm Reliability Test Vehicle

T.V. Description

- Chip size: 14.67 x 14.76
- # of Chips in wafers: 271(300 mm wafer)
- # of C4's in chip: 4,699 (200 μm pitch)
- Total C4s on wafer: 1.27 million
- Chip technology: 90 nm
- Package: FC-PBGA
- Solders: Sn1.8%Ag
- Migration/corrosion Ring: 3 parallel stitch pattern, center ring biased against two neighbor
- Electromigration: 4 sites, 4 point C4 resistance measurement with a thermal senser and short monitor

200 μm Reliability Test Vehicle

Transfer Technology

- UBM (BLM): Sputtered TiW / Cu, Plated Ni / Cu
- Transfer: Fluxless joining of solder from mold to wafer (C4NP)

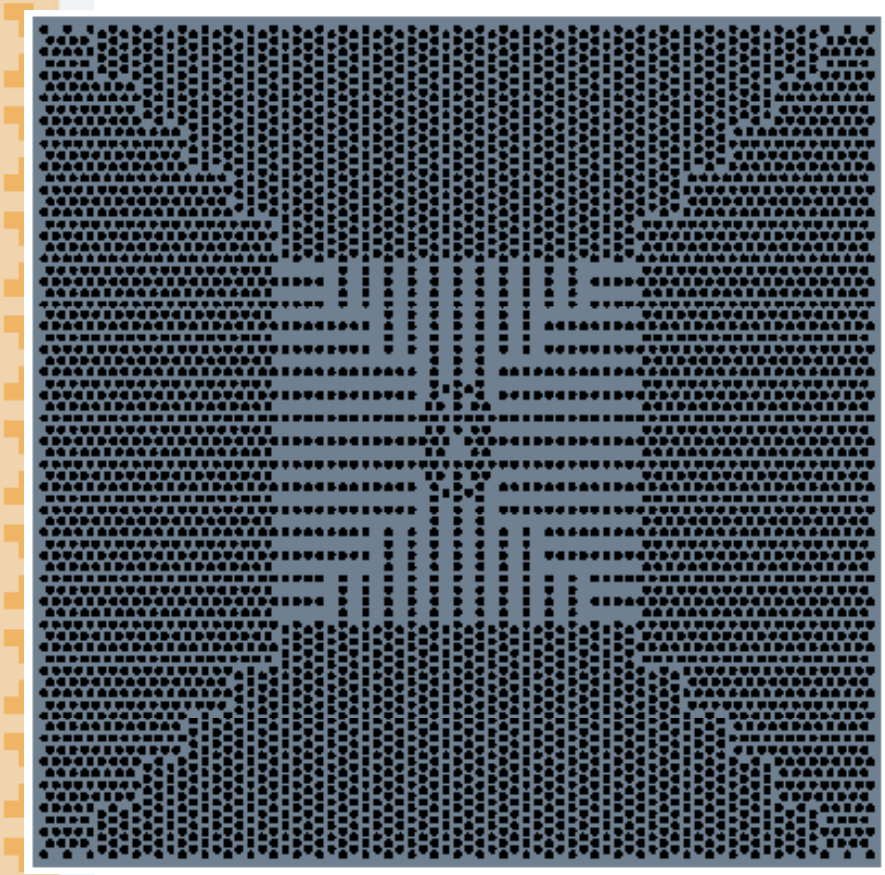
  Glass mold with empty C4 cavities

  Mold Fill with SnAg solder alloy

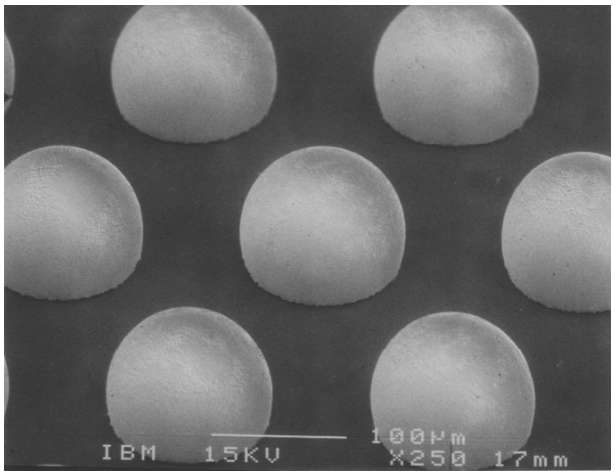
  Solder Transfer from mold to wafer at 235, 243, 250, 260 and 300C peak temperature

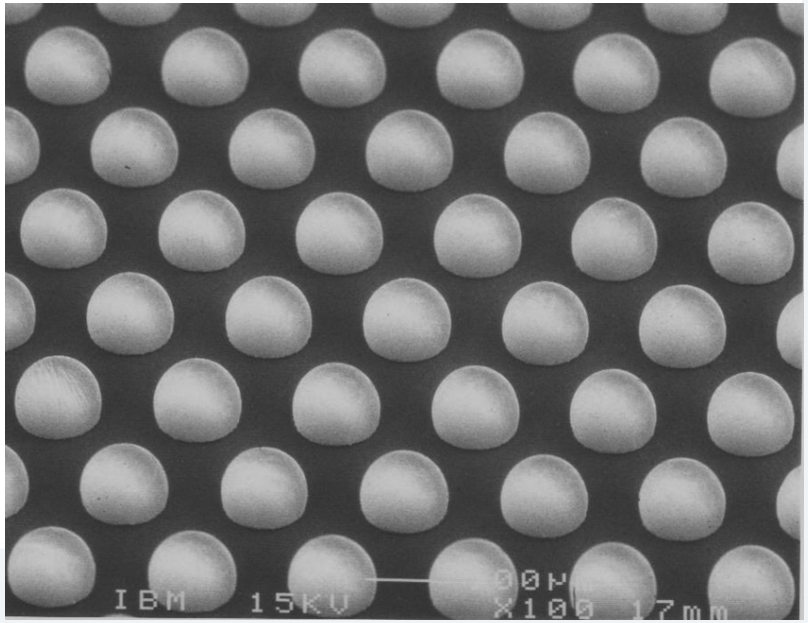
200 um Reliability Test Vehicle

Chip; 14.7x14.7 mm



C4s at 200 μm pitch



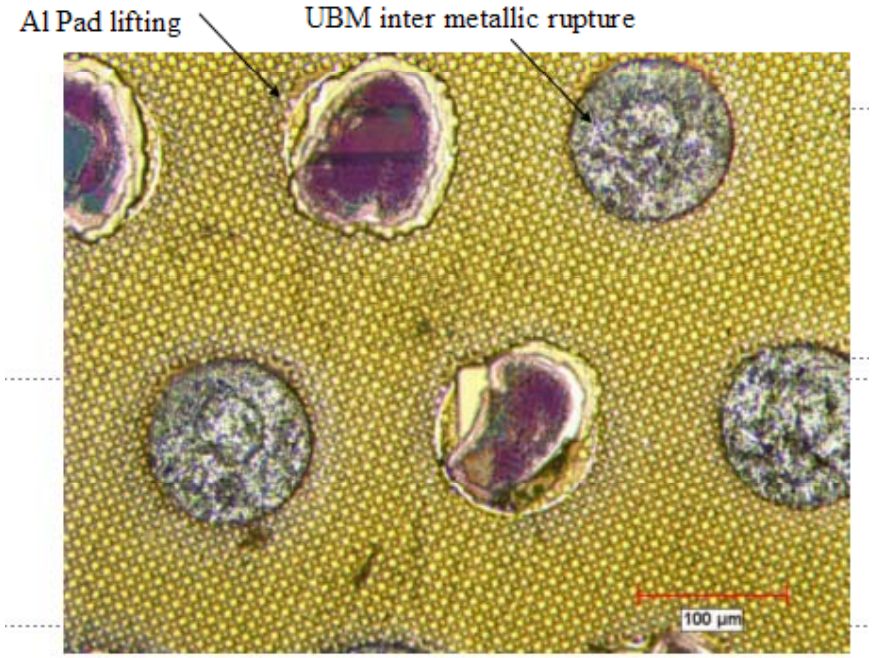


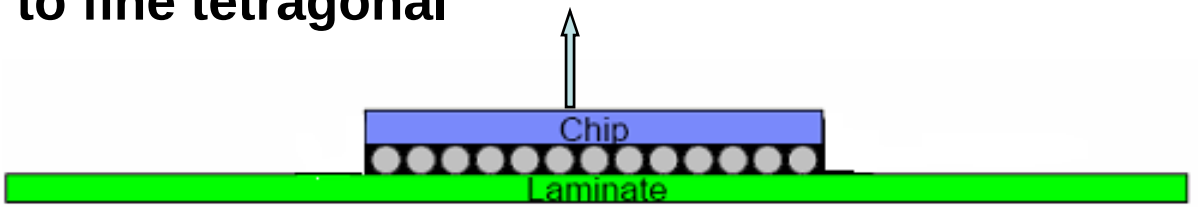
Outline

- C4NP Technology Overview
- 200um Reliability Test Vehicle
- Lead Free C4NP Reliability
- Conclusion

C4NP Lead Free Solder Reliability; Tensile Strength and Fracture Mode

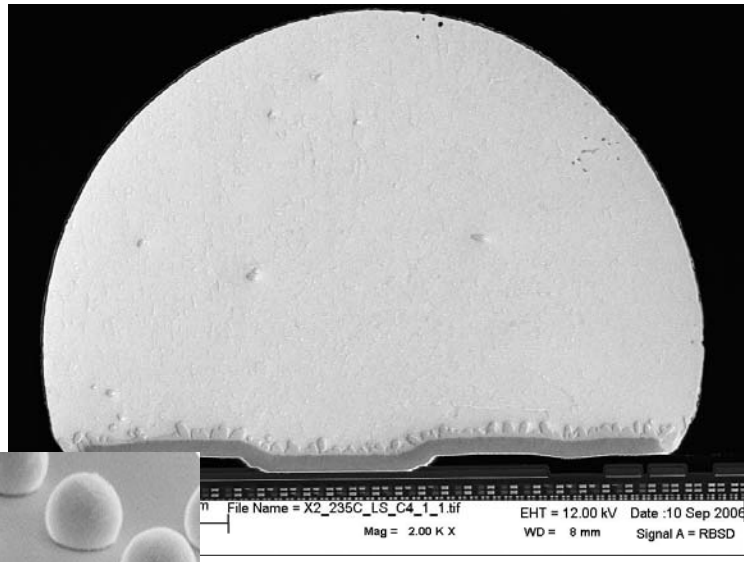
- ✓ **Pull strength**
- ✓ **Rupture in poly pull out or Al pad lifting**
  - ➢ **5% at 235 – 59% at 300C**
- ✓ **Grain structure change – hexagonal to fine tetragonal**

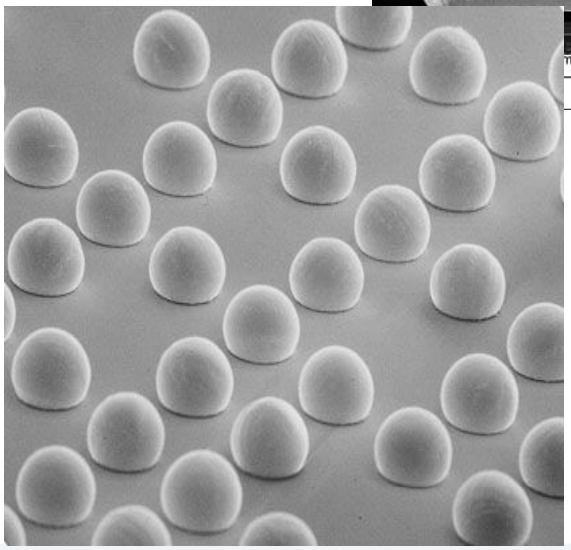




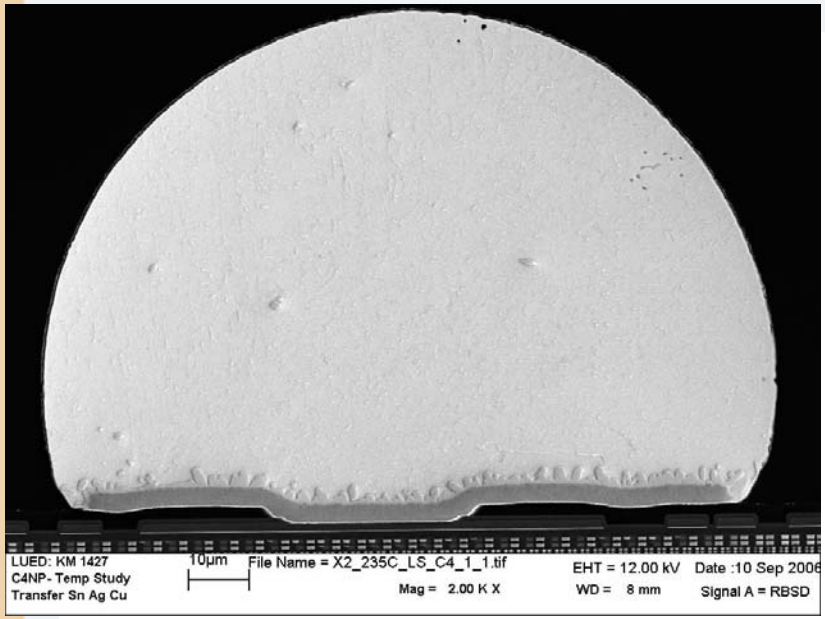
C4NP Lead Free Solder Reliability; SEM Analysis

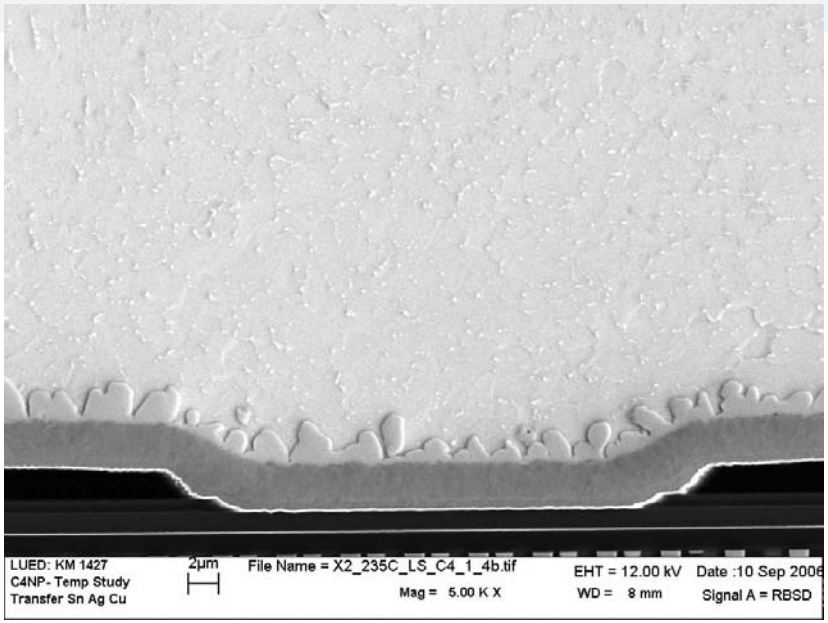
- ✓ **Ni barrier consumption**
- ✓ **Cu under Ni thermal undercut**
- ✓ **Rupture mode**

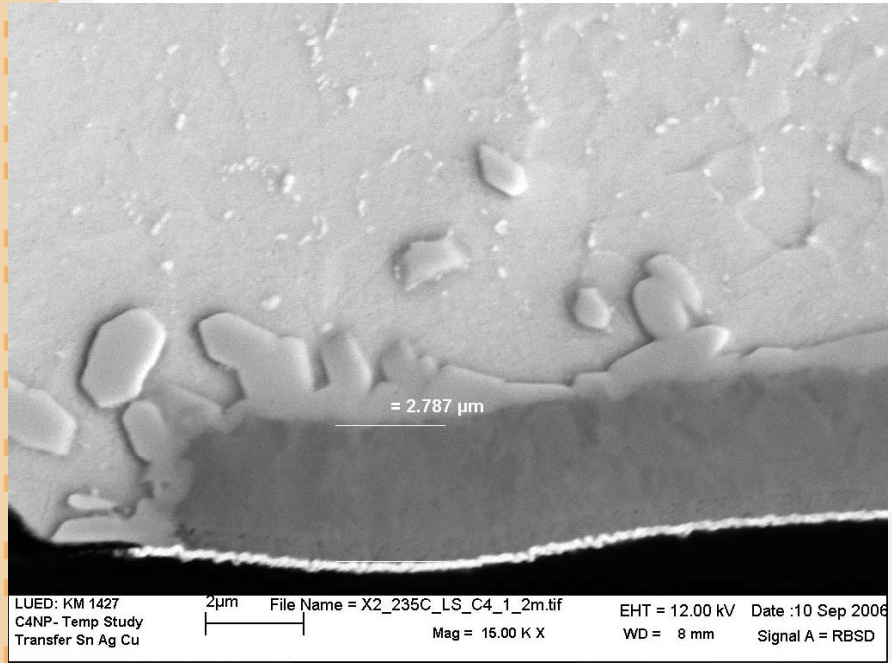


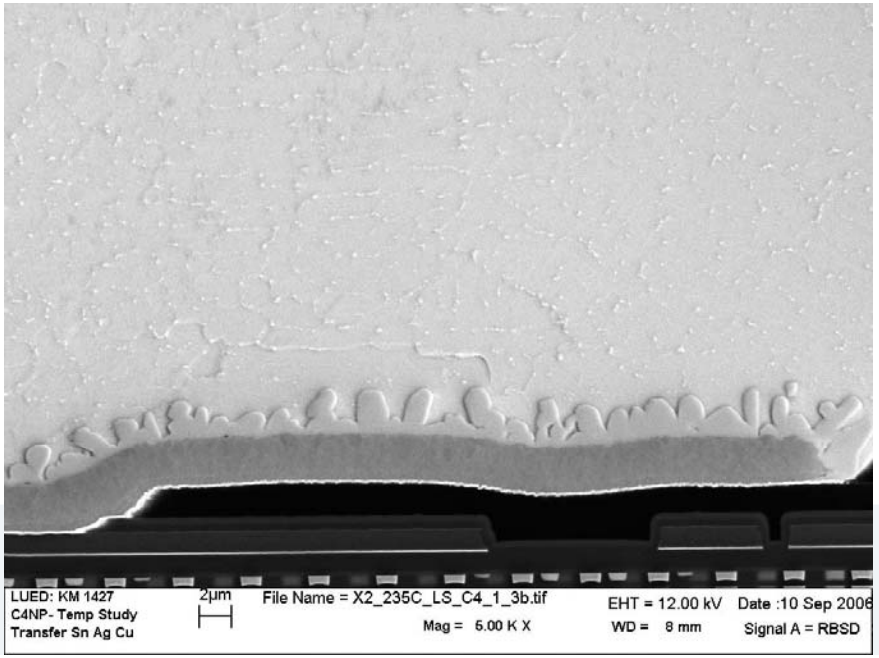


Plated Ni UBM / SnAg Solder Transfer at 235C

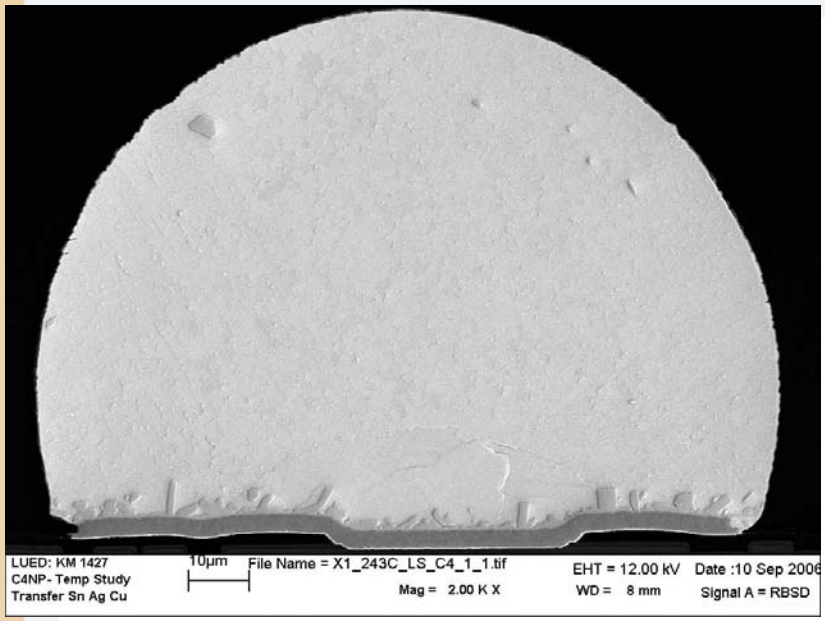


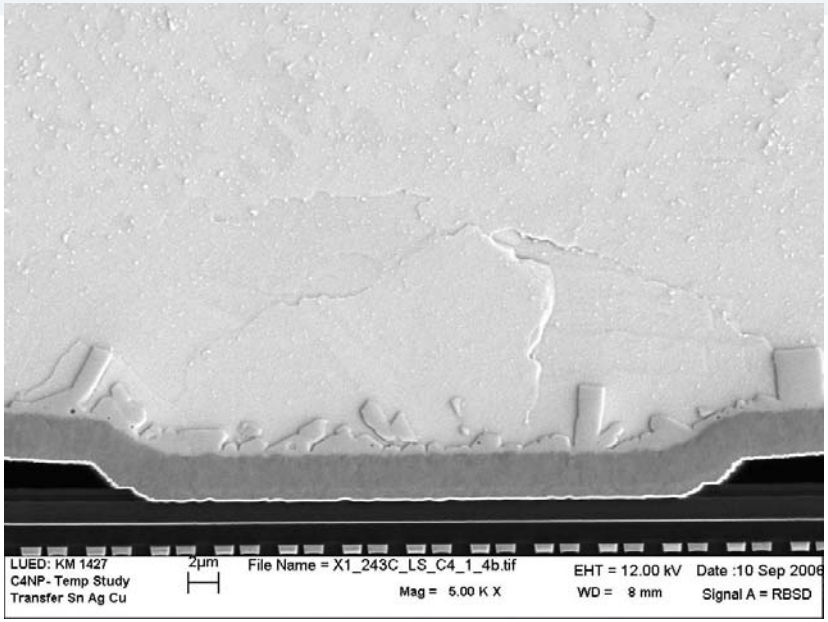


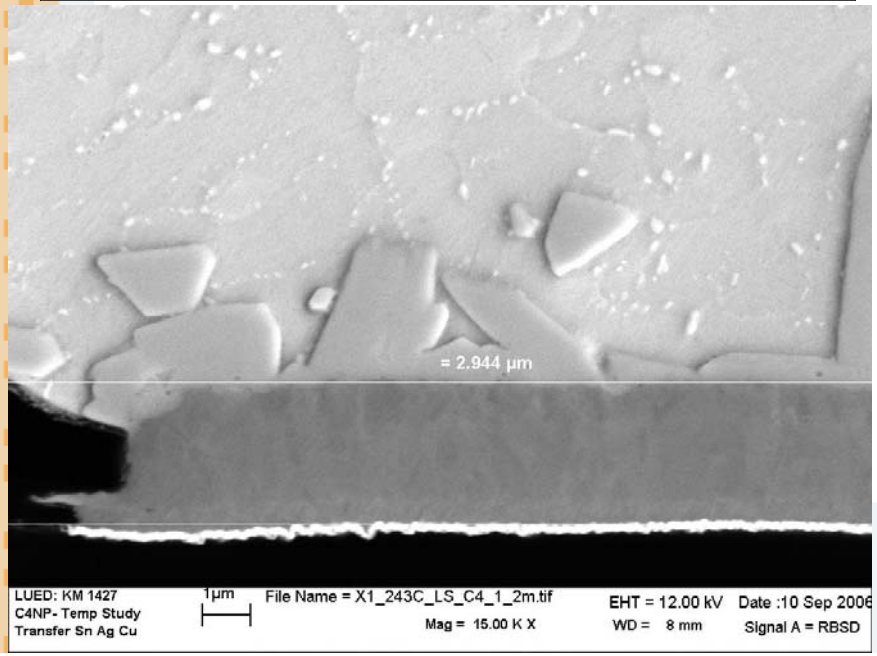


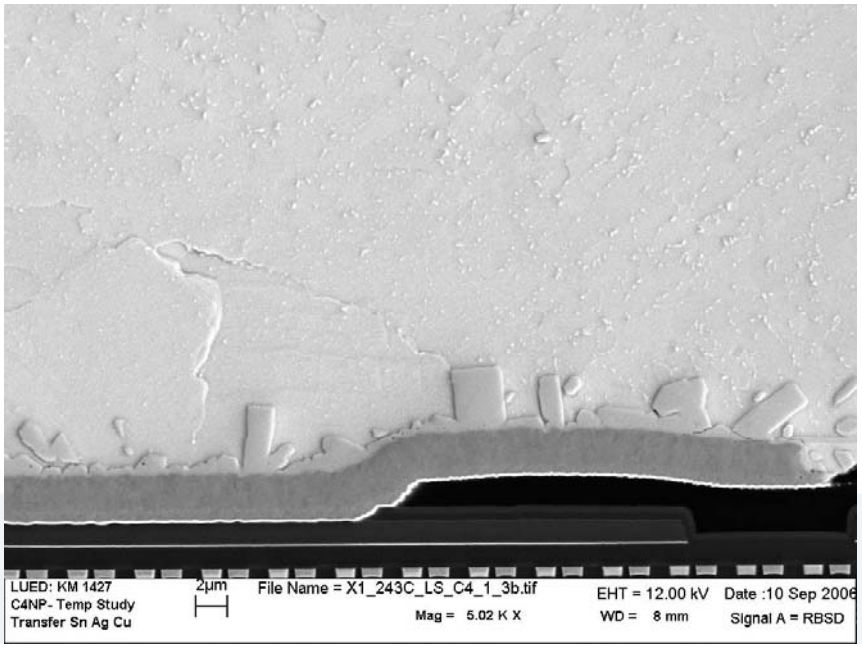


Plated Ni UBM / SnAg Solder Transfer at 243C

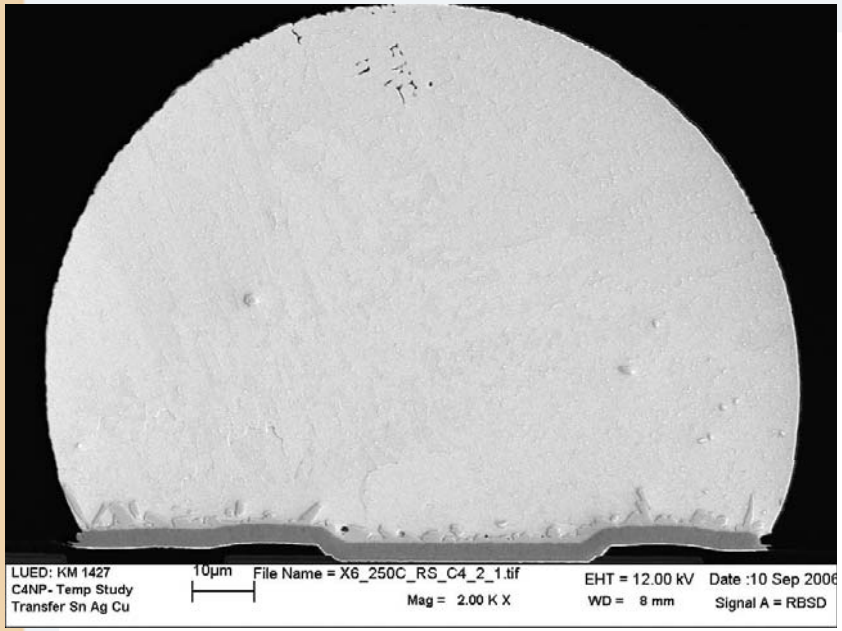


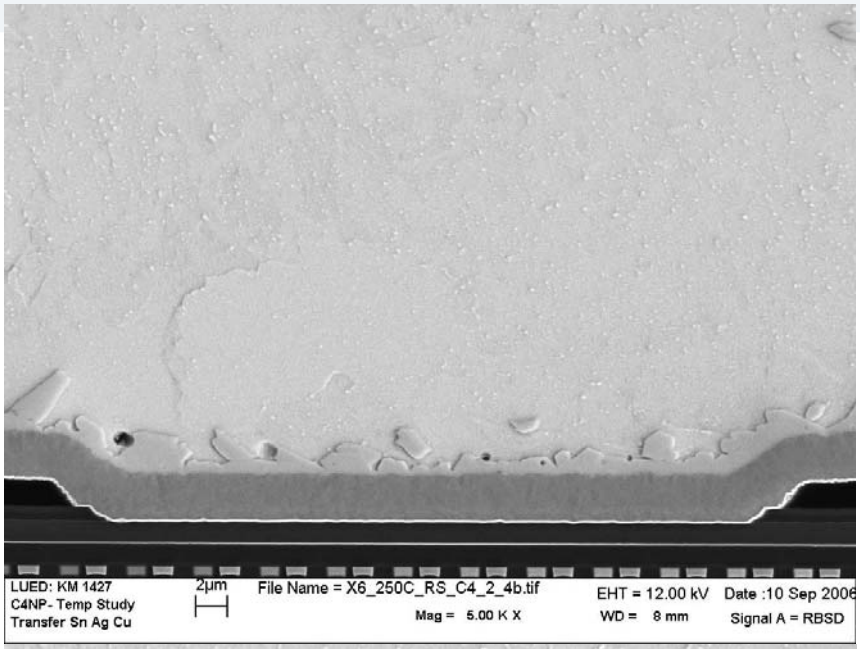


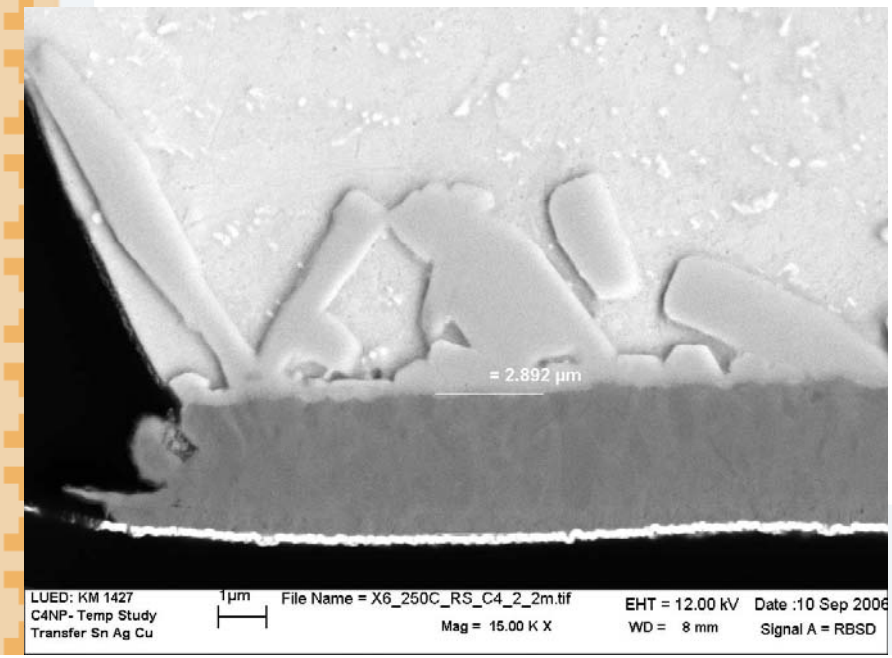


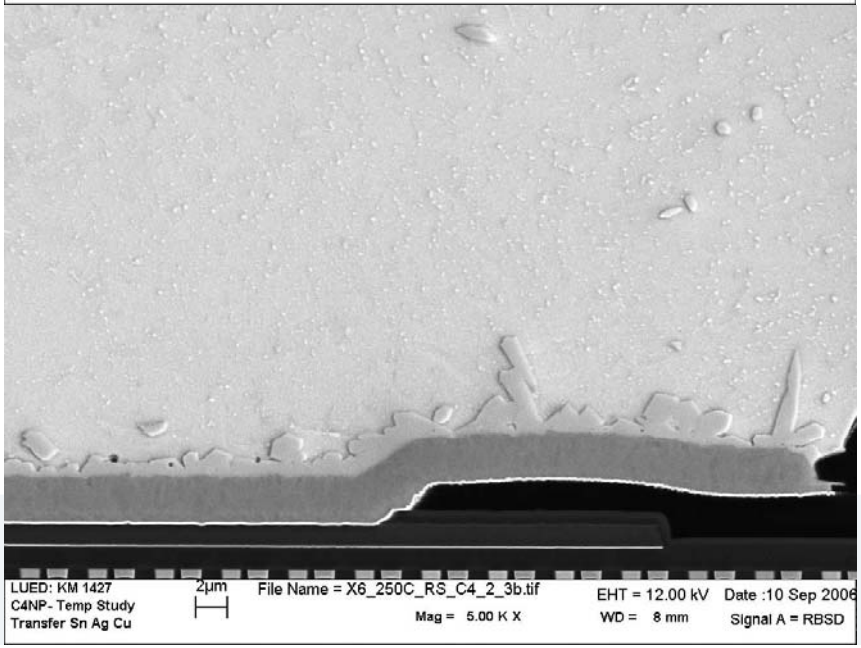


Plated Ni UBM / SnAg Solder Transfer at 250C

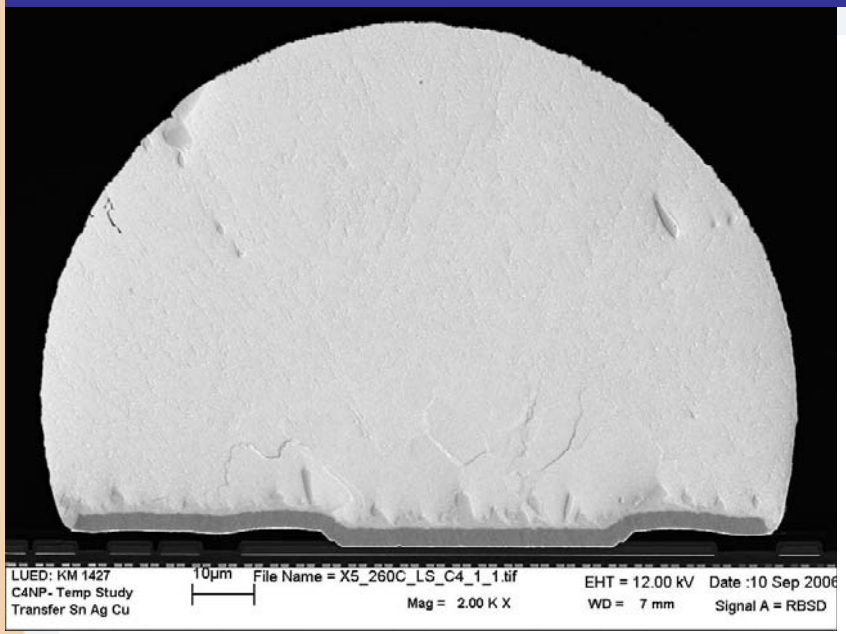


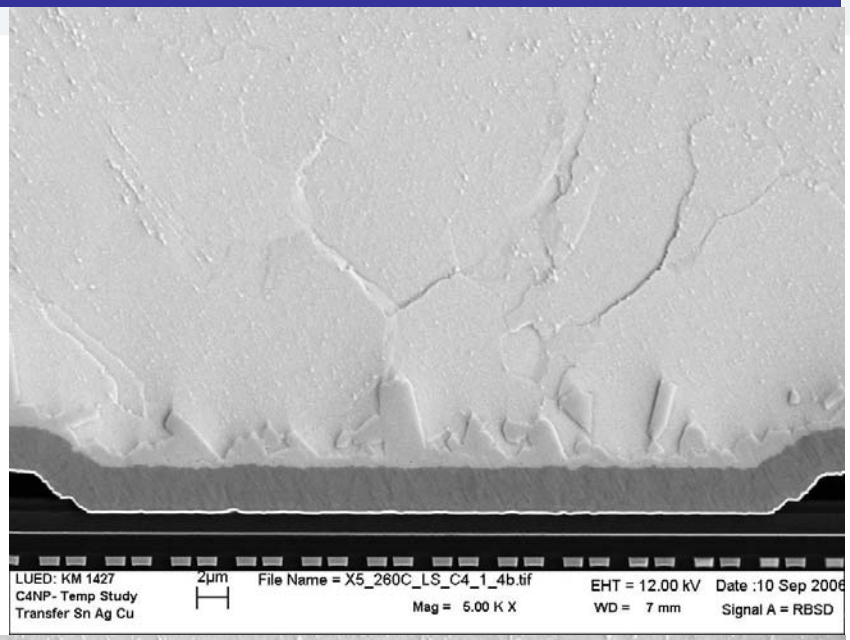


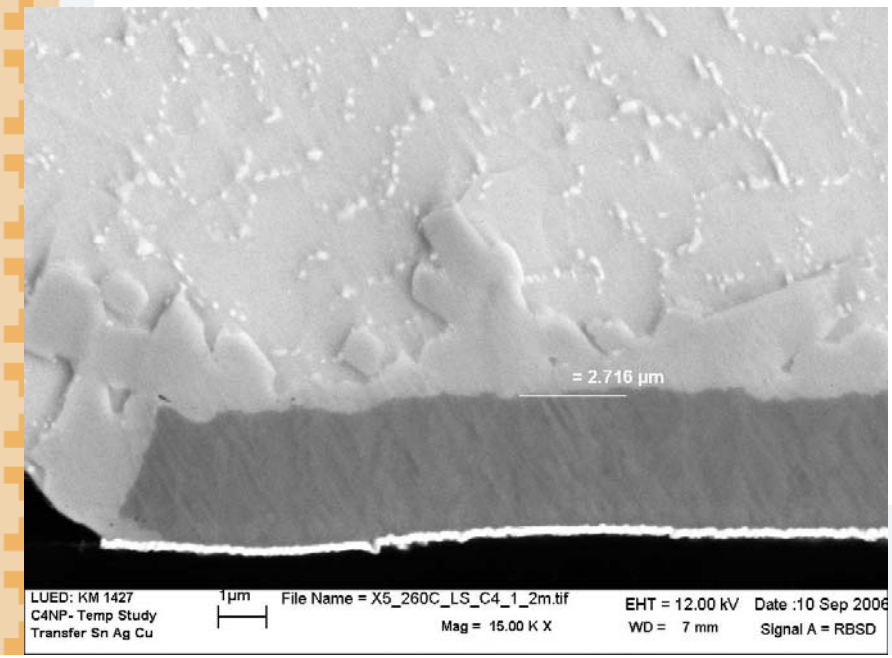


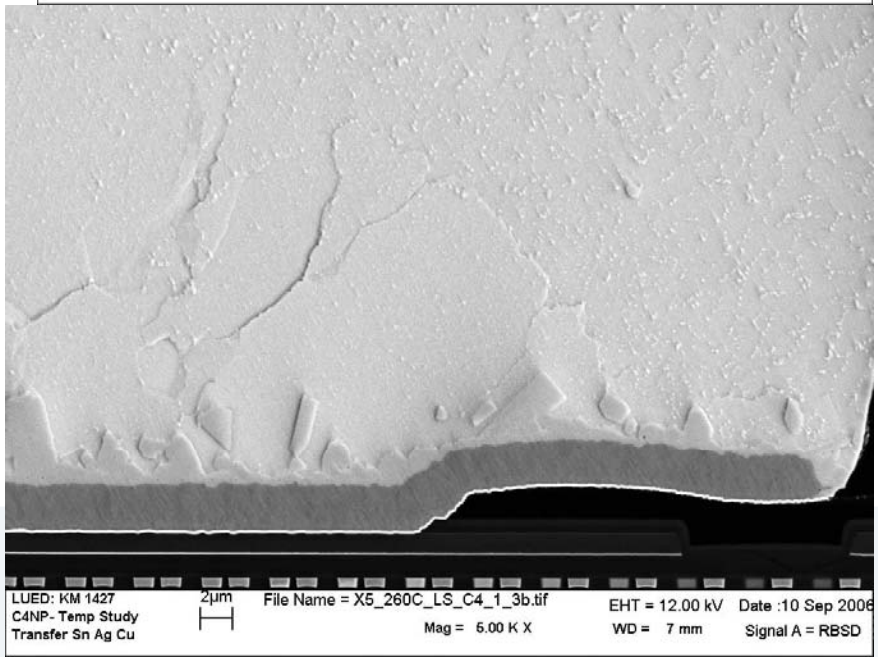


Plated Ni UBM / SnAg Solder Transfer at 260C

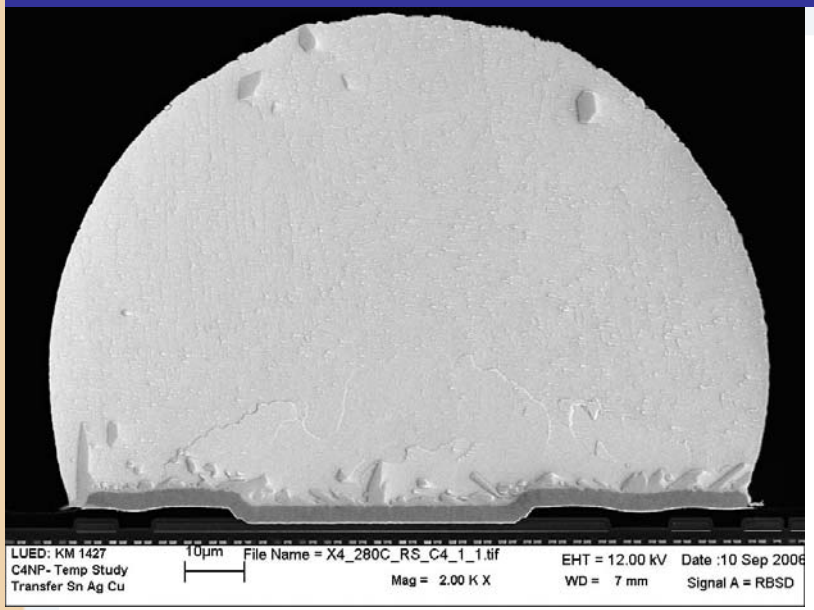


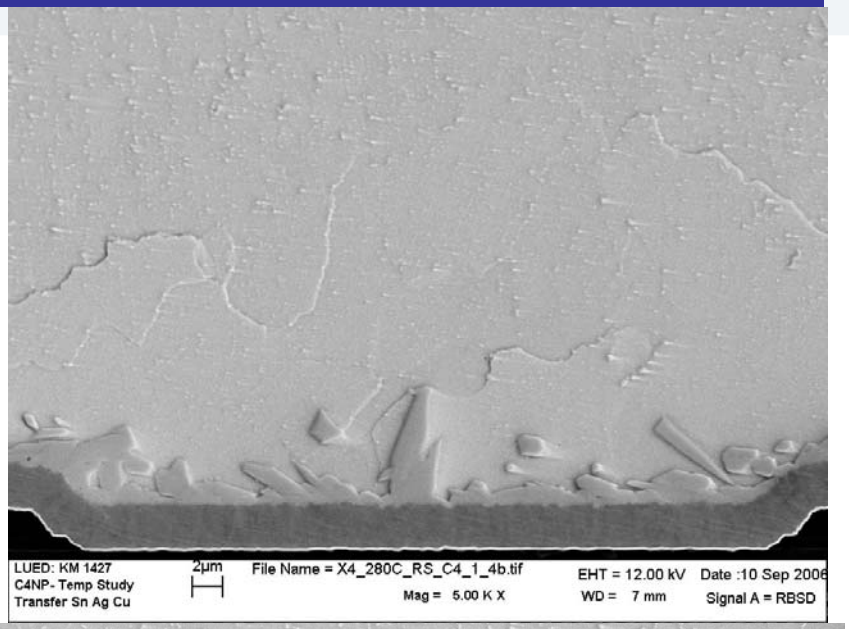


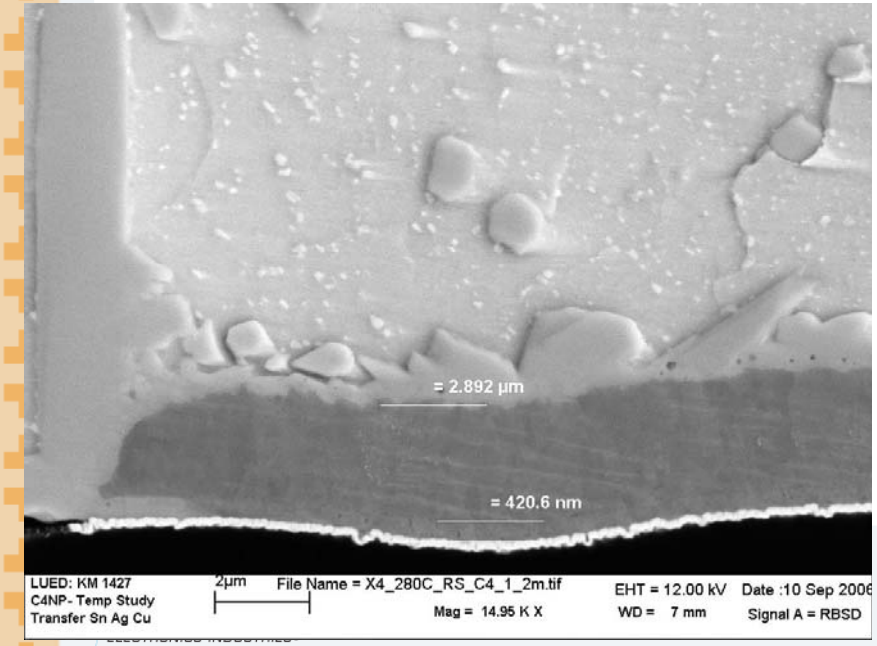


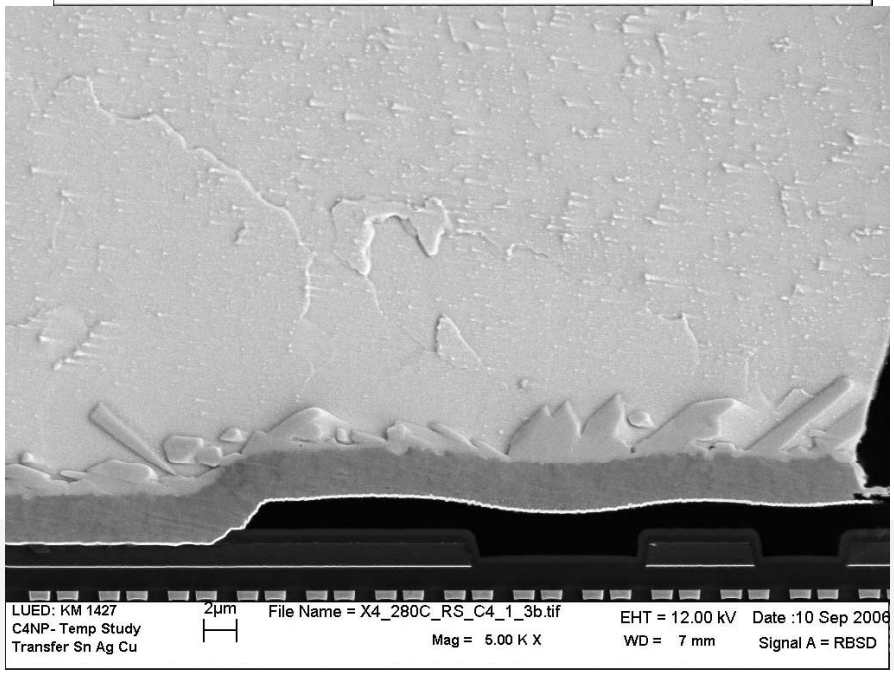


Plated Ni UBM / SnAg Solder Transfer at 280C

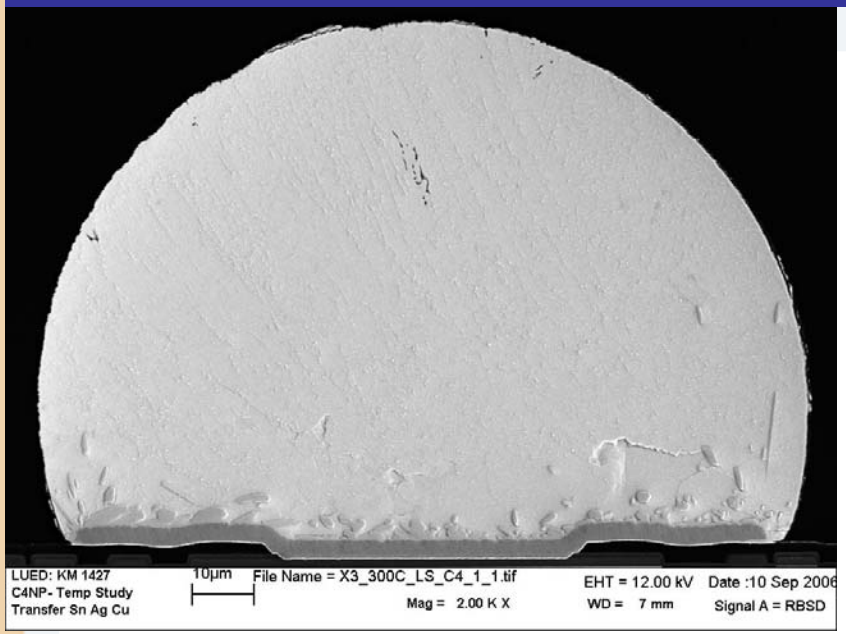


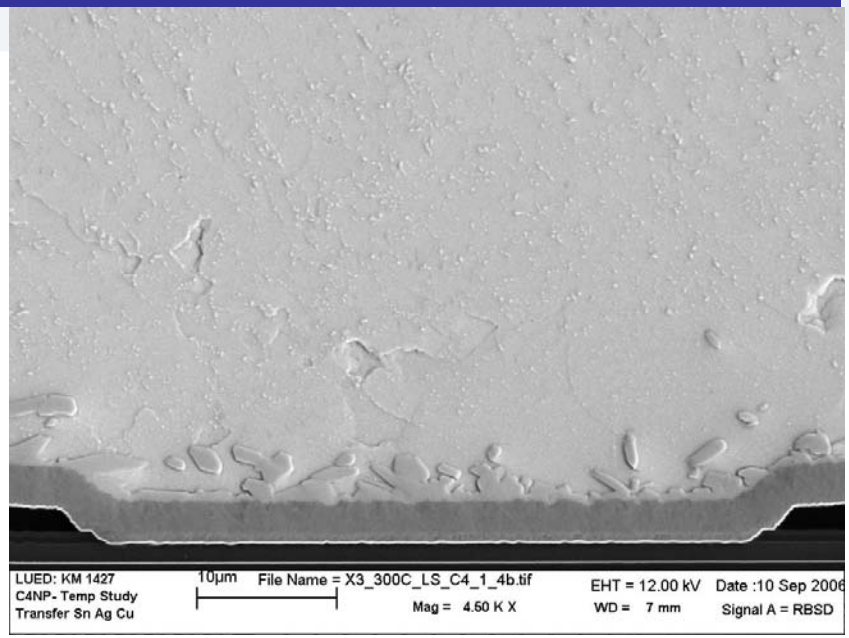


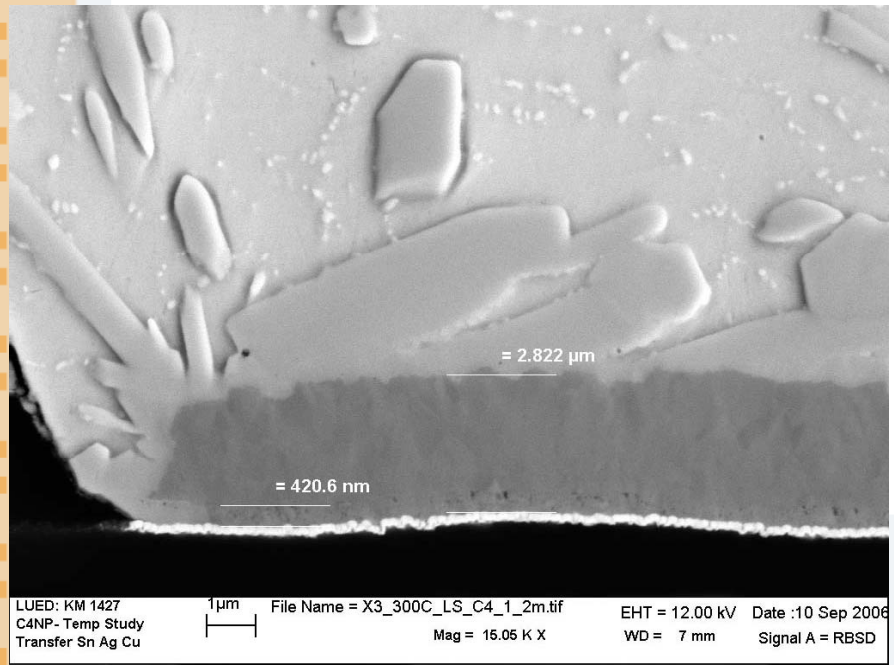


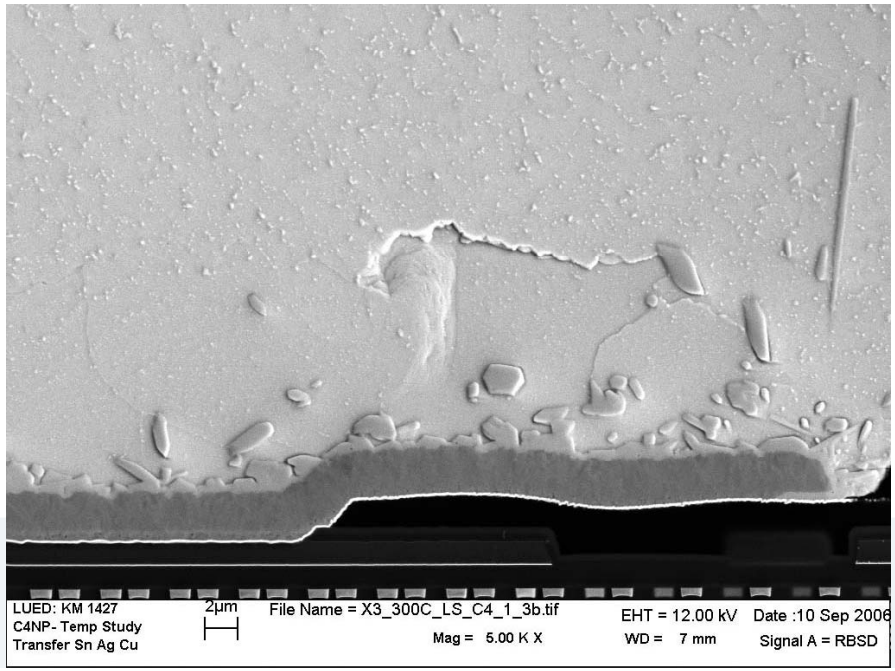


Plated Ni UBM / SnAg Solder Transfer at 300C



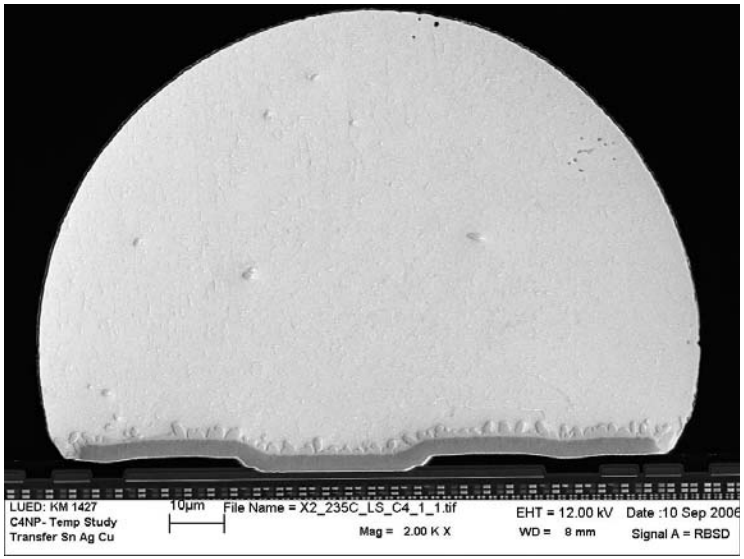






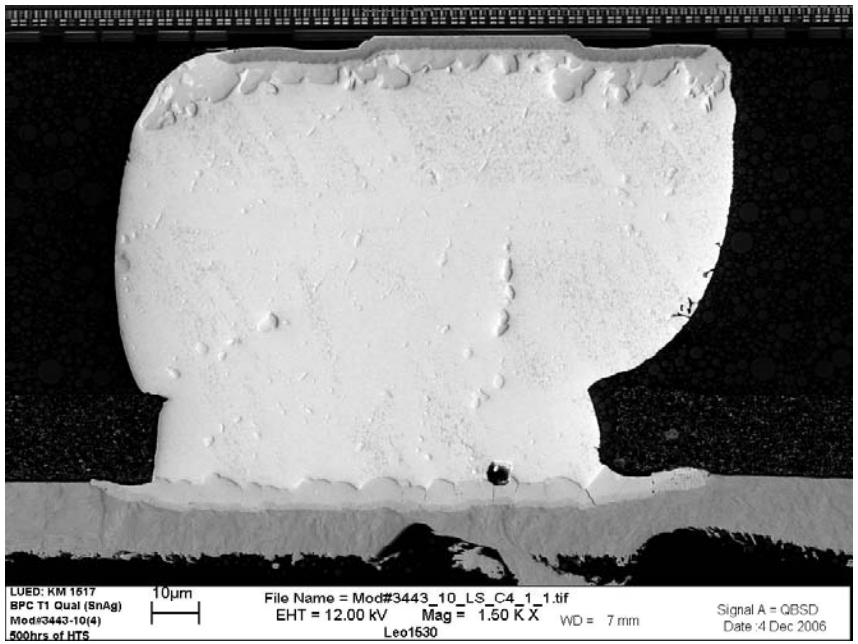
C4NP Lead Free Solder Reliability; SEM Analysis

- ✓ **No change in Ni barrier, unreacted**
- ✓ **Increased reaction of Cu under Ni – thermal undercut**
- ✓ **Stress concentration point , rupture in UBM and Aluminum pad**



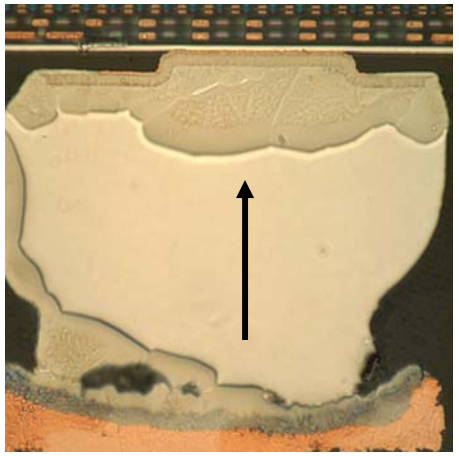
C4NP Lead Free Solder Reliability; High Temperature Storage

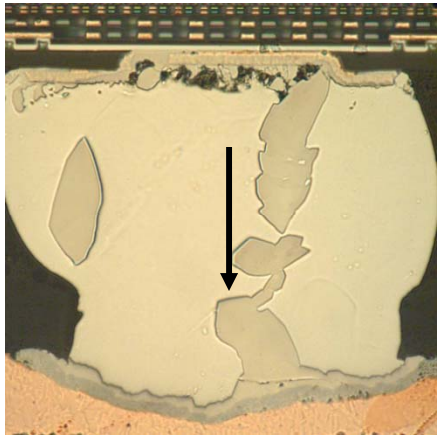
- ✓ **170C for 1000hrs, solid state aging**
- ✓ **No resistance change observed at T0, Post Jedec 3 precon or every 250hr reading to 1000hrs**
- ✓ **No Kirkendall voids found in SEM of cross section**



C4NP Lead Free Solder Reliability; Electromigration

- ✓ **140C and 0.7Amps post Jedec level 3 precon with 2X, 245C module and 1X card join reflow for 2000hrs**
- ✓ **Out of 12, 6 modules with electron flow from chip to substrate, and 6 with electron flow from substrate to chip**
- ✓ **No electrical fails. No difference in UBM, Cu, Ni and Sn intermetalics**





IPC Get Interconnected.™ MIDWEST CONFERENCE & EXHIBITION

Outline

- C4NP Technology Overview
- 200um Reliability Test Vehicle
- Lead Free C4NP Reliability
- Conclusion

IPC ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES®

Summary

- **Solder transfer temperatures impact UBM rupture at intermetallic level**
- **Grain structure for UBM intermetallic changed from hexagonal to fine tetragonal**
- **Pull strength showed robust bump integrity**
- **Apparent difference in intermetallic structure as function of transfer temperature was not found to have any impact on solder reliability in HTS and EM tests**