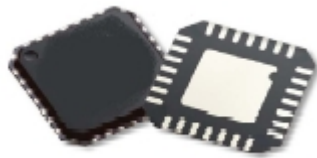


# QFN Rework Challenges in a Lead Free World

IPC Midwest - Sept. 2007



**FINETECH**  
*...simply accurate*

Neil O'Brien

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# Introduction/Abstract

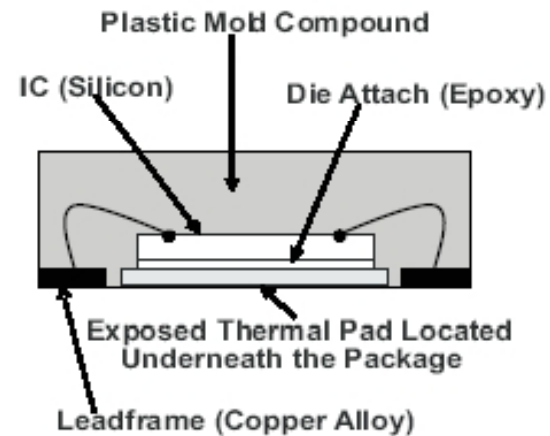
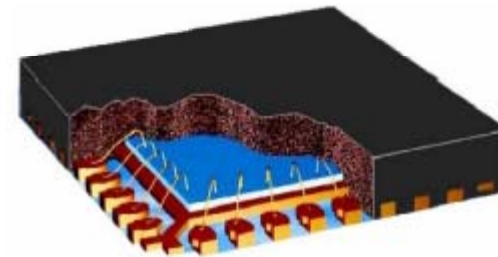
- Small component on densely populated board is a typical scenario today.
- The MLF/QFN package has seen rapid industry acceptance.
- Size, pitch, and density eliminates hand repair.
- Lead Free solder increases these challenges around the rework process.
- Higher reflow temperatures mean tighter thermal control needed. Smaller process window.

# Introduction/Abstract

- QFN Rework Practices Overview
  - Component Removal
  - Site Preparation/Solder Removal
  - Solder Paste Printing
  - New Component Soldering
- Components Studied:
  - 5mm MLF16 – 0.8mm
  - 3mm MLF12 – 0.5mm
  - 7mm QFN48 – 0.65mm
- Stencil Variations: 4mil, 5mil, 6mil

# Why QFN/MLF?

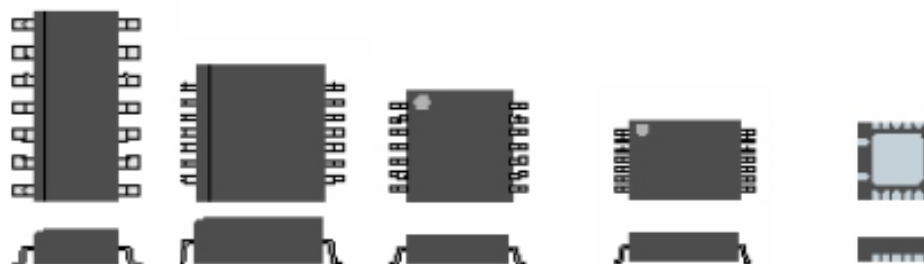
- Small size
- Cost effective
- Good yield/reliability
- Mechanical and Electrical Advantages
- Thermal performance – exposed pad
- Single, double, triple row. Rival BGA.



Courtesy of Texas Instruments

# Design Advantages

- Physical / Space saving.
- Area savings from 40% to 76% vs. SOIC.



Attribute	SOIC-14 (D)	SSOP-14 (DB)	TSSOP-14 (PW)	TVSOP-14 (DGV)	QFN-14 (RGY)
Length, mm	8.65 ±0.10	6.20 ±0.30	5.00 ±0.10	3.60 ±0.10	3.50 ±0.15
Width, mm	6.00 ±0.20	7.80 ±0.40	6.40 ±0.20	6.40 ±0.20	3.50 ±0.15
Height, Max., mm	1.75	2.00	1.20	1.20	1.00
Pitch, mm	1.27	0.65	0.65	0.40	0.50
Footprint, mm <sup>2</sup>	51.90	48.36	32.00	23.04	12.25
Weight, g	0.127	0.122	0.055	0.040	0.032
Area savings, %	76.40	74.67	61.72	46.83	-

Courtesy of Texas Instruments

# Design Advantages

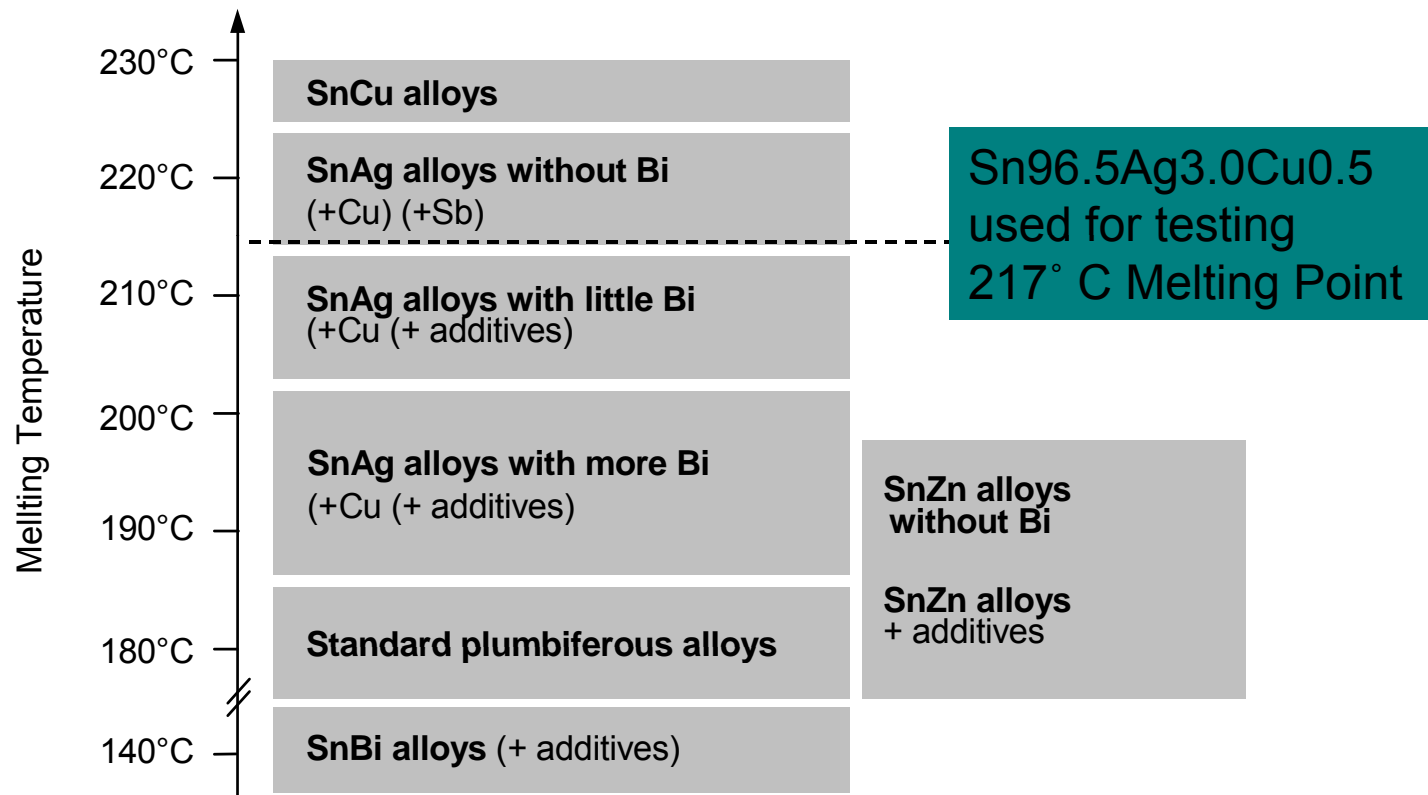
- Electrical performance due to unique package design.
- Improved Thermal Impedance due to ground pad soldered to PCB.
- Inductance (L) reduced due to ground pad and no leads. No long “wires” to act as inductor.
- Simplified alternative to BGA.

16-Pin QFN Package-Parasitics Comparison

	SOIC-16 (D)	SSOP-16 (DB)	TSSOP-16 (PW)	TVSOP-16 (DGV)	QFN-16 (RGY)
Average R, $\Omega$	0.039	0.048	0.045	0.039	0.039
Average L, nH	3.453	3.536	2.593	2.543	0.886
Average C, pF	0.521	0.376	0.281	0.386	0.327

Courtesy of Texas Instruments

# Lead Free Alloys- SAC Tin/Silver/Copper



*Melting temperature of different solder materials.*

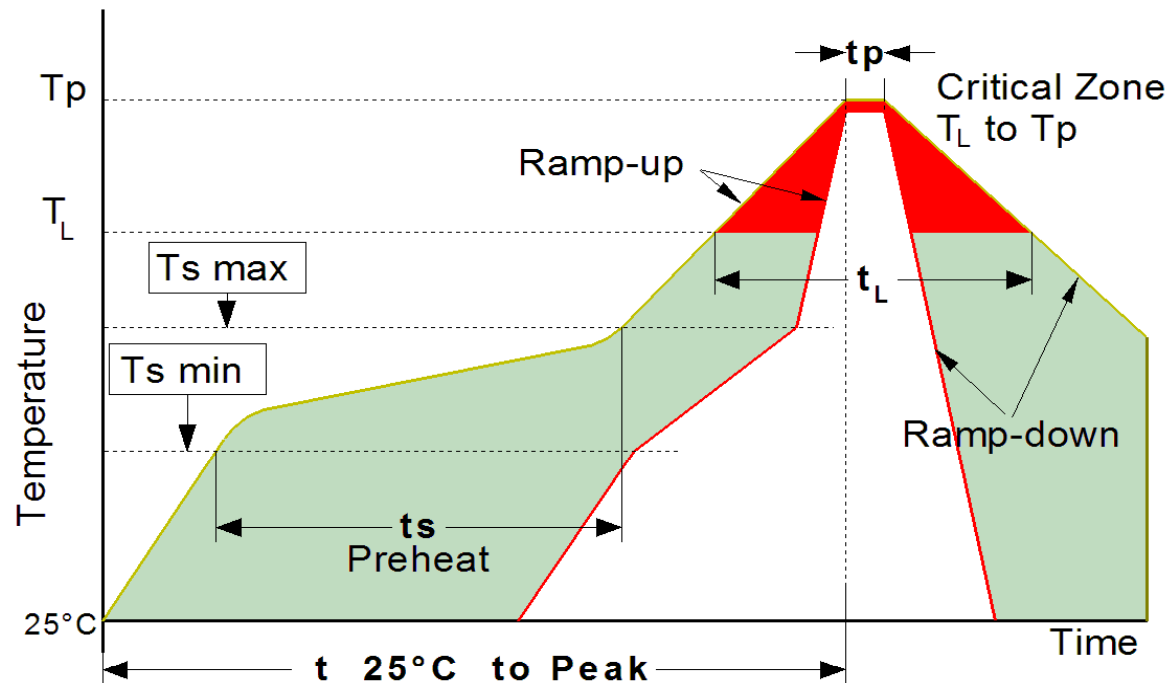
# QFN Pb Free – Rework Systems

- System capable of process control & repeatability.
  - preheating
  - activation phase
  - peak zone
  - Cooling
- Vision assisted with good resolution&accuracy.  
The Experimental System:
  - Also “Nitrogen Switching” via software programmable set points.
  - 10micron (.0004”) standard placement accuracy.
  - Precise control of temperature and airflow “Thermal Management”



# Following the Standard

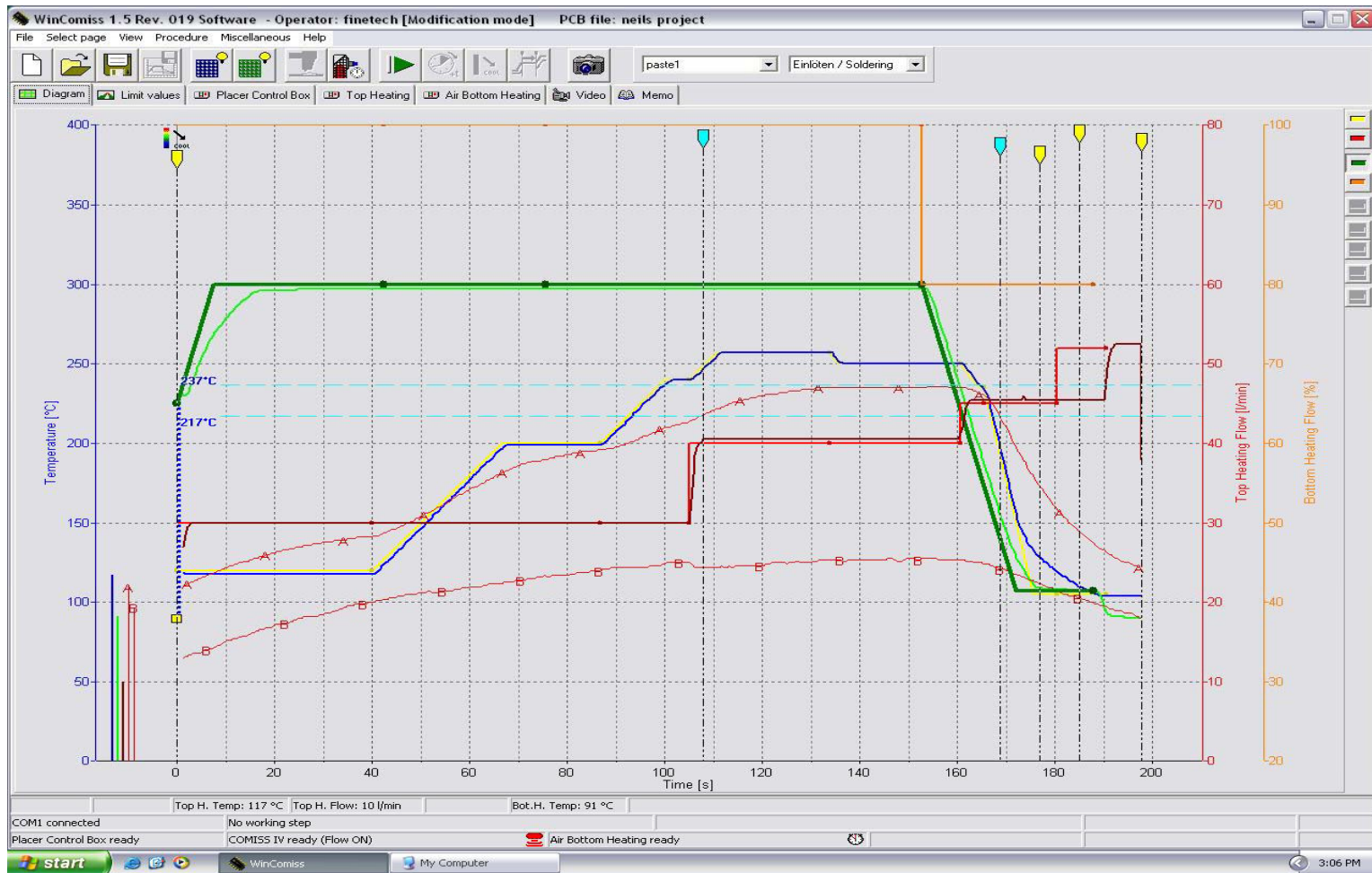
## IPC / JEDEC J-STD-020C



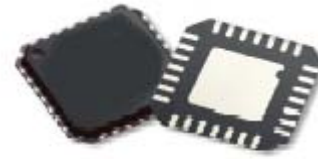
Peak  $T_p = 245^\circ\text{C}$  for large packages  $\geq 350\text{mm}^3$

Peak  $T_p = 250^\circ\text{C}$  for small packages  $\leq 350\text{mm}^3$

# QFN Profile - Lead Free



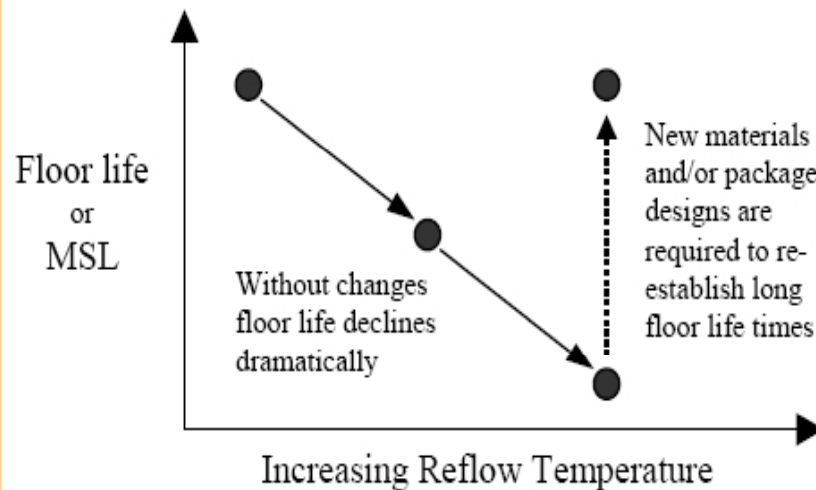
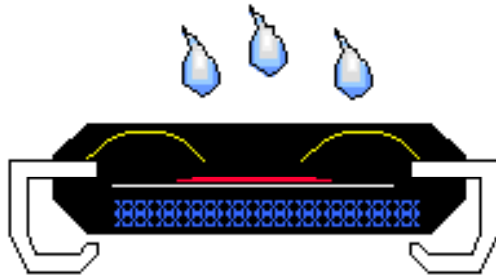
A = Solder joint temperature  
B = Board temperature



# QFN Lead Free Rework Practices

1. Board Preparation
2. Preheating: Bottom Heating
3. Component Removal
4. Residual Solder/Site Cleaning
- 5. Paste Printing/Component Handling**
6. Component Placement/Soldering

# Rework Practices 1



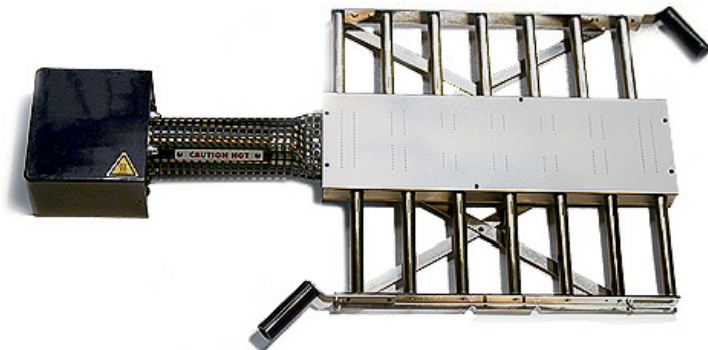
## PCB Preparation

- ✓ Moisture absorption by components depending on environment and technology.
- ✓ Vapor pressure causes internal damage to components and or PCB. Known as "pop corning"
- ✓ IPC standards (8 levels) for moisture sensitivity "MSL".
- ✓ Generally from 80° to 125°C for up to 24 hours.
- ✓ Bake and Bag option, dry storage.

# Rework Practices 2



Localized Heating example.



Full Area Board Heating example.

## Board Preheating:

- ✓ PCB – fiberglass, resin, copper, components, etc.
- ✓ Thermal expansion CTE varies with each.
- ✓ Unevenly applied heat will cause thermal stress and warpage.
- ✓ Increased temps. for Pb free magnifies PCB stresses.
- ✓ Underboard heating. Localized and full area (examples shown).

# Rework Practices 2

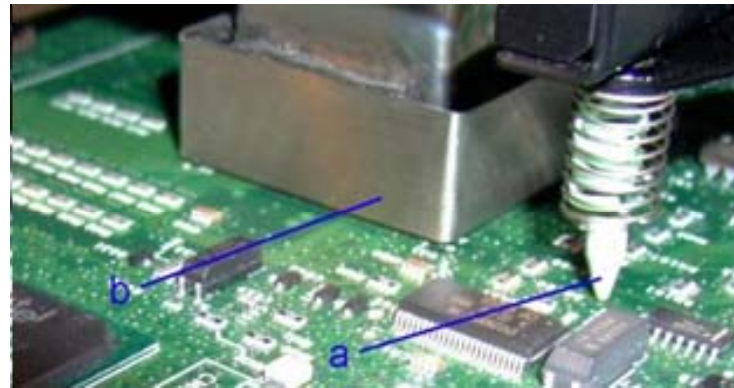
## Board Preheating Principles:

- ✓ Board Thickness will effect pre-heating phase.
- ✓ Lead Free Bottom temps.  $\sim 150^{\circ}$
- ✓ Start sensors

sometimes:

a = start sensor

b = nozzle

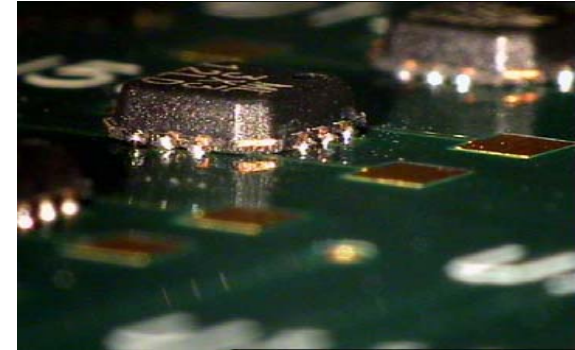


- ✓ External Thermocouples:
  - ✓ A. Directly underneath component to be reworked.
  - ✓ B. Near board edge - monitor delta.



# Rework Practices (3)

## Component Removal:



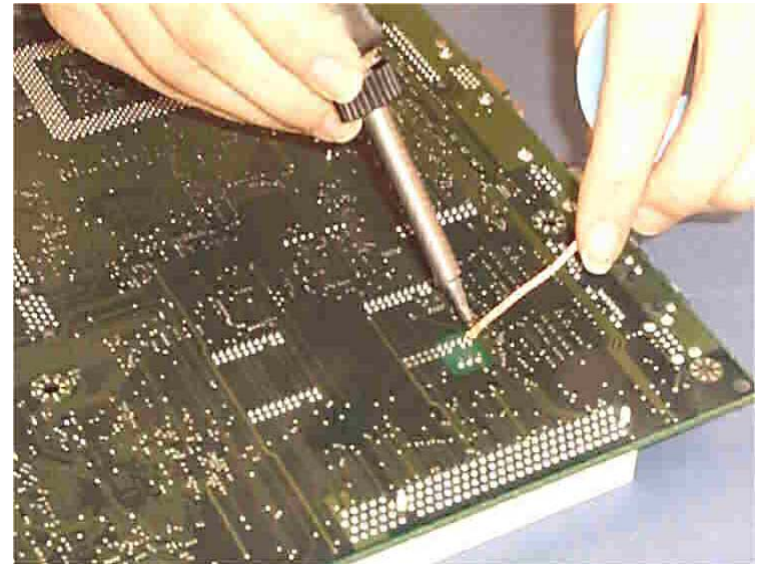
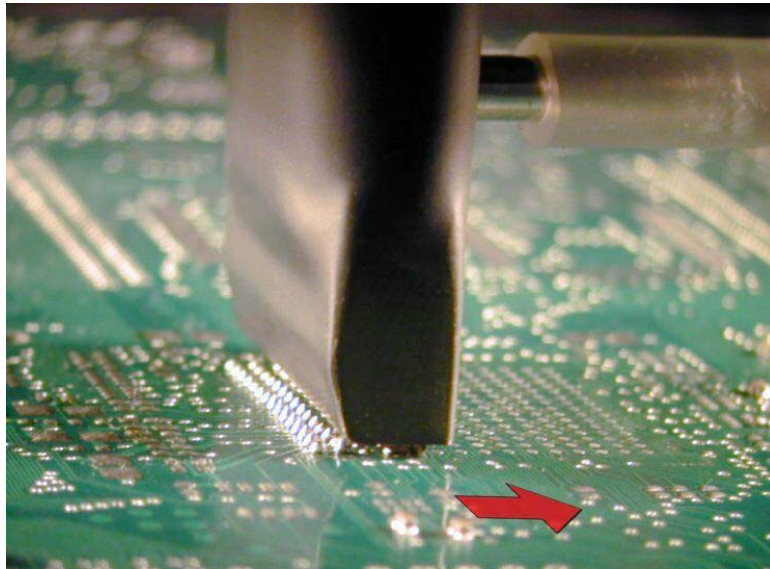
- ✓ Typical ramp rates between 2 and 5° deg/sec.
- ✓ Normally component not to be re-used. Then ramp rate can be higher.
- ✓ Caution for neighboring components. Temp and Airflow.
- ✓ QFN Rework:
  - a. Develop profile to ensure all solder has reflowed before attempting removal.
  - b. SURFACE TENSION OF SOLDER ON THERMAL PAD!
  - c. Nozzle design, vacuum pull considerations.



# Rework Practices (4)

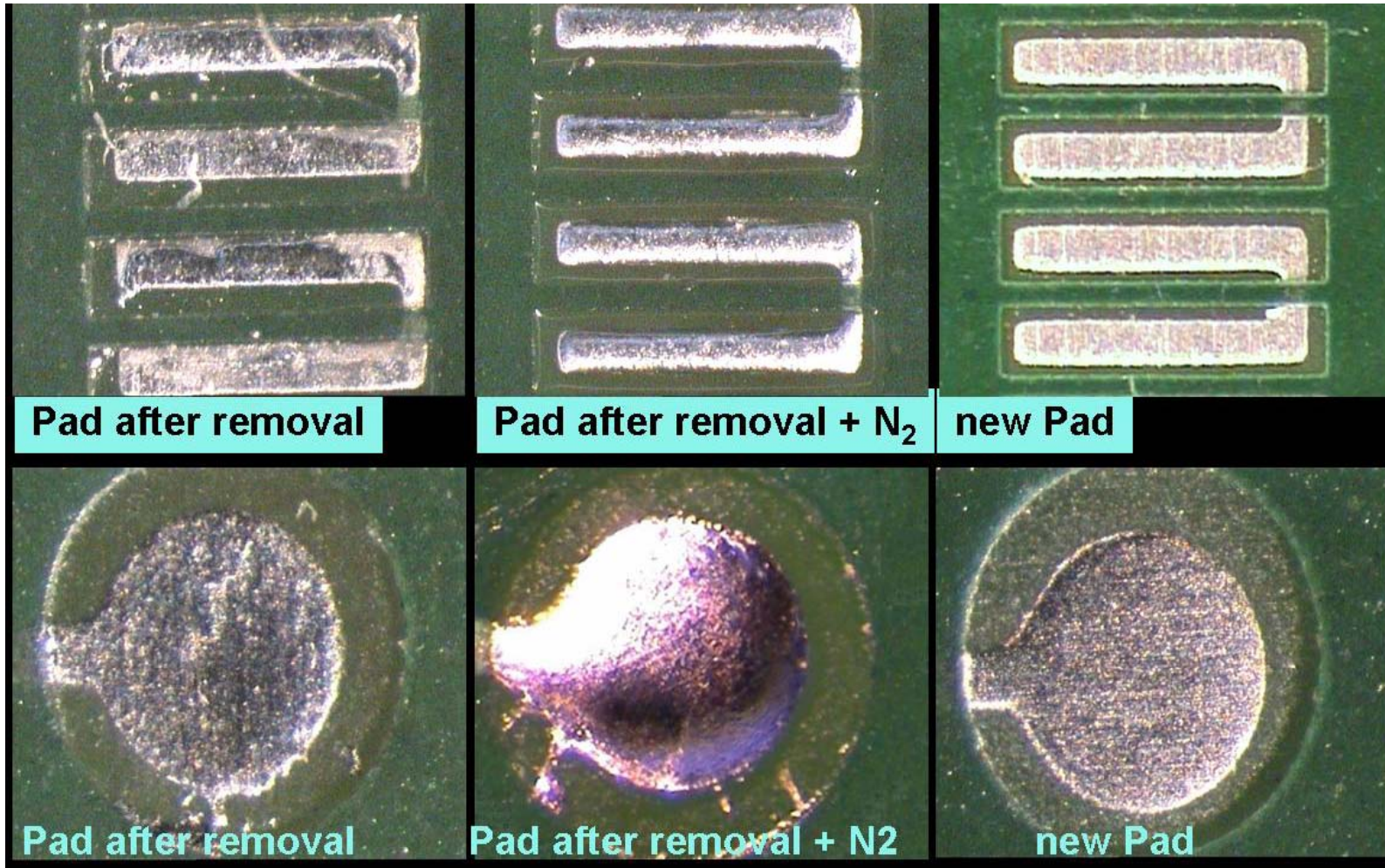
## Site Preparation - Residual Solder Removal:

1. Machine assisted methods via vacuum.
2. Solder wick and soldering iron.
3. Re-use residual solder (Nitrogen recommended). Not typical.

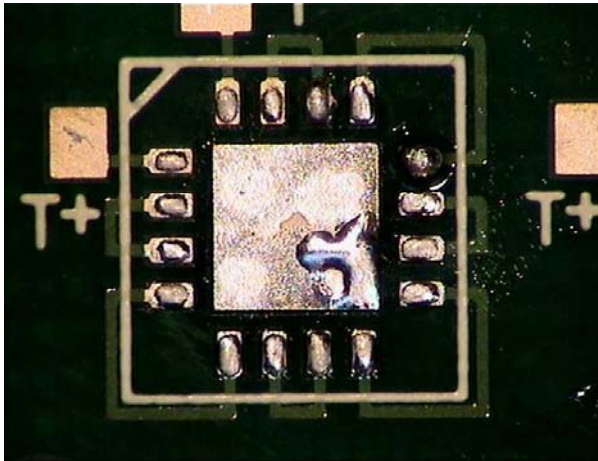




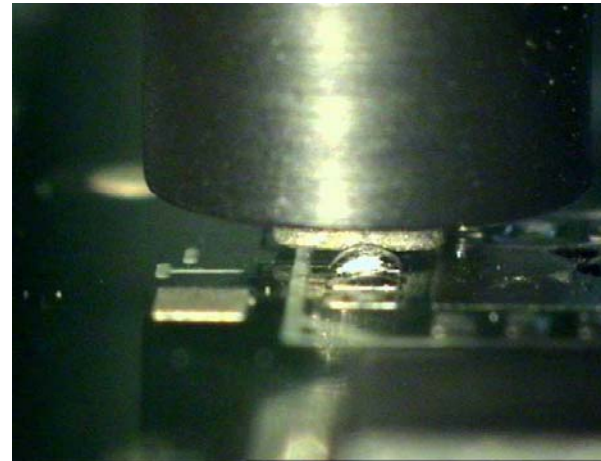
# Residual Solder Removal (4)



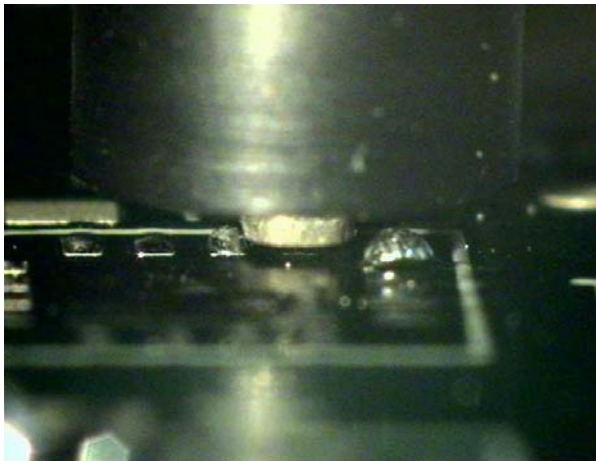
## Site Preparation - Residual Solder (4)



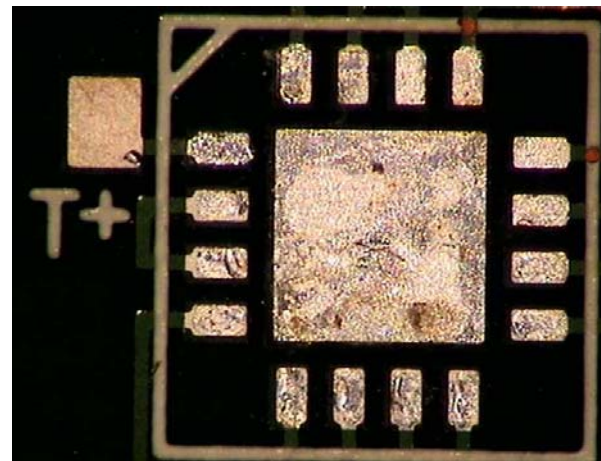
Before Site Clean



Process Observation



Process Observation



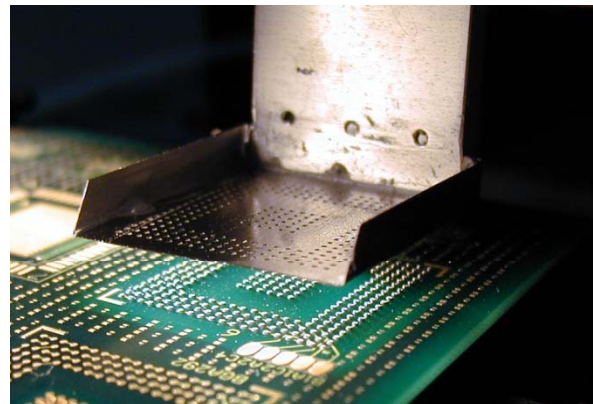
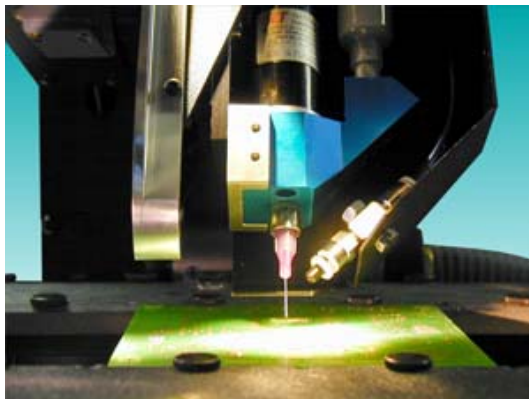
After Site Clean



# Rework Practices (5)

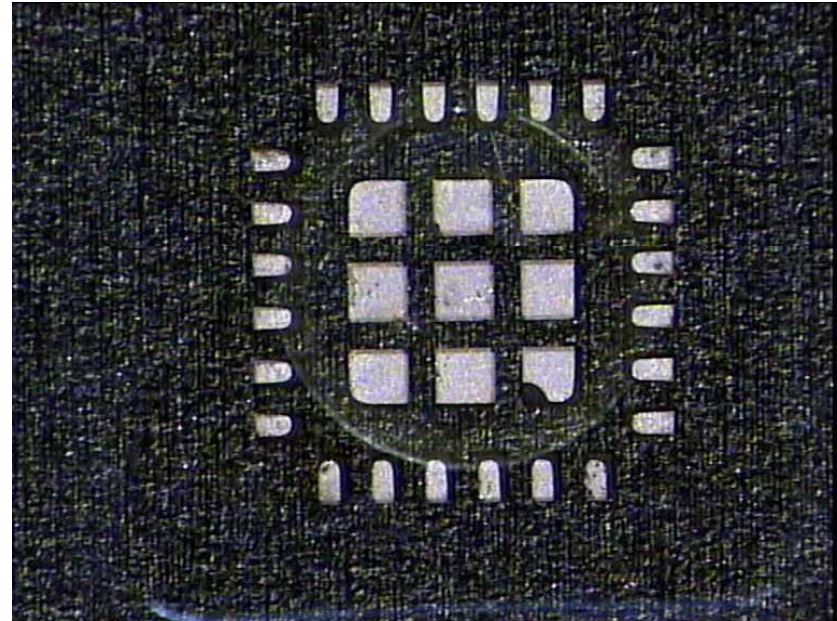
## Printing Solder Paste for QFN's:

1. Mini Stencil board or component.
  - Board Density and small QFN sizes make board printing difficult or impossible.
2. Dispense paste.
  - Requires dispenser system. Manual, semi, auto.
  - Volume control is an issue.
  - Board removal from rework system. More handling/time.



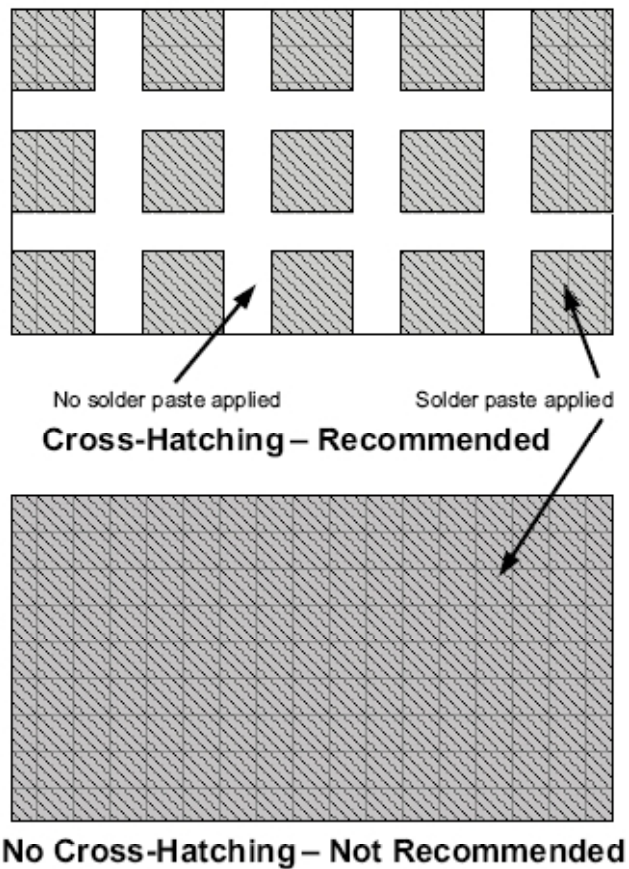
## Rework Practices (5) – Stencil Design

- Thickness 3 to 4mil  
75 to 100µm
- Area Ratio >.66 still applies.
- Transfer Efficiency > 80%
- Paste Type III, IV



Overlay Image: Component to Stencil

# Rework Practices (5) – QFN Stencil Design



Courtesy of Texas Instruments

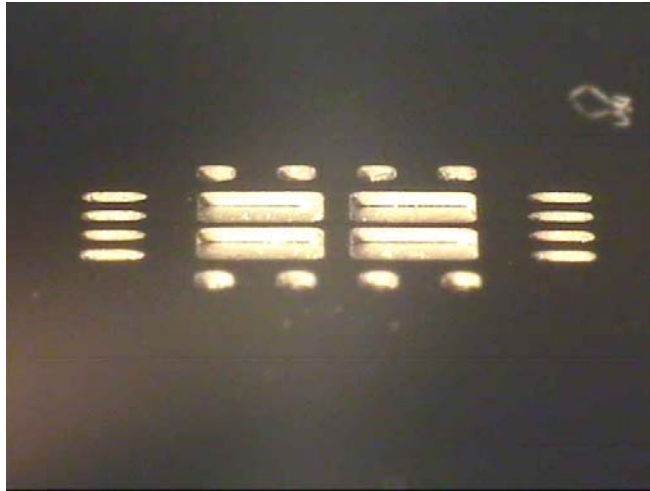


Ex. Cross Hatch “Window Pane”

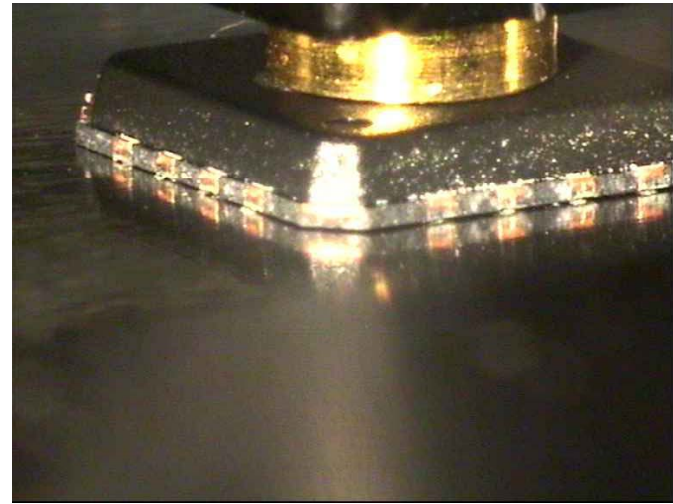




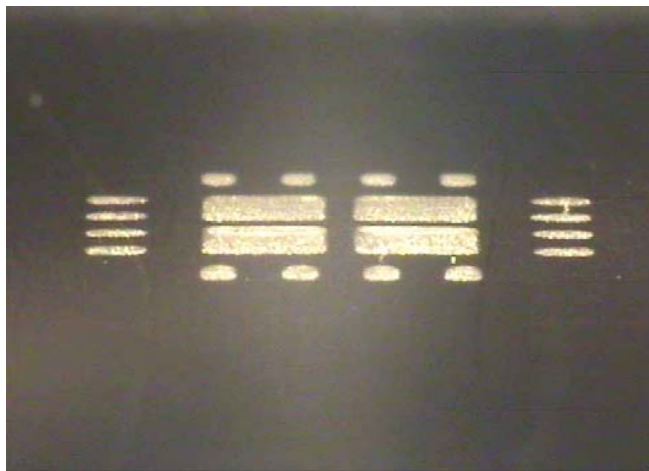
## Rework Practices (5) – QFN Stencil Design



4 mil stencil before paste



Component placed to stencil



4 mil stencil after paste



5mm QFN from 4mil stencil

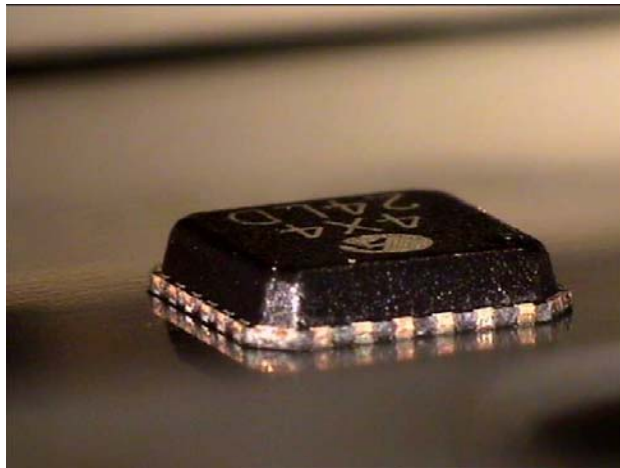
## “Hands Free” Component Handling (5)



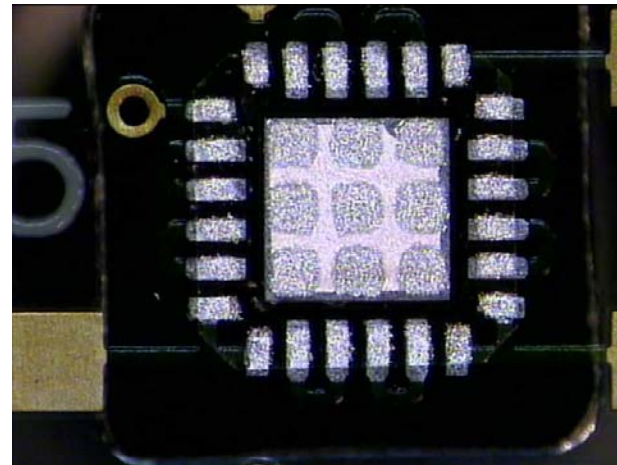
Printing component



Flip – ready for nozzle pickup



Pasted – ready for pickup.



Align, place and reflow.

# Rework Practices (6)

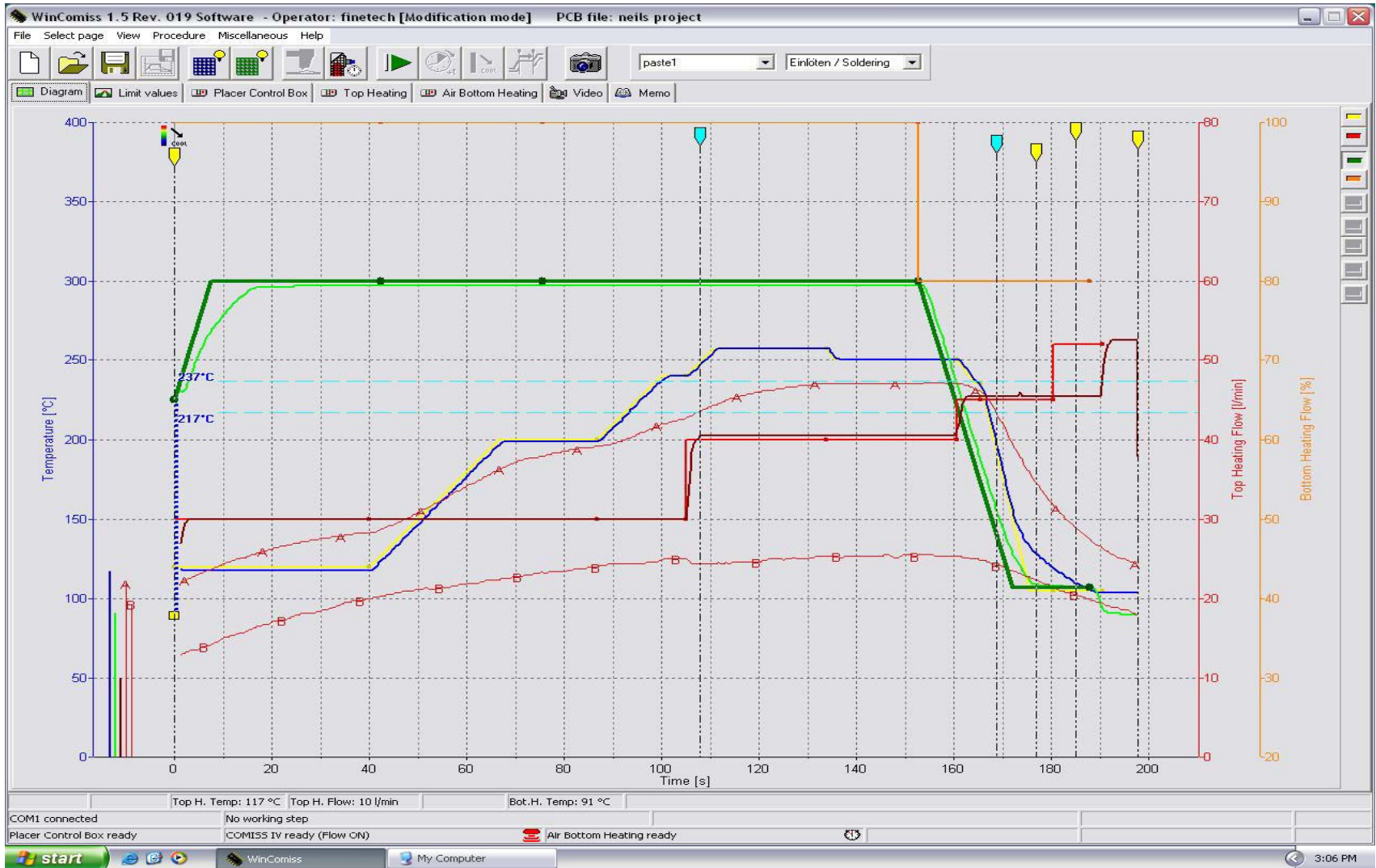
## Component Placement & Soldering:



1. Machine alignment of component to board. Overlay optics typical. Little "self alignment" noted.
2. Lead Free soldering profile following IPC/JEDEC 020
3. Solder Joint and Board Temperature profiled. Component top side temp. also confirmed within mfg. spec.



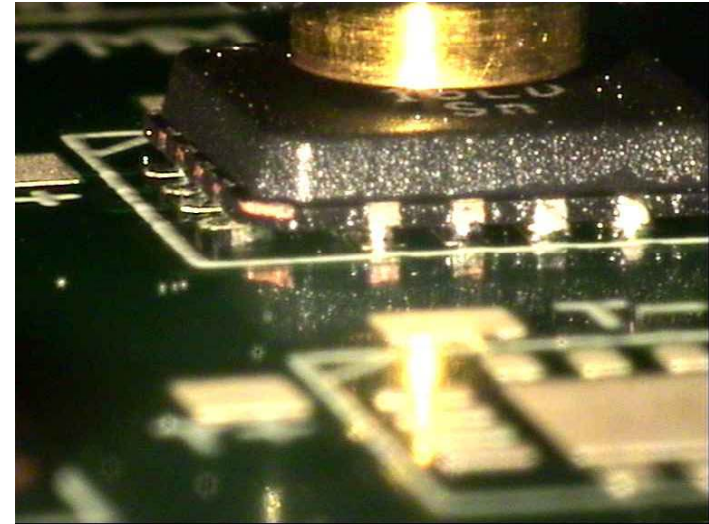
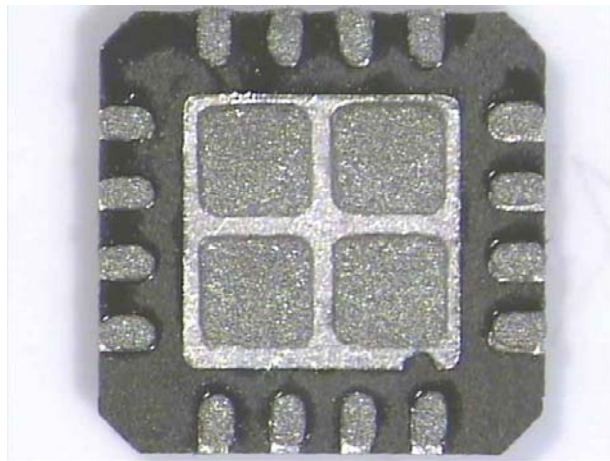
# QFN Placement & Soldering (6)



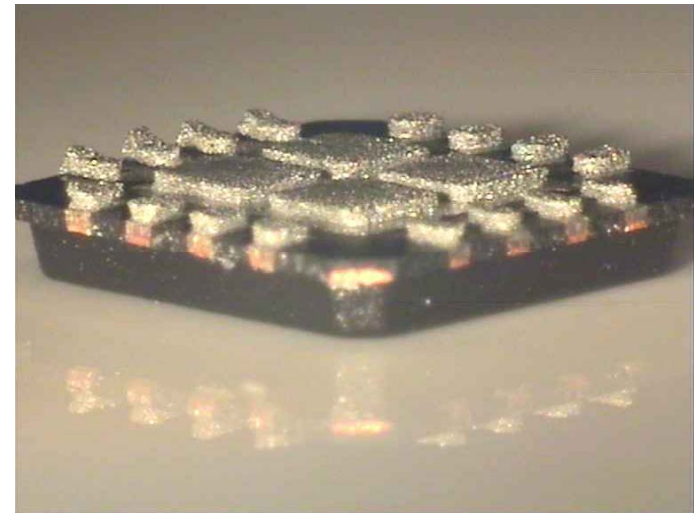
A = Solder joint temperature  
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## Rework Practices (6)

- 5mil stencil produced excessive paste volumes for small 5mm, 3mm QFN's
- Part “swimming”

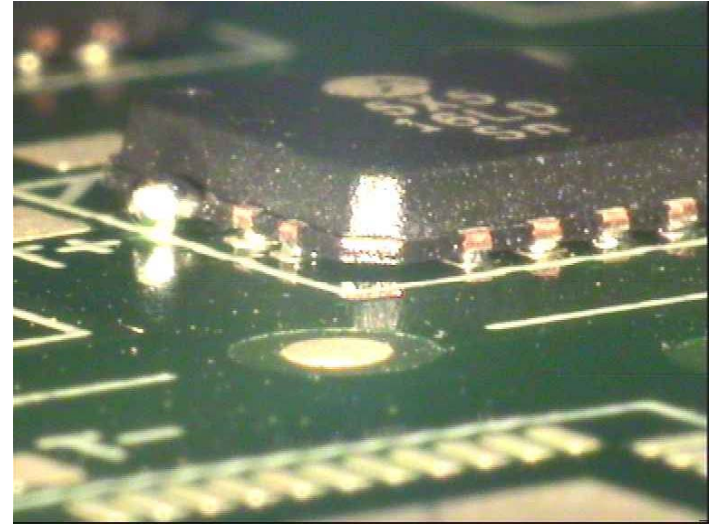
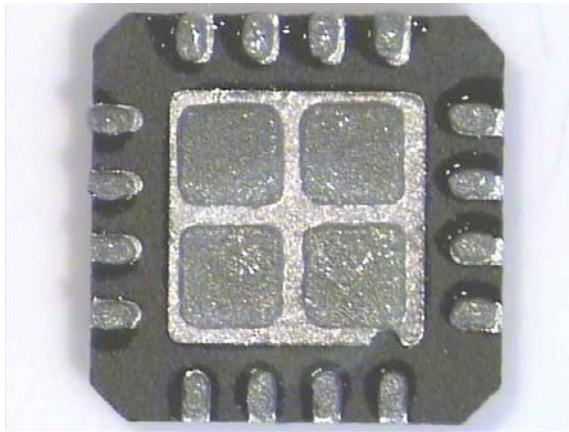


5mil Stencil Results

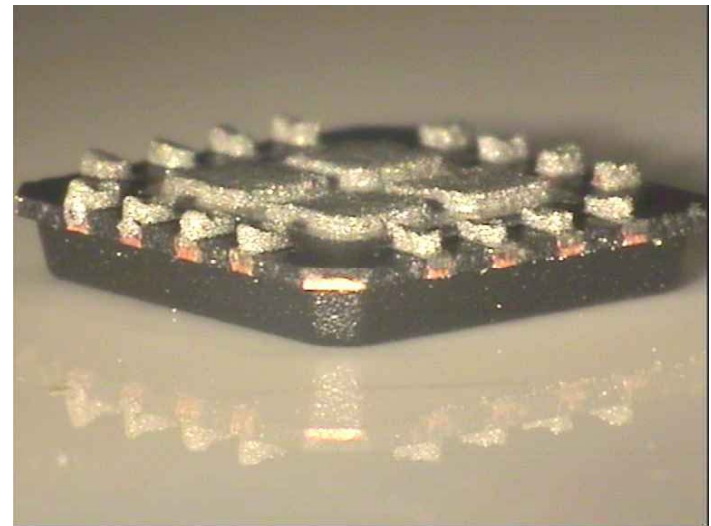


## Rework Practices (6)

- 6mil stencil ALSO produced excessive paste volumes for small 5mm, 3mm QFN's
- Part "swimming"



6mil Stencil Results





## Conclusions – QFN Lead Free Rework

- Pb Free = Higher Temperatures = smaller process window.
- Process Control = Thermal management includes Temperature & Airflow.  
(JEDEC std. can be achieved)
- QFN size&mass means strict airflow control and high placement accuracy.
- Reduced “self alignment” during reflow.  
Placement accuracy more important (ever increasing miniaturization).

## More Conclusions – QFN Lead Free Rework

- Hands free/machine assisted component handling reduces rework time and increases yield.
- Stencil printing process is KEY to high yield QFN rework.
- System optics help with stencil inspection and paste volume inspection.
- Follow Component supplier specifications.
- Nitrogen helps process window. Long term reliability improved.

THANKS FOR ATTENDING  
IPC Midwest!

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