Cost Comparison of Complex PCB fabrication Using Traditional Sequential Lamination Methods versus Interconnect with Conductive Paste

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Abstract
As feature sizes are driven to be smaller, the cost of PCB fabrication is driven higher. In particular, sequential lamination of complex circuit boards is a time consuming and expensive process. However, industry expectations are for smaller, faster, and cheaper products. In this paper, we present an alternative to sequential lamination for fabricating complex PCBs, where conductive paste is used as interconnect between cores. All costs associated with traditional methods and interconnect using conductive paste will be analyzed.

Introduction
Printed circuit board design and construction is meeting integrated circuit packaging requirements through any-layer interconnection schemes using combinations of copper-plated-microvias and paste-filled interconnects in stacked and offset configurations. Used independently, both copper-plated and paste-filled interconnects have advantages for specific types of product structures, but when combined, the resulting design and manufacturing flexibility provide a path to bridge the divide between the integrated circuit and motherboard packaging requirements.

Applications for high-layer count, complex RF design, high-density-interconnect and rigid-flex combinations are already manufactured in high volume, but the continuous demand is for smaller, lighter, thinner and lower-power-consumption products. The industry is struggling with the complexity of mixed-mode, multiple-process-step manufacturing and cost down targets. Paste-filled interconnects allow for the joining of mode-specific cores (e.g. flex) or sub- assemblies in single- or multiple-laminations. This allows each mode-specific core or subassembly to be manufactured cost-effectively to best-practices for that particular mode, and then joined into an integrated whole. This has the potential to significantly reduce time-to-market and manufacturing cost, and can enable assembly by breaking these complex structures into simpler mode-specific subunits that can be electrically interconnected at the end with paste-filled vias. It is conceivable that these products could be manufactured at above a ninety nine percent yield.

The demand for rigid-flex products is increasing. Due to the imbalance in the mechanical characteristics (such as coefficient of thermal expansion) of base materials with conventional methods, these products are complex and cumbersome. If a Z-interconnect scheme is employed, the rigid and flex subassemblies can be manufactured separately under their respective best-mode manufacturing techniques and then joined with a bonding layer containing paste-filled interconnects at high Tg FR4 temperatures (~180ºC). This same type of construction scheme can also enable the combination of multiple signal speed channels into a single construction. For another example, it would also allow for the high-density portion of a circuit to be miniaturized, manufactured as an independent subassembly and then joined to the main portion of the circuit board so that the whole fits within the tight physical limits desired for a specific product.

High-density-interconnect with anywhere, any-layer interconnects is the core technology that enables the miniaturization required for the feature-packed smartphone market segment. As designs approach the need to have five or more outer build-up layers containing stacked copper-plated microvias, fabricators seek relief from the repetitive lamination steps to save time, energy and water resources and to maintain yield. By breaking the outer layers into subassemblies and using paste-filled interconnect bonding layers to join them to the core construction, the number of lamination cycles can be reduced and yields substantially improved. This manufacturing strategy produces more products in less time within the same manufacturing space. Making HDI layers with state of the art conventional practices and then joining them to the core with paste-filled interconnect bonding layers provides design freedom to the client, excellent electrical properties for the device and higher yields with a reduced number of lamination cycles to the fabricator.

Every layer interconnection (ELIC) and subassembly core to core interconnects are delivering:

- Tighter wring densities
- Improved performance through shorter traces
- Separation of low and high speed signal channels
- Ability to join different materials in optimum press cycles
- A framework for embedded components

These assembly advantages, coupled with proper design, offer cost advantages when products are built in large-scale production or in low volume, high mix assembly lines. It is the intent of this paper to outline the costs associated with manufacturing ELIC structures employing a Z-interconnect paste technology. Two example designs were chosen to analyze the cost of using this technology versus conventional interconnect. The first case is a small 10 layer board similar to most smart phone motherboards. The second case is a large 28 layer circuit board similar to those found in servers.

Activity Based Cost Modeling

Activity based cost modeling and parametric cost modeling are the two dominant cost modeling methods. Parametric cost modeling is done by statistically analyzing a large number of actual results and creating a model that matches as closely as possible. This "black box" approach, as an extrapolation based on historical data, is only appropriate for modeling processes that change slowly over time or cannot be decomposed into individual activities.

For reliable and dynamic trade-offs, activity based cost modeling is the most accurate cost modeling method because individual activities are characterized and analyzed. The total cost of any manufacturing process is calculated by dividing the process into a series of activities and totaling the cost of each activity. The cost of each activity is determined by analyzing the following attributes:

- The time required to complete the activity
- The amount of labor dedicated to the activity
- The cost of material required to perform that activity—both consumable and permanent material
- Any tooling cost
- The depreciation cost of the equipment required to perform the activity
- The yield loss associated with the activity

Activity based cost modeling is also well suited to comparing different technologies and manufacturing processes. The total cost of a product can be divided into the following three categories:

- Direct manufacturing cost
- Allocated factory overhead
- Profit margin

The direct manufacturing cost is easy to quantify and reasonably consistent across the industry. However, factory overhead and profit margin vary significantly between different manufacturing sites and companies. By using activity based cost modeling, the specific differences in manufacturing cost can be determined by comparing the direct manufacturing costs. This "relative" cost modeling makes it much easier to understand the cost impacts—good or bad—of design decisions and technology tradeoffs.

The graph in Figure 1 shows a partial example of an activity based cost graph for a high density interconnect (HDI) PCB substrate. Each activity contributes cost in at least one of the six categories shown. These categories are represented by the colored bars, and the running total is the line on the graph. The example shows the first series of activities in the fabrication process.

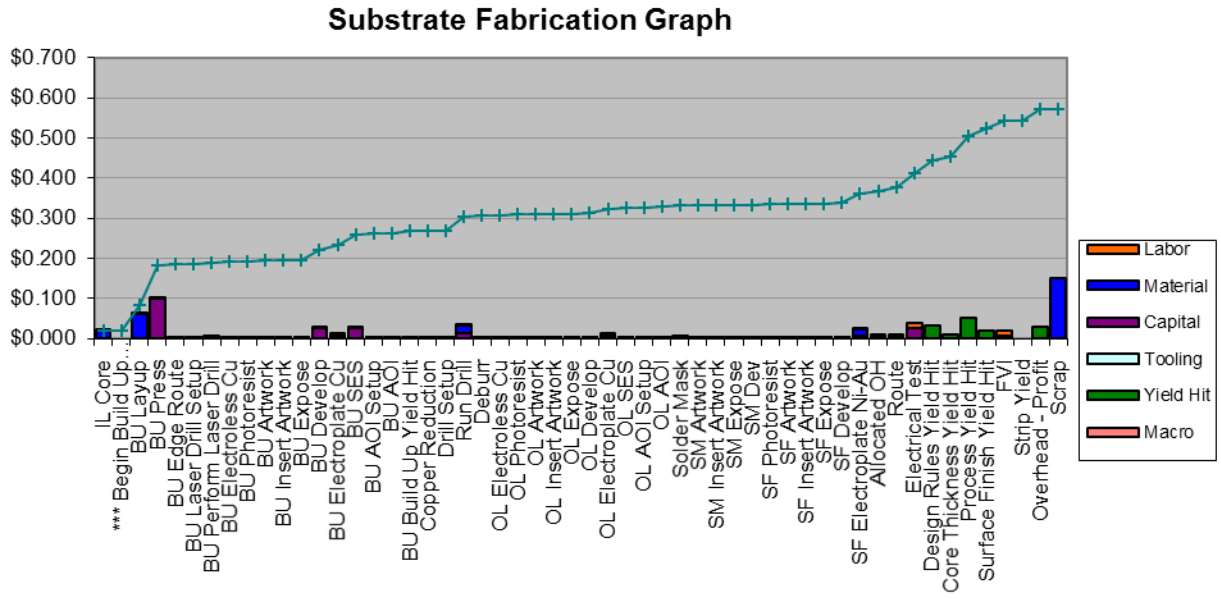


Figure 1. Example of Activity Based Cost Modeling

The inner layer core and HDI buildup activities contribute significant material costs, as shown by the blue bars for those two steps. Any type of via drilling—either laser or mechanical—will contribute capital costs since the throughput per panel is usually low. Many of the other activities contribute labor and equipment depreciation costs, as shown by the orange and purple bars.

Conductive Paste Interconnect

Conductive pastes are commonly used to make electronic interconnects and printed circuits. They come in several variations, ranging from Nano silver to epoxy-based metal fillers. They serve several markets and have been used in commercial and high reliability applications. Most are air-cured formulations and may display a wide discrepancy in electrical resistance.

Conductive paste can be used in printed circuit board fabrication as an alternative to copper plated vias. The conductive paste vias are created by laser drilling holes in a prepreg layer. A screen printing process is used to fill these holes with conductive paste and then the panel is heated and cured to sinter the paste. At this point, the core with the conductive paste vias (Z-interconnect layer) can be included in the normal PCB layup and press lamination process.

Sintering is a process in which adjacent surfaces of metal powder particles are bonded by heating. Liquid phase sintering is a special form of sintering during which solid powder particles coexist with a liquid phase. Densification and homogenization of the mixture occur as the metals diffuse into one another and form new alloys and/or intermetallic species.

In Transient Liquid Phase Sintering (TLPS), compositions comprising powder metallurgy, a relatively low melting point (LMP) alloy and a relatively high melting point (HMP) metal are mixed in particulate form. At least one element within the alloy is either highly soluble in, or is reactive with, the receptive HMP metal. As the temperature is raised to the melting point of the LMP alloy, the alloy particles become molten. This transition can be observed as an endothermic event in differential scanning calorimetry (DSC). The reactive elements within the relatively low melting point alloy then react with the receptive high melting point metal to form new alloy compositions and/or intermetallic compounds. The formation of intermetallic species may be observed as an exothermic event using DSC. Thus, the typical TLPS DSC “signature” is an endotherm followed by an exothermic phase. The diffusion and reaction of the reactive elements from the LMP alloy and the receptive HMP metal continues until one of the reactants is fully depleted, there is no longer a molten phase at the process temperature, or the reaction is quenched by cooling. After cooling, subsequent temperature excursions (even beyond the original LMP alloy melt temperature) do not reproduce the original melt signature of the mixture. This is the “signature” of a typical low temperature transient liquid phase sintered metal mixture.

Cost Modeling Results

As part of this project, the total costs of the following two scenarios were analyzed using proprietary activity based cost modeling software described in the previous section.

Case 1 – Mobile phone board

This printed circuit board uses a 10 layer high density interconnect (HDI) structure. The board is 2 inches by 2.5 inches, and is similar in size and complexity to a smart phone motherboard. Using traditional HDI fabrication, this board would be a 4-2-4 structure—a 2 layer core with four sequential buildup layers on the top and bottom. Using the proprietary Z-interconnect technology, this board could be constructed using 5 cores and 4 Z-interconnect layers. The cross section of each option is shown in Figure 2 below.

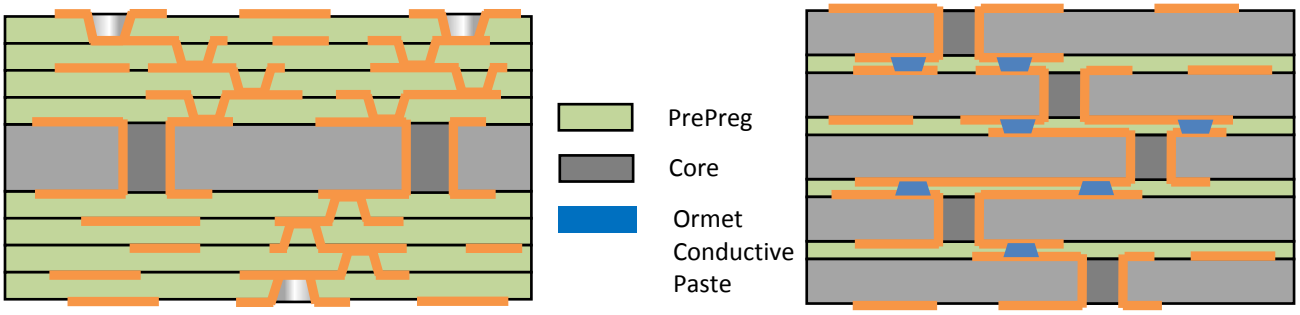


Figure 2. Cross section of a 4-2-4 board and a 5 core Z-interconnect board

The traditional HDI board is built by starting with a copper clad laminate core. The copper on this core is patterned on both sides, and through holes are drilled for the core vias. These through holes are plated to complete the core processing. Then, four HDI build up processes are done, including lamination, laser drilling of the vias, imaging, and electroplating. These processes are done sequentially, and the board is completed with a surface finish and solder mask process.

The 5 core Z-interconnect process uses five cores instead of one. Each core is fabricated using the same process as the core in the traditional HDI structure. However, instead of insulating each core using a solid sheet of prepreg, this prepreg is laminated and laser drilled to create core to core vias. These vias are filled with conductive paste to complete the core to core interconnect.

4-2-4 Build Up Case	Cost
Core	$0.454
Build Up layer 1	$0.479
Build Up layer 2	$0.479
Build Up layer 3	$0.479
Build Up layer 4	$0.479
Final Processing	$1.024
Scrap	$1.674
Total 4-2-4 Cost	**$5.060**

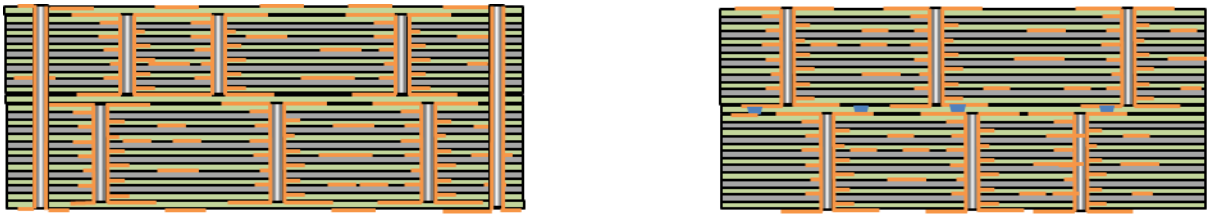
Z-Interconnect Case	Cost
Core 1	$0.454
Core 2	$0.454
Core 3	$0.454
Core 4	$0.454
Core 5	$0.454
Z-Interconnect 1	$0.312
Z-Interconnect 2	$0.312
Z-Interconnect 3	$0.312
Z-Interconnect 4	$0.312
Layup	$0.095
Final Processing	$1.024
Scrap	$0.406
Total Z-Interconnect Cost	**$5.043**

Figure 3. Cost Modeling Results

Figure 3 shows the total cost of both options. The Z-Interconnect option is slightly less expensive, primarily due to the higher fabrication yields. For traditional HDI, each buildup layer introduces a cumulative yield loss that is combined with any prior yield losses. Conversely, each core in the Z-Interconnect case is processed in parallel instead of sequentially. Each core is thus tested in parallel instead of sequentially as well. Furthermore, the process to create the Z-Interconnect interconnect is a high yield process since it only involves laser drilling through a prepreg screen printing of conductive paste.

Case 2 – Large 28 layer server board

In this case, a 28 layer board is constructed using two cores made up of either 12 layers or 14 layers. The board is 15 inches by 20 inches (one board per panel) and 140 mils thick. All vias are 12 mil holes, and each core has a 90% yield. Using traditional PCB technology, the cores would be connected to each other using plated through hole (PTH) vias that extend all the way through both cores. However, another option is to use a Z-interconnect layer between the two cores to provide core to core connections. The cross sections of these two scenarios are shown in Figure 4.



28 Layers – Two cores connected with PTH

28 Layers – Two cores connected with one Z-interconnect layer

Figure 4. Two cores connected with PTH Versus a Z-Interconnect layer

The following key cost and yield assumptions were used for this comparison.

- Each core can be 100% tested in the Z-interconnect case, but only 50% tested in the PTH case – The yield of the cores is the same for both cases, but since all the core to core interconnect is done through the Z-interconnect layer in the second case, the nets are all accessible for testing prior to lamination. However, when the core to core interconnect is done using PTH vias, all the nets are not routed to the surface. These nets cannot be tested until after final lamination.
- Outer layer PTH drilling has a 10% yield loss – One of the major factors for PTH drilling yield loss is the aspect ratio of the vias. In this case, that aspect ratio is 11.67 (140 mil thick board and 12 mil PTH vias). That is a very high aspect ratio and could result in significant yield loss. In many cases, this yield loss can be minimized by using larger vias for the outer layer interconnect. However, larger vias consume more board area, which may not be available in all cases.

The table in Figure 5 shows the cost of the Z-interconnect case to be lower than the conventional case based on the assumptions presented above.

28 Layer – PTH Interconnect	Cost
12 layer core	$81.78
12 layer core scrap before lamination	$4.42
14 layer core	$95.75
14 layer core scrap before lamination	$5.75
Outer layer and final processing	$64.41
Final scrap	$81.85
Total Cost	**$333.96**

28 Layer - Z-interconnect layer	Cost
14 layer core	$95.75
14 layer core scrap before lamination	$9.47
14 layer core	$95.75
14 layer core scrap before lamination	$9.47
Z-Interconnect between the cores	$40.77
Final Processing	$44.62
Final scrap	$32.84
Total Cost	**$328.67**

Figure 5. Cost Comparison of PTH Interconnect and Z-Interconnect Interconnect

In both cases above, the cost of fabricating the cores is the same. A 14 layer core is assumed to cost $95.75 before any test and scrap, and the cost of a 12 layer core is $81.78. For the PTH via interconnect case, the construction of the final board is done using two outer layers combined with a 12 layer core and a 14 layer core. One of the first differences apparent in the cost comparison is the difference in scrap cost before lamination. As described in the assumptions, one advantage of using the Z-interconnect layer to interconnect the core is the fact that all nets in the core are accessible for testing before final lamination. In the PTH case, many nets are not routed to the surface of the core and are therefore not available for testing until final lamination. This means there is less scrap before lamination, but there are undetected defects still in the cores that will cause additional scrap at the end of the process.

The other major difference in cost is the final scrap, which is due to a lower final yield in the PTH case. The lower final yield is due to residual defects in the core and high aspect ratio outer layer drilling yield loss.

Summary

The use of a Z-interconnect layer with conductive paste vias is a cost effective alternative to copper plated microvias. The two cases analyzed showed that the addition of Z-Interconnect layers can be used to reduce total product cost. In both cases, this cost reduction was achieved through a variety of yield improvements as summarized below.

- When using Z-interconnect layers with conductive paste instead of copper plated microvias (case 1), the need for sequential buildup layers is eliminated. The example in this paper is a 4-2-4 structure requiring four sequential lamination cycles compared to a single lamination cycle using Z-interconnect layers between 5 cores. Sequential lamination can cause significant yield loss; avoiding it improves the final yield.
- When using Z-interconnect layers with conductive paste instead PTH vias (case 2), the final yield is improved by allowing more complete core testing before lamination and avoiding the need for high aspect ratio, low yield outer layer through hole drilling.

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Agenda

- Introduction
- High Density Interconnect
- Conductive Paste Interconnect
  - Using Transient Liquid Phase Sintering Technology
- Cost & Yield Comparison of Two Scenarios
- Summary

Introduction

- PCB fabrication cost is increasing as feature sizes are driven smaller
- Sequential lamination is a time consuming and expensive step
- Alternative to sequential lamination is presented
  - Conductive paste used as interconnect between cores
  - Cost and yield of traditional methods and conductive paste methods analyzed
  - Two example designs:
    - Small, 10 layer board (similar to most smartphone motherboards)
    - Large, 28 layer circuit board (similar to those found in servers)

High Density Interconnect (HDI)

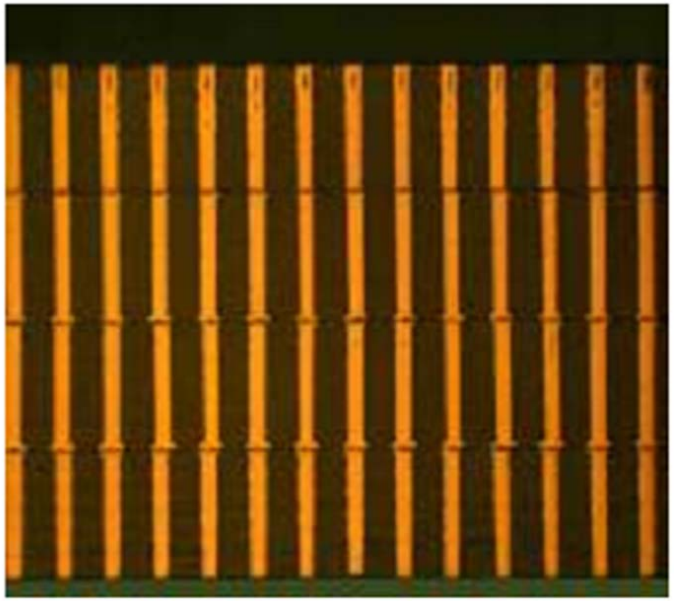
- Copper-plated-microvias and paste-filled interconnect both being used in PCB design and construction
  - Each method currently has advantages for different products
- Applications for high-layer count, complex RF design, HDI and rigid-flex already in HVM
  - Industry driving these to be smaller, lighter, thinner, and consume less power
- Some current HDI designs need to have five or more outer build-up layers containing stacked copper-plated microvias
  - Repetitive lamination steps consume time, energy, and water resources
  - Costly to maintain yield

Conductive Paste Interconnect

- Accomplished with Transient Liquid Phase Sintering Technology
- Every layer interconnection (ELIC) and subassembly core-to-core interconnects deliver:
  - Tighter wring densities
  - Improved performance through shorter traces
  - Separation of low and high speed signal channels
  - Ability to join different materials in optimum press cycles
  - A framework for embedded components
- Allows for the joining of mode-specific cores (e.g. flex) or sub-assemblies in single or multiple laminations

Features of PCBs with Core-to-Core Interconnects

- Break up high aspect ratio through holes
- Cores processed in parallel
- RoHS robust (reliable through lead-free reflow)
- Continuous metal joint – alloys to pads
- Substantially reduces plating time for high throughput
- High yields



Source: DDI

Transient Liquid Phase Sintering: Technology Highlights

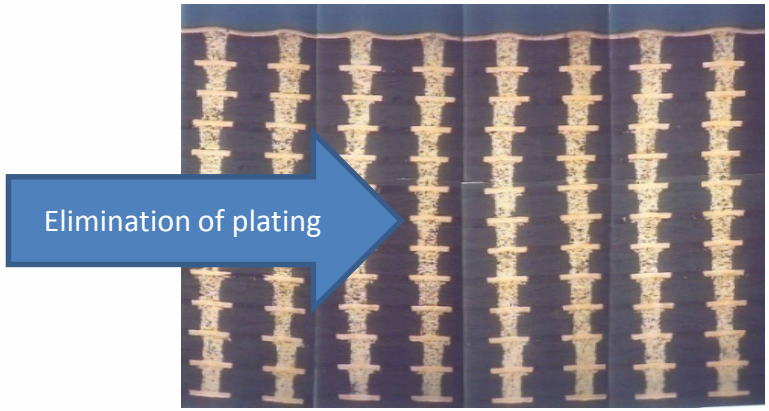
- Low temperature metallic joining to copper catch pads
  - Cures with pre-preg lamination at 175-205C
- Will not re-melt when exposed to Pb-free solder reflow profiles
  - Thermally stable up to 280C
- Superior shear strength versus metal filled polymers at elevated temperatures
  - Metallic joining is stronger than adhesive bonding
- Pb-free & Halogen-free composition
  - Environmentally friendly alternative to plating

Lower Cost, Increased Throughput

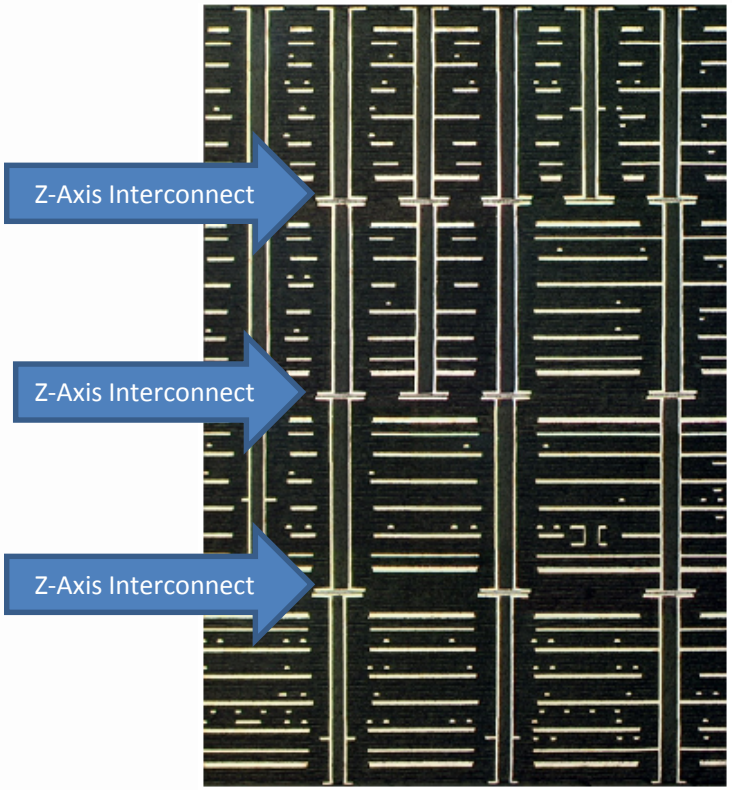
- Transient Liquid Phase Sintering materials enable:
  - Single lamination process replaces sequential plating in high density PCB applications
  - High yield plating steps done in parallel → Increases throughput without increasing capital
- Fewer sequential steps reduces yield loss and lead time
- High reliability performance and lower overall fabrication costs

Fabrication of Advanced Technology PCBs

- Sintering pastes enable low cost, high performance PCB structures.
- Z-axis interconnection
  - High layer count boards for RF, servers, telecom
  - High density applications for mobile electronics



Source: DDI Corp.

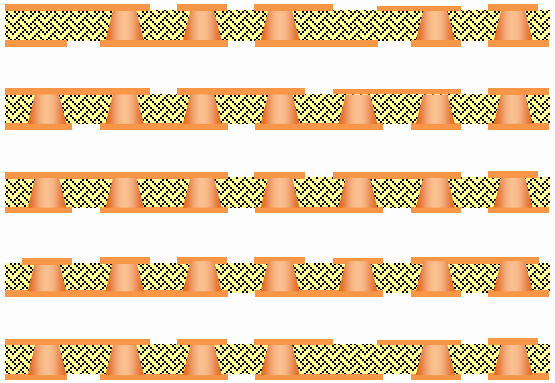


Source: Endicott Interconnect Technologies

Example Process Flow

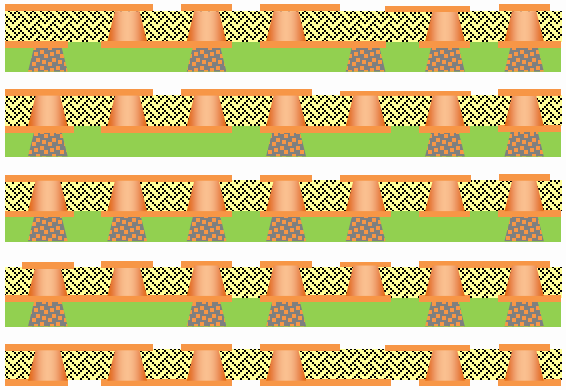
Parallel fabrication process leverages existing infrastructure to increase throughput and lower cost.

Step 1



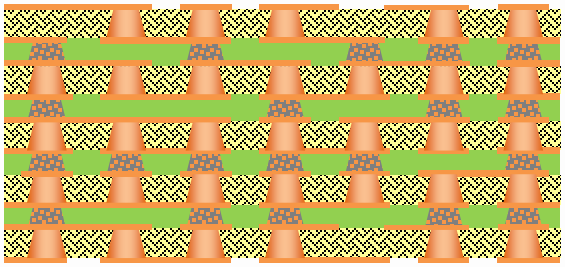
1. Convert existing 10 layer designs into five 2-layer PCBs
2. Use market competition and/or internal capacity to obtain 2-layer 'cores'

Step 2



3. Inspect the 2 layer 'cores' to ensure high yield
4. Use sintering paste + pre-preg to interconnect the 2-layer boards into the 10 layer final PCB

Step 3



5. Single lamination process reduces cycle time and ensures no sequential yield loss

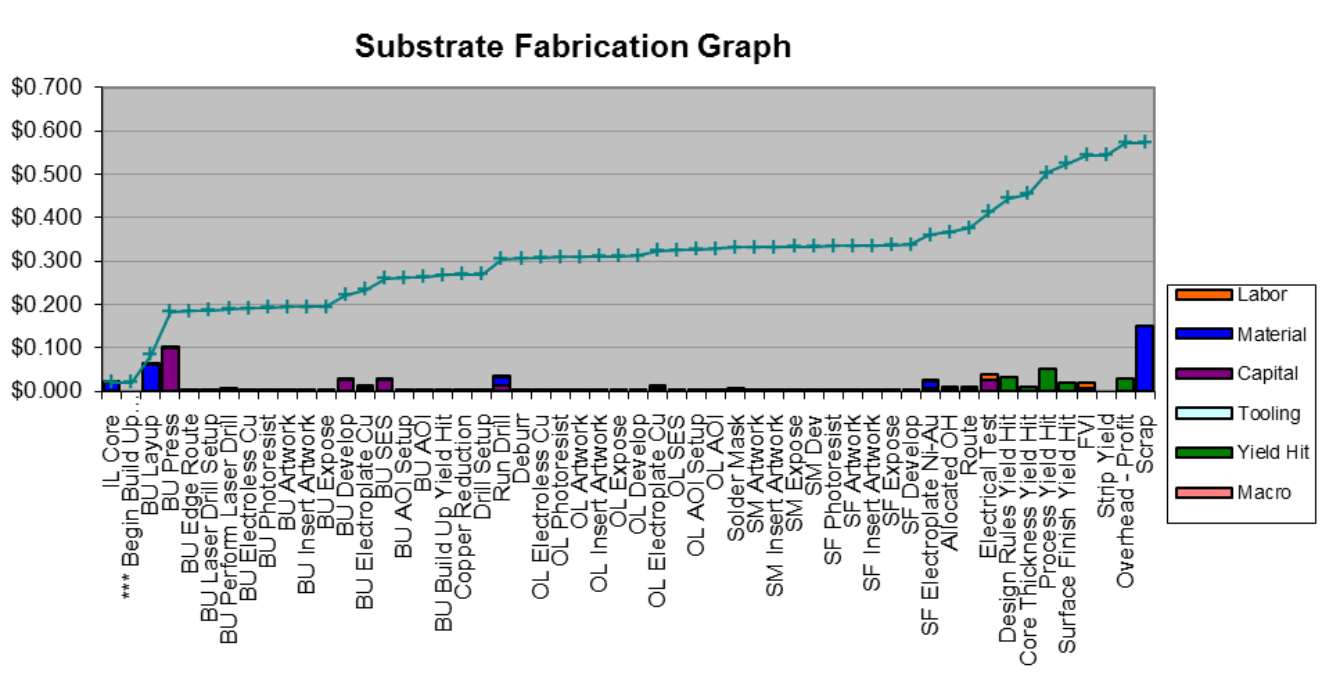
Activity Based Cost Modeling

- Cost Components of each Activity
  - The time required to complete the activity
  - The amount of labor dedicated to the activity
  - The cost of material required to perform that activity – both consumable and permanent material
  - Any tooling cost
  - The depreciation cost of the equipment required to perform the activity
  - The yield loss associated with the activity
- Sample Output

Substrate	Labor	Material	Capital	Tooling	Yield	Macro	Running Total
2-[IL-Core]	$0.0007	$0.2000	$0.0007	$0.0000	$0.0000	$0.0000	$0.2014
3-[IL-Photoresist]	$0.0007	$0.0120	$0.0011	$0.0000	$0.0000	$0.0000	$0.2152
4-[IL - Image]	$0.0007	$0.0144	$0.0045	$0.0000	$0.0000	$0.0000	$0.2349
5-[IL-DES]	$0.0009	$0.0072	$0.0088	$0.0000	$0.0000	$0.0000	$0.2517
6-[IL - Oxide]	$0.0010	$0.0001	$0.0026	$0.0000	$0.0000	$0.0000	$0.2554
7-[IL-AOI]-[Setup]	$0.0001	$0.0000	$0.0006	$0.0000	$0.0000	$0.0000	$0.2561
7-[IL-AOI]-[Test]	$0.0025	$0.0000	$0.0099	$0.0000	$0.0000	$0.0000	$0.2686

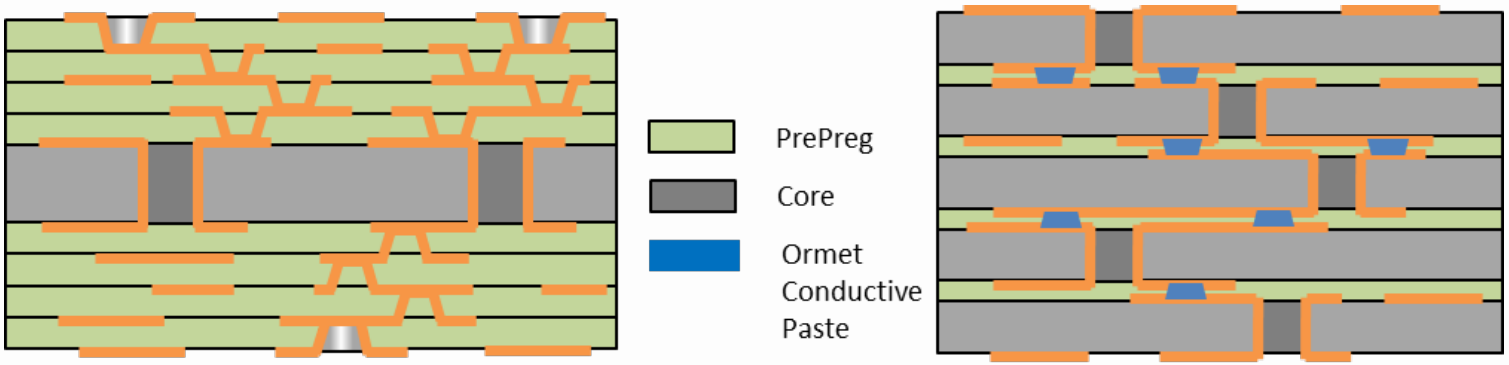
Sample Cost Detail Graph

- Sample graph shows first set of activities in fabrication
  - Inner layer core and HDI buildup contribute significant material costs
    - Shown by blue bars
  - Any type of via drilling will contribute capital costs due to low throughput
  - Many activities contribute labor and equipment depreciation costs
    - Shown by orange and purple bars



Cost Comparison – Scenario 1

- Mobile phone board
  - 10 layer HDI structure
  - 2in by 2.5in
  - Similar in size and complexity to a smart phone motherboard
  - Using traditional HDI fabrication, this board would be a 4-2-4 structure: a 2 layer core with four sequential buildup layers on the top and bottom
  - Using Ormet Z-interconnect technology, this board could be constructed using 5 cores and 4 Z-interconnect layers

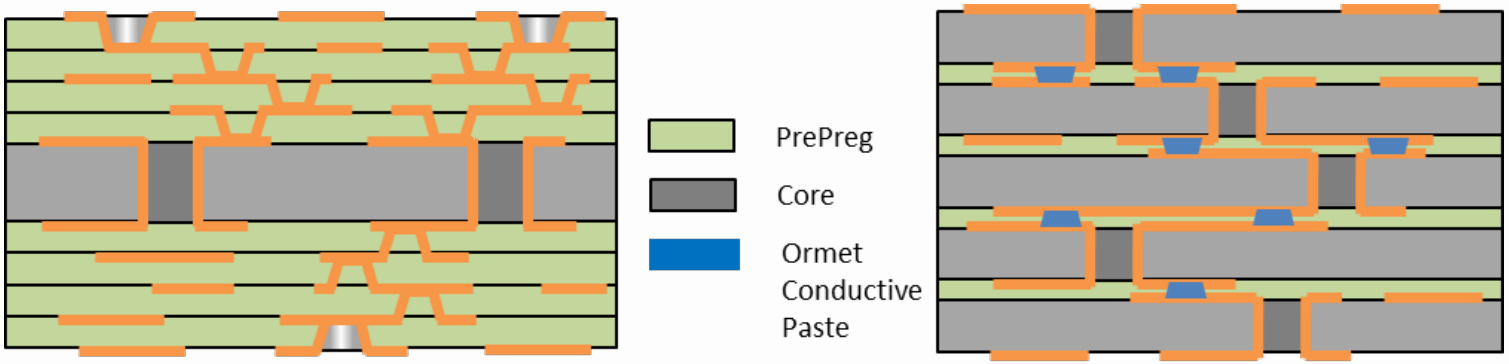


4-2-4 HDI Structure

5 Core Ormet Z-interconnect Structure

Cost Comparison – Scenario 1

- Traditional HDI board
  - Cu clad laminate core, patterned on both sides; through holes are drilled and plated for core vias
  - Four HDI build up processes are done sequentially
  - Board completed with surface finish and solder mask
- 5 core Ormet Z-interconnect process
  - Five cores: each fabricated with the same process as above
  - Instead of insulating each with a solid sheet of prepreg, prepreg is laminated and laser drilled to create core to core vias, which are filled with conductive paste



4-2-4 HDI Structure

5 Core Ormet Z-interconnect Structure

Cost Comparison – Scenario 1

- Ormet case slightly less expensive, due to higher fabrication yields
  - For traditional HDI, each buildup layer introduces a cumulative yield loss
  - Each core in Ormet case is processed and tested in parallel, not sequentially
  - Process to create the Z-Interconnect interconnect is high yield—only involves laser drilling through a prepreg screen printing of conductive paste.

4-2-4 Build Up Case	Cost
Core	$0.454
Build Up layer 1	$0.479
Build Up layer 2	$0.479
Build Up layer 3	$0.479
Build Up layer 4	$0.479
Final Processing	$1.024
Scrap	$1.674
Total 4-2-4 Cost	$5.060

Ormet Case	Cost
Core 1	$0.454
Core 2	$0.454
Core 3	$0.454
Core 4	$0.454
Core 5	$0.454
Ormet Z-Interconnect 1	$0.312
Ormet Z-Interconnect 2	$0.312
Ormet Z-Interconnect 3	$0.312
Ormet Z-Interconnect 4	$0.312
Layup	$0.095
Final Processing	$1.024
Scrap	$0.406
Total Ormet Cost	$5.043

Cost Comparison – Scenario 2

- Server board
  - 28 layer board (two cores of either 12 or 14 layers)
  - 15in x 20in (one board per panel), 140 mils thick; all vias are 12 mil holes
  - Each core has a 90% yield
  - Using traditional PCB technology, cores would be connected with plated through hole (PTH) vias
  - Alternatively, use an Ormet Z-interconnect layer between the two cores to provide core to core connections

28 Layers – Two cores connected with PTH

28 Layers – Two cores connected with one Ormet Z-interconnect layer

Cost Comparison – Scenario 2

- Cost and yield assumptions used for cost modeling:
  - Each core can be 100% tested in the Ormet Z-interconnect case, but only 50% tested in the PTH case
  - Outer layer PTH drilling has 10% yield loss
    - One of the major factors for PTH drilling yield loss is the aspect ratio of the vias (in this case, 11.67)
    - Yield loss can be minimized by using larger vias for outer layer interconnect—this consumes more board area, and may not always be an applicable option

28 Layers – Two cores connected with PTH

28 Layers – Two cores connected with one Ormet Z-interconnect layer

Cost Comparison – Scenario 2

- In both cases, cost of fabricating the cores is the same
- Scrap cost before lamination is one cost difference
  - One advantage of Ormet Z-interconnect technology is accessibility to all nets, for testing prior to final lamination; in PTH case, many nets are not routed to the surface and not available for testing
  - Less scrap before lamination, but undetected defects cause scrap at the end of the process
- Final scrap also a cost contributor
  - Lower final yield in the PTH case, due to residual defects in the core and outer layer drilling yield loss

28 Layer – PTH Interconnect	Cost
12 layer core	$81.78
12 layer core scrap before lamination	$4.42
14 layer core	$95.75
14 layer core scrap before lamination	$5.75
Outer layer and final processing	$64.41
Final scrap	$81.85
Total Cost	$333.96

28 Layer - Ormet Z-interconnect layer	Cost
14 layer core	$95.75
14 layer core scrap before lamination	$9.47
14 layer core	$95.75
14 layer core scrap before lamination	$9.47
Ormet Z-Interconnect between cores	$40.77
Final Processing	$44.62
Final scrap	$32.84
Total Cost	$328.67

Sintering Pastes Improve Throughput

- A time-based model for manufacturing a 10 layer Smartphone has been developed.
  - Prismark: market research firm provided baseline time data
  - 4 processes modeled for 10 layer PCB
    - 4-2-4 Stack-up Plating
    - 3 Sintering paste processes

	Key Process Steps				Minimum
	PTH	Microvia	Lam.	Ormet	Cycle Time
n-m-n Plating	2	4	4	0	107 hrs
Process #1	5	0	1	4	37 hrs
Process #2	0	0	6	8	53 hrs
Process #3	0	0	1	9	28 hrs

Sintering pastes offer cycle time reduction,
and the opportunity to reduce or eliminate plating

Future Work

- Cost + time Benefits
  - Cost is measured in this presentation
  - Value to shorter manufacturing cycles
    - Beneficiaries: Client, OEM, Fabricator
- Expand cost tradeoff analysis to a 14 layer HDI case
  - Compare cost of 6-2-6 to a variety of core combinations – 2 cores up through 7 cores.
- Expand cost tradeoff analysis to very high layer count boards (75+ layers)
  - Analyze how many cores and optimum layer count for each

Summary

- Use of a Z-interconnect layer with conductive paste vias is a cost effective alternative to copper plated microvias
  - Two cases analyzed show a reduction in total product cost, primarily archived through yield improvements
- Yield improvements from Z-interconnect
  - When using Z-interconnect layers with conductive paste instead of copper plated microvias (scenario 1), the need for sequential buildup layers is eliminated
    - Sequential lamination can cause significant yield loss; avoiding it improves final yield
  - When using Z-interconnect layers with conductive paste instead PTH vias (scenario 2), final yield is improved by:
    - Allowing more complete core testing before lamination
    - Avoiding the need for high aspect ratio, low yield outer layer through hole drilling