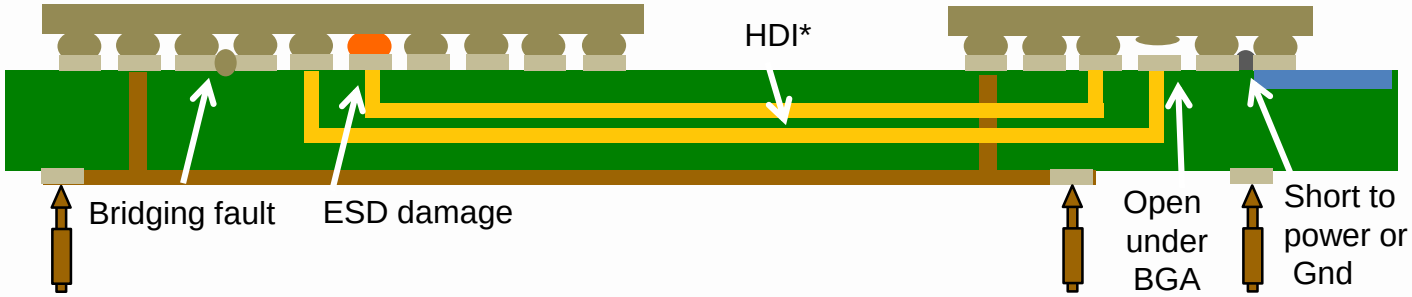
APEX EXPO IPC
NEW IDEAS ... FOR NEW HORIZONS
MARCH 25-27, 2014
MANDALAY BAY RESORT AND CONVENTION CENTER
LAS VEGAS, NEVADA

Board-Assist Built-In Self-Test (BA-BIST), Short-Term and Long-Term Strategies for Use Case Standardization

Zoë Conroy, Cisco
Al Crouch, Asset InterTech
iNEMI BIST Project Chairs

About this Presentation

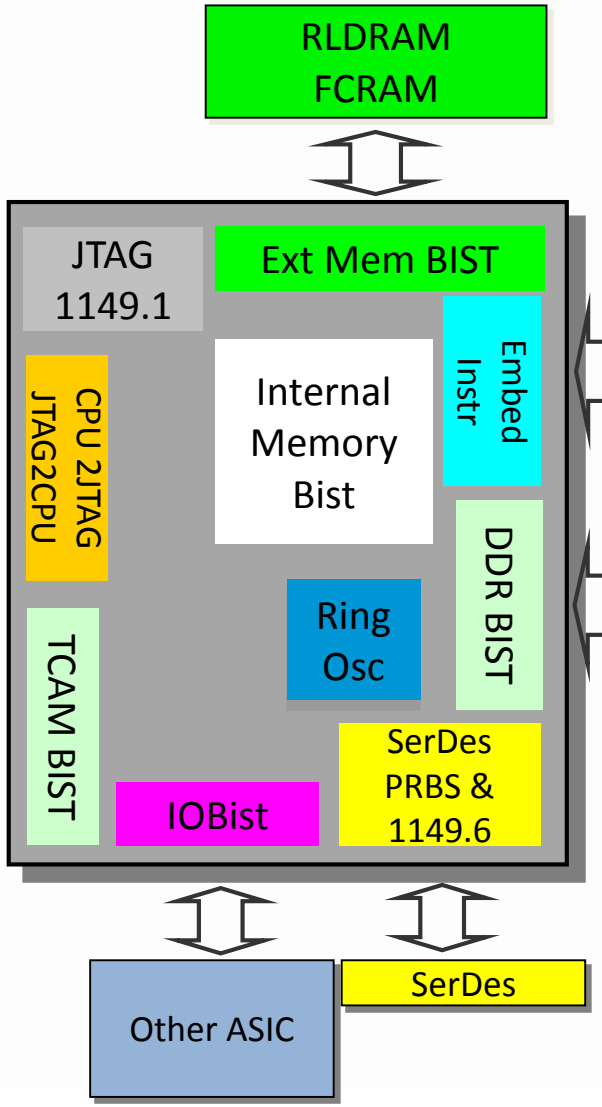
- Board-Assist (BA-BIST) is introduced as enhanced IC BIST functionality for board testability and fault isolation.
- Why is this needed?
  - Increasing chip interface speeds and board integration (HDI*) make traditional board manufacturing test less capable.
- BA-BIST requirements are presented from board test engineers perspective.



* High Density Interconnect

Outline

- The industry gap filled by INEMI's 'BIST Project'.
- Board defects targeted by BA-BIST.
- The most required BISTs.
- Industry '**use-cases**' for Board Test BA-BIST.
- Relation to existing Standards.



Purpose of iNEMI's BIST Project

- Address the diminishing number of board level test points.
- How?….
  - Adapting "chip" level BISTs designed for IC manufacturing
  - Showing how tests and algorithms can be used for board test
  - Develop and promote board/system test adoption of IC BIST.
  - Steer IC providers toward BIST functions helpful for board/system test.
  - Provide BA-BIST use-cases for interfaces and algorithms.
  - Encourage IC and ATE/Instrument vendors to provide products and tools.

Major Contributors

Company	Participants
Agilent	Hui Li, Jun Balangue
Alcatel Lucent	Brad van Treuren
Asset InterTech	Al Crouch
Cisco	Zoë Conroy, Rob Pike
Corelis	Harrison Miles
Dell	Phil Geiger
EMC	Jeffrey Moore
Hewlett Packard	Skip Myers
IBM	Derek Robinson
Intel	James Grealish,
Teradyne	Tony Suto

Industry Surveys on IC BIST Usage

Objectives:

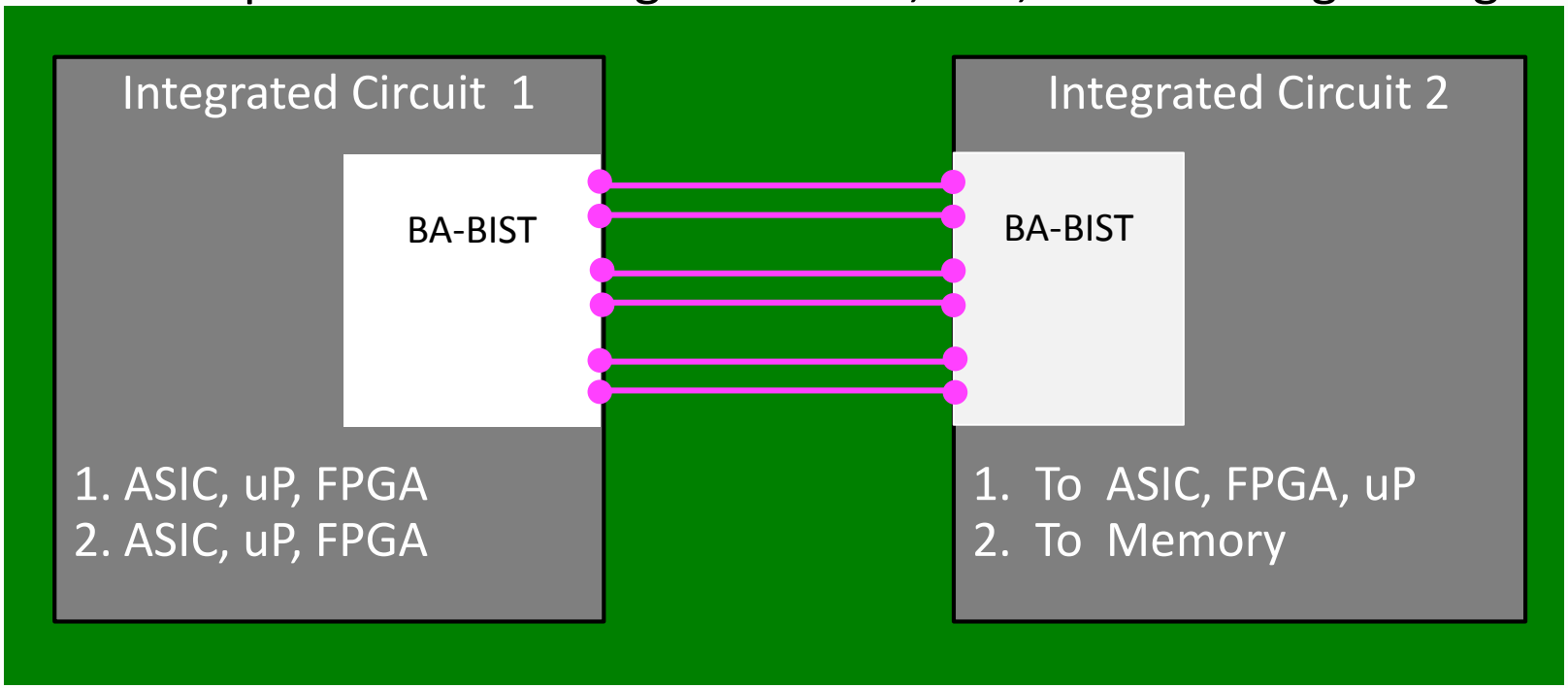
- Gauge how much IC BIST is currently run at board test.
- Evaluate its usefulness.
  - Get board/system test/debug engineers to identify what their problems are and what may be solved with a “BIST function”.
  - Agreement on a board BIST definition.
  - Identify BIST Use Cases for board test standardization.

How did the Industry Respond?

- Many IC BISTs are available and run at board level
  - 60% Board designers are requesting access to IC BIST
- BIST run at the board level is good at catching defects
  - Seen to be critical for future fault isolation
  - Would like BIST coverage to be > 80% at board test
  - Currently run at many different board/system test steps
- Access to BIST is predominantly via IEEE1149.1 TAP
  - > 75% respondents see BIST coupled with boundary-scan replacing lack of test point access.

BA-BIST Requirements

- BA-BIST needs to SOQ-FAM* interconnect between 2 ICs.
- BA-BIST is existing IC BIST, with features/support for board test.
- Test steps: manufacturing board test, NPI, board debug & diagnosis.



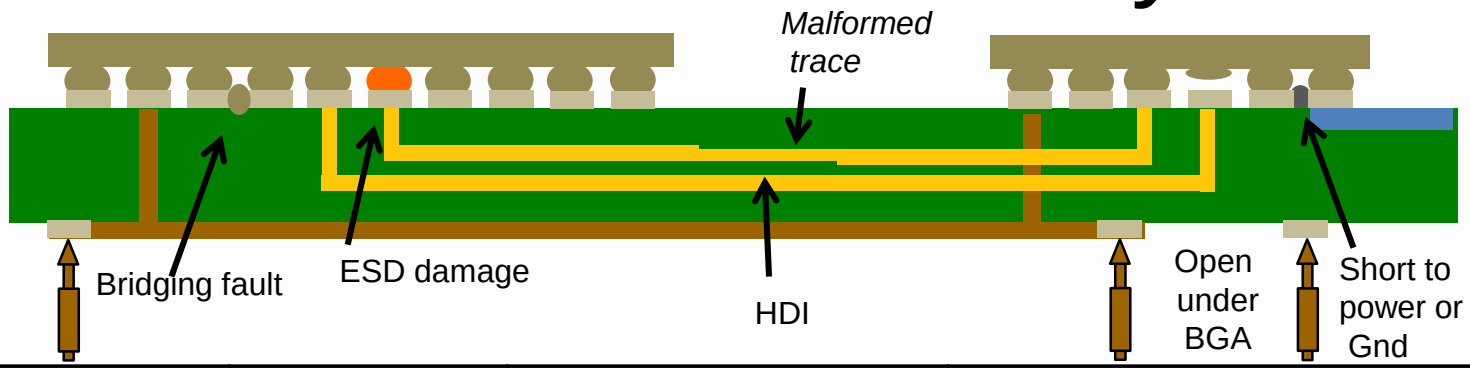
* Shorts, open, quality - function, at-speed, measure

BA-BIST Definition

Board-Assistance BIST *is an embedded capability within an IC that is fully or partially self-contained, and incorporates some or all of the following:*

- *pattern/signal generation,*
- *pattern/signal delivery,*
- *response or data capture,*
- *response evaluation functions.*

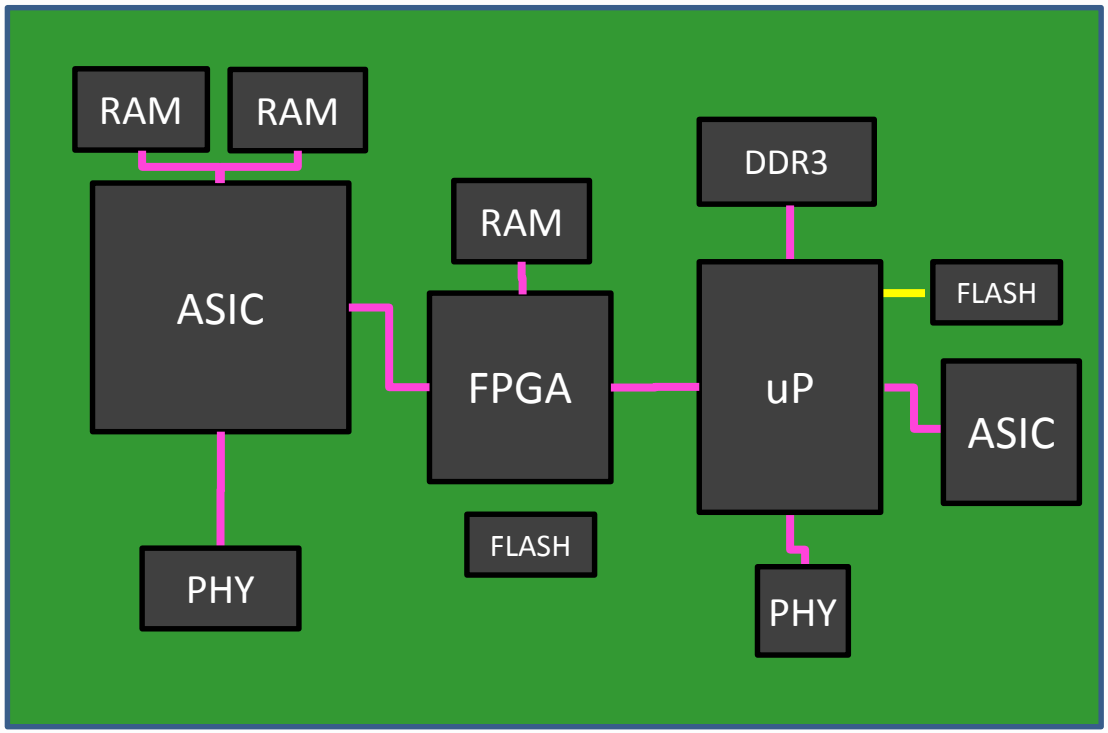
Board Defects covered by BA-BIST



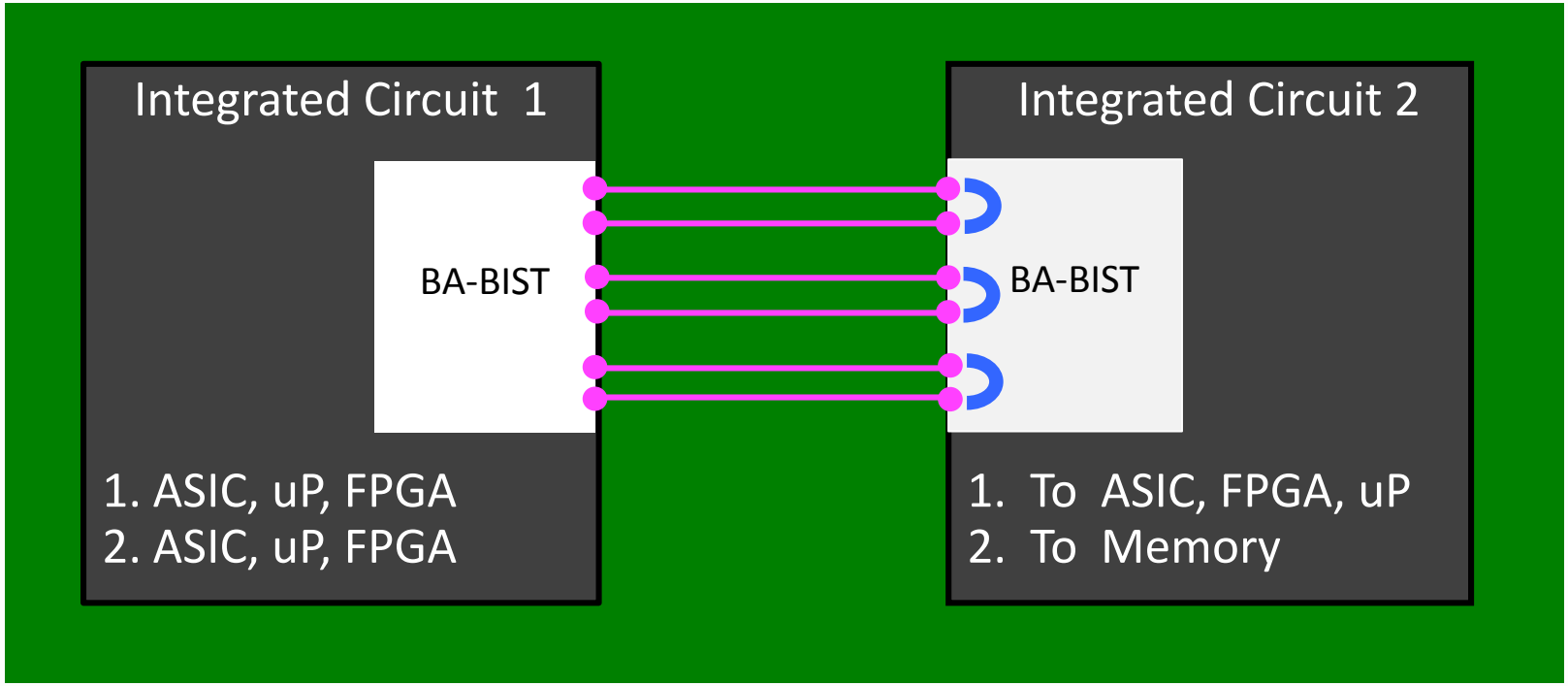
Fault Model Category	Traditional Test Type	Typical Use Environment	Defect Classes	BA-BIST coverage
Trace stuck-at-1,0	ICT, boundary scan	NPI, mfg test, debug, yield	Signal trace shorted/open to power/GND, bridged to signal	yes
Trace transitions randomly	ICT, boundary scan	NPI, mfg test, debug, yield	Broken trace, open trace, undriven open	yes
Trace impedance	ICT, boundary scan	Mfg test	Malformed trace	no
High speed trace specification	At-speed functional	NPI, debug ,yield	Chip drive, malformed trace	yes
Signal integrity	At-speed functional	NPI, debug, yield	Malformed traces	yes

Board Test and Existing ICs

- What can a board test engineer do with existing ICs?
- Many ASICs have BIST already.
- Run at boundary scan or 1st functional test.

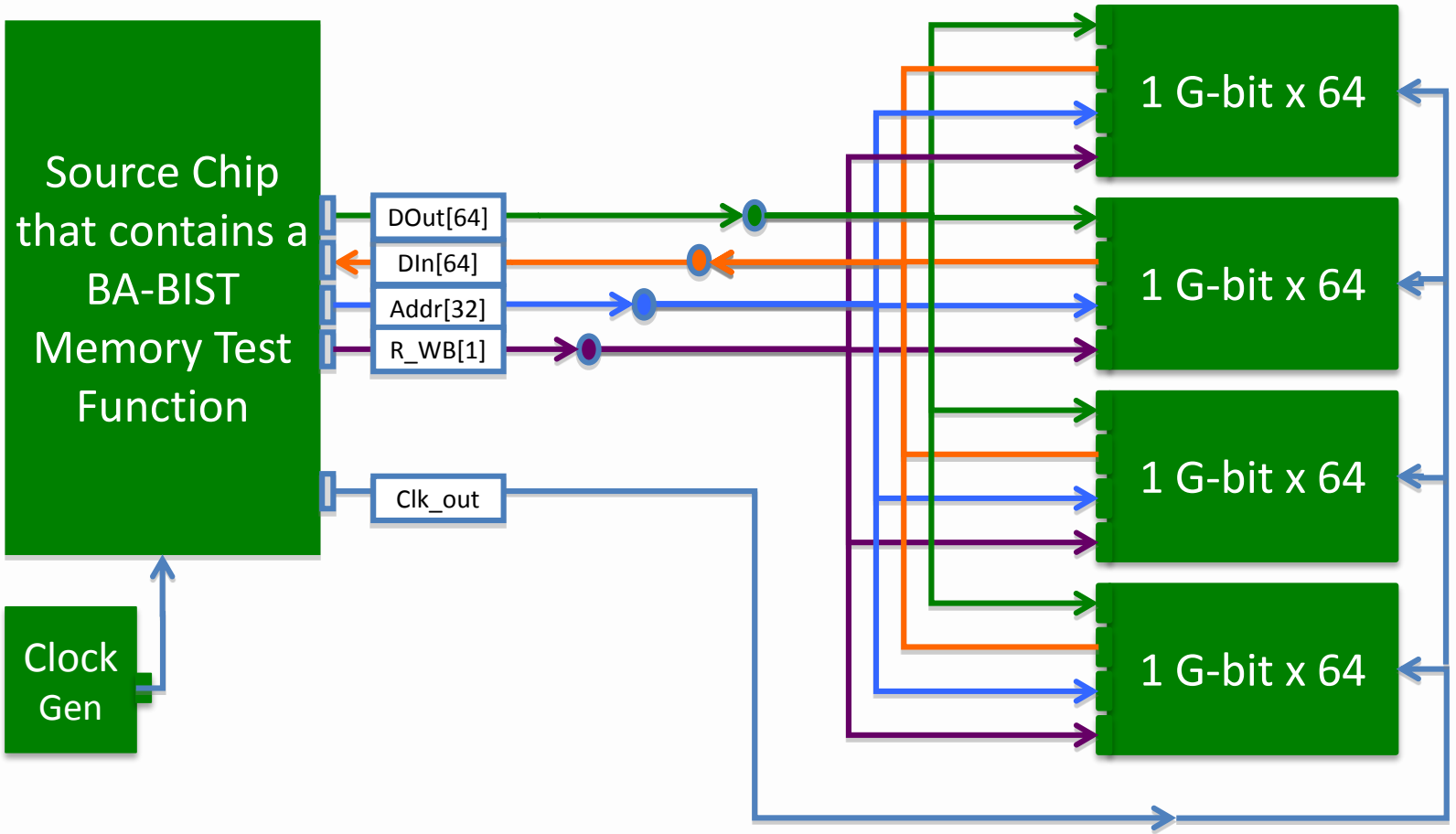


BA-BIST Use Case Standard Scenarios



- IC1 BA-BIST communicates to IC2 IO.
- IC1 BA-BIST communicates to IC2 IO and loops back.
- IC1 and IC2 have BA-BISTs that work together.

Template Example: Memory Test



iNEMI Position Proposal

This position statement presents a BA-BIST Standardization Template for board designers and test developers.

The template provides a means to request from the IC designers, the test features, functions, control, access and algorithms required in the IC BIST, to provide the necessary coverage at board test.

The functions and features may be targeted at (although not limited to) the fault models in slide 11.

Note that the template can also be used for BA-BIST features needed in IC embedded instruments and for generation of specific pseudo-functional tests for use during board and system testing.

iNEMI Position Proposal (Cont.)

What the template is:

The template is a means to enable testing of the IC and board in their mission mode environment.

The template provides guidelines for board design/test engineers to define their ask in a standardization terminology format that IC designer will understand.

The intent is for IC designers to be able to meet requirements or specifications that come out of a board design/test engineers adherence to the template.

The template's 'standardized terms' enable requirements for BA-BIST supporting features and functions needed in the IC design to be defined.

The template fits into the IEEE-P1687 Standard's Ecosystem.

The template usage means 'compliant to the iNEMI membership position'.

iNEMI Position Proposal (Cont.)

What the template is not:

The template intent is not a standard, but uses language such as to define the basis of a potential, future standard.

It does not specify the IC design or architecture, but allows the user to hone in on defining features and behavior of the BIST and embedded instruments.

BA-BIST Requirements Template

Given two connecting chips:	
Goal:	To provide a test that exercises board level nets to identify faults.
Assumptions:	Board test assumptions on pre-testing, board state, board config.
Pre-requisites:	Board conditions needed to set up and run the BA-BIST
Dependencies:	Links to other chips, tests, or board conditions.
Consequences:	From assumptions, pre-requisites and dependencies.
Target:	Manufacturing test step and debug/diagnosis requirement.
Action:	To enable BA-BIST(s) within one chip that is connected to a 2nd chip.
Sequence:	To write to n-locations using k-data (0, F, 5, A, etc.) in the following address sequence (addr<0>, addr<5>, etc.)
Metric:	Fail test data that provides correct diagnosis can be retrieved.

Completed Template: Goal

BA-BIST Instrument to Memory:	
Goal:	T
Assumpti	
Pre-requisite	
Dependencies:	
Consequences:	
Target:	
Action:	
Sequence:	
Metric:	Fa

Goal:

To provide a test that will exercise all nets (signals, clocks, power, ground) to identify faults (shorts, opens, bridges) on the interface from an ASIC , uP or FPGA to a DRAM.

(1) To verify mfg process

(2) To diagnose fail. The fault/fail will be diagnosed/ isolated to the component and to the bad net or pin,

(3) to verify timing problem on the net or do an at-speed test to assist with (1) and (2).

Assumptions

BA-BIST Instrument to Memory:	
Goal:	T
Assumptions:	
Pre-requisites:	
Dependencies:	
Consequences:	
Target:	
Action:	
Sequence:	
Metric:	

Assumptions:

- No test point access on these nets.
- Memory has no boundary scan on this interface.
- Board passes ICT power test.
- All analog and low speed IO's on components can still be ICT tested prior to BA-BIST.
- Board had an unpowered shorts tests of power rails.
- Devices in BA-BIST test have been verified as live - PCOLA is already done.
- Any pins needing termination are terminated according to the chip specification.
- Not proving chip specification, but verifying 'structure is correct'.

Pre-requisites

BA-BIST Instrument to Memory:	
Goal:	To provide a test that exercises board level nets to identify faults.
Assumptions:	
Pre-requisites:	
Dependencies:	
Consequences:	
Target:	
Action:	
Sequence:	
Metric:	

Pre-requisites:

- Chip is already correctly powered.
- Able to do global reset.
- BA-BIST has access to Address, Data, Control lines,
- Access to JTAG port on chip with embedded instruments.
- Access to compliance pins.
- Ability to deliver Clock. BIST clocks (crystals, clock buffers) provided externally are running.
- Clock frequencies on BA-BIST components are validated before BA-BIST is run.
- PLLs are set up and running.
- Test is able to run outside BIOS.

Dependencies

BA-BIST to Memory:	
Goal:	To provide a test that exercises board level nets to identify faults.
Assumptions:	Board test assumptions on pre-testing, board state, board config.
Pre-requisites:	
Dependencies:	
Consequences:	
Target:	Manufacturing test step and debug/diagnosis requirement.
Action:	To enable a BA-BIST within a chip that is connected to the memory
Sequence:	To write to n-locations using k-data (0, F, 5, A, etc.) in the following address sequence (addr<0>, addr<5>, etc.)
Metric:	Test data provides correct diagnosis.

Dependencies:
- On other components needed to support BA-BIST function.
- That these components can be run in a state to support BA-BIST.

Target

BA-BIST to Memory:	
Goal:	To provide a test that exercises board level nets to identify faults.
Assumptions:	Board test assumptions on pre-testing, board state, board config.
Pre-requisites:	Conditions of the board needed to be able to set up and run the BA-BIST
Dependencies:	
Consequences:	
Target:	
Action:	
Sequence:	
Metric:	

Target #1:
Manufacturing Test: Provide only pass/fail data.
Target #2:
Debug-Diagnosis: Provide data that identifies failing chip, pin or net.
Target #3:
Validation-Characterization: Performance fail data with respect to specs.

Action

BA-BIST to Memory:	
Goal:	To provide a test that exercises board level nets to identify faults.
Assumptions:	Board test assumptions on pre-testing, board state, board config.
Pre-requisites:	Conditions of the board needed to be able to set up and run the BA-BIST
Dependencies:	Links to other chips, tests, or board conditions.
Consequences:	Impact to test coverage, or items not covered by this method.
Target:	Manufacturing test step and debug/diagnosis requirement
Action:	
Sequence:	
Metric:	Test data provides correct diagnosis.

Action:

To enable a BA-BIST within a chip that is connected to the memory.

Sequence

```
FAST;

IC( CE, WE, OE, ROW, COLUMN, DATA, BLE, BHE )
IL( CE, ROW, COLUMN, DATA, BLE, BHE ) IH( WE, OE );

.'WRITE'( ZERO, ZERO, FIVE );
.'READ'( ZERO, ZERO, FIVE );
.'WRITE'( ZERO, ZERO, AAAA );
.'READ'( ZERO, ZERO, AAAA );

.REPEAT D'8';
   .'WRITE'( ZERO, NEXTA, FIVE);
   .'READ' ( ZERO, NEXTA, FIVE);
   .'READ' ( ZERO, ZERO, AAAA);
   .'WRITE'( ZERO, NEXTA, AAAA);
   .'READ' ( ZERO, NEXTA, AAAA);
    LET NEXTA = NEXTA * D'2';
.END REPEAT;

 LET NEXTA = D'1';

.REPEAT D'8';
   .'WRITE'( NEXTA, ZERO, FIVE);
   .'READ' ( NEXTA, ZERO, FIVE);
   .'READ' ( ZERO, ZERO, AAAA);
   .'WRITE'( NEXTA, ZERO, AAAA);
   .'READ' ( NEXTA, ZERO, AAAA);
    LET NEXTA = NEXTA * D'2';
.END REPEAT;

END FAST;
```

Initialize all signals = 0,
Except Write-Enable, Output-Enable = 1

Data Line Test: Write Address 0 with 5; Read Address 0 for 5
Then: Write Address 0 with A; Read Address 0 for A

Address Line Test: Write Column Address 1 with a 5;
Then: Read Address 1 for a 5
Then: Read Address 0 for an A
Then: Write Address 1 with an A
Then: Read Address 1 for an A
Then: Change Address (Walk a 1 across Address Lines)

Address Line Test: Write Row Address 1 with a 5;
Then: Read Address 1 for a 5
Then: Read Address 0 for an A
Then: Write Address 1 with an A
Then: Read Address 1 for an A
Then: Change Address (Walk a 1 across Address Lines)

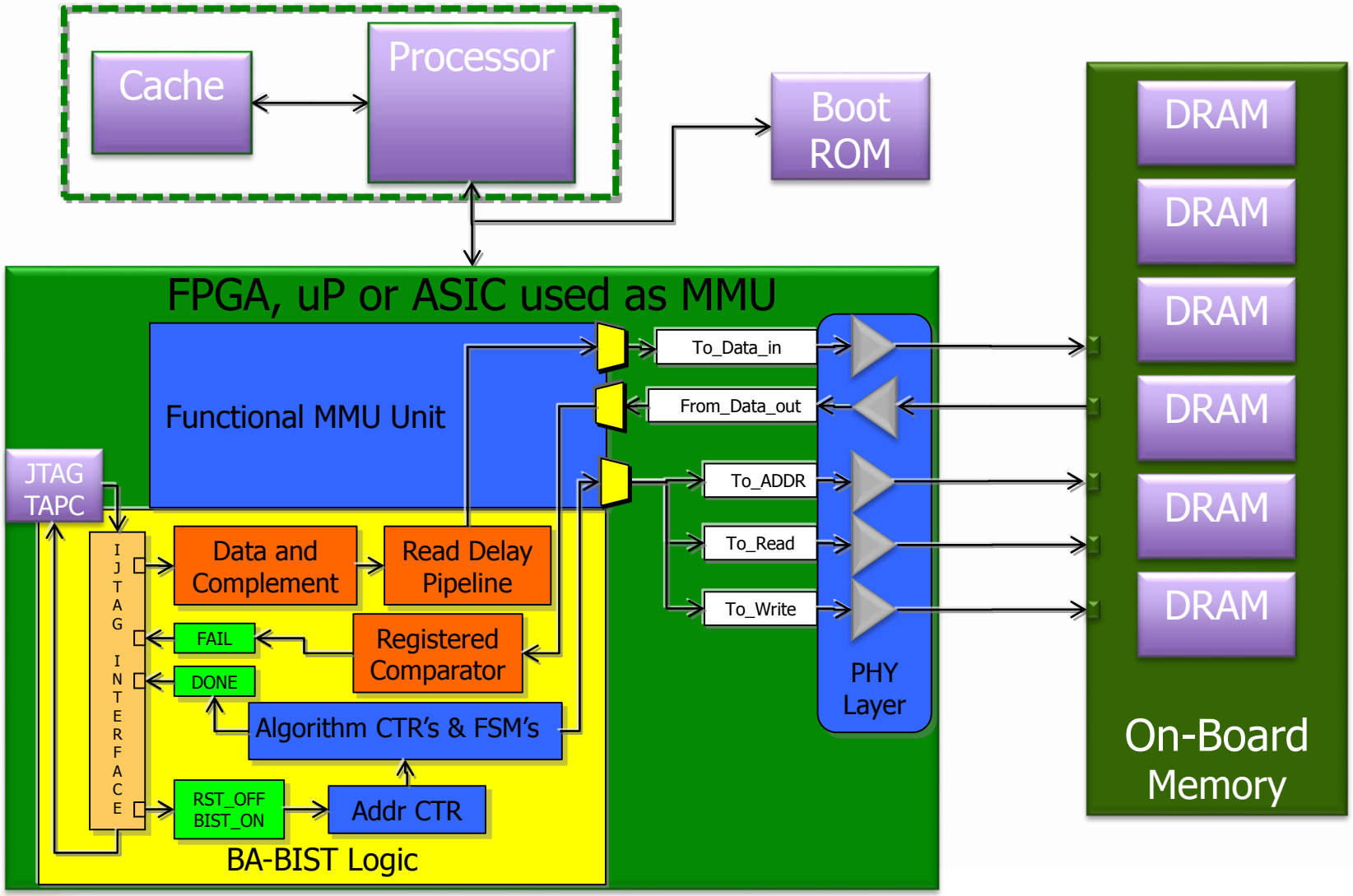
Metric

BA-BIST to Memory:	
Goal:	To provide a test that exercises board level nets to identify faults.
Assumptions:	Board test assumptions on pre-testing, board state, board config.
Pre-requisites:	Access to Address lines, Data lines, Control lines, ability to deliver clock, and Power, access to JTAG port on chip with embedded instrument.
Dependencies:	Links to other chips, tests, or board conditions.
Consequences:	Impact to test coverage, or items not covered by this method.
Target:	Manufacturing test step and debug/diagnosis requirement.
Action:	To enable a BA-BIST within a chip that is connected to the memory
Sequence:	
Metric:	

Metric:

To provide read data associated with failing locations to JTAG TDO port, (or all reads to TDO to allow software to assess mis-compares/fails).

BA-BIST to DDR Memory



BA-BIST to DDR Memory

Goal:

To provide a test that exercises board level nets from FPGA to DDR at speed.

Assumption:

Can use JTAG in FPGA to run test.

Pre-requisites:

Add JTAG header, access to USB, Tck is supplied.

Dependency

Onboard clocks, power and memory

Sequence:

Walk data through each address to isolate bad address or data net.

P1687 End To End BA-BIST Use Model

Design-Side

IP Instruments
Network Creation
- RTL-Insertion
- Network Synthesis
- Documentation Gen
- BSDL/ICL/PDL

IC Test-Side

IC Test Generation
Embedded Instrument
- Access
- Vector Retargeting
- Vector Translation
- SVF/PDL to STIL

Board Test

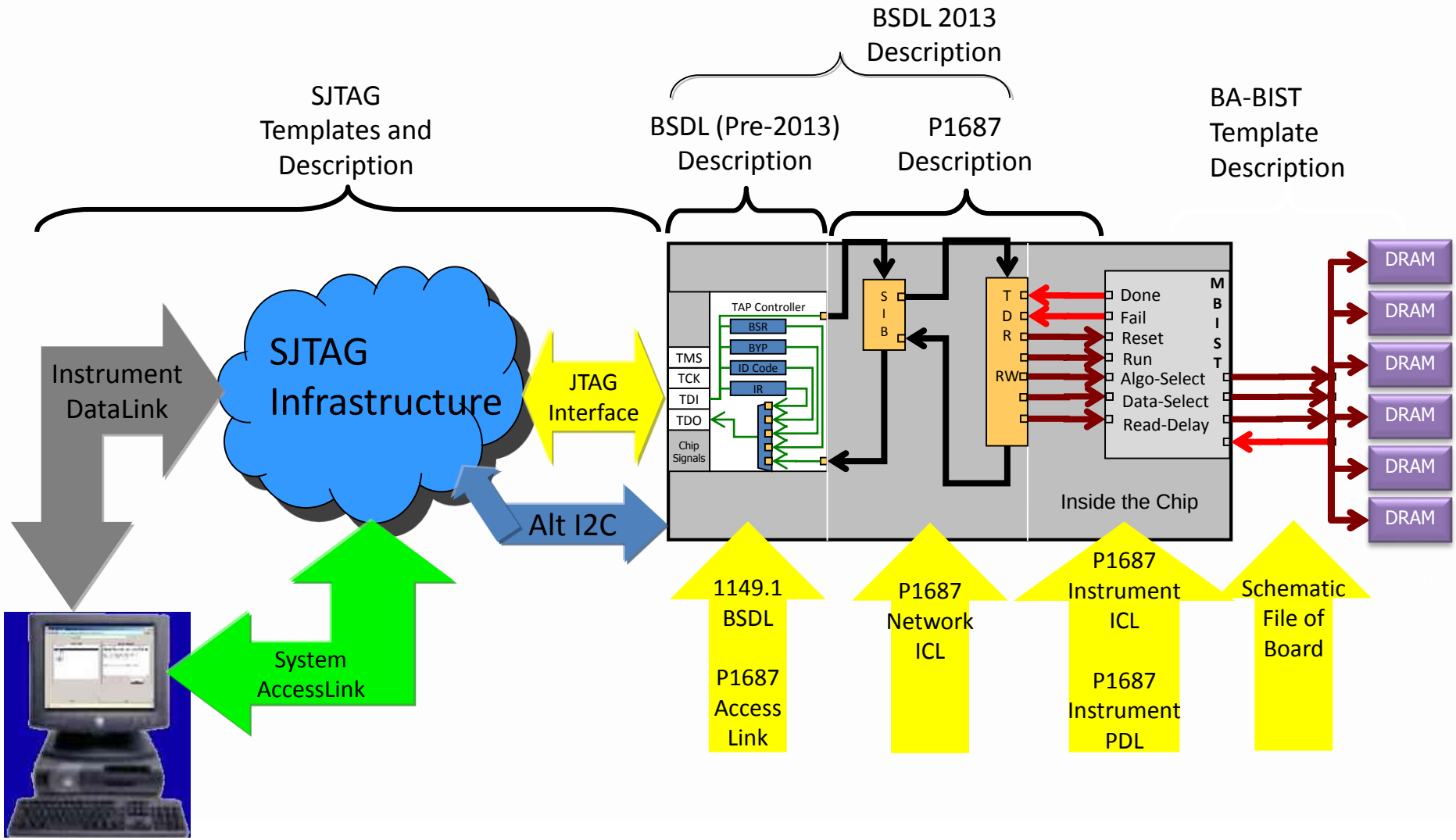
Embedded Instrument
- Access
- Configuration
- Vector Retargeting
- Operation

Chip Providers
EDA Tools

ATE Testers
Translation Tools

JTAG Testers/
Functional Testers

E-MBIST Eco-System for Data Transfer



Conclusions

- Defined Industry usable BA-BIST to:
  - Add test coverage for test point reduction
  - Improve debug and diagnosis
  - Link to existing standards
- Proposed board test *Standardization Template*.
- iNEMI Position Paper endorsed by members.
- Adoption by EDA and design/system companies.
- Future project phase will start later in 2014.

References

- Z. F. Conroy et al, “Board Assisted-BIST: Long and Short Term Solutions for Testpoint Erosion”, Proc IEEE ITC, Nov 2012.
- Z.F. Conroy et al, “Current and Future Manufacturing Test Solution Strategies - iNEMI Boundary-scan and Built in Self Test (BIST) Technology Integration for Future Standardization”, Proc IEMTC, Nov 2012.
- A. Crouch et al, “The IJTAG Tools Flow: Demonstrating re-use of embedded instruments and test vectors from chips to circuit boards and systems”, www.asset-intertech.com, 2014.

Speaker was not required to provide a paper for the 2014 APEXPO™ Technical Conference