Simulation of the Influence of Manufacturing Quality on Thermomechanical Stress of Microvias

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Abstract
The advancement of area-array packages, such as flip chips and chip scale packages, has driven the adoption of high density interconnects (HDIs) that allow for an increased number of I/Os with a smaller footprint area. HDI substrates and printed circuit boards use microvias as interconnects between conductor layers. HDIs have evolved from single-level microvias to stacked microvias that traverse sequential layers. A stacked microvia is filled with electroplated copper to make electrical interconnections and support the outer level(s) of the microvia or components mounted to the upper capture pad. A common problem in copper-filled microvia fabrication is that the copper plating process can result in incomplete filling, dimples, or voids. However, the effects of these copper filling defects on the reliability of microvias are unknown. This study is the first known investigation and analysis of the influence of voiding and incomplete copper filling defects on the thermomechanical stresses in microvias.

Single-level and stacked microvias were modeled using the finite element method to simulate fully filled and partially filled microvias, as well as filled microvias with voids of different sizes. The stress states of these microvia models under thermal shock loads were investigated to determine the effects of the filling defects on the reliability of microvias.

The finite element modeling and simulation results demonstrated that stacked microvias experienced greater stresses than single-level microvias. With the same microvia geometry and material properties, copper filling reduced the stress level on the microvia structure, where fully copper-filled microvias had a lower stress level than partially filled microvias. The presence of voids generally increased the stress level in the microvia structure, but with a very small void size, the maximum stress in the microvia can be less than in a non-voided microvia. The stress level and the location of the maximum stress varied with changes in the void size.

1. Introduction

Driven by the demand for portable and miniaturized consumer products, the electronics industry must achieve fast, light, and reliable products, with increased product functionality. This requires an increased number of I/Os with a smaller footprint area for packages. Microvias are used as interconnects between layers in high density interconnect (HDI) substrates and printed circuit boards (PCBs) to accommodate the high I/O density of advanced packages, such as flip-chip ball grid arrays (FCBGAs), chip scale packages (CSPs), and direct chip attachments (DCAs).

Microvias are blind or buried vias that are equal to or less than 150 μm in diameter and have a target pad equal to or less than 350 μm [1][2]. Buried microvias were usually filled with non-conductive materials or solder. According to IPC-6016 Standard [3], blind microvias on the external layers do not have any fill requirements. With the advancements in packaging technology, the number of HDI layers on package substrates and PCBs has increased. Figure 1 shows a schematic diagram of a [2+4+2]-layer HDI board (2 HDI layers on each side of the board, and 4 layers of traditional PCB core board in the middle) with stacked and staggered microvias. A stacked microvia is plated closed with electroplated copper to support the outer level(s) of the microvias or components mounted to the upper capture pad and make electrical interconnections. However, incomplete via filling or voids can be generated from the copper plating process. Figure 2 shows examples of incomplete microvia filling and voiding. The effect of these manufacturing quality issues on microvia reliability is unknown.

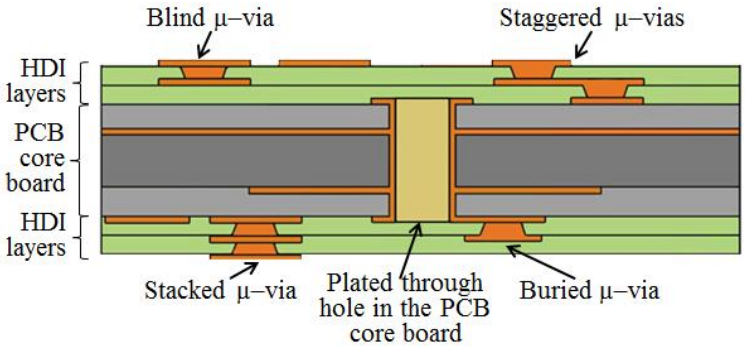
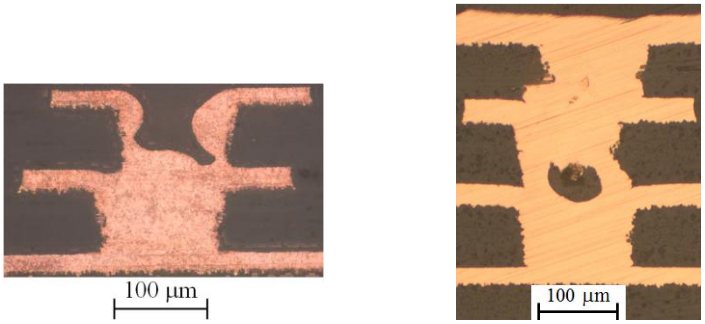


Figure 1 - Illustration of an HDI Board with Various Microvias



(a) incomplete microvia filling (b) microvia with void

Figure 2 - Examples of Microvia Filling Issues

Microvia research has focused on experimental assessment of the reliability of single-level unfilled microvias [4]-[9]; Birch [10] tested multiple-level, stacked microvias, and the Weibull analysis on the test data showed that single- and 2-level stacked microvias last longer than 3- and 4-level microvias (e. g. 2-level stacked microvias experienced about 20 times more cycles to failure than 4-level stacked microvias). The previous research [4]-[10] has identified different types of microvia failures, including interfacial separation (separation between the base of the microvia and the target pad), barrel cracks, corner/knee cracks, and target pad cracks (also referred to as microvia pull out). These failures result from the thermomechanical stresses caused by coefficient of thermal expansion (CTE) mismatch, in the board thickness direction, between the metallization in a microvia structure and the dielectric materials surrounding the metal. However, none of the research addressed the effect of incomplete via filling or voids on the reliability of microvias.

Researchers have also developed numerical models using the finite element method to obtain local stress/strain states in the microvia structure, and employed analytical models to estimate the microvia fatigue life [7][8][11],[12]. Prabhuet *et al.* [11] and Ogunjimiet *et al.* [12] conducted finite element analysis (FEA) on polymer-overlaid HDI microvia structures in multichip modules (MCMs) using 2D and 3D models, respectively. Prabhu *et al.* [11] investigated the effect of accelerated temperature cycling and thermal shock, and the total strain range from FEA were used to estimate the fatigue life of the microvia structure, while Ogunjimi et al. [12] found that the strain concentration factor, copper ductility, and microvia wall thickness had more significant effects on microvia reliability than the wall angle and epoxy height. Ramakrishna et al. Authors of [7][8] investigated the effects of geometry and material properties on microvia reliability through FEA and found that different microvia wall thicknesses, wall angles, diameters, dielectric thicknesses, or dielectric properties result in different stress/strain levels. Wang and Lai [13] investigated the potential failure sites of microvias in the substrate of a multichip module (MCM) using the submodeling technique in FEA. They found that filled microvias have a lower stress than unfilled microvias in their model.

The FEA studies in the literature focused on single-level flaw-free microvias. Effects of incomplete via filling and voiding were never addressed. In this study, the authors compared single-level and stacked microvias with complete or partial filling, and fully filled microvias with the presence of voids of different sizes. The effects of copper filling quality were investigated on the stress distributions in microvias under thermal shock loads.

Section 2 of the paper describes the FEA modeling and analysis process. Section 3 addresses the simulation results of microvia filling quality issues, such as partial via filling and voiding. It would be reasonable to expect that different stress

levels on the microvia structures due to copper filling quality may result in different field reliability. Section 4 presents discussions and conclusions.

2. Finite Element Modeling

The in-plane dimensions of a PCB are many orders of magnitude larger than the height of a microvia. Therefore, an acceptable approximate model is to isolate an appropriate "unit cell" containing only one microvia structure [14]-[16]. Assuming microvias are periodically arranged in a PCB with equal distance between two neighboring microvias in a row or column, suitable "periodic" boundary conditions [14]-[16] can be imposed on the unit cell to simulate the presence of the surrounding microvias and board materials. The unit cell extends half-way to the neighboring microvias in the same row or column in the periodic arrangement (Figure 3).

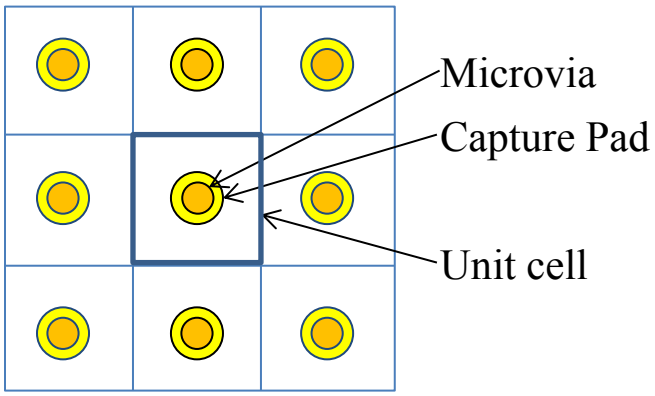
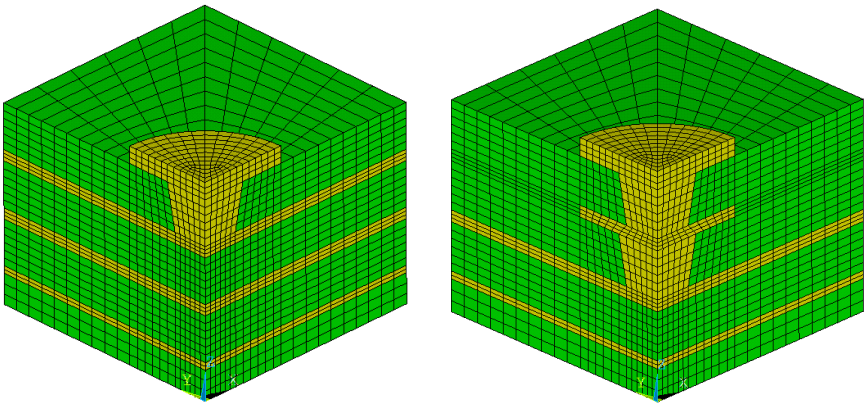


Figure 3 - Illustration of a Unit Cell

The periodic boundary conditions were applied to the unit cell model to simulate the effect of neighboring microvias on it. The periodic boundary conditions permitted the boundaries to deform, but constrained them to remain plane and parallel to the original face. This ensured compatibility with adjacent microvias around the unit cell. The constraints of periodic boundary conditions are tighter than free boundary conditions, which do not constrain the in-plane displacement at all, but looser than complete constraints of displacement in the PCB plane, which may be over restrictive and unrealistic.

The geometric dimensions of the microvia models are listed in

Table 1. The models simulate a [2+4+2]-layer HDI board. There were stacked two-level microvias and single-level microvias, which located only in the most outside dielectric layers of the board. The top half of the HDI board was modeled due to symmetry about the board mid-plane. A 3D model was created for the unit cell, and a quarter model was used due to symmetry. Figure 4 shows stacked and single-level microvia models with complete copper filling. Solder masks on the surface of the HDI board was ignored in these models, because it is very ease to deform compared to copper and the dielectric materials.



(1) single-level microvia model (b) stacked microvia model

Figure 4 - Finite Element Model of the Microvia

Table 1 - Geometric Dimensions of the Microvia Models

	Location	Dimension (μm)
Thickness	1st copper layer	28
	1st dielectric layer	75
	2nd copper layer	18
	2nd dielectric layer	75
	3rd copper layer	18
	3rd dielectric layer	75
	4th copper layer	12
	middle dielectric layer	100
Microvia diameter	top	150
	bottom	120
Distance between two neighboring microvias		800

Error! Reference source not found. lists the material properties used for the FEA models. The fabric reinforced composite, which most PCBs are constructed from, is used for the dielectric materials in the core board and the HDI layers. The woven-fabric reinforced resin is an orthotropic material with two principal material directions running along the board plane and orthogonal to each other, and a third direction along the out-of-plane normal. The reinforced resin was modeled as an elastic material [17]. Copper is used for the conductor layers and fills the microvias. The electroplated copper of the microvias was modeled as an elastic-plastic material having a bilinear kinematic hardening relationship [8].

Table 2 - Material Properties

Material		CTE (ppm/^{o}C)	Young's Modulus (GPa)	Poisson's Ratio	Shear Modulus (GPa)
FR4 (Transverse isotropic)	X-axis/YZ plane	16	17	0. 42	2. 4
	Y-axis/XZ plane	16	17	0. 42	2. 4
	Z-axis/XY plane	50	7. 45	0. 13	3
Copper (Isotropic)		17	103. 42	0. 34	
		Yield strength (MPa)		**Hardening Modulus (MPa)**	
		172. 3		1034. 2	

Note: the PCB plane is the XY plane and the PCB thickness direction is the Z-axis

The thermal load emulated on the finite element model was -55^{o}C to +125^{o}C thermal shock. Each thermal shock cycle consists of two 15-minute dwell times at the high and low temperatures, with a sudden change between the two temperature extremes. Under the thermal shock load, the microvia experiences cyclic tensile and compressive stresses. These stresses and corresponding strains are due to CTE mismatch between the dielectric material and copper, and the geometry of the microvia (including voiding geometry). At +125^{o}C, the CTE mismatch reaches the maximum and consequently, the thermomechanical stress in the microvias is the maximum. In this study, von Mises stresses at the highest temperature were monitored to examine the effects of incomplete copper filling and voiding.

3. Simulation Results – Effects of Microvia Manufacturing Quality

To investigate the influence of microvia manufacturing quality, the authors conducted three FEA studies. Incomplete copper filling was simulated as filling of partial height in the microvia. Partially filled single-level and stacked microvias were compared with fully filled microvias. For stacked microvias, the inner level of the stack must be filled to support the outer level. Therefore, partial filling were simulated only on the outer level of the stacked microvias. The third study addressed the effects of voiding on microvia stress distributions. The stress levels were correlated to different void sizes.

3.1 Incomplete filling of microvias

Incomplete filling was simulated as partial height of the microvia filling. Three different filling ratios (height of filling over depth of microvia), 80%, 60%, and 40% were simulated. The stress results were compared with the stress on fully filled microvias. The stresses were normalized based on the maximum von Mises stress of the fully filled microvia for single-level microvias and stacked microvias, respectively. According to the comparison in **Figure 5Error! Reference source not found.**, incomplete copper filling increased the stress level on microvia structures; the stresses for all the partially filled microvias were larger than the fully filled microvias, for both single level and stacked microvias. A lower filling ratio resulted a larger stress for the stacked microvias. Although the single-level microvia with 40% filling had a smaller stress level than that with 60% filling, the 40% filling still generated a higher stress than fully copper filled microvias. Consequently, incompletely filled microvia would last shorter than fully filled microvias under the same life cycle loads.

Compared with single-level microvias, the stacked microvias had larger stresses. For example, the maximum von Mises stress on the single-level fully filled microvias was 91.5 MPa, while it was 139.1 MPa – over 1.5 times – on the fully filled stacked microvia. Corresponding partially filled stacked microvias also experienced higher stress levels than single-level microvias. The thermomechanical stress generated from CTE mismatch of copper and dielectric materials is mainly in the out-of-plane direction. The dielectric expands/shrinks more than copper. With the stacked microvias, there is a greater volume of the dielectric around the copper, which generates a greater amount of expansion on the microvia. The thermomechanical stress in the microvia increases with the dielectric thickness and the level of microvia stacks.

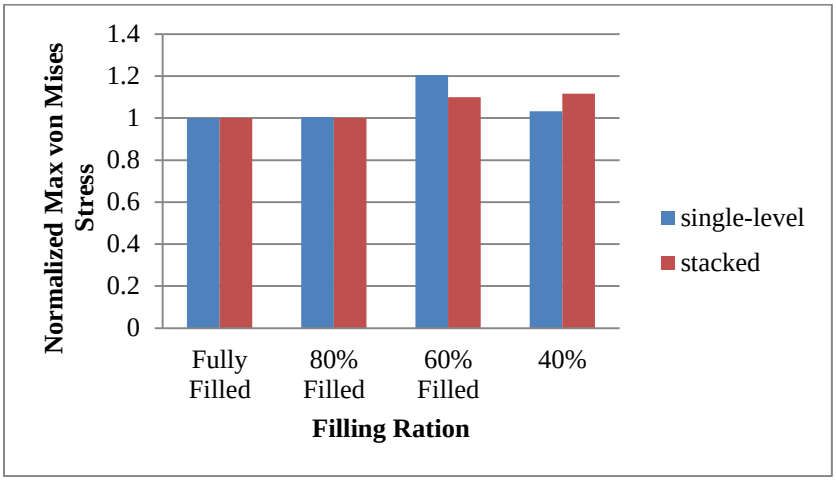


Figure 5 - Effects of Filling Condition on von Mises Stress

3.2 Voids in stacked microvias

Volume fraction was used to measure the void size in this study. Volume fraction was defined as the ratio of the void volume to the microvia volume. A spherical void shape was simulated, based on abstractions from observed void shapes in commercial HDI boards. It was assumed that the voids were located right at the center of the microvia in the board plane view.

As shown in Figure 6, the von Mises stress first declines and then rises with the increase of the void size. Before reaching the cut-off point between 16% and 20% volume fraction, the von Mises stress of voided microvias was smaller than that of the non-voided microvia. This means the microvia structure is more compliant with a small void (less than 16% volume fraction). When the voids get larger than the cut-off point, the stress level increases because less material in the microvia is present to support the load. Moreover, the existence of the minimum stress level when the volume is less than 16% indicates the possibility of a beneficial void size with respect to the stress level, and possibly the reliability, of the microvia. If this benefit is verified in future studies, small voids could be deliberately incorporated in microvias to improve reliability.

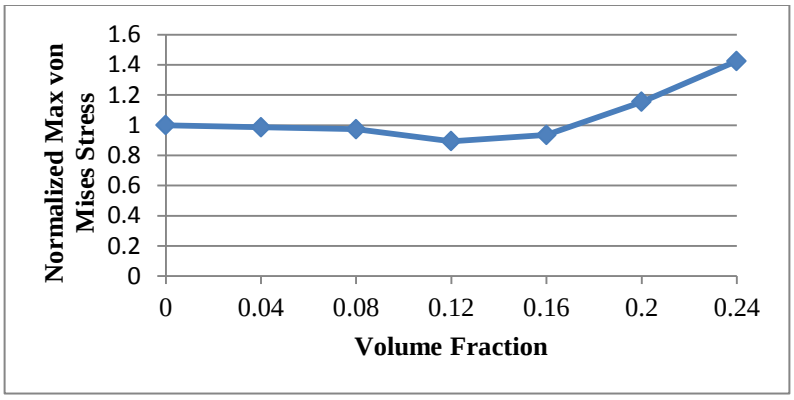


Figure 6 - Partial Filling Model for Stacked Microvias

4. Discussions and Conclusions

A known failure mechanism in HDI substrates and PCBs is fatigue due to CTE mismatch between the dielectric material and metallization in a microvia structure. However, the effects of process-induced defects on microvia reliability were not studied in the past. FEA studies were conducted to investigate the influence of partial via filling and voiding conditions on the strain/stress distribution. Different filling ratios (percentage) and voiding sizes in a microvia structure were examined in the research. Fully copper-filled microvias had a lower stress level than partially filled microvias, while the existence of voids was found to be not necessarily detrimental to microvia stress levels, depending on the void conditions.

(1) With the same microvia geometry and material properties, copper filling reduced the stress level on the microvia structure, where fully copper-filled microvias had a lower stress level than partially filled microvias.

(2) A small void can subtly reduce the thermomechanical stress in the microvia. As the void gets larger (within a threshold), the microvia structure is more compliant and results in even smaller stress. However, if the void size exceeds the threshold (the value of the threshold depends on many factors), the stress will start to increase.

The FEA studies provide insights regarding the effects of partial copper filling and plating voids on microvia reliability. Some of the results are not so intuitive or not reported in the past.

Acknowledgments

The authors would like to thank the over 100 companies that support the Center for Advanced Life Cycle Engineering (CALCE) consortium at the University of Maryland, College Park.

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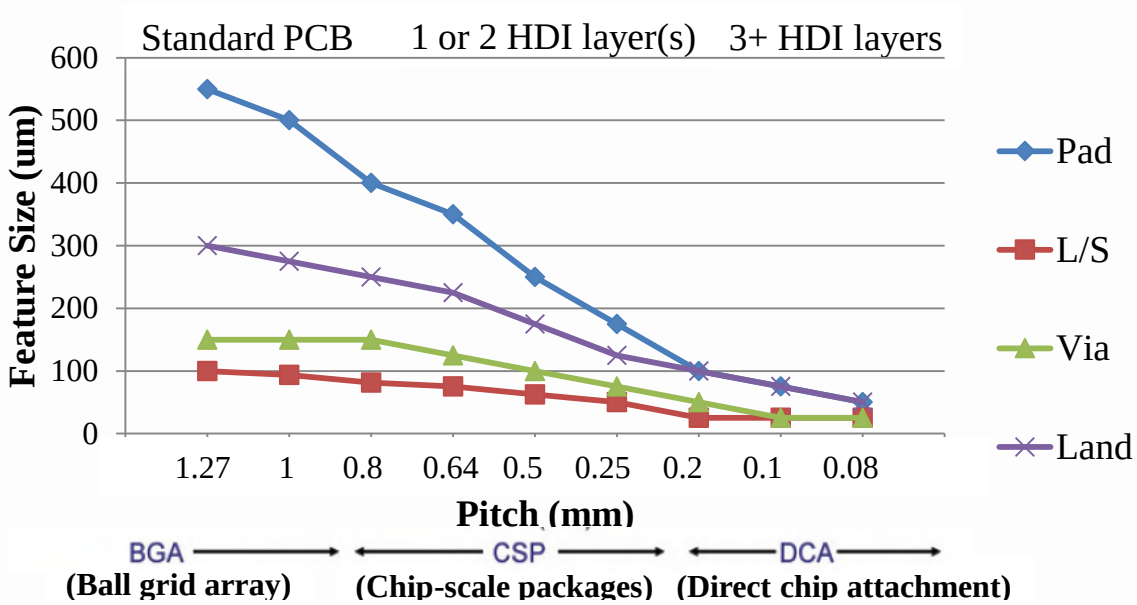
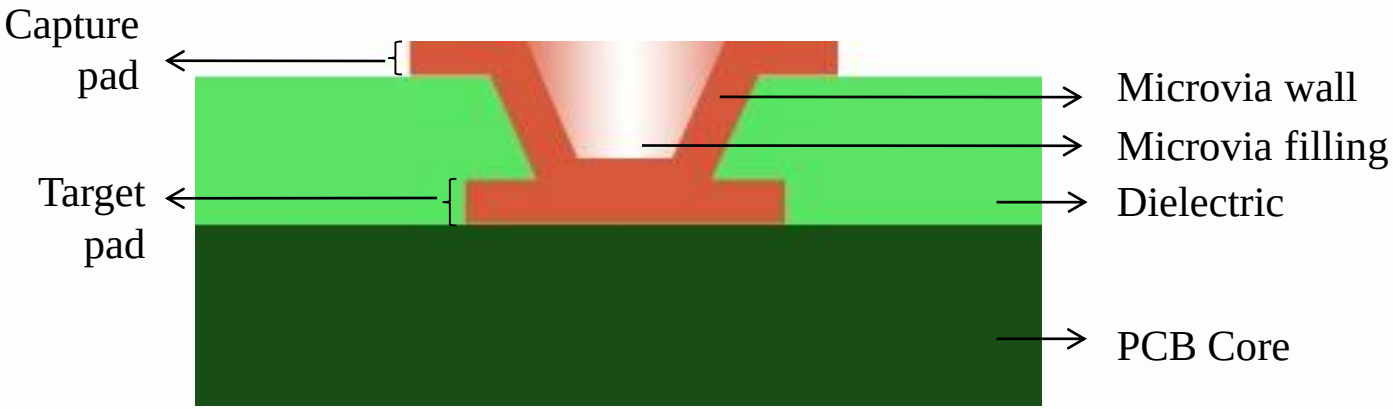
Introduction

The large number of I/Os on fine-pitch area-array packages has driven the adoption of high density interconnect (HDI) printed circuit boards (PCBs).



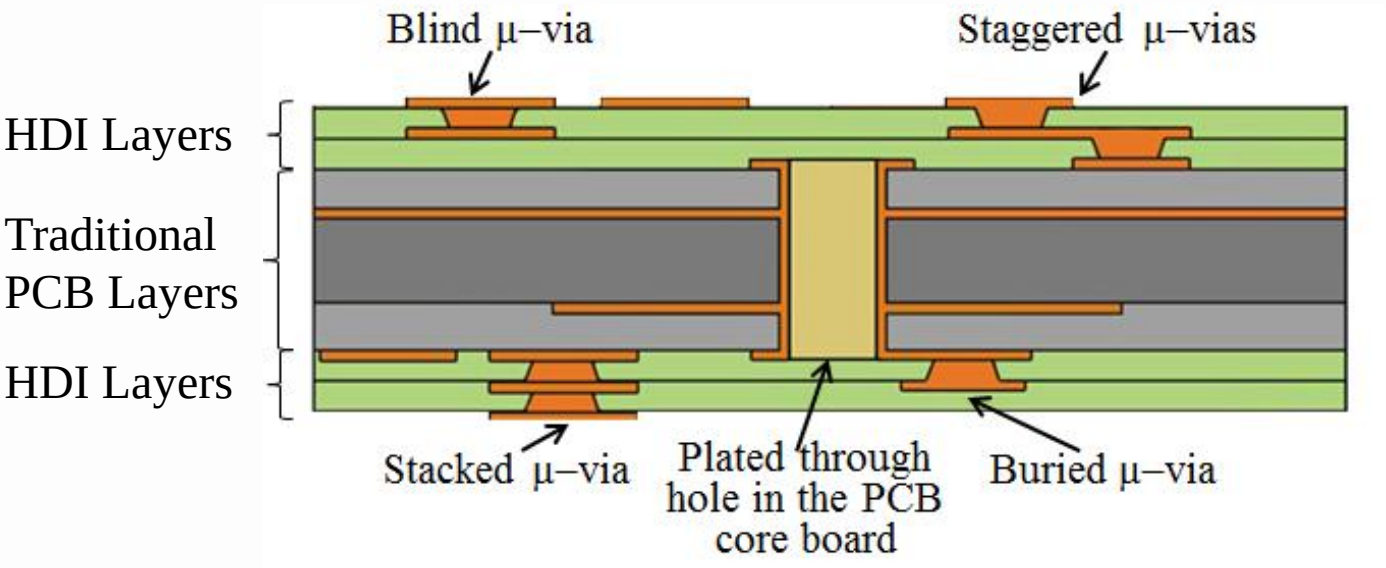
IC packaging feature roadmap with via size, via-pad size, lines and spaces (L/S), and SMT land size [ref: www.hdihandbook.com**]**

Illustration of Single Level Microvia



- Microvias are used as interconnects between layers in high density interconnect (HDI) circuit boards to accommodate the high I/O density of advanced packages.
- Microvias are blind or buried vias that are equal to or less than 150 μm in diameter [ref: IPC/JPCA-2315 and IPC-2226].

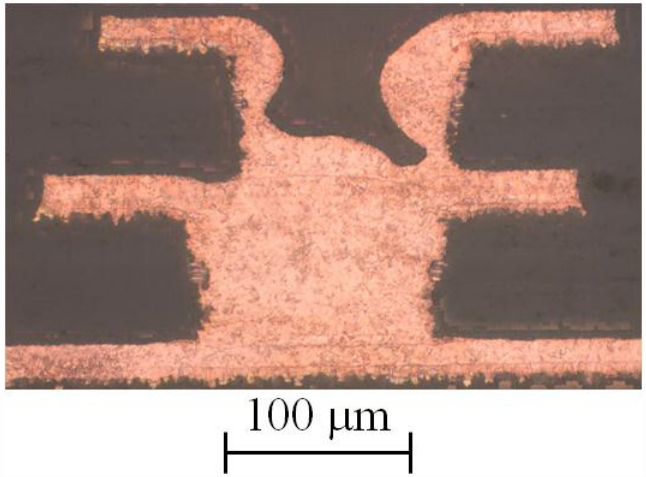
Illustrations of HDI Board



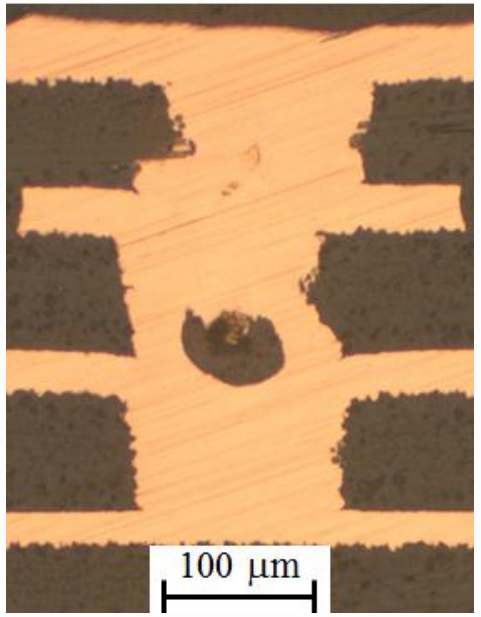
- Buried microvias should be filled, while blind microvias on the external layers do not have any filling requirement based on IPC-6016.
- Stacked microvias are plated closed with electroplated copper, to support the outer level(s) of the microvias or components mounted to the upper capture pad, and to make electrical interconnections.

Microvia Quality Issues

- A common problem in copper-filled microvia fabrication is that the copper plating process can result in incomplete filling or voids.
- The effect of these manufacturing quality issues on microvia reliability has not been previously reported.



Cross-section view: incomplete microvia filling



Cross-section view: microvia with void

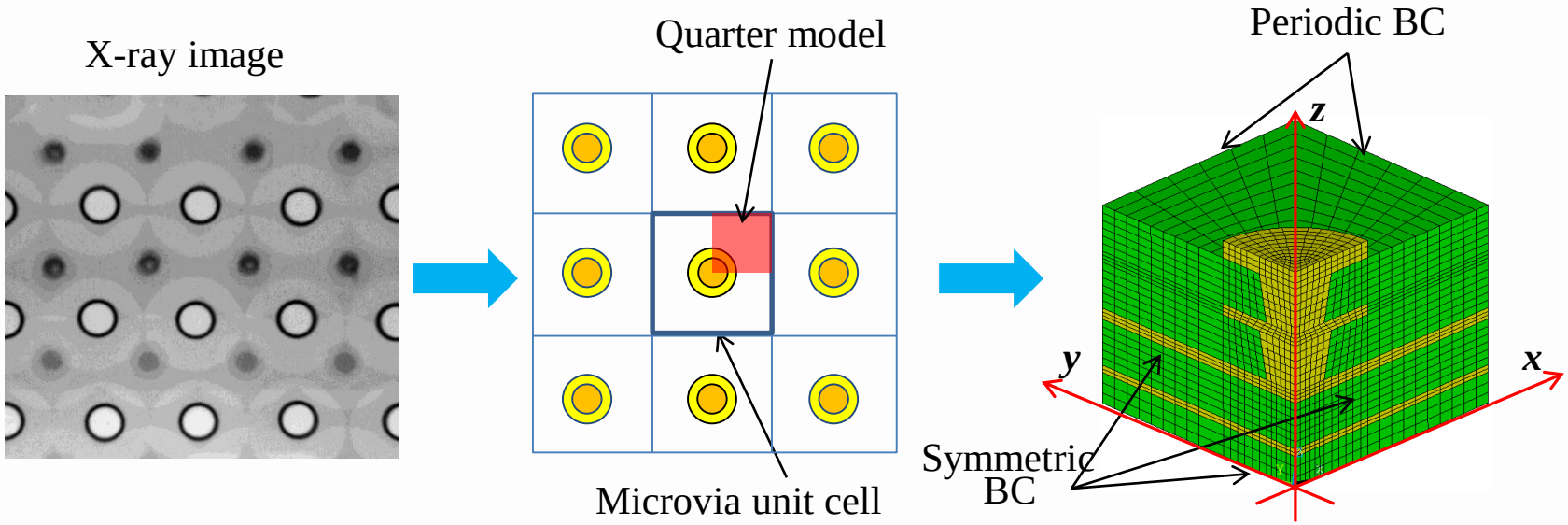
Previous Work on Microvia Reliability

- Most microvia reliability research has focused on experimental assessment of the reliability of single-level unfilled microvias.
- Birch tested multiple-level copper-filled microvias, but did not consider defects [ref: *Circuit World*, 2009].
- Previous studies involving finite element analysis (FEA) of microvias have all focused on single-level defect-free microvias.

Objectives of this Study

- Single-level and stacked microvias are modeled using FEA to simulate **fully filled** and **partially filled** microvias, as well as **filled microvias with voids** of different sizes.
- The stress distributions within these microvias under thermal cycling loads are investigated to determine the effects of the filling defects on the reliability of microvias.
- Parametric studies are conducted to correlate different filling levels and void sizes with the thermomechanical stress.

Modeling a Microvia

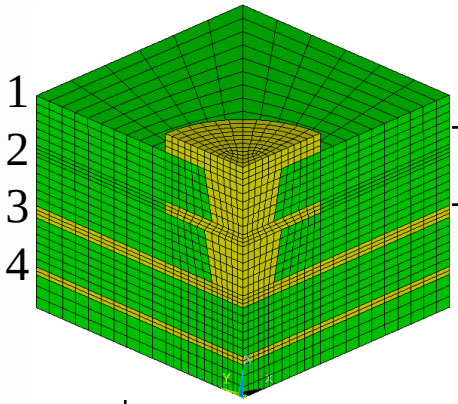


- Symmetric boundary conditions (BCs) at x=0, y = 0, and z = 0 faces
- Periodic BCs at the outside lateral faces of the unit cell
  - Periodic BCs simulate the effect of neighboring microvias on the unit cell.
  - The periodic BC permits the boundaries to deform, but constrains them to remain in plane and parallel to the original face.

Material Properties for FEA

Material		CTE (ppm/°C)	Young's Modulus (GPa)	Poisson's Ratio	Shear Modulus (GPa)
Fabric-Reinforced Composite (orthotropic)	X-Axis/YZ plane	16	17	0. 42	2. 4
	Y-Axis/XZ plane	16	17	0. 42	2. 4
	Z-Axis/XY plane	50	7. 45	0. 13	3
Copper (Isotropic)		16	17	0. 42	2. 4
		Yield Strength (MPa)		Tangent Modulus of Plasticity (MPa)	
		172		1034	

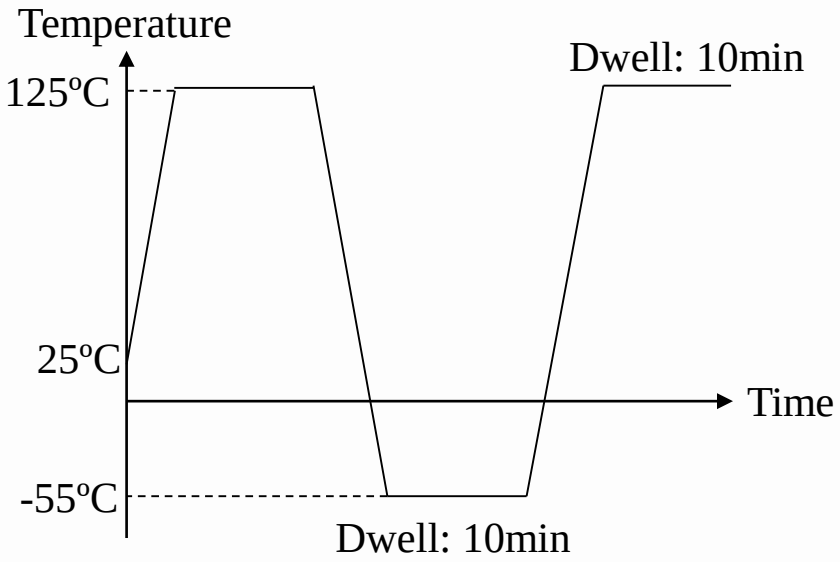
Microvia Dimensions



	Location	Dimension (μm)
Thickness	1st copper layer	28
	1st dielectric layer	75
	2nd copper layer	18
	2nd dielectric layer	75
	3rd copper layer	18
	3rd dielectric layer	75
	4th copper layer	12
	4th dielectric layer	100
Microvia diameter	top	150
	bottom	120
Distance between two neighboring microvias		800

Note: dimensions are based on a commercial board under investigation.

Loading Condition for FEA

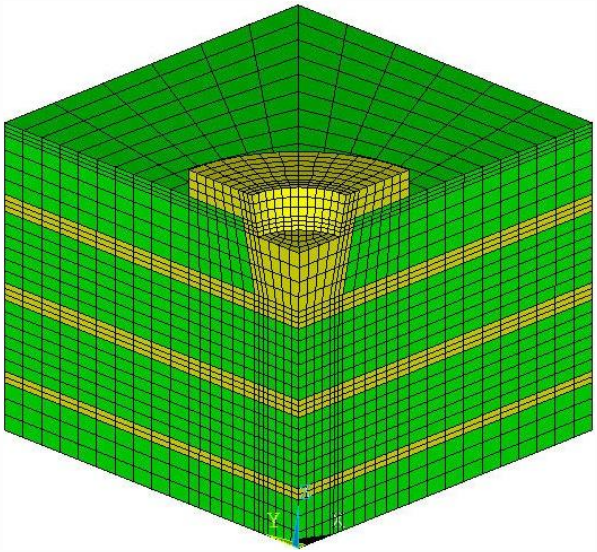


- Thermal load: -55ºC~+125ºC thermal cycling
  - 5 minutes ramp
  - 10 minutes dwell

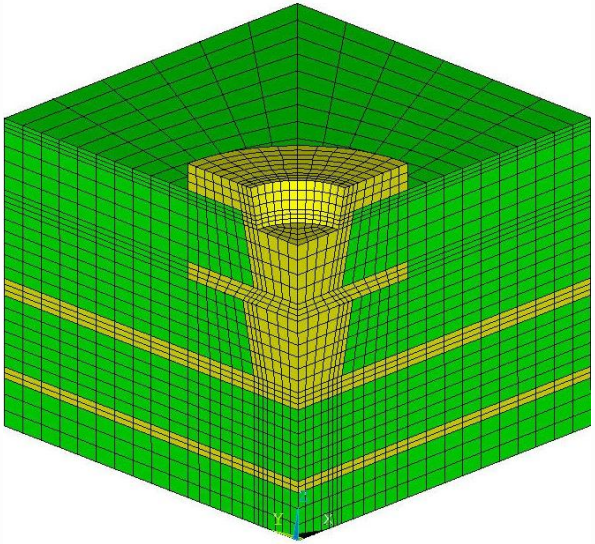
- Under the thermal cycling load, the microvia experiences cyclic tensile and compressive stresses.
- At 125ºC, the CTE mismatch reaches a maximum, and consequently the thermomechanical stress in the microvias is a maximum.
- Von Mises stresses at 125ºC are monitored to examine the effects of incomplete copper filling and voiding.

Incomplete Filling of Microvias

- Three different filling ratios (height of fill over depth of microvia) were simulated: 80%, 60%, and 40%.
- Partially filled single-level and stacked microvias were compared with fully filled microvias.

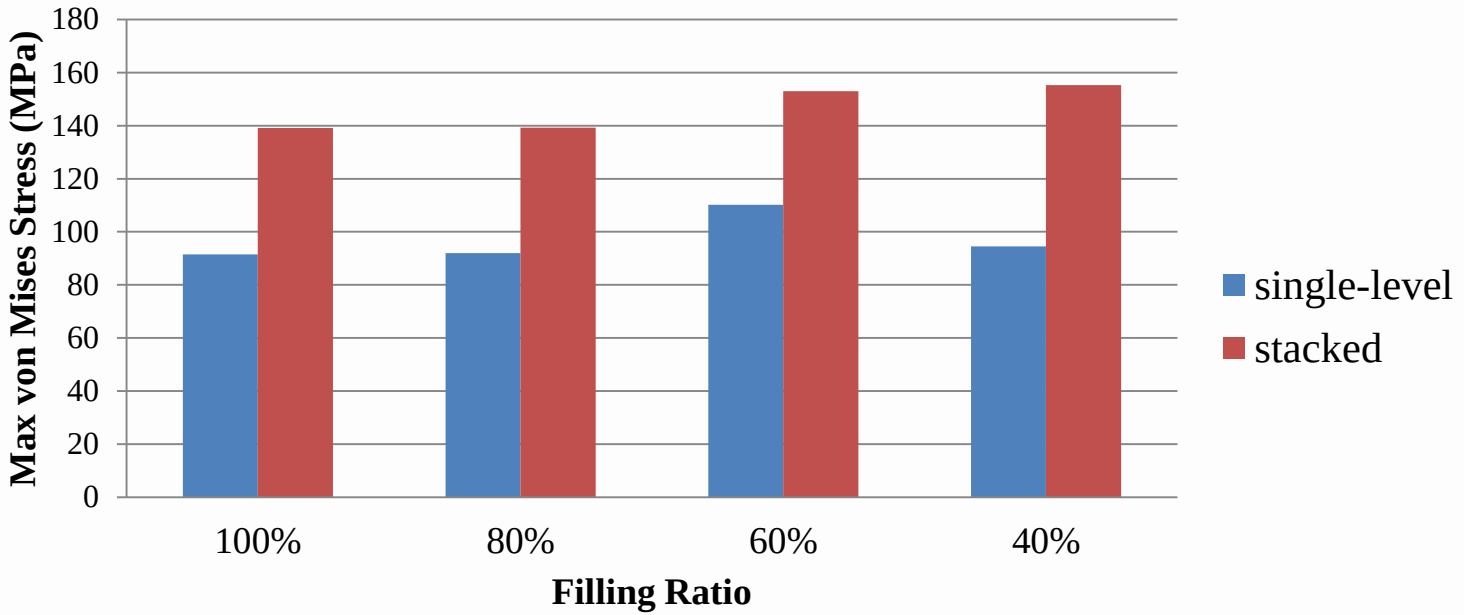


Single-level microvia with partial filling



Stacked microvia with partial filling

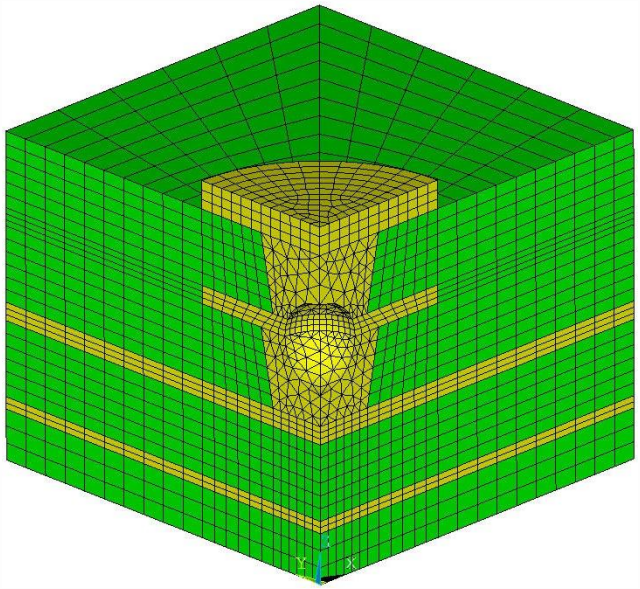
Effects of Incomplete Filling



- The stress of all partially filled microvias is larger than the fully filled microvias.
  - A lower filling ratio generally resulted in a larger stress.
- Stacked microvias have larger stress than single-level microvias for all the filling ratios.

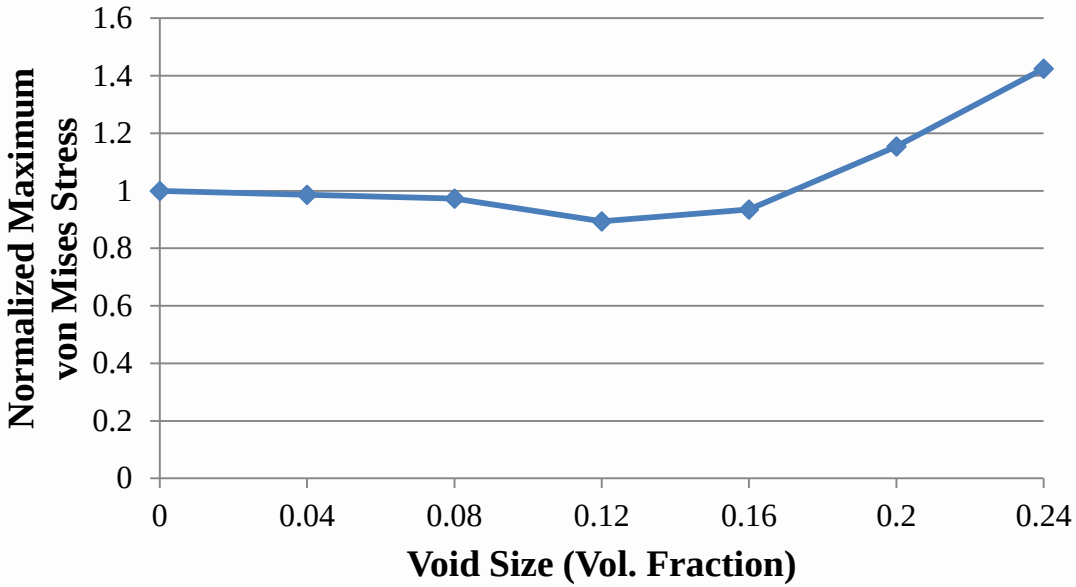
Voids in Stacked Microvias

- Void size is defined as the ratio of the void volume to the microvia volume.
- Void sizes of 4%, 8%, 12%, 16%, 20%, and 24% are used for the simulation.
- A spherical void shape was simulated, based on abstractions from observed void shapes in commercial HDI boards. It was assumed that the voids were located at the center of the microvia.



Microvia with void

Results of Voided Microvia

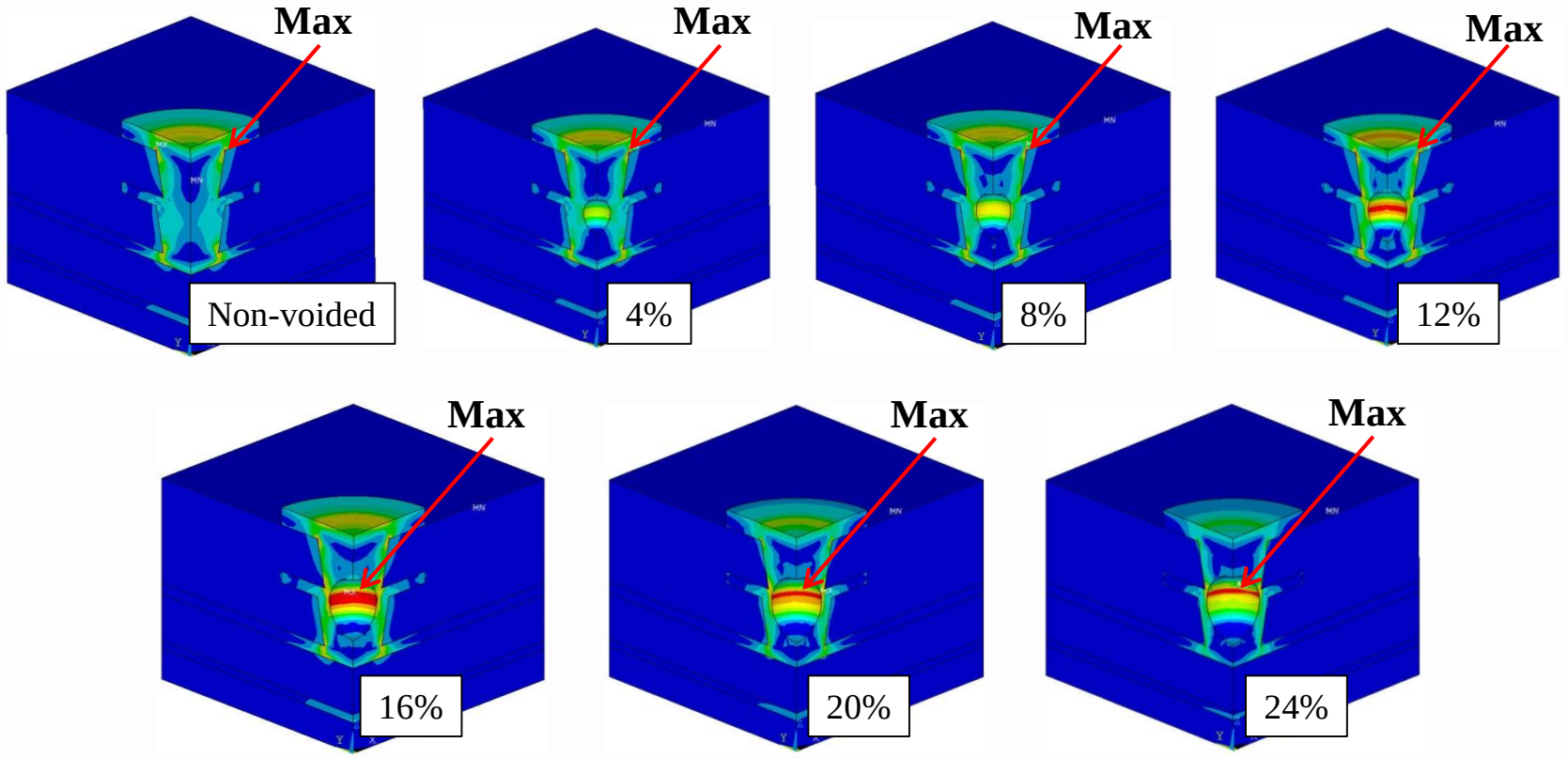


- Note: the stresses are normalized based on the maximum von Mises stress of the non-voided microvia.

- The maximum von Mises stress first declines and then increases with void size.
- The microvia structure is more compliant with a small void, which is beneficial up to a certain void size (about 0.16).
- When the voids get larger than the cross-over point, the thinner microvia walls lead to higher stress levels because there is less material to support the thermal load.

Change of Maximum Stress Site

- As the void size increases, the site of maximum von Mises stress (potential failure site) changes from the microvia upper pad corner to the void borders, where the thinnest microvia wall is located.



Conclusions

An FEA study of effects of process-induced defects on thermomechanical stress in microvias showed:

- Stacked microvias had larger maximum stress than single-level microvias.
- Partially filled microvias had a higher stress level than fully copper-filled.
- Voids were found to raise microvia stress levels when the void size exceeded a critical value.
  - The critical size is expected to be sensitive to void shape, location, and microvia characteristics.
- The stress increase due to a large void exceeds that due to the equivalent amount of incomplete filling.

Thank you.

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