"Reliability of Stacked Microvia"

Hardeep Heer & Ryan Wong

FTG Corp.

Abstract

Reliability of Microvia has been a concern since microvias were introduced to our industry. This study was designed to understand the reliability of Type 1, Type 2, and Type 3 Microvias. Reliability Test Coupon design was developed in co-operation with PWB Interconnect to include up to four stacks of microvias placed on and off a buried via. Standard FR4 material, meeting the requirement of IPC-4101/24, was selected and IST thermal cycling was chosen as a reliability test method. Staggered microvias were not considered because previous testing has shown that staggered microvias are as reliable as single stage microvias. It was also decided to have all the microvias plated shut during the copper plating process. Samples were produced as one lot, utilizing FTG's standard manufacturing processes. Efforts were made to include all possible test conditions required to understand microvia reliability.

Introduction:

The Printed Circuit Board industry has seen a steady reduction in pitch from 1.0mm to 0.4mm; a segment of the industry is even using or considering a 0.25mm pitch. This has increased the use of stacked microvias in these designs. The process of stacking microvias has been practiced for several years in handheld devices; however, the devices generally do not operate in harsh conditions. Type 1 and Type 2 microvias have been tested over the years and have been found to be very reliable. We do not have enough test data for 3 and 4 stack microvias when placed on and off buried via. The main objective of this study was to understand the reliability of 3 and 4 stack microvias placed on and off a buried via.

Board and Coupon Design:

A 2.25mm (0.090") thick eighteen layer board was designed (see Fig.1). Microvias with a diameter of 0.15mm (0.006") were ablated from layers 1-3 and layers 18-16 for 2 stacks, layers 1-4 and layers 18-15 for 3 stacks and layers 1-5 and layers 18-14 for 4 stacks. Buried vias were between layers 3-16, 4-15 and layers 5-14, respectively. All microvias were plated shut.

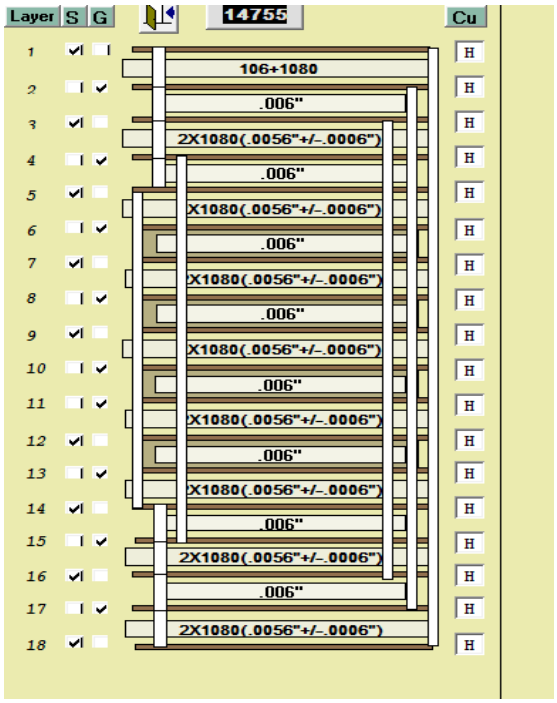


Fig. 1: Design Stackup

Coupons were designed for 2/3/4 stacks (See Fig.2), on and off buried vias and pitches of 0.8mm (0.032) and 1.0mm (0.40") as controlled variables. Each variation was placed in a sub-panel form (see Fig.3). Six of these subs were placed on an 18x24 panel. In all, each panel contained 6 on buried via and 6 off buried via IST coupons.
There were a total of 568,512 microvias per panel and 3 of such panels were produced.

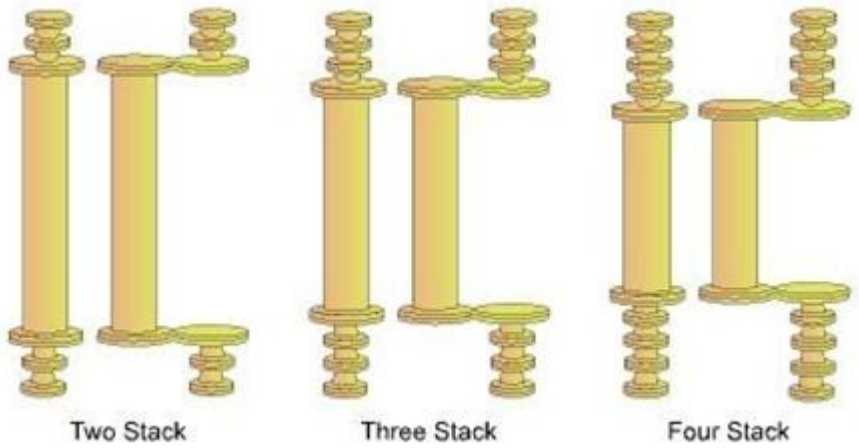


Fig. 2: Via Structure Diagram

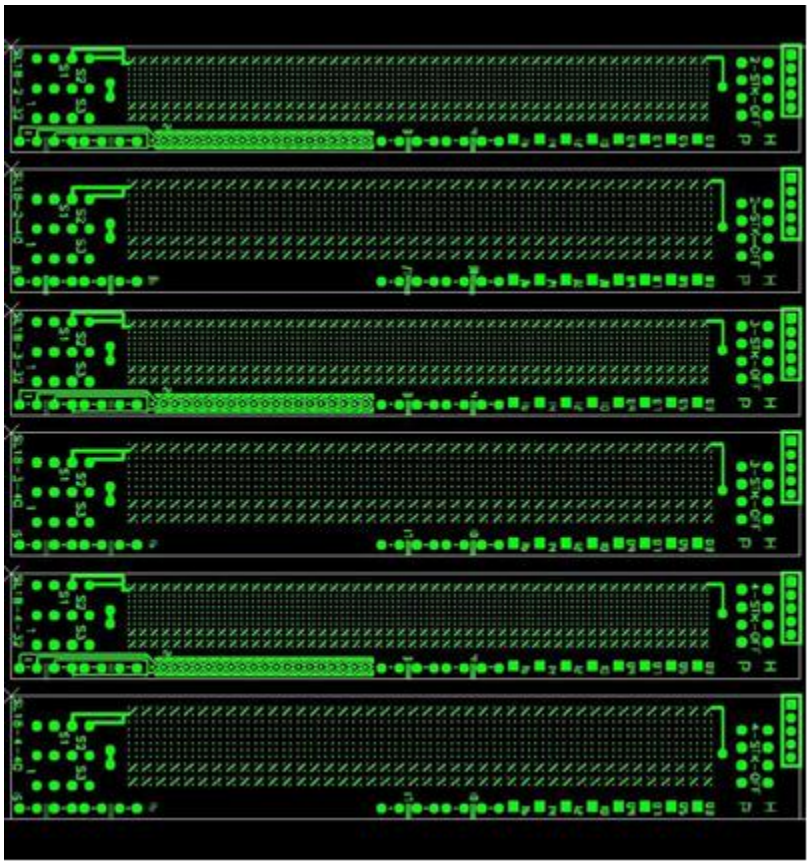


Fig.3: Sub-Panel Coupon Layout

Each coupon contained a power sense (P), one circuit of microvia sense (S1), one of buried via sense (S2) and one combined microvia and buried via sense (S3), as depicted in Figure 4. For the scope of this project, only sense P, S1 and S3 were measured.

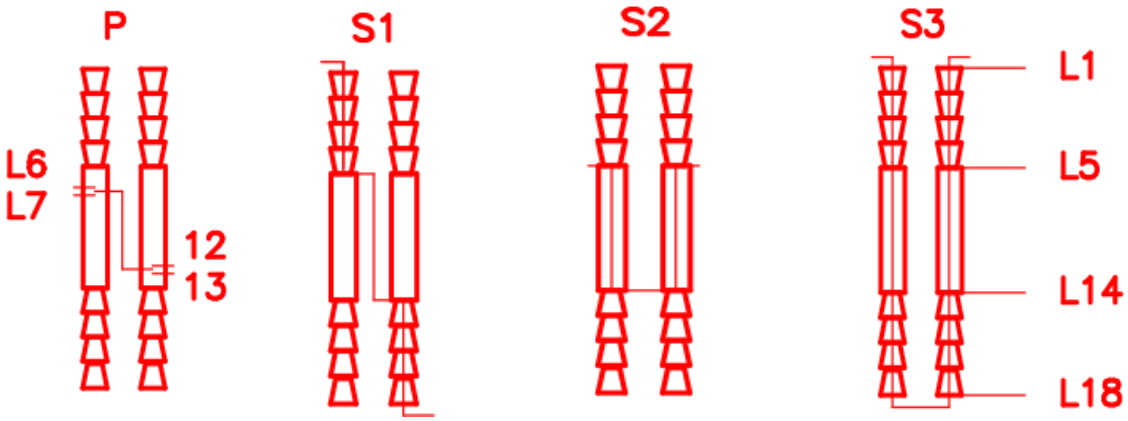


Fig.4: Circuit Sense Summary

Test Method and Test Parameters:

Preconditioning:

Two pre-conditioning cycles were selected.

1. 6x@245ºC
2. 6x@260ºC

Pre-conditioning was done using the IST heating method. Capacitance testing was done on as-received coupons, during cycling and after cycling. A delta of > -4% was considered as a sign of degradation. Sections were done to evaluate and confirm the damage to the vias and material.

Thermal cycling:

IST test method was used for thermal cycling. Below are the various test conditions employed:

Pre-Conditioning	Cycling Temperature	Number of Cycles
6x@245ºC	150ºC	1,000
6x@260ºC	150ºC	1,000
6x@260ºC	170ºC	1,000
6x@260ºC	180ºC	1,000

A starting test temperature of 150ºC was selected. Based on the results, the temperature was increased to 170ºC and 180ºC incrementally.

Follow-on testing was conducted on 3 & 4 stacks from coupons that were cycled at 150ºC and 170ºC for 1,000 cycles in an attempt to instigate failure at higher temperature. 100 additional cycles at 180ºC were conducted. Furthermore, all pre-conditioned failures were tested at 190ºC for 100 cycles. This was done to validate preconditioning failures.

Data Collection & Analysis:

Data was collected for pre-conditioning and thermal cycling. During pre-conditioning at 245ºC, four coupons failed. A second set of coupons was tested at 6x@260ºC. Out of 236 coupons tested, only 24 coupons failed. The failed coupons (for both 245ºC and 260ºC) were set aside for further analysis and the coupons that passed were thermal cycled.
During pre-conditioning testing, it was observed that some of the coupons were showing higher than expected change in resistance. It should be kept in mind that a 10% or greater change in resistance limit was set in the 1960's for through hole technology with the baseline resistance value set after pre-conditioning.

A 10% change was observed after conditioning and stabilized after that. After pre-conditioning, the upper limit in resistance change was raised 50% and proceeded to thermal cycling. The change in resistance was monitored continuously. It was observed that the change in resistance in almost all cases had stabilized after pre-conditioning. Below is the chart that outlines the number of assembly failures where resistance change exceeded 50% at 245ºC and 260ºC pre-conditioning and 150ºC to 180ºC thermal cycling.

Table 1: Stacked Microvia Structures Reliability

Assy. Simulation	IST Test Temp	# of Assy. Failures (>50% Resistance Change)		
		2 Stack	3 Stack	4 Stack
6X 245ºC	150ºC	0	0	4
6X 260ºC	150ºC	0	5	6
6X 260ºC	170ºC	0	1	3
6X 260ºC	180ºC	0	5	4
TOTAL		0	11	18

The experimental data showed that all of the coupons failed at Sense 3, which is a microvia and buried via combination. No failures were observed at Sense 1 (pure microvia). At a 10% resistance change limit, the number of failures increases (see Table 2). This data is based upon 12 coupons of each protocol tested.

Table 2: % IST - Resistance Change >10% as Failures

Assy. Simulation	IST Test Temp	# of Cycles	% IST Failures (>10% Resistance Change)			# of IST Failures Consistent With Assy Failures
			2 Stack	3 Stack	4 Stack	
6X 245ºC	150ºC	1000	0%	0%	25%	3 of 3
6X 260ºC	150ºC	1000	0%	0%	25%	3 of 11
6X 260ºC	170ºC	1000	75%	25%	63%	2 of 4
6X 260ºC	180ºC	1000	91%	67%	44%	4 of 6

Assembly Simulation vs. Thermal Cycling

Further analysis was done to see what percentage of failures detected during assembly simulation (pre-conditioning) were also detected during IST testing. Table 3 below summarizes the failures detected.

Table 3: % IST - Resistance Change >50% as Failures

Assy. Simulation	IST Test Temp	# of Cycles	# of IST Failures (>50% Resistance Change)			# of IST Failures Consistent With Assy Failures
			2 Stack	3 Stack	4 Stack	
6X 245ºC	150ºC	1000	0%	0%	18%	2 of 5
6X 260ºC	150ºC	1000	0%	0%	17%	2 of 11
6X 260ºC	170ºC	1000	8%	0%	18%	2 of 4
6X 260ºC	180ºC	1000	73%	17%	22%	1 of 6

Table 3 above shows that all failures seen during assembly simulation were not detected during IST testing. There two possible reasons for this:

1. The test temperature needs to be raised even higher than 180ºC to cause this failure.
2. Material was delaminated and once that happens, the stresses during the IST test are absorbed by the delamination and it does not affect via reliability. Further evaluation is needed to determine the root cause.

To test the hypothesis of insufficient temperature, 24 of the pre-conditioning failure coupons were subjected to 190ºC IST test temperature. Over 90% of the failures were detected under these conditions.

Via To Via Pitch

To understand if the pitch made any contribution to reliability failures, the data for 3 and 4 stacks were sorted by 0.8mm (0.032") and 1.0mm (0.040") via to via pitch and data was further segregated by on buried and off buried vias. Pre-conditioning was also taken into account. Table 4 and 5 below shows the yield for 3 and 4 stacks by pre- conditioning temperature, on / off buried vias and 0.8mm (0.032") and 1.0mm (0.040") pitch.

Table 4: 3-Stacks Failures found during Assy. Simulation

3 Stack Structure					
Assy. Simulation	On Buried Via		Off Buried Via		Yield
	0.032" / 0.8mm	0.040" / 1.0mm	0.032" / 0.8mm	0.040" / 1.0mm	
6X 245ºC	0	0	0	0	100%
6X 260ºC	5	1	2	3	72%

Table 5: 4- Stacks Failures found during Assy. Simulation

4 Stack Structure					
Assy. Simulation	On Buried Via		Off Buried Via		Yield
	0.032" / 0.8mm	0.040" / 1.0mm	0.032" / 0.8mm	0.040" / 1.0mm	
6X 245ºC	0	0	3	1	87%
6X 260ºC	1	3	5	4	60%

As mentioned previously, 2 stack microvias for all the combinations did not show any failures at 150ºC for both pre-conditioning cycles. At 170ºC, one failure was observed on Sense 3 at an off buried via location, indicating that it is a buried via failure rather than a microvia failure, since there were no failures on Sense 1. It was observed that 9 out of 11 coupons failed at a thermal cycle temperature of 180ºC. These failures again were on Sense 3, indicating that the failure was located at the buried via. The data is shown below in Table 6.

Table 6: 2- Stacks Microvia Structures Reliability

Assy. Simulation	IST Test Temp	# of Cycles	On Buried Via		Off Buried Via	
			0.032" / 0.8mm	0.040" / 1.0mm	0.032" / 0.8mm	0.040" / 1.0mm
6X 245ºC	150ºC	1000	0 of 6	0 of 6	0 of 7	0 of 7
6X 260ºC	150ºC	1000	0 of 3	0 of 3	0 of 3	0 of 3
6X 260ºC	170ºC	1000	0 of 3	0 of 3	1 of 3*	0 of 3
6X 260ºC	180ºC	1000	3 of 3*	0 of 3	2 of 2*	3 of 3*

Structure reliability data for 3 and 4 stacks is shown in Tables 7 and 8. Three stacks did not have any failure but 4 stacks had one failure. At 180ºC, failures are observed for 4 stack microvias at both on and off locations. The plots of resistance over time indicate that these coupons exceed the 10% resistance change limit and continue to gradually increase. This sort of behavior is indicative of material degradation rather than a via structure failure because of the gradual nature of the resistance change. A via structure failure would cause a significant increase in resistance.

Table 7: 3- Stacks Microvia Structures Reliability

Assy. Simulation	IST Test Temp	# of Cycles	On Buried Via		Off Buried Via	
			0.032" / 0.8mm	0.040" / 1.0mm	0.032" / 0.8mm	0.040" / 1.0mm
6X 245ºC	150ºC	1000	0 of 6	0 of 6	0 of 7	0 of 7
6X 260ºC	150ºC	1000	0 of 3	0 of 3	0 of 3	0 of 3
6X 260ºC	170ºC	1000	0 of 3	0 of 3	0 of 3	0 of 3
6X 260ºC	180ºC	1000	0 of 3	0 of 3	0 of 3	2 of 3

Table 8: 4- Stacks Microvia Structures Reliability

Assy. Simulation	IST Test Temp	# of Cycles	On Buried Via		Off Buried Via	
			0.032" / 0.8mm	0.040" / 1.0mm	0.032" / 0.8mm	0.040" / 1.0mm
6X 245ºC	150ºC	1000	0 of 7	0 of 7	3 of 7	2 of 7
6X 260ºC	150ºC	1000	0 of 3	0 of 3	2 of 3	0 of 3
6X 260ºC	170ºC	1000	0 of 3	0 of 3	2 of 2	0 of 3
6X 260ºC	180ºC	1000	1 of 3	0 of 3	0 of 0	1 of 3

IST Data - Analysis of Thermal Cycling:

As outlined in the test method, the process was defined to start testing of coupons pre-conditioned 6x245ºC at a thermal cycle temperature of 150ºC for 1,000 cycles. If no microvia failures were observed, then the pre- conditioning temperature would be raised to 260ºC, while keeping the thermal cycling temperature at 150ºC. If still no failures were observed, the thermal cycle temperature would be increased to 170ºC for 1,000 cycles. If limited failures were observed, then a final thermal cycling temperature increase to 180ºC would be conducted.

Only five 4 stack coupons failed during pre-conditioning at 6x245ºC. There were no failures identified during thermal cycling at 150ºC. The same test was repeated with a pre-conditioning temperature of 260ºC. Out of 236 coupons tested, 24 coupons failed at Sense 3 (combination of buried and microvia) on the 4 stack via structure. The experimental objective was to evaluate microvias and this did not show any microvia failures. Cross-sectional analysis of the coupons showed no failure in via structures but material degradation was observed (see Image 3, Fig. 5 below).

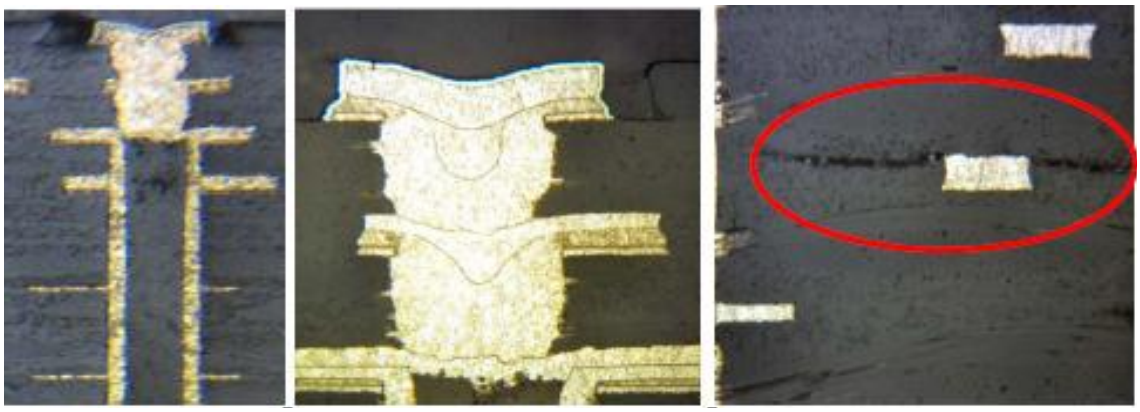


Image 1 Image 2 Image 3

Fig. 5: Two Stack Microvias after 6x@ 260°C Pre-Conditioning and 1, 000 cycles at 150°C

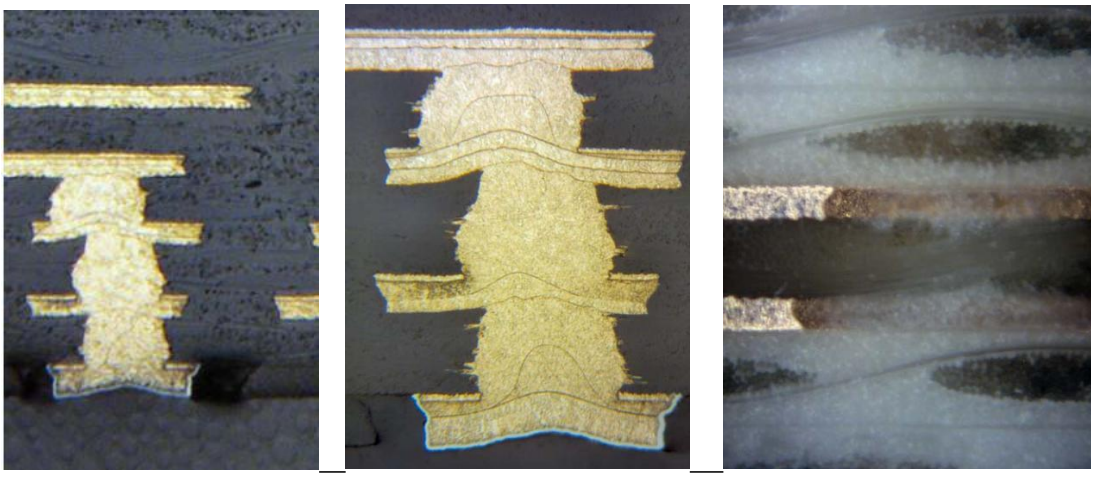


Image 4 Image 5 Image 6

Fig. 6: Three Stack Microvias after 6x@ 260°C Pre-Conditioning and 1,000 cycles at 150°C

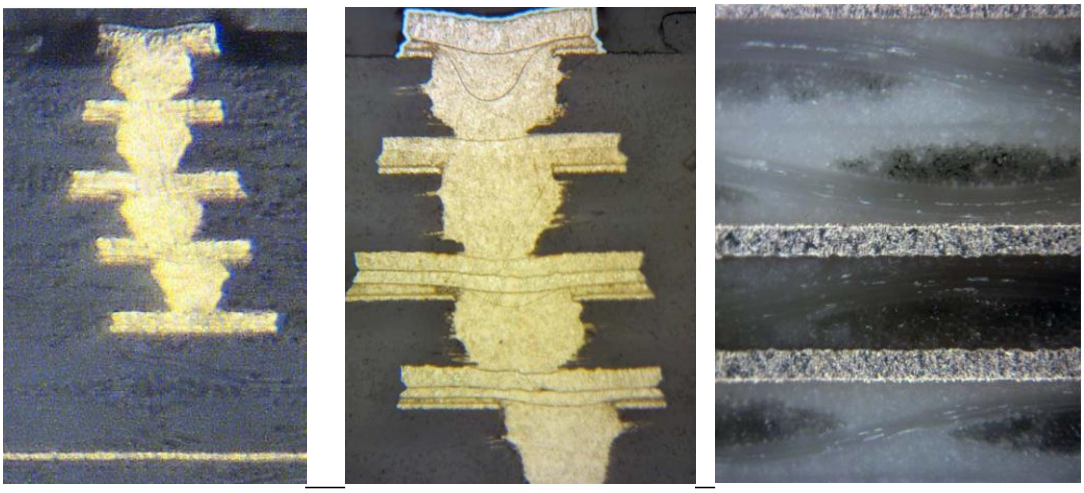


Image 7 Image 8 Image 9

Fig. 7: 4 Stack Microvias after 6x@ 260°C Pre-conditioning and 1,000 cycles at 150°C

At this point the cycling temperature was increased to 170ºC and a new set of coupons that were pre-conditioned at 260ºC were tested. Failures for 2-stack and 4-stack structures were identified and these failures were also found on Sense 3. Since the test temperature of 150ºC and 170ºC did not show microvia failures, the test temperature was increased to 180ºC and another set of coupons preconditioned at 6x260ºC was tested.

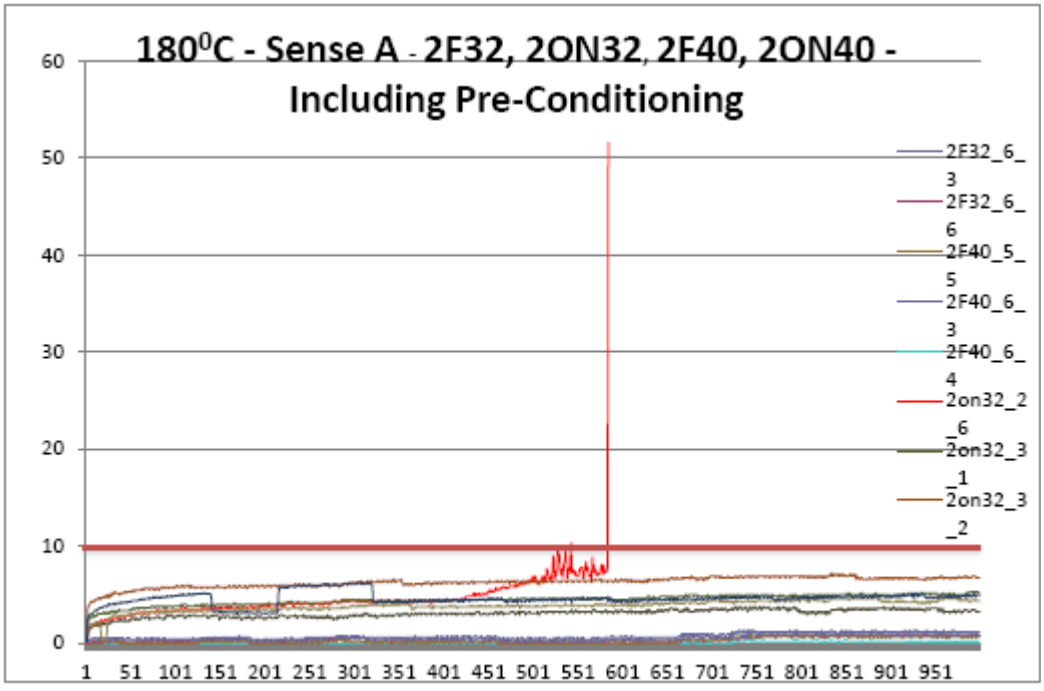
Change in resistance was monitored throughout pre-conditioning and thermal cycling. Initially, a greater than 10% change in resistance limit was raised to 50% change while still monitoring the rate of change and slope of the curve. During preconditioning, a rise in resistance change was noticed. This resistance change stabilized and in the majority of cases a very slow rate of change was measured.

The data below shows that there can be a resistance change of up to 10% during pre-conditioning. Cross-sectional analysis was completed after 1,000 cycles on the coupons which had shown a higher degree of resistance change during preconditioning, but had survived 1,000 cycles. No abnormalities in the cross-sections could be identified. At this stage, the data was analyzed in two ways. The first method included the resistance change during pre- conditioning while the second method excluded the resistance change during pre-conditioning. In the second method, a 10% change in resistance during thermal cycling was considered a failure.

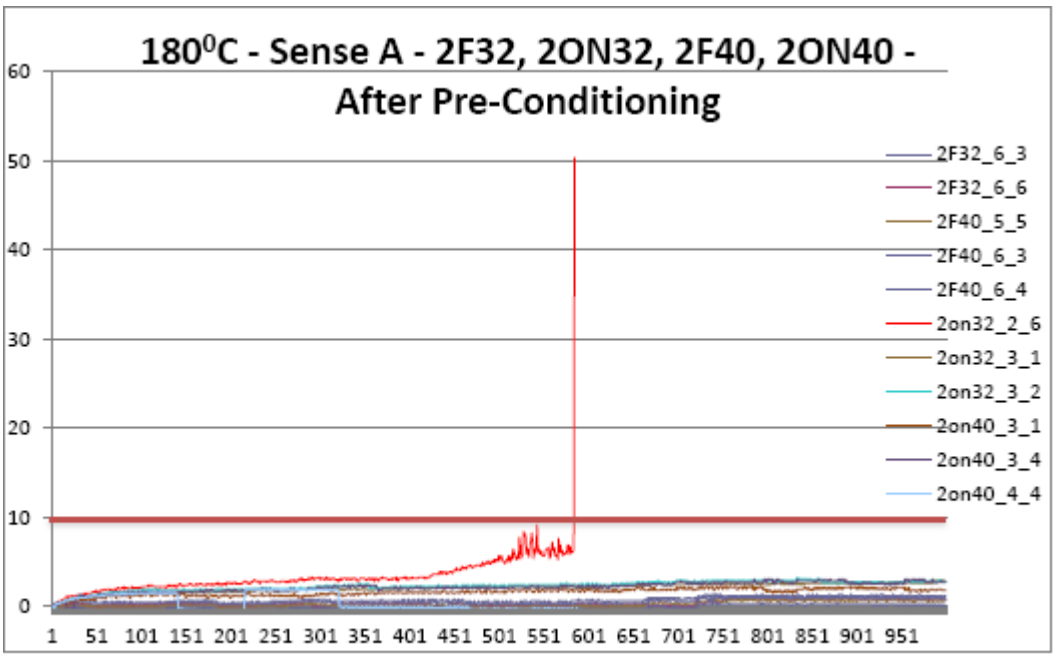
Considering the amount of data available and the scope of this study, only data from 180ºC thermal cycling temperature was analyzed in detail. The graphs below include both sets of data where pre-conditioning change in resistance was factored and not factored.

Plot 1 through Plot 4 shows data for two stack on and off buried vias. Plot 1 includes pre-conditioning change in resistance, whereas Plot 2 is showing data from after pre-conditioning to 1,000 cycles. Sense A has one microvia failure at the 585th cycle. The failure is clearly indicated by a straight vertical line. All other data points are well below 10% resistance change.

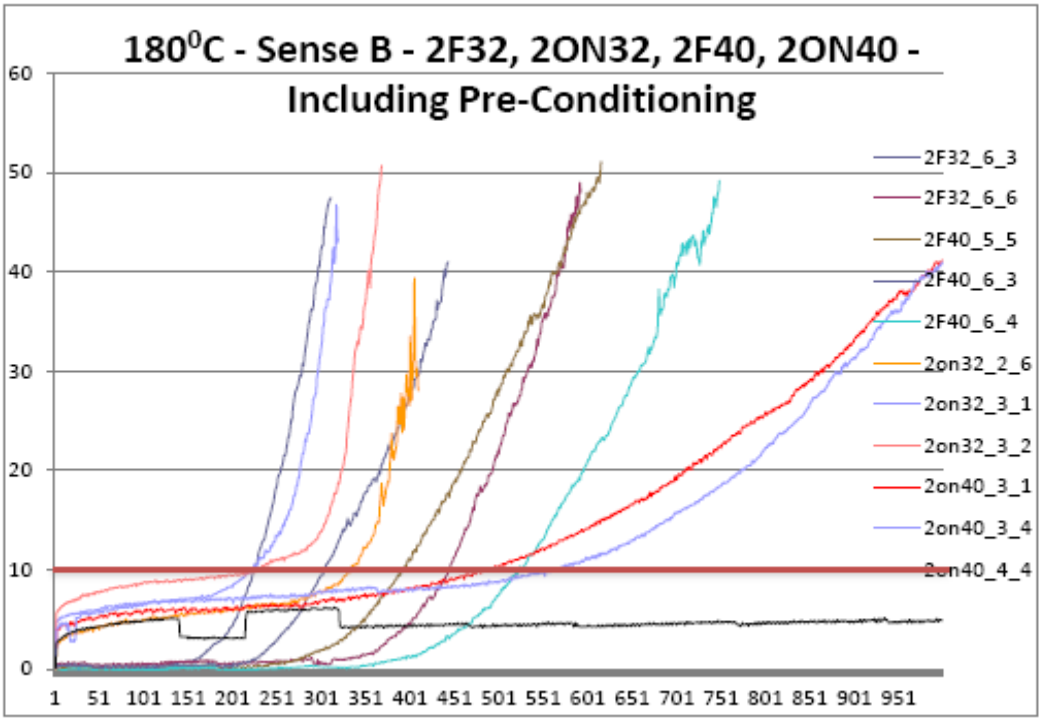
Plot 2 is for Sense B and shows much different results. Majority of the coupons show a steeper upward curve indicating that vias are degrading fast. This is being caused by the test temperature of 180ºC. The test temperature is above the Tg of the material, resulting in almost 10 times the thermal expansion factors below Tg of the material. It must be understood that the thermal cycling temperature is above the Tg of the material and at this point, shear forces are playing a role in the barrels' failure mode. It is also believed that the length of the barrel is playing a significant role here. The barrel of the buried via below the 2-stack microvia structure is the longest of all the combinations in this design and at this temperature the thermal expansion is extremely high. Even under these severe conditions, the coupons were able to reach a mean IST cycle of 452 which is indicative of reliable copper plating structure.



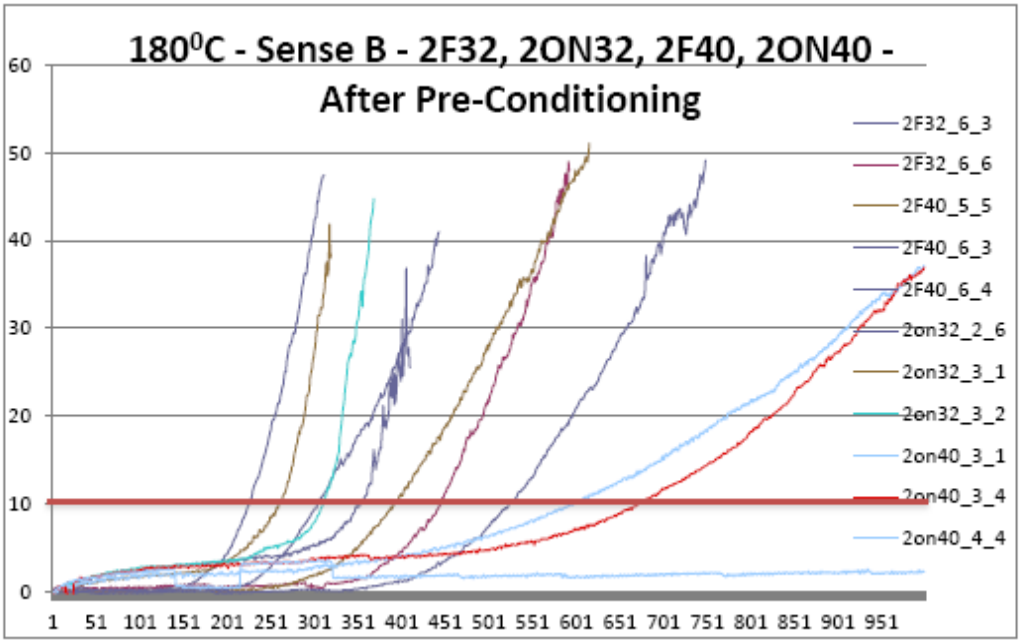
Plot 1 – 2 Stack Microvias off Buried via – Sense A



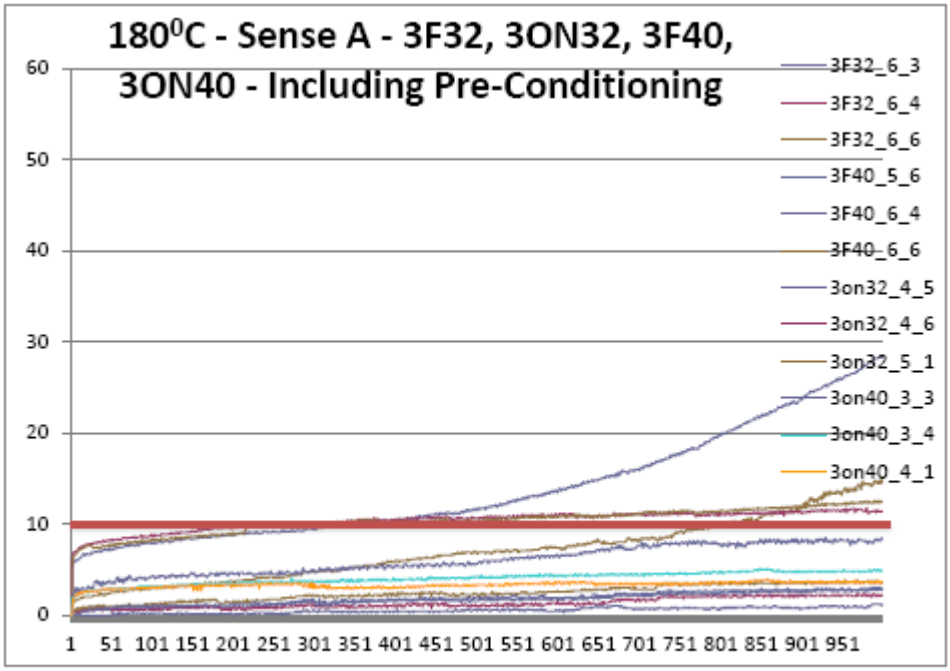
Plot 2 – 2 Stack Microvias on Buried via – Sense A



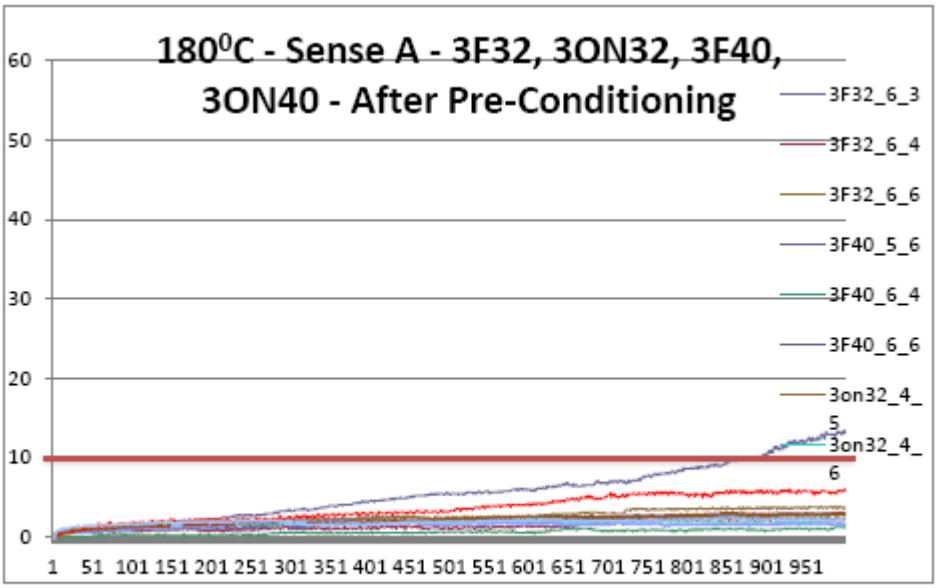
Plot 3 – 2 Stack Microvias Off Buried via – Sense B



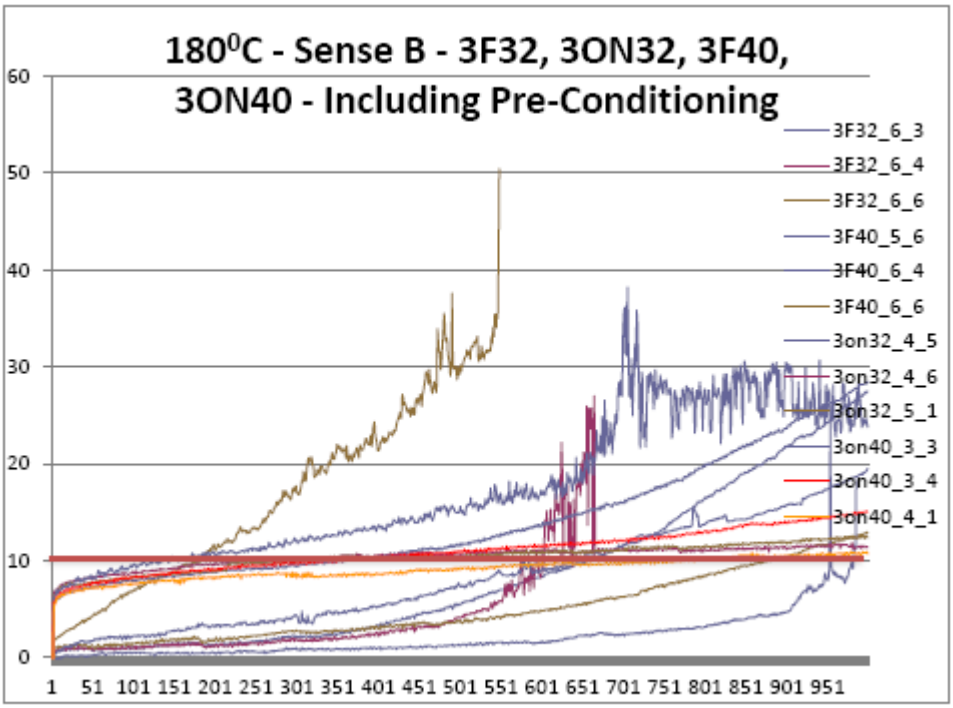
Plot 4 – 2 Stack Microvias On Buried via – Sense B



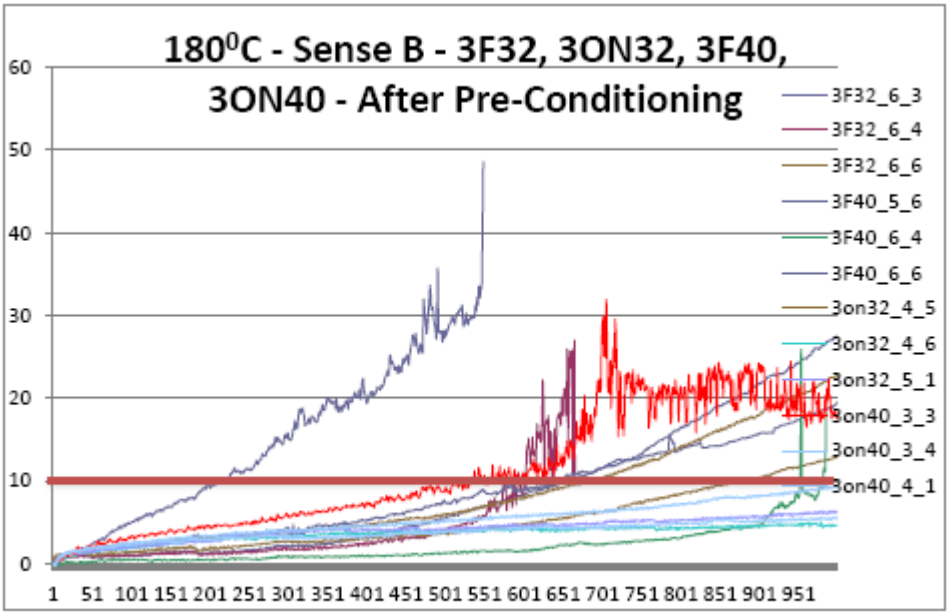
Plot 5 – 3 Stack Microvias on Buried via – Sense A



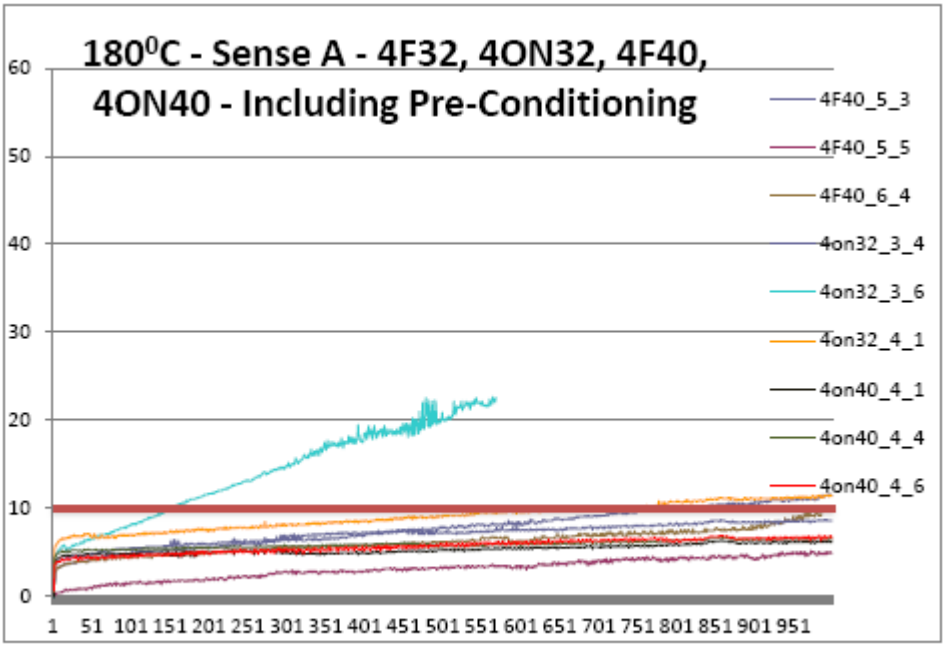
Plot 6 – 3 Stack Microvias on Buried via – Sense A



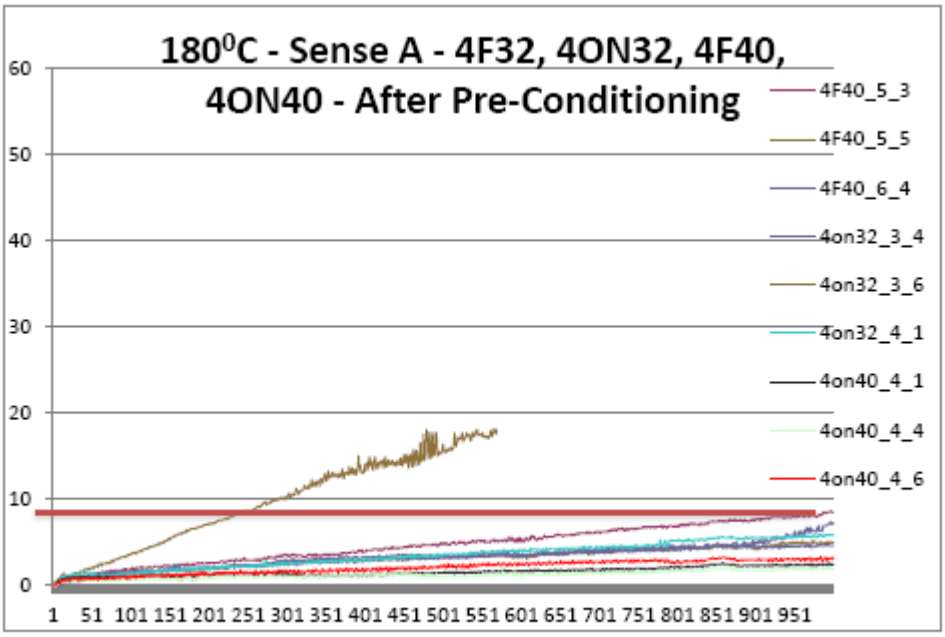
Plot 7 – 3 Stack Microvias on Buried via – Sense B



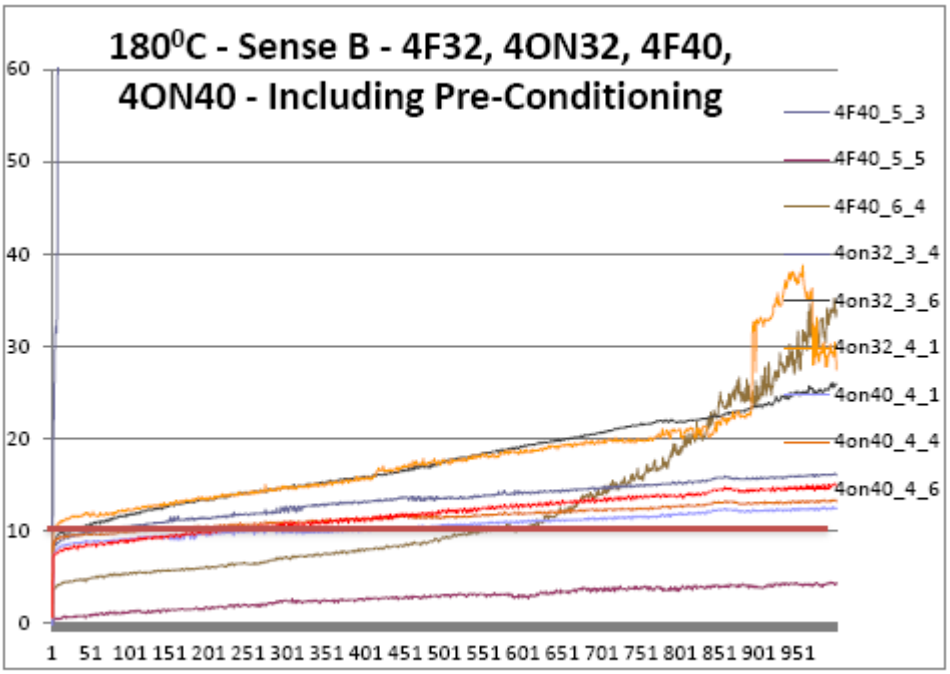
Plot 8 – 3 Stack Microvias on Buried via – Sense B



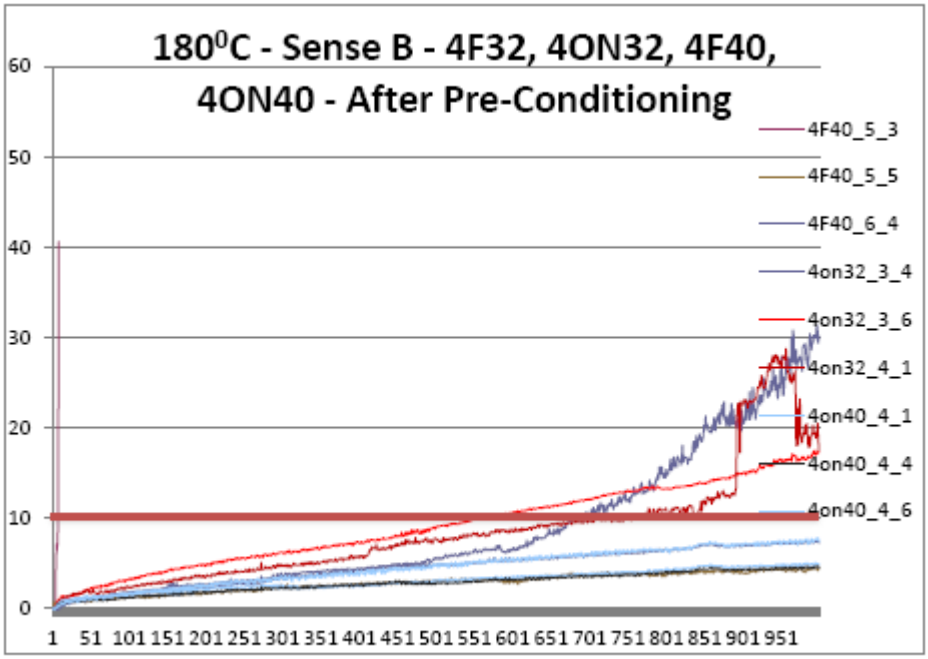
Plot 9 – 4 Stack Microvias on Buried via – Sense A



Plot 10 – 4 Stack Microvias on Buried via – Sense A



Plot 11 – 4 Stack Microvias on Buried via – Sense B



Plot 12 – 4 Stack Microvias on Buried via – Sense B

Results for 3 and 4 stacks were different than what we saw for 2 stacks. The change in resistance for one 3 stack microvia (Sense A) went over 10% at 893 cycles. The change in slope for this microvia is still gradual. All other microvias are still showing a change in resistance below 7%. Similar to 2 stack microvias, Sense B is showing different results than Sense A. Here we see one test coupon starting to degrade at 216 cycles.
There are several other coupons starting to move above the 10% threshold resulting in one complete failure at 543 cycles. The other coupon crossed the 10% threshold at 557 cycles and continues to degrade over the remaining test period without completely failing. Only one more coupon had a complete failure at 949 cycles.
Four stack microvias show an improvement over 2 and 3 stacks. For Sense A, there is one microvia coupon that starts to show degradation at 280 cycles and has a complete failure at 561 cycles. All other coupons for Sense A stayed below a 10% change in resistance. Sense B also shows improved results over 2 and 3 stack coupons. The first coupon to cross 10% limit had completed 570 cycles but didn't show a complete failure. This coupon reached a maximum resistance change of 28% at 944 cycles. The third coupon reached 695 cycles before crossing the 10% change threshold and showed a failure at 993cycles.

It is interesting to note that Sense B showed higher degree of failure for 2 stacks than for 3 and 4 stacks. This confirms the hypothesis that the barrel length of buried vias is contributing significantly to the degree of failures. It must be kept in mind that the material used for the test is an FR4 material with a Tg of 173^0C. Thermal expansion for this material in the Z-axis is 44ppm below Tg and 255ppm above Tg. A test temperature of 180^0C induces a tremendous amount of stress on the material. It also worth noting that this test vehicle has gone through 4 lamination cycles and 6 pre-conditioning cycles at 260^0C. All these lamination and thermal cycles have resulted in degradation of the material to an extent.

Conclusion:

This study was a preliminary study and the objective was to understand the behavior and reliability of stacked microvias based on the number of stacks, the pitch between the vias and the effect of stacking microvias on a buried via compared to off a buried via. A secondary objective was also to understand FTG's manufacturing process for multiple stacked microvias, since this is not yet a typical design requirement in the Aerospace and Defense industries.
The test data shows that stacked microvias placed on a buried via are in themselves as reliable as stacked microvias off the buried via. Although Sense B data shows a higher failure rate, it is believed that the failure mode is related to the buried via and material degradation rather than a microvia failure. Two-stack microvias located on buried vias

performed worse than the other on-buried via structures, but it is hypothesized that this is caused by the longer barrel length of the buried via in the board design. The length of barrel of buried vias has a higher degree of effect on the IST results for test temperatures above the Tg of the laminate. Shorter buried vias are more reliable even when operating at temperatures above the Tg of the material. Increasing the number of lamination cycles and higher pre-conditioning temperature also contributed to a higher degradation effect on standard laminates.

Increasing the number of stacks did not appear to have a major effect on failures. Although resistance increased nominally in Sense A measurements, the reliability of the microvias generally was maintained b e l o w the resistance change threshold. However, the number of stacks introduces registration challenges during the manufacturing process. A robust registration system is required to ensure that the microvias are registered in a controlled manner to reduce variation that can result in poor connectivity to the underlying plated shut microvia. Reducing via pitch from 1.0mm (0.04") to 0.8mm (0.032") also had a marginal effect on reliability.

A conventional IST cycling temperature to test microvias may not be the optimal temperature to test microvia reliability. Resistance changes of greater than 10% should be the failure criteria after pre-conditioning. A gradual rise in the resistance change plot is an indication of degradation of the material and is not necessarily indicative of avia failure. Further testing will be required to understand the effect on microvias when resistance is gradually increasing above the 10% threshold. This study also showed that the selection of material is critical to product reliability. If the circuit board application demands performance under temperatures higher than the material's Tg, then a material with a higher Tg should be selected.

This was a preliminary study to investigate the general reliability of stacked microvia structures. The number of variables being evaluated required a significant number of test coupons. This resulted in limiting the sample size for higher temperature cycling. With these results and observations on test temperatures and failure modes, further testing with a narrowed scope can be completed to determine statistically proven reliability of different microvia structures. This study has provided a foundation of knowledge that can be built upon by a multitude of testing in the future.

Hardeep Heer,
VP Engineering & CTO
Firan Technology Group (FTG)

Ryan Wong,
Engineering Manager
Firan Technology Group (FTG)

Acknowledgement:
Authors would like to thank Bill Birch and his team of PWB Interconnect solutions Inc. for their help in coupon design and testing.

APEX EXPO IPC
NEW IDEAS ... FOR NEW HORIZONS
MARCH 25-27, 2014
MANDALAY BAY RESORT AND CONVENTION CENTER
LAS VEGAS, NEVADA

Stacked - on/off Buried Via - Microvia Reliability

FIRAN TECHNOLOGY GROUP

Hardeep Heer
VP Engineering & CTO Ryan Wong Engineering Manager

Introduction

- As a PWB manufacturer we are comfortable manufacturing single and 2 stack microvia structures. That meets the stringent requirement specified by our customers.
- Study was undertaken to investigate the further addition of three and four level structures to determine if the reliability will be negatively affected.

Scope

- Initial investigation into manufacturing capability and quantification of reliability in HDI Structures
- Build 2/3/4 level of Microvia structures in various design configurations.
- Test structures before and after lead free assy. temperatures (6X260^0 C)
- Measure material integrity using capacitance methodology.
- Validate the testing methodology and test temperature to confirm microvia reliability.
- Establish relative reliability of stacked microvia on buried and offset to buried.
- Compare the number of stacks in relation to grid size and position to the buried via.

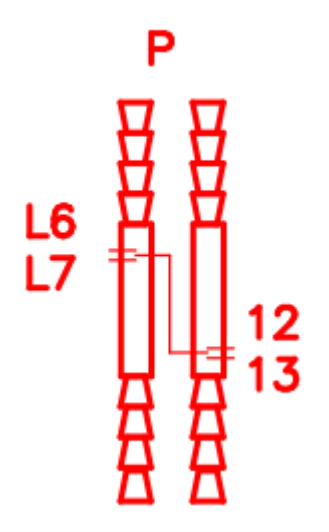
2/3/4 Levels of Microvia Structures

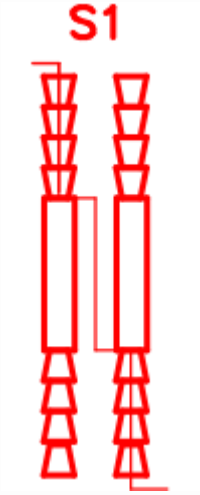
- 18 Layer construction, all configurations (2/14/2, 3/12/3, 4/10/4) built in single test panel.
- Total board construction 0.090”/2.25mm.
- Lead free compatible High Tg FR4 material used.
- 0.006”/0.15mm ablated into 0.0035”/0.085mm dielectric.
- 0.008”/0.2mm buried via, filled with Non-conductive epoxy.
- Two via to via spacing’s: 0.032”/0.8mm and 0.040”/1mm.
- All microvia structures copper plated shut.
- Stack structures ablated on and offset to the buried vias.
- Over 500,000 via / panel (3 panels built).

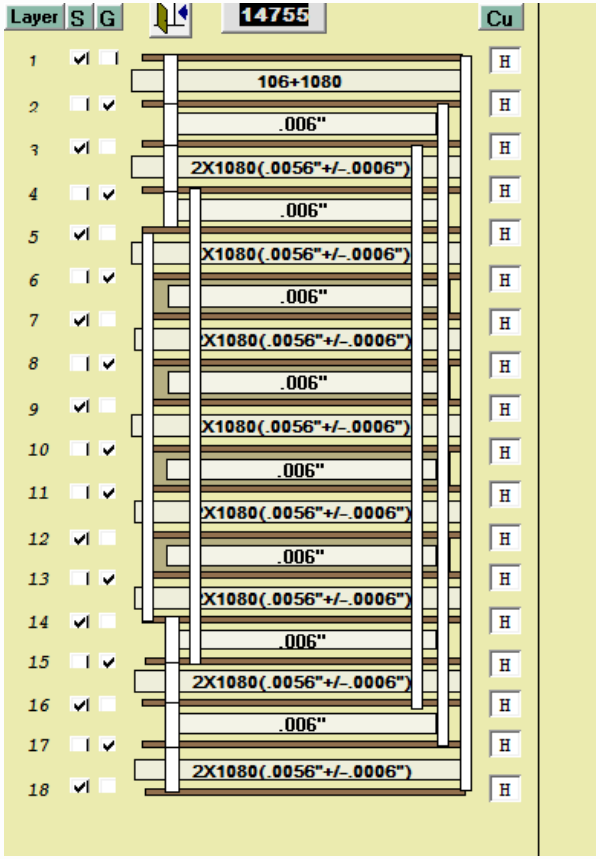
Via Count Summary

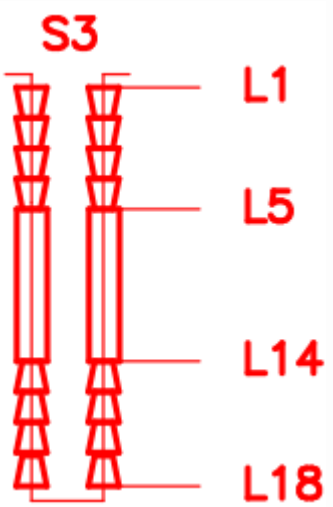
Stack	Grid	On	Off	Buried	Microvia	Coupons 12X
2	32	X		1248	4992	29,952
			X	1248	4992	29,952
	40	X		1008	4032	24,192
			X	1008	4032	24,192
3	32	X		1248	7488	44,928
			X	1248	7488	44,928
	40	X		1008	6048	36,288
			X	1008	6048	36,288
4	32	X		1248	9984	59,904
			X	1248	9984	59,904
	40	X		1008	8064	48,384
			X	1008	8064	48,384
Total of Via Type				81216		487,296
Total of all Vias Per Panel						568,512

Board Stack up

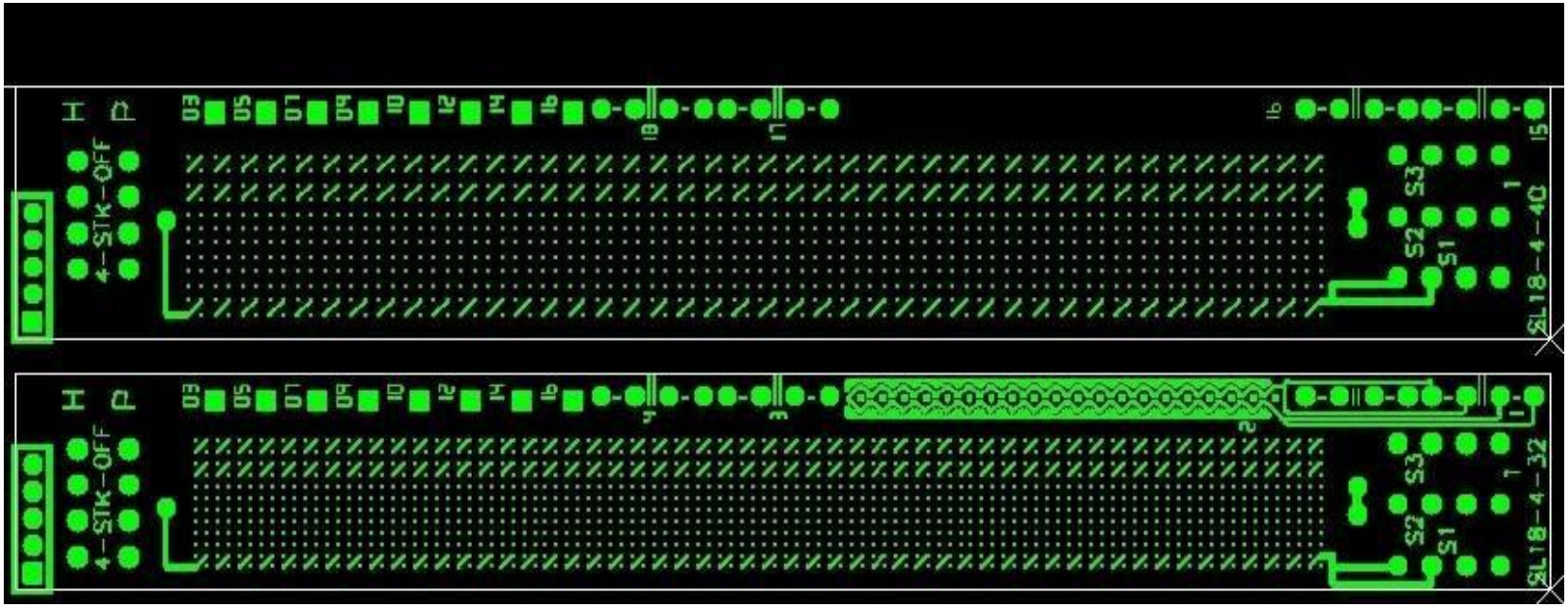








Test Coupon Layout



Exposure to Lead Free Assy. Thermal Cycles (6X 245^0 C & 6X 260^0 C)

- Simulated assy. cycles were created on IST test equipment.
- Continuous electrical monitoring completed throughout each assy. cycle.
- Five failures found during 6X 245^0 C.
- 24 failures found during 6X 260^0 C (only 3 and 4 stack structures)
- Capacitance testing completed after assy.

Material Integrity Using Capacitance Methodology

- Capacitance measurements taken between each internal pwr/gnd plane.
- Baseline measurements taken in as build condition, then compared to measurement after assy. and end of test.
- Capacitance delta of >-4% after assy. and raised to, >-6% after end of test, indicates onset of material degradation (damage).
- Microsections were completed to confirm or refute material degradation.

Validate the Testing Methodology and Test Temperature

- Utilized Interconnect Stress Testing (IST) to quantify microvia reliability.
- Test temperatures started at 150^0 C, raised to 170^0 C and 180^0 C until failures were detected.
- Continuous electrical monitoring completed throughout testing.
- Coupon testing completed to 1,000 cycles at each temperature level.
- Maximum of three coupons for each configuration at each temperature.

Test Conditions for Stacked Microvia Structures Reliability Testing

- Test combinations-
  - 6X@245ºC – test temp. 150ºC –1,000 cycles
  - 6X@260ºC – test temp. 150ºC – 1,000 cycles
  - 6X@260ºC – test temp. 170ºC – 1,000 cycles
  - 6X@260ºC – test temp. 180ºC – 1,000 cycles
  - Follow on testing on 3 & 4 stacks from coupons tested at 150ºC and 170ºC.
    - 100 Cycles – 180ºC
  - Follow on testing on 3 & 4 stacks from coupons that failed during preconditioning.
    - 100 Cycles – 190ºC

IST Rejection Criteria

- Industry standard (IPC, MIL, JEDEC) requires 10% increase in resistance; established in 1961 for PTV reliability assessment
- Microvia structures fail differently than PTV's – there can be inherent resistance changes that do not necessarily constitute failures
- Two levels of rejection were utilized for this study, comparing the failures at both 10% and 50%

DATA ANALYSIS

Test Results for Stacked Microvia Structures Reliability Testing

Assy. Simulation	IST Test Temp	# of Assy. Failures (>50% Resistance Change)		
		2 Stack	3 Stack	4 Stack
6X 245ºC	150ºC	0	0	5
6X 260ºC	150ºC	0	5	6
6X 260ºC	170ºC	0	1	3
6X 260ºC	180ºC	0	5	4
	TOTAL	0	11	18

- Results based on 12 test coupons for each protocol

Test Results for Stacked Microvia Structures Reliability Testing

Assy. Simulation	IST Test Temp	# of Cycles	% IST Failures (>10% Resistance Change)			# of IST Failures Consistent With Assy Failures
			2 Stack	3 Stack	4 Stack	
6X 245ºC	150ºC	1000	0%	0%	25%	3 of 3
6X 260ºC	150ºC	1000	0%	0%	25%	3 of 11
6X 260ºC	170ºC	1000	75%*	25%	63%	2 of 4
6X 260ºC	180ºC	1000	91%*	67%	44%	4 of 6

* All failures occurred at microvia / buried via locations

- Results based on 12 test coupons for each protocol

Test Results for Stacked Microvia Structures Reliability Testing

Assy. Simulation	IST Test Temp	# of Cycles	# of IST Failures (>50% Resistance Change)			# of IST Failures Consistent With Assy Failures
			2 Stack	3 Stack	4 Stack	
6X 245ºC	150ºC	1000	0%	0%	18%	2 of 5
6X 260ºC	150ºC	1000	0%	0%	17%	2 of 11
6X 260ºC	170ºC	1000	8%*	0%	18%	2 of 4
6X 260ºC	180ºC	1000	73%*	17%	22%	1 of 6

* All failures occurred at microvia / buried via locations (S3 Test Circuit)

Test Results of Failures Found During Assy. Simulation

3 Stack Structure					
Assy. Simulation	On Buried Via		Off Buried Via		Yield
	0.032" / 0.8mm	0.040" / 1.0mm	0.032" / 0.8mm	0.040" / 1.0mm	
6X 245ºC	0	0	0	0	100%
6X 260ºC	5	1	2	3	72%

4 Stack Structure					
Assy. Simulation	On Buried Via		Off Buried Via		Yield
	0.032" / 0.8mm	0.040" / 1.0mm	0.032" / 0.8mm	0.040" / 1.0mm	
6X 245ºC	0	0	3	1	83%
6X 260ºC	1	3	5	4	60%

Test Results for 2-Stack Microvia Structures Reliability Testing

Assy. Simulation	IST Test Temp	# of Cycles	On Buried Via		Off Buried Via	
			0.032" / 0.8mm	0.040" / 1.0mm	0.032" / 0.8mm	0.040" / 1.0mm
6X 245ºC	150ºC	1000	0 of 6	0 of 6	0 of 7	0 of 7
6X 260ºC	150ºC	1000	0 of 3	0 of 3	0 of 3	0 of 3
6X 260ºC	170ºC	1000	0 of 3	0 of 3	1 of 3*	0 of 3
6X 260ºC	180ºC	1000	3 of 3*	0 of 3	2 of 2*	3 of 3*

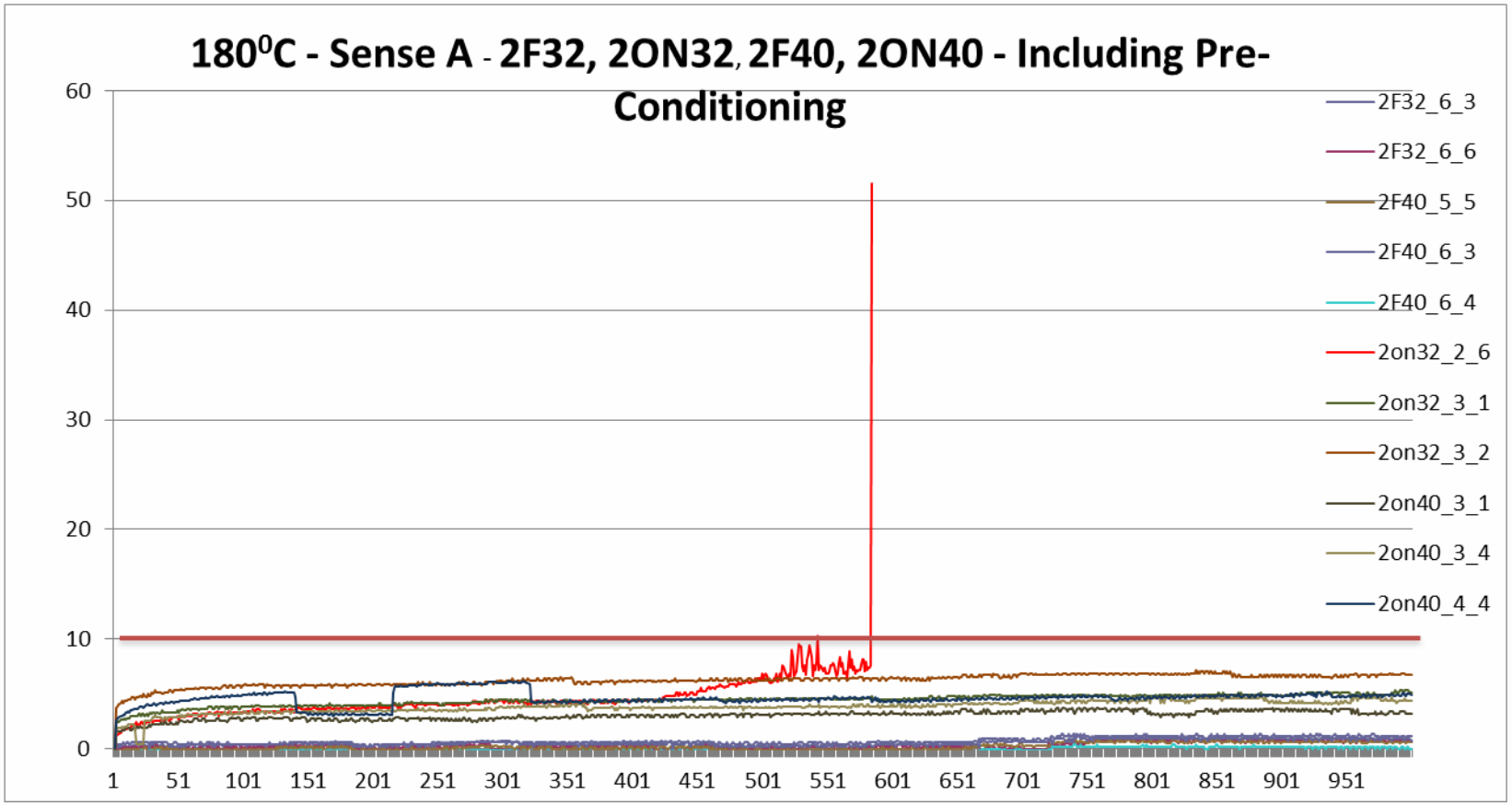
Test Results for 3-Stack Microvia Structures Reliability Testing

Assy. Simulation	IST Test Temp	# of Cycles	On Buried Via		Off Buried Via	
			0.032" / 0.8mm	0.040" / 1.0mm	0.032" / 0.8mm	0.040" / 1.0mm
6X 245ºC	150ºC	1000	0 of 6	0 of 6	0 of 7	0 of 7
6X 260ºC	150ºC	1000	0 of 3	0 of 3	0 of 3	0 of 3
6X 260ºC	170ºC	1000	0 of 3	0 of 3	0 of 3	0 of 3
6X 260ºC	180ºC	1000	0 of 3	0 of 3	0 of 3	2 of 3

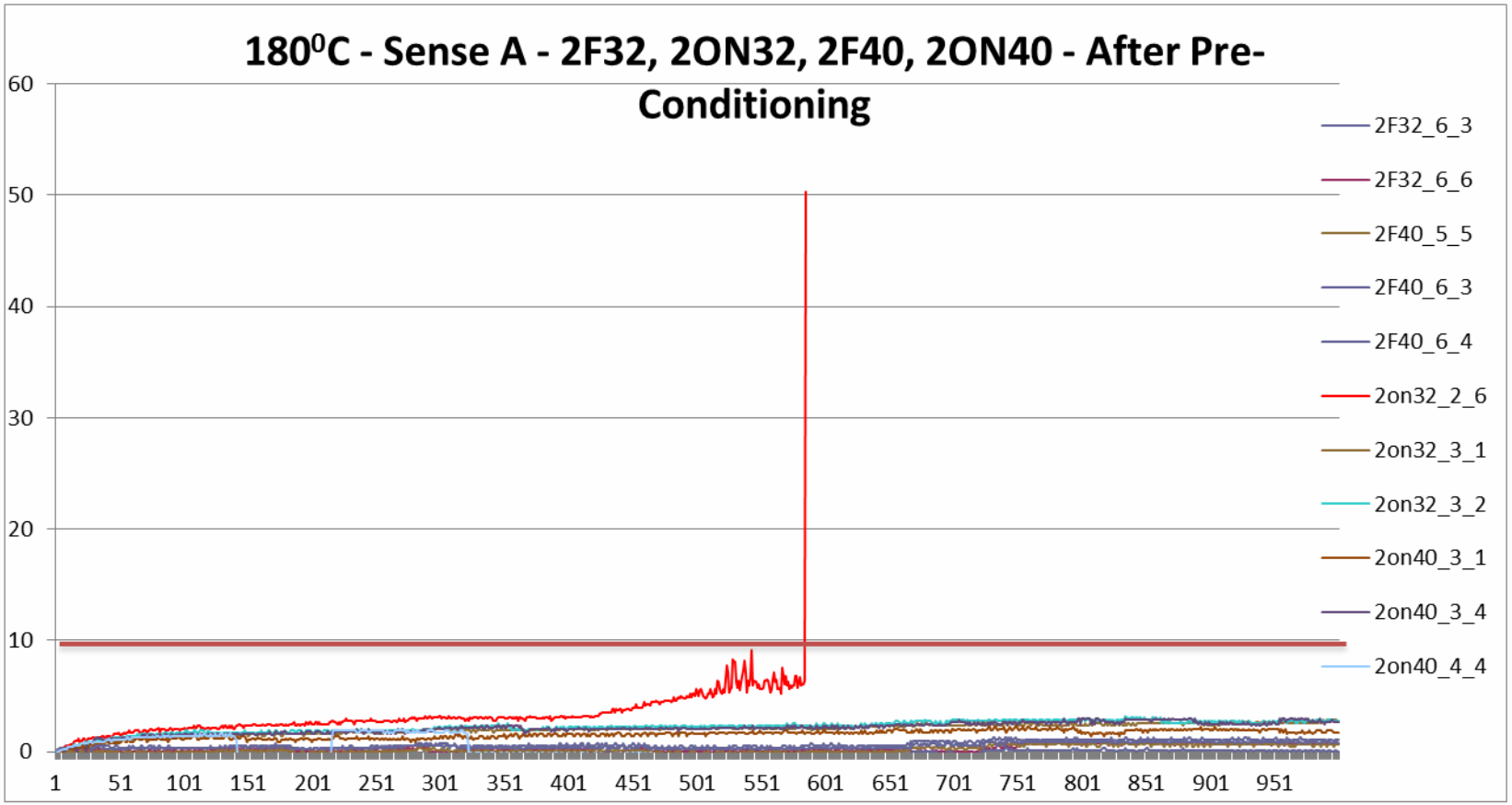
Test Results for 4-Stack Microvia Structures Reliability Testing

Assy. Simulation	IST Test Temp	# of Cycles	On Buried Via		Off Buried Via	
			0.032" / 0.8mm	0.040" / 1.0mm	0.032" / 0.8mm	0.040" / 1.0mm
6X 245ºC	150ºC	1000	0 of 7	0 of 7	3 of 7	2 of 7
6X 260ºC	150ºC	1000	0 of 3	0 of 3	2 of 3	0 of 3
6X 260ºC	170ºC	1000	0 of 3	0 of 3	2 of 2	0 of 3
6X 260ºC	180ºC	1000	1 of 3	0 of 3	0 of 0	1 of 3

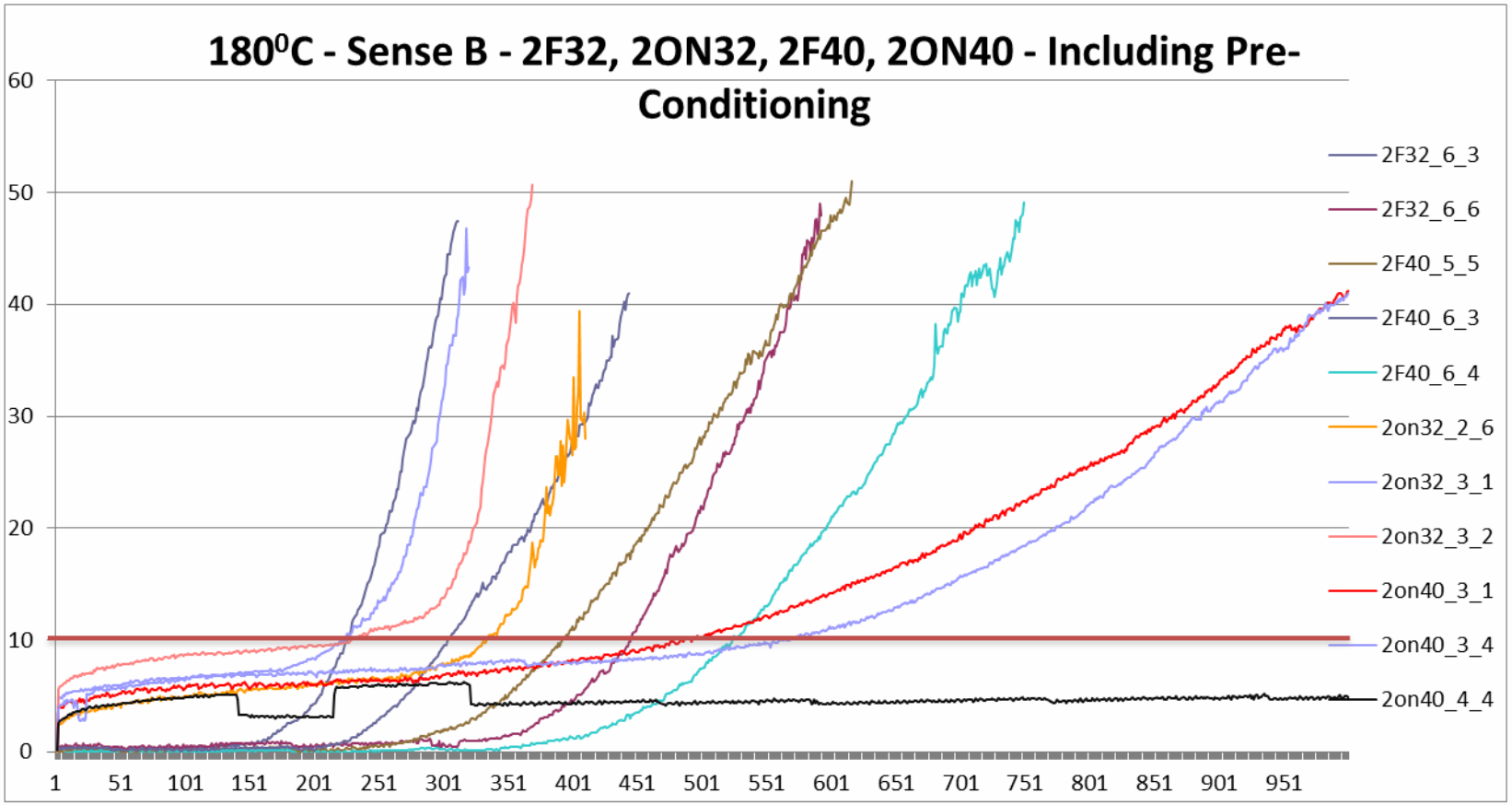
Resistance Analysis – 2 Stacks



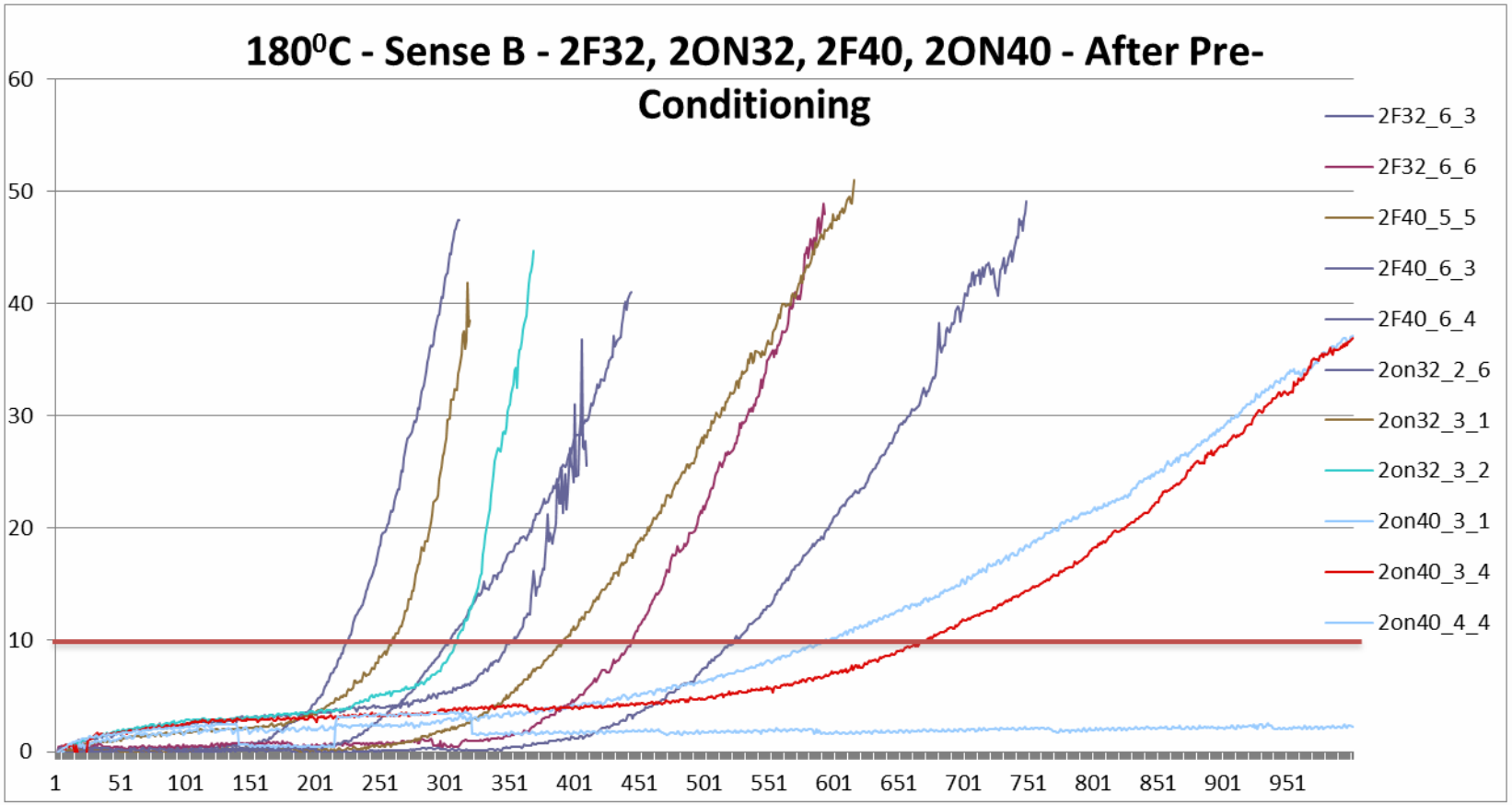
Resistance Analysis – 2 Stacks



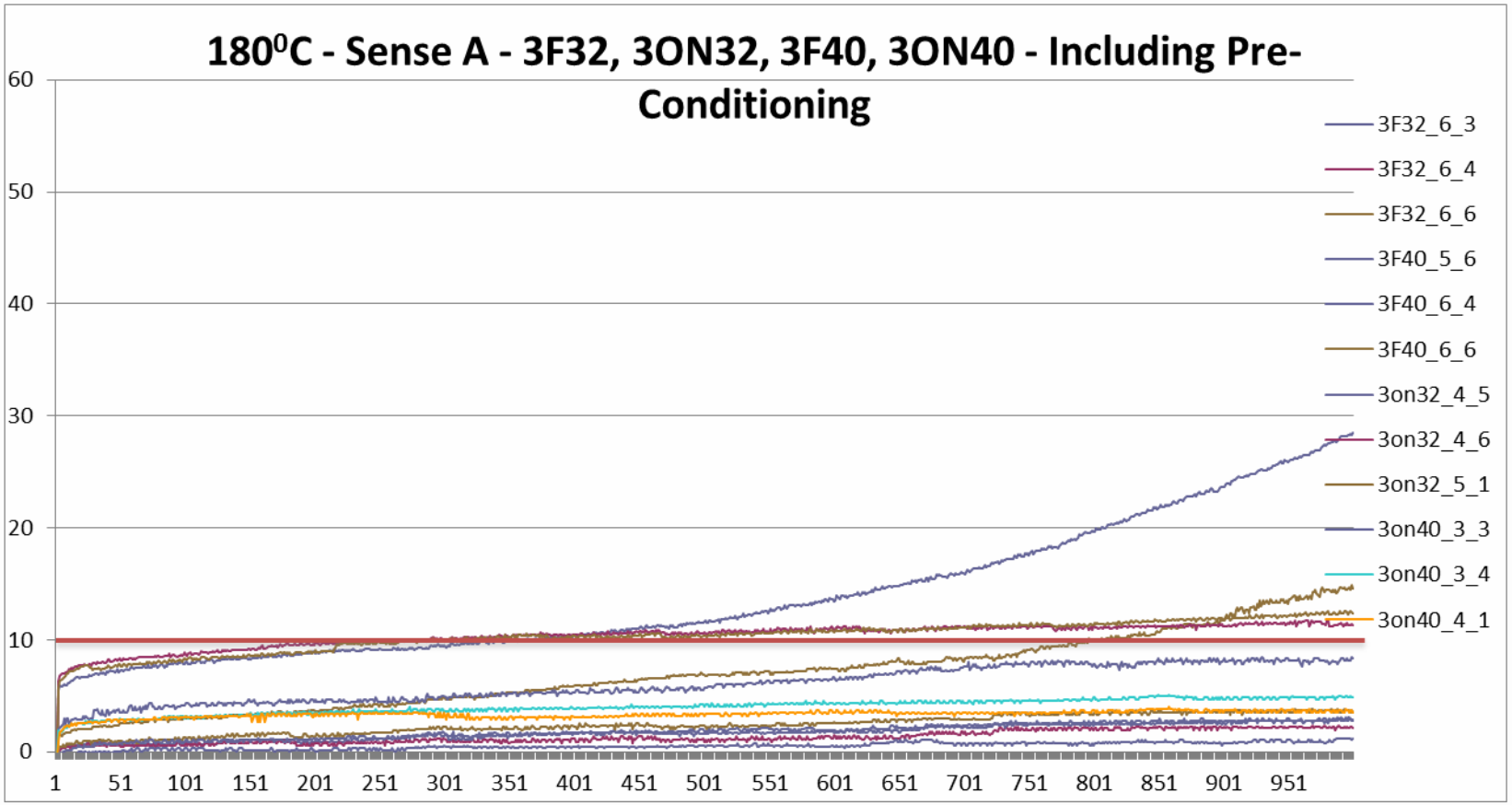
Resistance Analysis – 2 Stacks



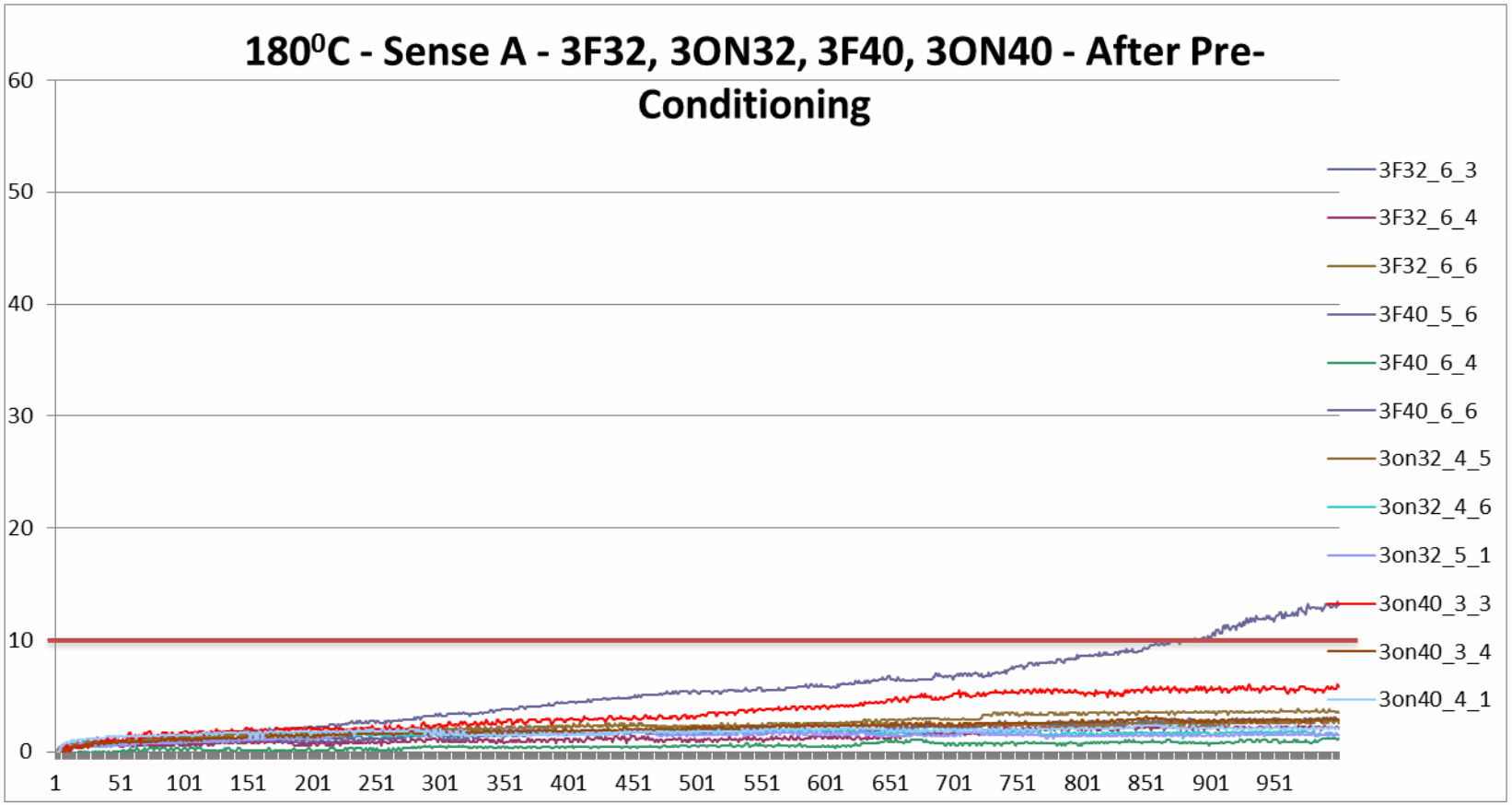
Resistance Analysis – 2 Stacks



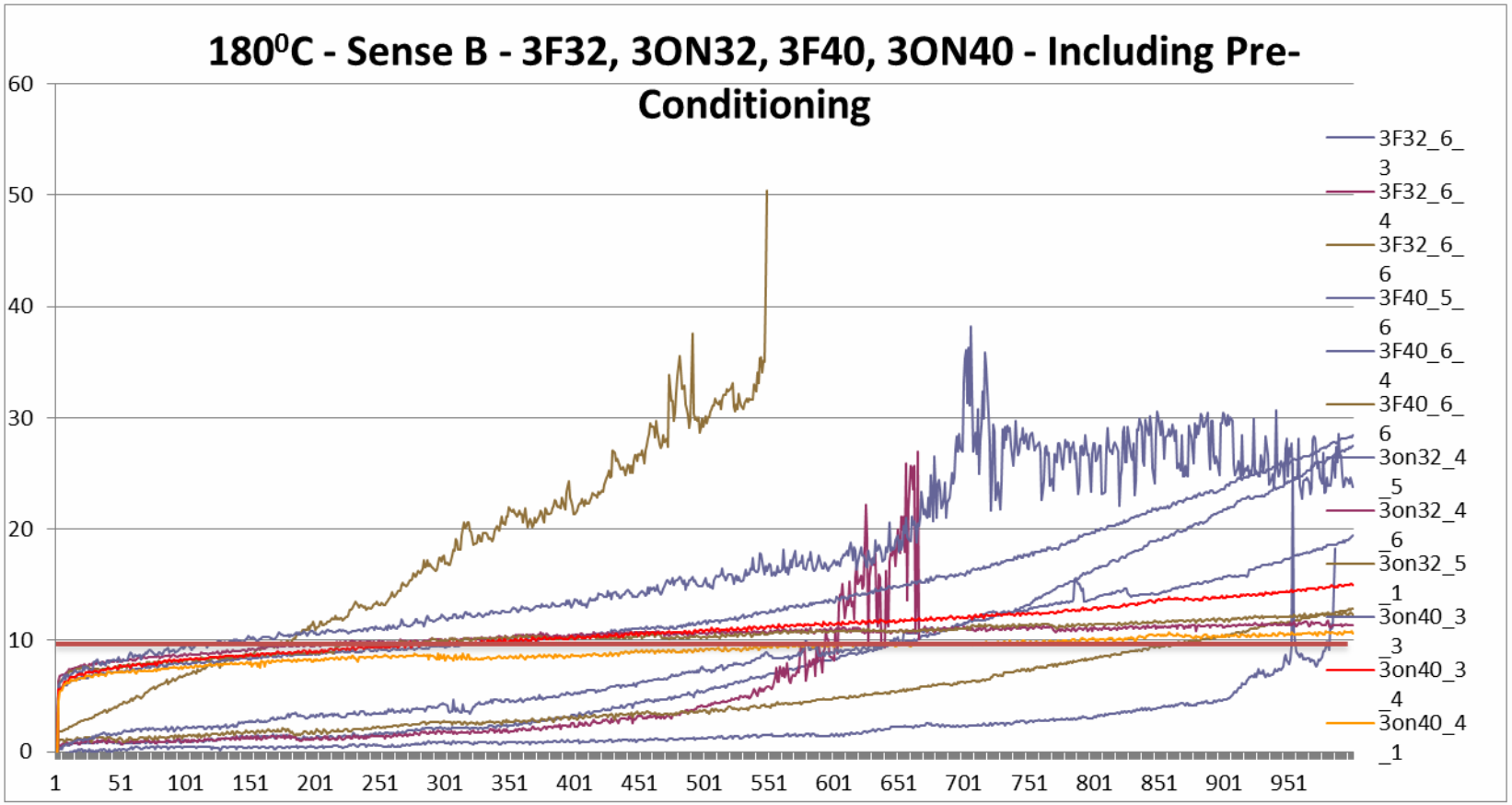
Resistance Analysis – 3 Stacks



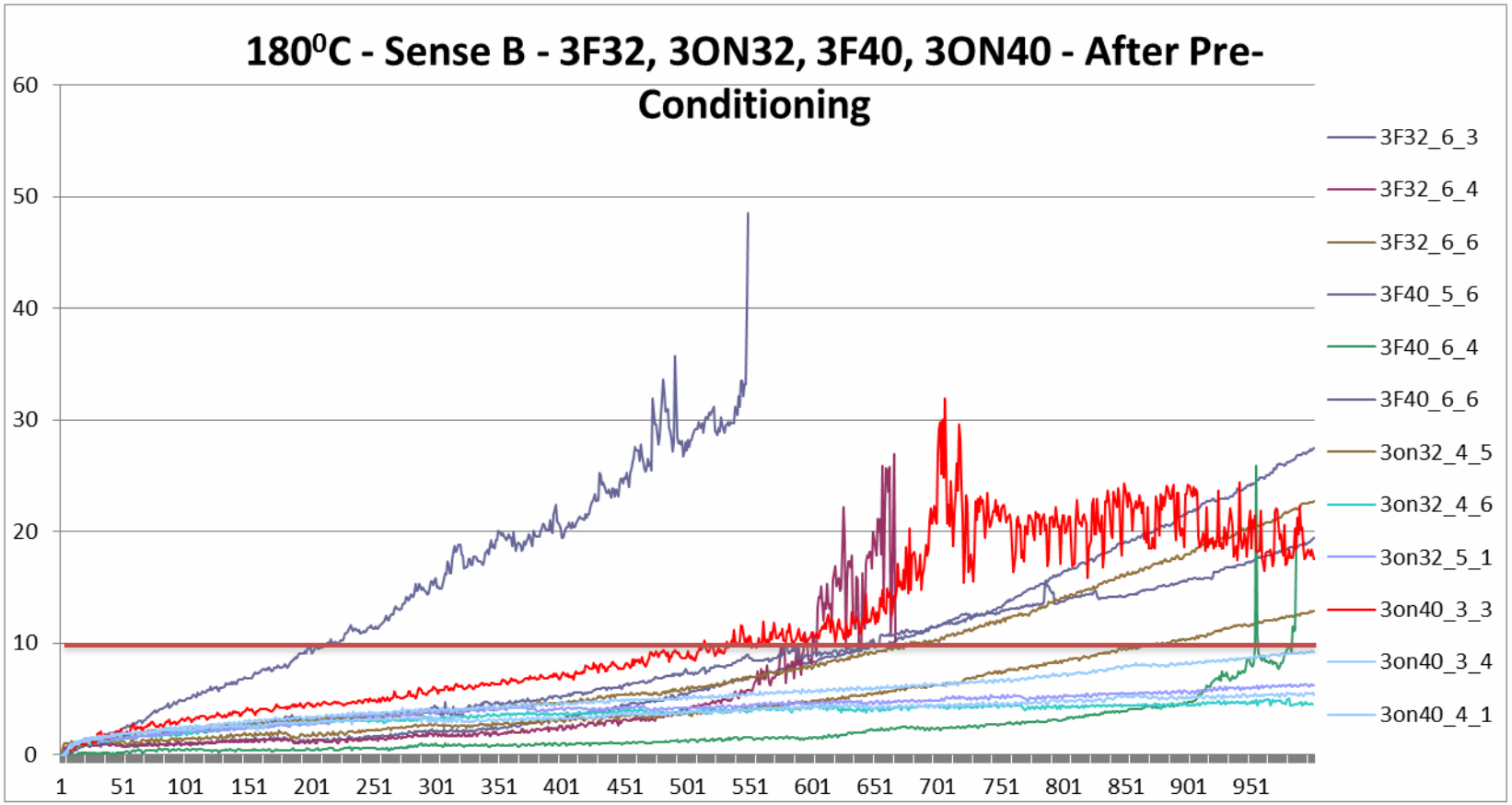
Resistance Analysis – 3 Stacks



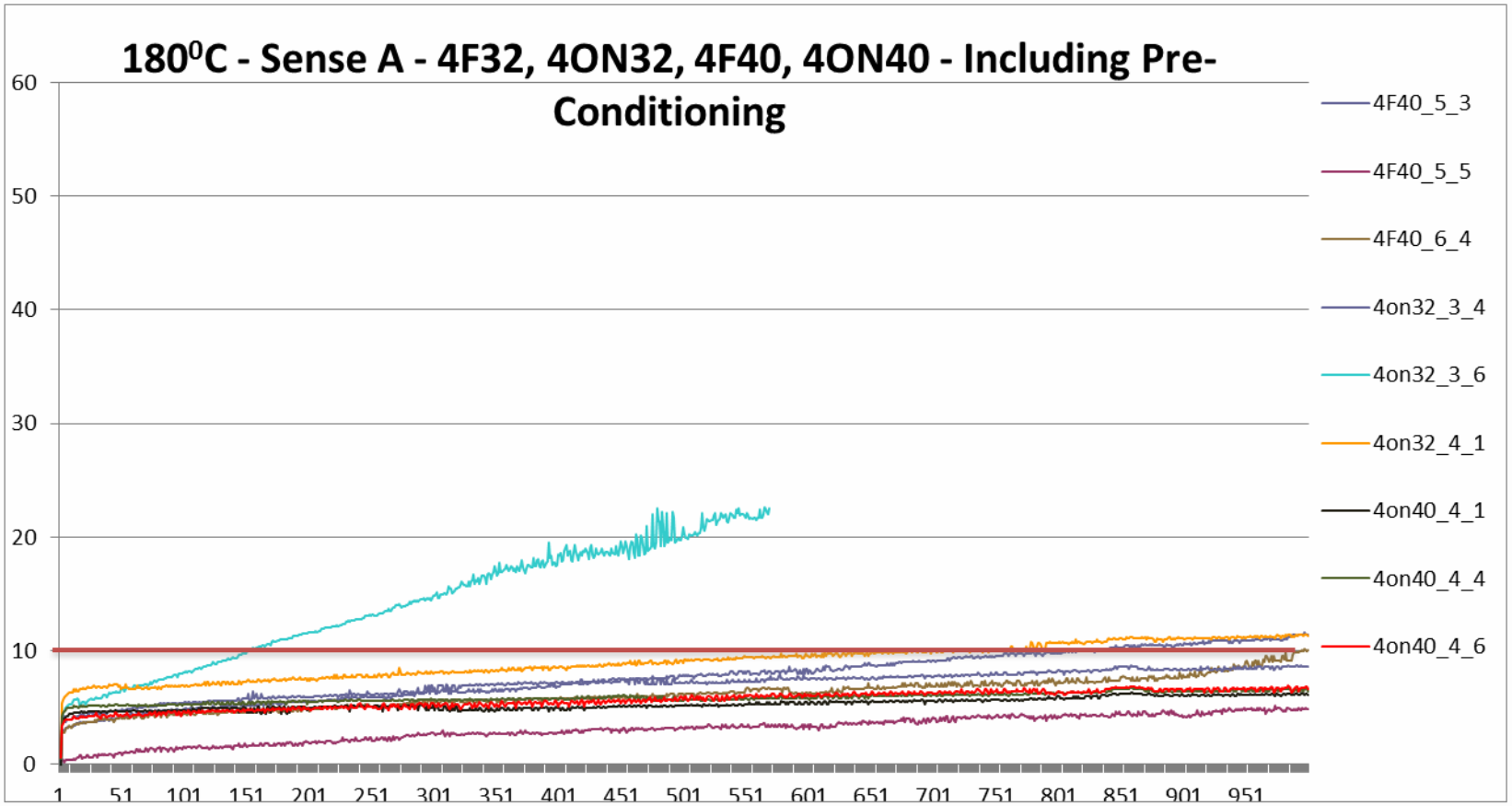
Resistance Analysis – 3 Stacks



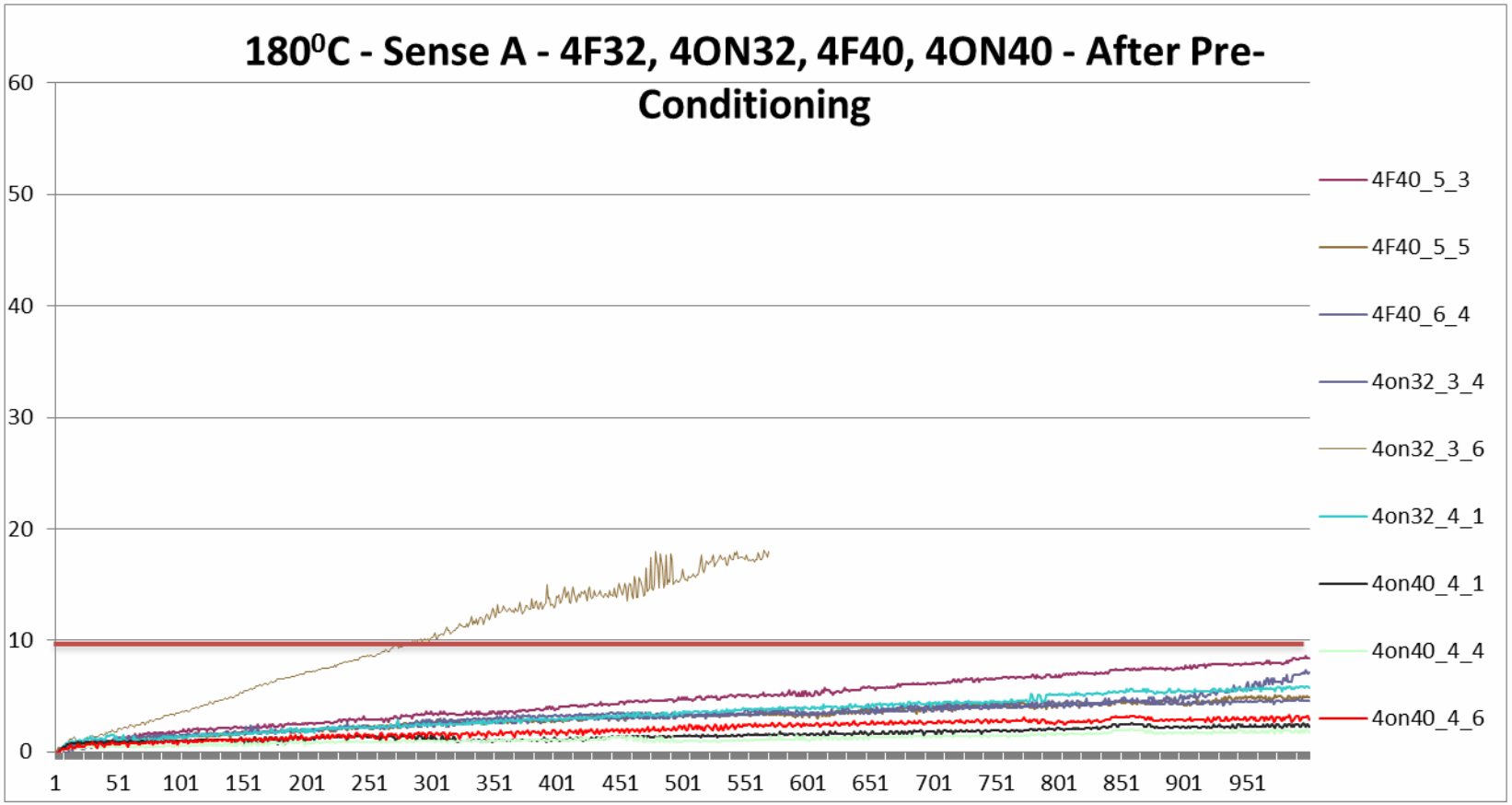
Resistance Analysis – 3 Stacks



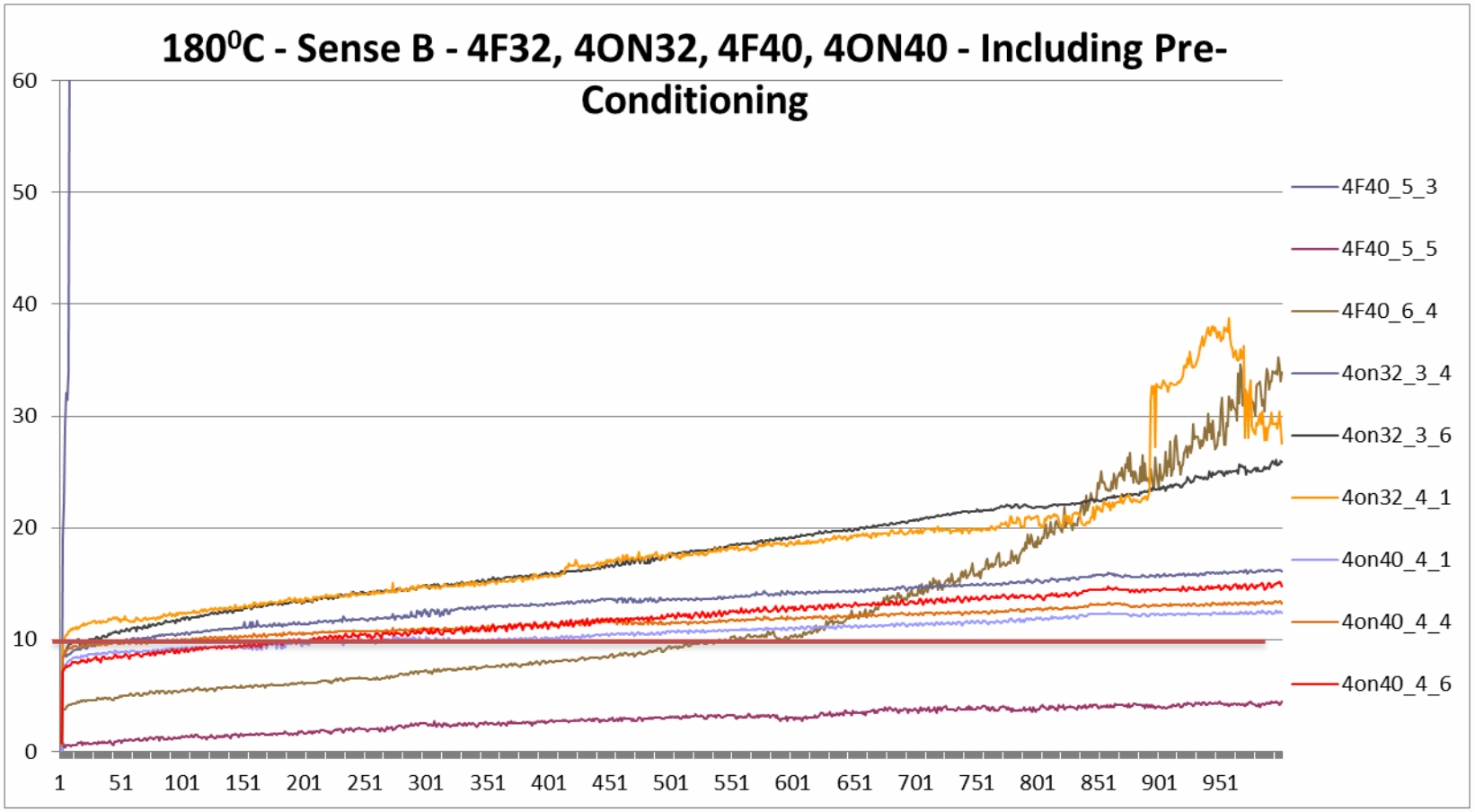
Resistance Analysis – 4 Stacks



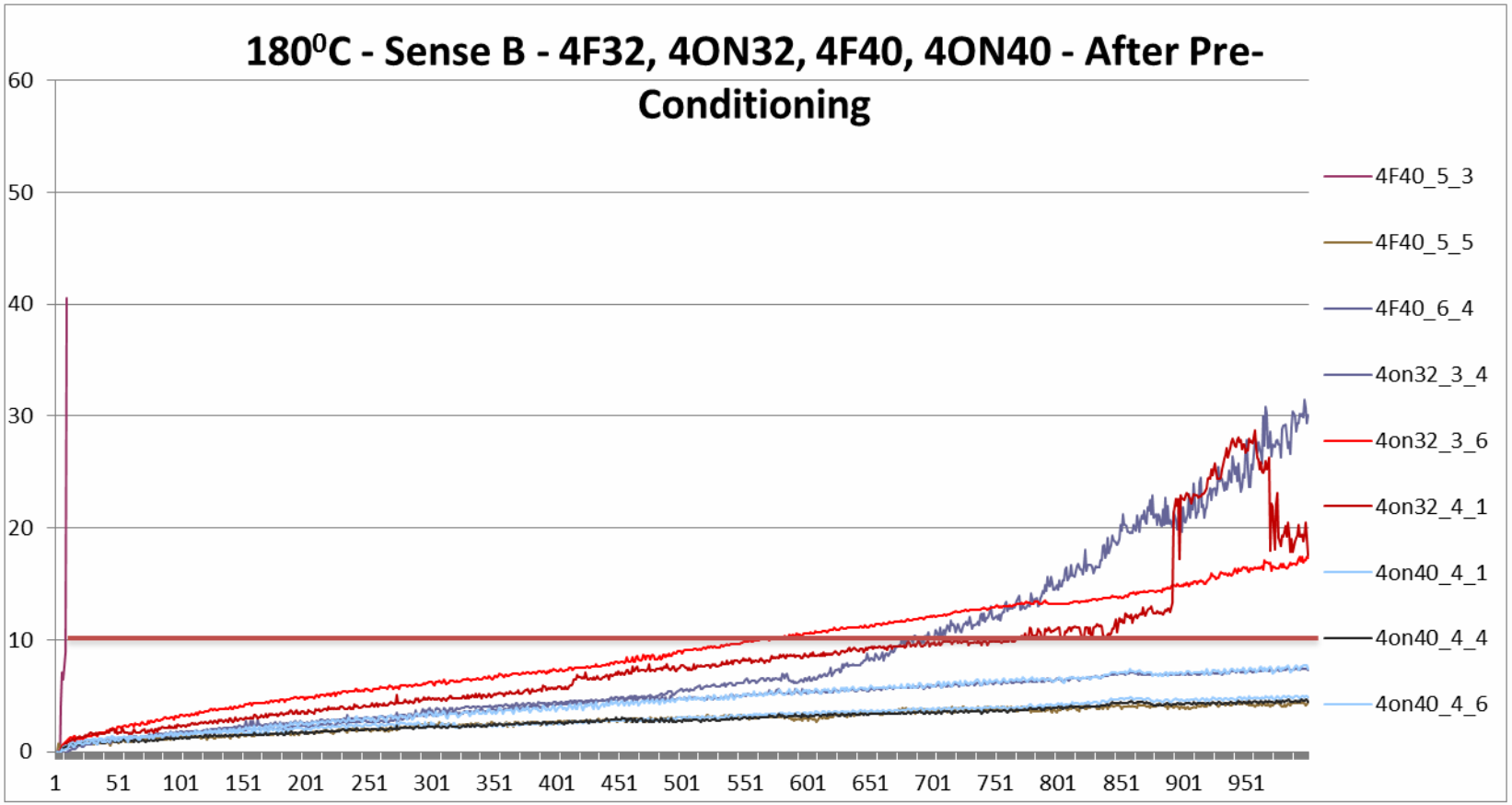
Resistance Analysis – 4 Stacks



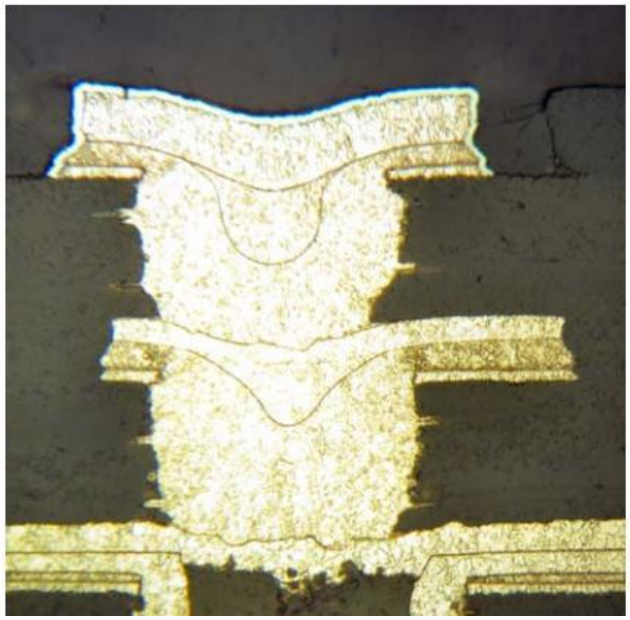
Resistance Analysis – 4 Stacks

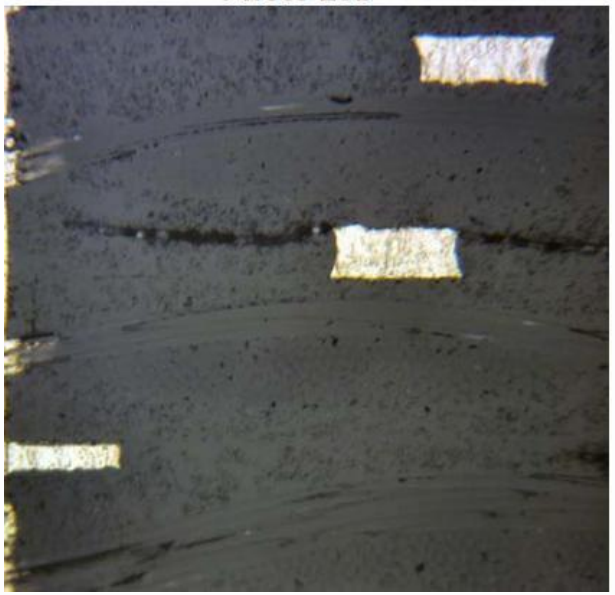


Resistance Analysis – 4 Stacks



Microsectional Analysis

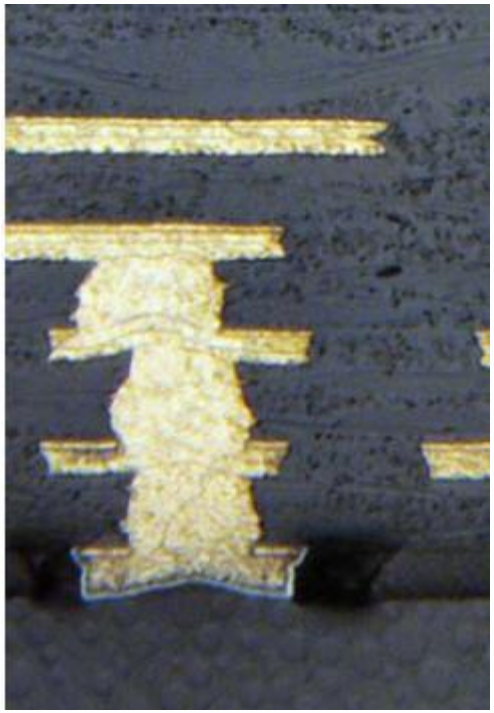
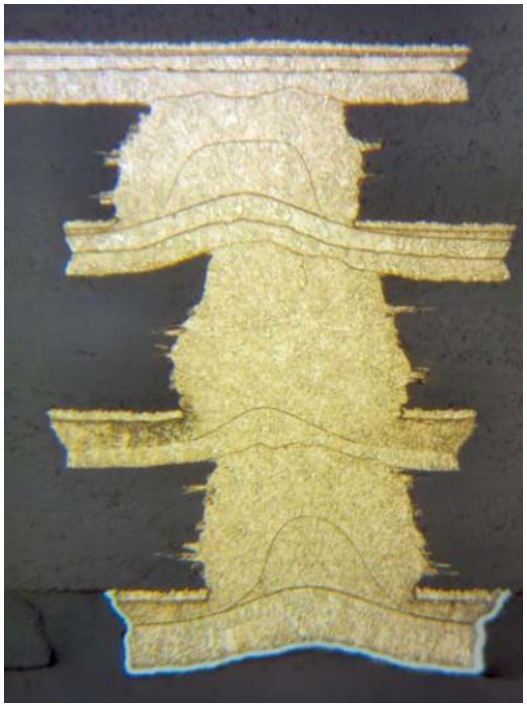
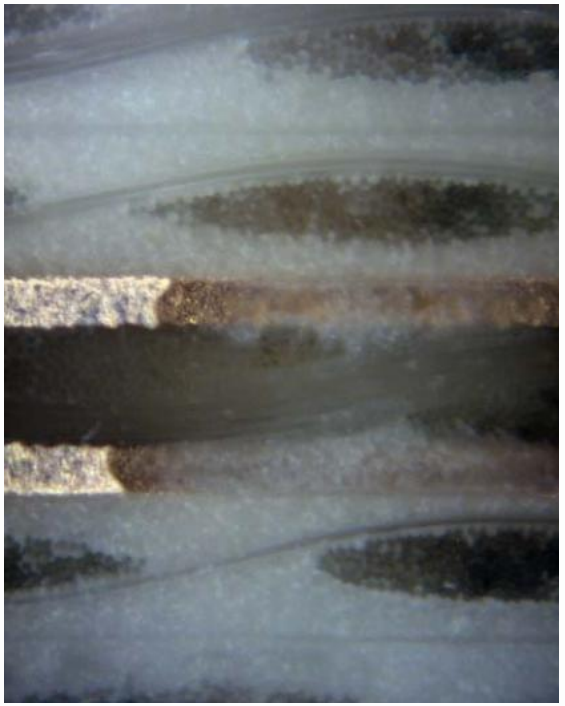




Two Stack Microvia, no failure after 1,000 cycles @150^0 C after 6x@260^{0}C

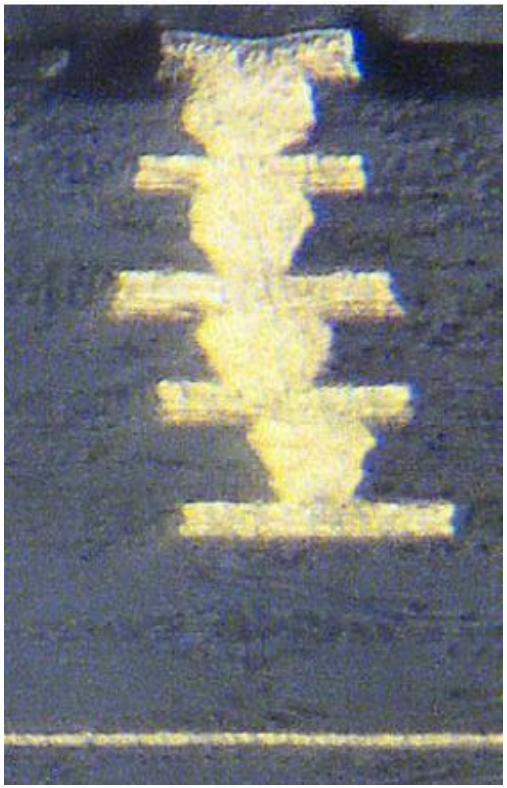
Material degradation observed

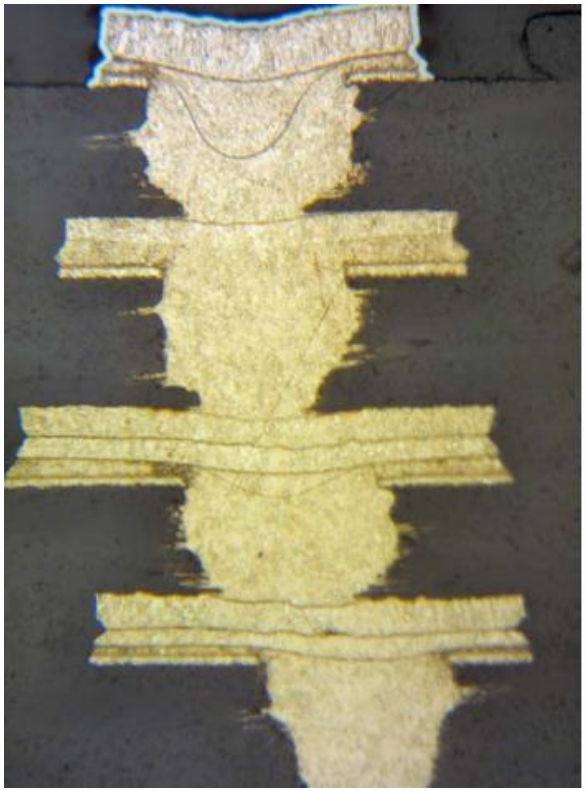
Microsectional Analysis

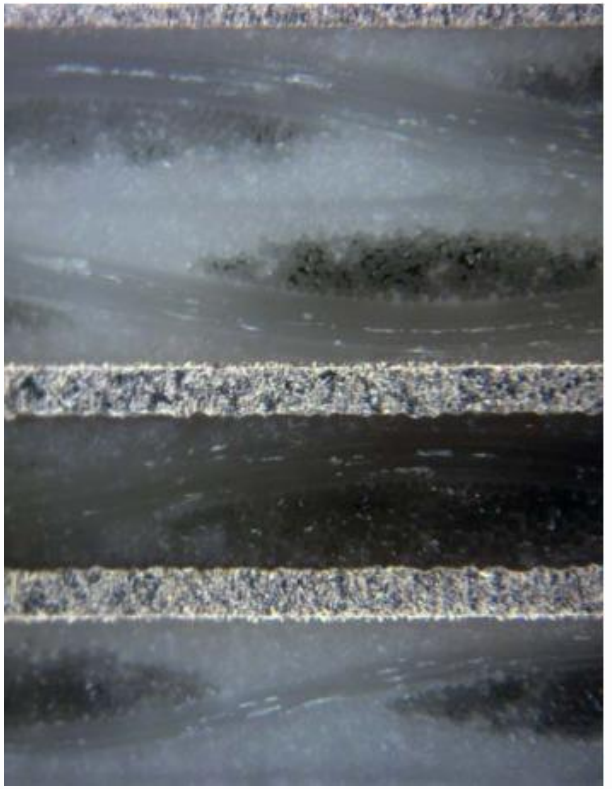




Three Stack off Microvia, no failure after 1,000 cycles @150^0 C after 6x@260^{0}C

Microsectional Analysis







4-Stack off Microvia, no failure after 1,000 cycles @150^0 C
after 6x@260^{0}C

Manufacturing Capability: Areas For Further Investigation

- Via to via registration
- Dielectric thickness variation between layers
- Materials capable of withstanding multiple lamination cycles and lead-free assembly cycles
- This study increased our understanding of our manufacturing capabilities and how it affects our customer's product reliability.

Conclusions

- Standard FR4 High Tg material starts to show degradation after 4 lamination cycles and 6X @ 260ºC pre-conditioning
- Increasing levels of microvias has a negative effect on product yields
- Assembly temperatures between 245ºC and 260ºC demonstrated significant impact on microvia over buried via performance
- Higher temperature (above Tg) thermal cycling and continuous monitoring was required to identify failures that occurred during simulated assembly cycles

Conclusions

- No clear indication that via to via spacing or on/off buried structures have a dominant effect on reliability
- Microvias are more reliable than buried vias
- Higher degree of sense B failures for 2 stacks shows that
  - Higher thermal coefficient of material contributes to failures
  - Negative effect of lower stack buried vias compared to higher via stacks due increased buried via barrel length.

Further Work

- Repeat this testing with associated Material /process modifications with the intention of measuring improved yields, especially through the simulated assembly stage
- Further testing requires a statistically significant sample size – this test was intended to be an introductory evaluation
- Production of test coupons should be conducted in a standard production environment
- Once fatigue is identified as the only failure mode, acceleration studies can be completed to determine life in the field

Thank You

FIRAN TECHNOLOGY GROUP