Alternative Concepts for High Speed, High Frequency and Signal Integration into the PCB

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Abstract

Transmission of data is a major driver in the electronics industry. Higher data volumes, high speed data transfer and short time signal transmission have to be realized to meet these requirements. To minimize losses, the Radio Frequency (RF) application and standard PCB requirements have to be realized on the same board. This additional technology puts additional demands on the PCB. To achieve these targets, the material, build up and design need to be adjusted to both requirements. Test procedures, focussed on particular RF properties have to be considered as well.

This paper examines the development of mixed Microwave and Digital Multilayer printed circuit boards (PCB) for high density application. The major innovations include Radio Frequency (RF) functions, coupled with stacked copper filled Microvia and High Density Interconnection (HDI) technologies, made together into one multilayer construction.

The aim of this study shows the development and validation of raw materials to meet dielectric, power and signal loss properties. From a manufacturing point of view, asymmetrical build up of raw materials with specific RF properties and other PCB raw materials will be investigated, to demonstrate the compatibility of mixed materials in a multilayer PCB´s.

This research was carried out by the company in cooperation with MIDIMU, a European Consortium Project.

Introduction

RF applications on the PCB are an increasing demand in the PCB industry, especially in new personnel networks (like WiGig), driver assistance systems, railway process controls, radio relay systems etc.

Therefore a novel concept was established, which is based on two Projects.

The first project is to investigate particularly RF materials for this application. The goal of this project is to produce PCBs with a mixture of FR4 material and particularly materials for high speed applications in one hybrid build up. **Figure 1** shows the material opportunities for different frequency ranges.

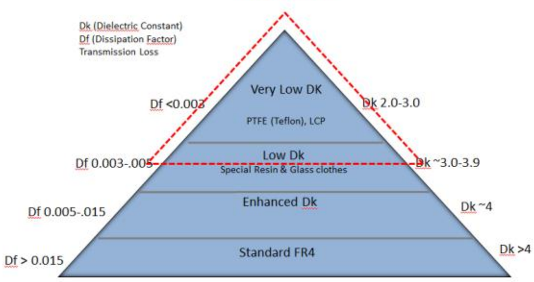


Figure 1 – Dk / Df Material pyramid

Out of this material pyramid, three low Dk/Df materials were selected with different characteristics. These materials need some additional processes to produce PCBs with high reliability performance.

The second project is focussed on intelligent design & stack up, simulation and required RF testing. The major scope is the development of a PCB which includes an integrated radio frequency module with Q Band filter (42 GHz) and fine pitch BGA. The build up will be realized with an organic low Dk/Df material. The target is to optimize the design to meet the RF specification for such applications, and find the most cost effective material/design/layer construction solution.

Materials

A) In Test Vehicle 2 an organic based low Dk/Df material was used. The process is quite similar to standard PCB material production and required characteristics are realized by special resin and glass cloths. This improves the RF properties which can be seen in the **Figure 2** below.

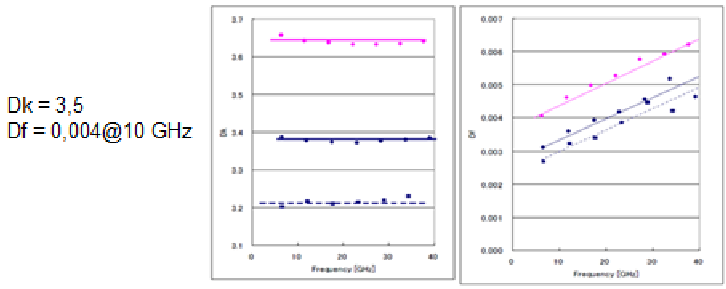


Figure 2 – Dk / Df Material (IPC TM-650 2.5.5.5)

B) Usage of a very low Dk / Df material based on PTFE (PolyTetraFluoroEthylene) with ceramic filler. The characteristics (Dk / Df) of this material can be aligned with the variation of the ceramic fillers. See **Figure 3**. The PCB manufacturing does require special processes. These materials with high Dk / low Df are common for high speed applications with high power or for higher thermal transfer.

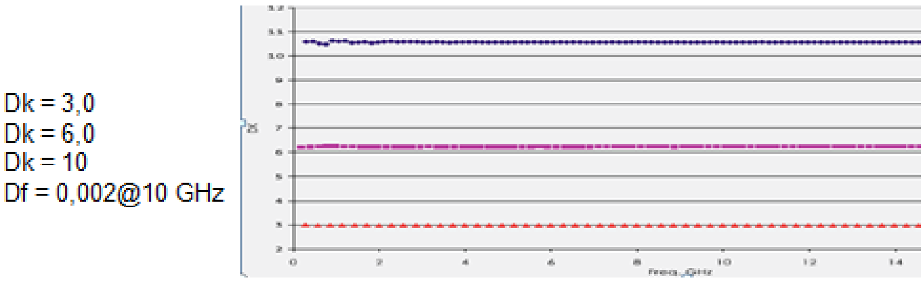


Figure 3 - Dk / Df Material (IPC TM-650 2.5.5.5)

B) Usage of a very low Dk material (PTFE with Polyimide layers, flexible/bendable material) with a minimum core thickness of 50µm **Figure 4**.

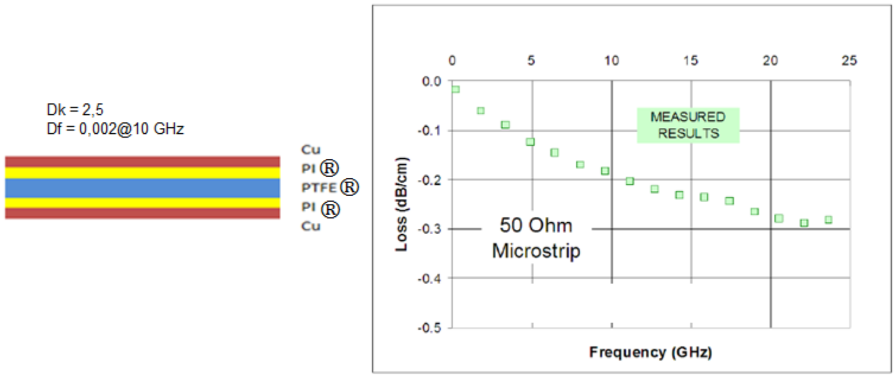


Figure 4 – Build up Core / Losses

Test vehicles

1) Test vehicle for material qualification:

For the material qualification, a multilayer build up with four layers comprising two cores of RF material pressed together with FR4 prepreg was investigated.

Unbalanced stack ups are very common for high speed applications with digital requirements. The high speed design will be realized on the RF Core. The signal layer is placed on the outer layer, whereas the ground layer is placed on layer two. All other layer constructions are used for typically PCB (digital) applications. In this test vehicle a symmetric hybrid was chosen due to the focus on process development and qualification. Therefore, the design was selected to find out the required PCB manufacturing processes and parameters with mechanical drilled holes with a diameter of 250µm, Laser Vias with a diameter of 150µm, structuring with line and width spaces of 75µm. In the solder mask process it has been focused on good performance of the adhesion between the base material and solder resist, with a minimum annular ring of 50µm around the pads. As a final board surface finish, Electroless Nickel Immersion Gold was chosen.

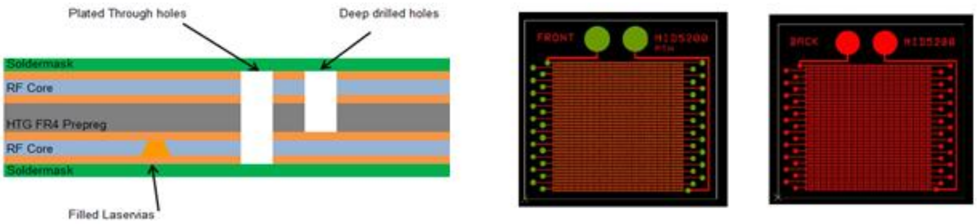
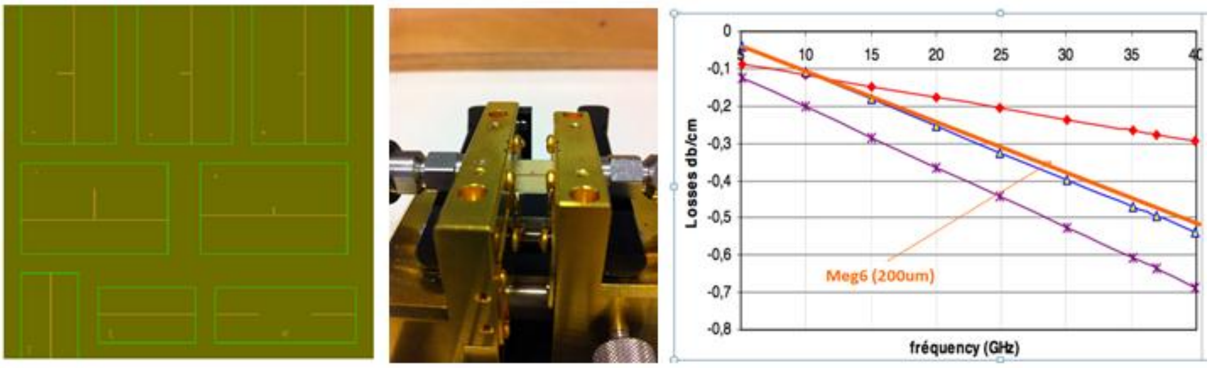


Figure 5 – Build up and Design

All reliability tests which are commonly used for standard PCBs were performed: reflow sensitivity (lead free specification), solder dip, solder float and thermal cycle tests. For a PCB manufacturer it is mandatory to pass all these reliability tests for such high speed boards.

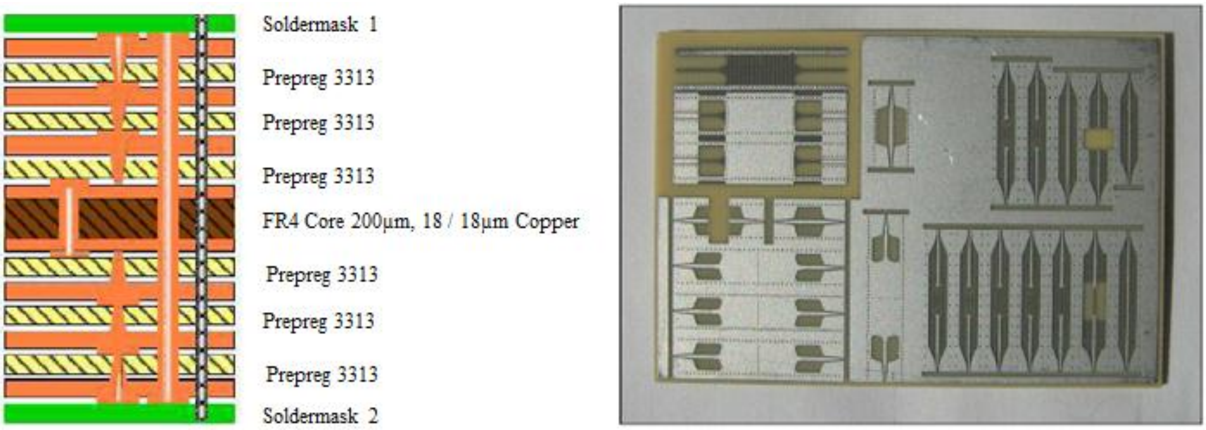
2) Test vehicle for Q Band Filter

The goal of this test vehicle was to develop a 42 GHz Filter with fine pitch BGA based on an organic material. Therefore, we needed the extraction of Dk and Df (see in **[*] Figure 6**). A specific layout with different test patterns has been designed and test vehicles were etched on 100, 200 and 254µm substrate thickness. Planar test vehicles have been investigated at different frequencies from10 – 50 GHz.



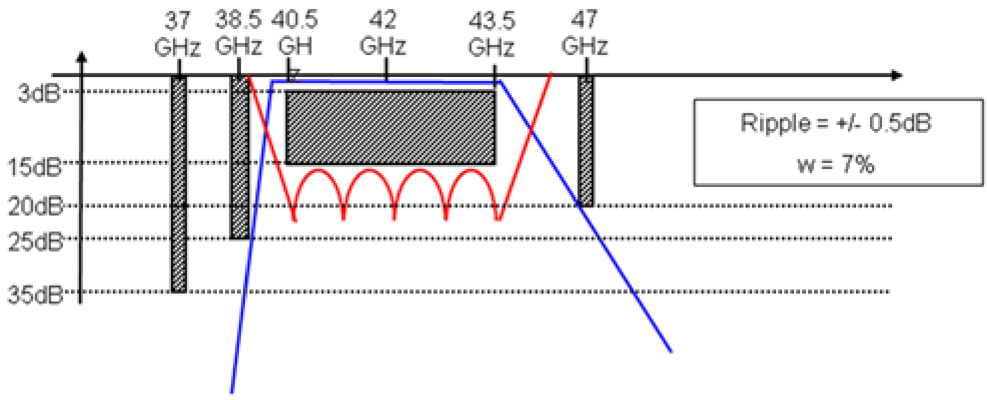
[*] Figure 6 – Test Vehicle Layout / Test Equipment / Results of Losses

Dk, Df, Losses and Q Factor were measured with the test equipment. Based on this data the build up (**[*] Figure 7**) and a design was prepared. The buildup was an eight layer multilayer board with filled mechanical drilled holes on the inner layer and stacked micro vias. The design showed different filter characteristics with SIW (Substrate integrated Waveguides), which is a novel topology of filters combining the advantage of planar and waveguide technologies.



[*] Figure 7 – Stack up and Design

Different planar filters have been designed to compare the impact on both rejections and loss. The selected material has been used for fabrication of these planar references. Expected results are shown in Figure 8. The band width is specified between 40.5 to 43.5 GHz. Losses < 3dB.Target of Rejection are -25dBc under 38.5 GHz, and > -20dBc over 47 GHz.

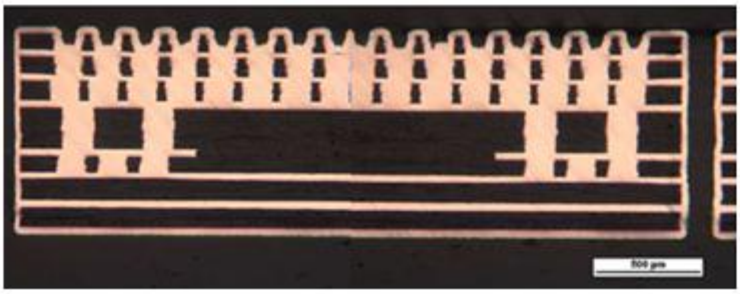


[*] Figure 8 – Filter Requirements

In further studies, the thermal mechanical effects on passive microwaves and effects of moisture absorption were investigated. With these results the simulations of bandwidth, losses and rejections were carried out.

The optimized design was used to build the Printed Circuit Board and RF properties were realized with special imaging structure, stacked micro vias and filled mechanical Plated Through holes (PTH).

Fabrication and measurements: The PCB was produced as an eight layer board, starting with a 200µm thick core, which was mechanical drilled and photo trace structured. Mechanical drilled holes with a diameter of 150µm were filled with copper. Layers 2-4 and 7-5 were produced with Stacked Laser Vias. The diameter of the laser hole was 140µm. In **[*] Figure 9** we can see a shielded coupling iris in the filter between different layers.



[*] Figure 9 – Shielded coupling iris

The Structuring of Traces: This has a big impact on high speed behavior. Two possibilities of structuring are “Panel Plating” or “Pattern Plating”. In panel plating the copper will be plated on the surface, after the drilling processes. After the structuring of lines and spaces in a photo imaging process the line shape gets more roughness on the head and the etch factor (**Figure 10**) is around 4. In pattern plating process the structuring in photo imaging will be done before copper plating. Therefore, the line shape becomes more straight and the corresponding etch factor is around 6.

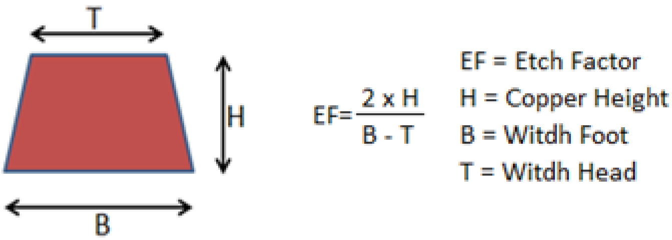


Figure 10 – Etch Factor

The drawback is a higher tolerance on copper height distribution as in the panel plating process. Therefore it depends on the application which process is preferred. For our application we have selected the panel plating process, because of the requirements of the PCB specification.

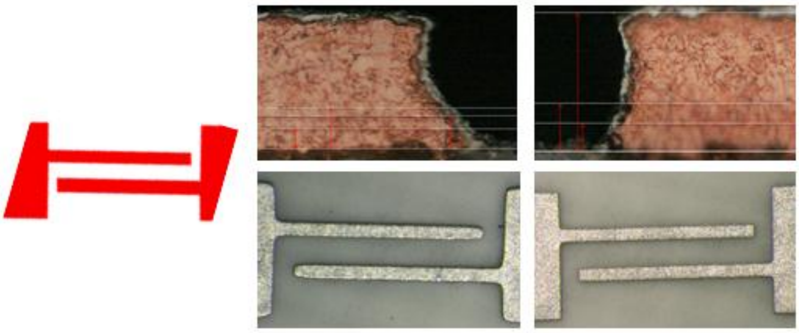
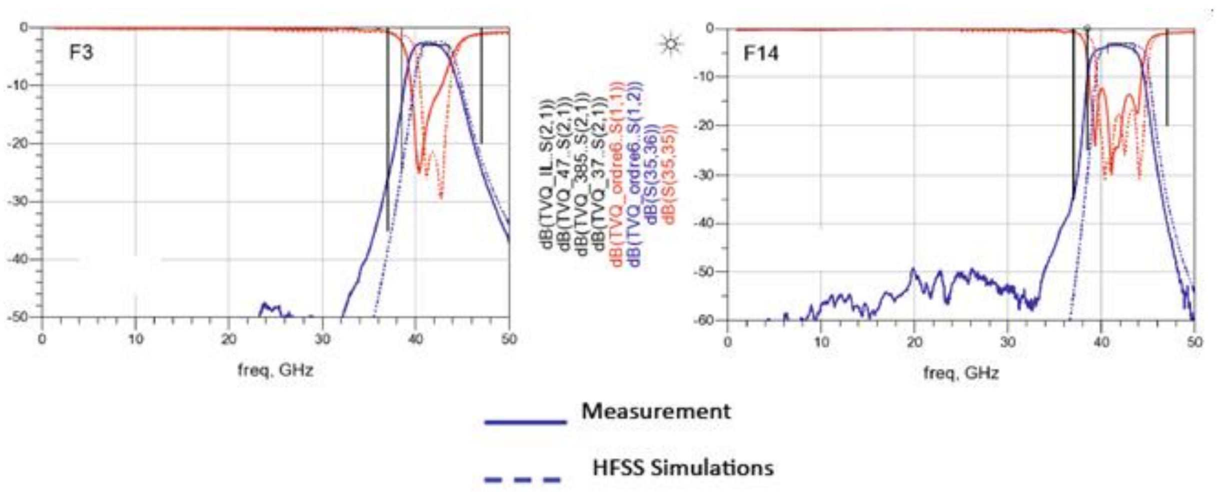


Figure 11 – Design and Structuring Opportunities

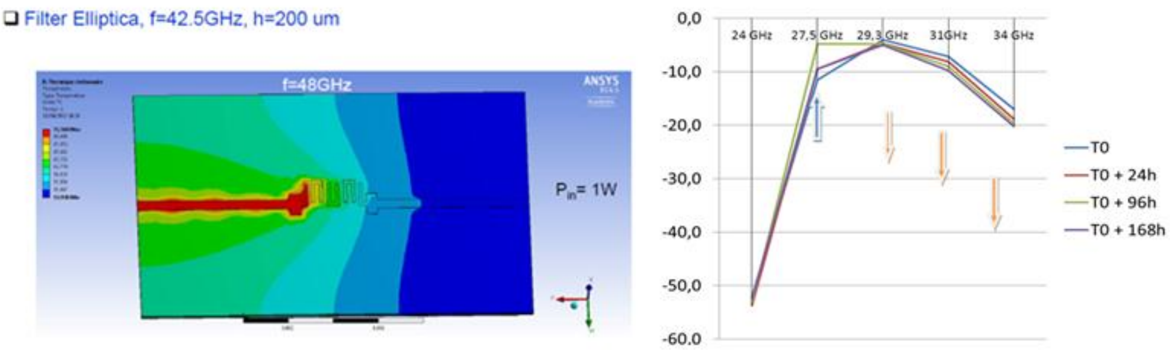
Results: Electrical and Radio Frequency performance

The rejections on the filter board meet the specification. In **[*] Figure 12**, the left graph shows a frequency shift of approx. 1.4%. This weakness could be caused by a coupling effect. Therefore the design has been optimized. The results (right graph) after modified design shows a performance result within the required tolerance.



[*] Figure 12 – Filter behaviour before and after redesign

Thermal aspect:



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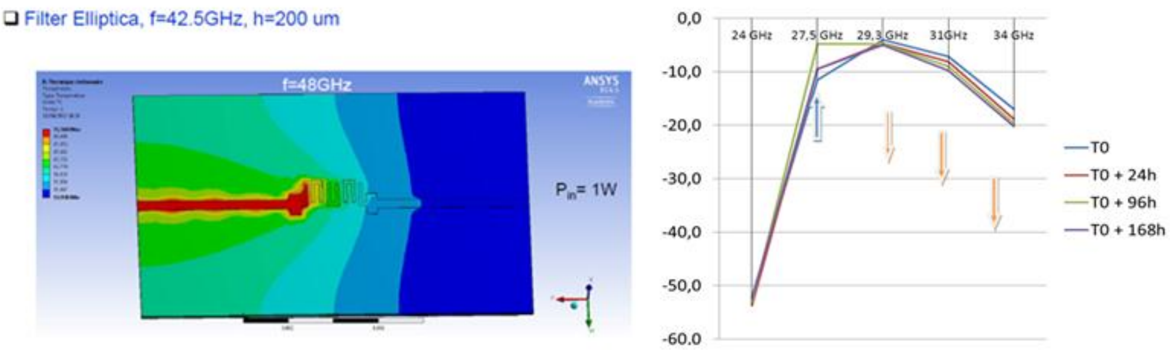
[*] Figure 13) Due to a RF input signal power, a thermal mechanical influence is generated. This fact can change the material properties, so it is important to include the results already in the design phase.

The conclusion of this investigation is that the thermal stress influences the change of material properties at higher temperature, as well as change of DK, loss tangent and Dilitation.

Moisture effect:



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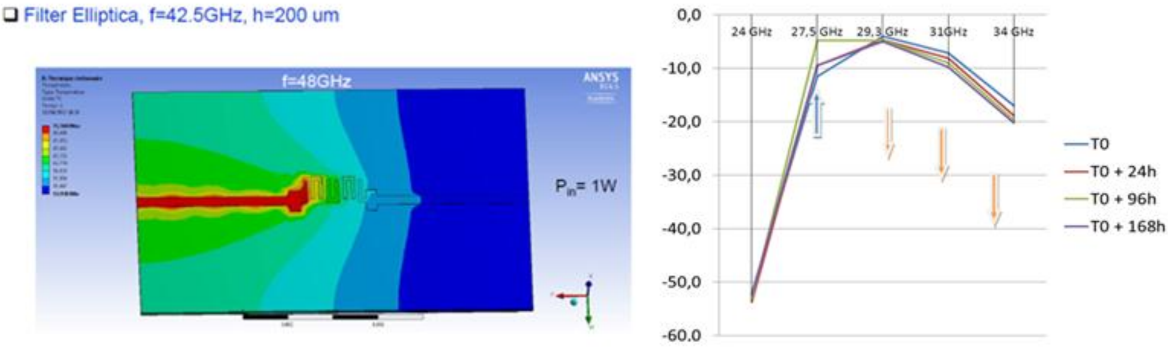
[*] Figure 13) The test vehicles are measured after 24hours, 96 hours and after 168 hours. The parameters according to IPC TM 650 2.6.3.3 are 85% relative humidity, 85°C and a maximum duration of 168 hours. All test vehicles are cleaned and dried (4 hours @ 80°C) before the test procedure. Test features include: machine test model. S21 parameters are tested and recorded for 5 frequencies.

The conclusion of the investigation is that the moisture effect generates a shift of the filter pass band and is not leading to direct losses.



[*] Figure 13 – Thermal and moisture aspects

Reliability Tests. Cross sections were used to analyze the interconnection of plated holes. In Figure 12 mechanical drilled holes and laser drilled holes are illustrated. The ratio between copper on the surface and copper in the holes should be approx. 1.2 : 1. As was expected with organic Low Dk material, the result is very similar to standard FR4 results and the drill wall roughness is < 15µm for mechanical drilled holes and laser vias. The analysis of Low Dk material types shows that the adhesion of copper on PTFE or Polyimide material needs additional surface treatment. The corresponding wall roughness for FR4 and PTFE / Polyimide is up to 30 µm. This effect is linked to a more aggressive desmear treatment, which is necessary to get a proper copper adhesion. An extremely high hole roughness were detected at laser vias on PTFE with ceramic filler material, because of the ceramic fillers. The titanium oxide fillers are very difficult to remove by laser. (**Figure 14**).

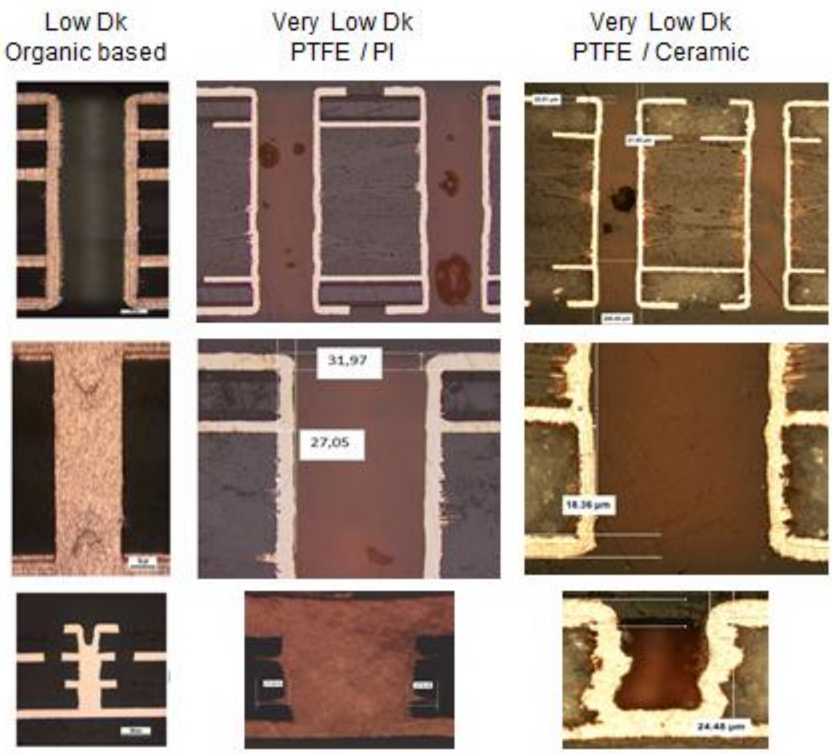


Figure 14 – Cross sections

No cracks were detected during solder float or delamination tests (**Table 1 – Results Solder Float Test (IPC-TM-650 2.6.8)**). These results are an indicator for good thermal stability. The correlation between decomposition temperature, resin system and oxide replacement process seems to be quite good.

Table 1 – Results Solder Float Test (IPC-TM-650 2.6.8)

Material	Sample	Solder Float Test (10 sec @ 288°C)	Delamination Test 10 sec @ 270°C 60 sec @ 270°C
Low Dk Organic Material	1	ok	ok
	2	ok	ok
	3	ok	ok
Very Low Dk PTFE / Ceramic	1	ok	ok
	2	ok	ok
	3	ok	ok
Very Low Dk PTFE / Polyimide	1	ok	ok
	2	ok	ok
	3	ok	ok

Temperature Cycle Testing (TCT), determines the ability of the parts to resist extremely low and extremely high temperatures, as well as their ability to withstand cyclical exposures to these temperature extremes. A mechanical failure resulting from cyclical thermo mechanical loading is known as a fatigue failure, so temperature cycling primarily accelerates fatigue failures. Tests were done with the following parameters:

Heating / Cooling rate up to 17°C/min
Temperature: -40°C to 125°C,
Soak Time: 5 min
Cycles / hour: 2

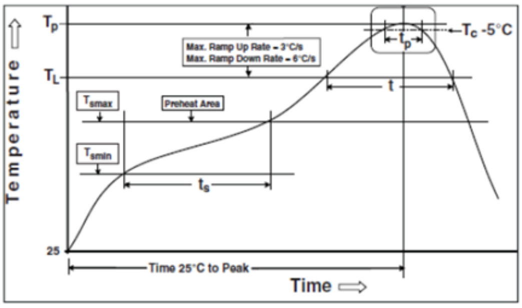
Table 2 – Temperature Cycle Test (TCT) (JESD22-A104B standard)

			Temperature cycle test [cycles]										
Material	Sample	Pre check electrical & visual	100	200	300	400	500	600	700	800	900	1000	Final inspection electrical & visual
Low Dk Organic Material	1	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	2	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	3	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
Very Low Dk PTFE / Ceramic	1	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	2	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	3	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
Very Low Dk PTFE / Polyimide	1	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	2	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	3	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok

After 100 cycles, visual inspection was done and no delamination in the PTHs occurred. The results of the thermal cycle test is an indicator between the correlation of low CTE (Coefficient of Thermal Expansion) values of materials and well known plated through hole conditions.

In the "Lead Free Reflow Test" the PCB must be able to withstand reflow temperatures without incurring warpage or other surface damage.

Table 3 – Profile and Results of Lead Free Reflow Test (IPC / JEDEC J STD-020D) for the PCB



Pre-treatment	24h @ 125'C (+5/-0'C)
Pre-treatment	40h @ 60'C/60%RH
Reflow	Minimum 8 x Pb-free reflow

Material	Sample	Pre check electrical & visual	Drying 24h@125°C Humidification 40h@ 60/60	Standard Lead Free Reflow Profile 1	2	3	4	5	6	7	8	9	10	...	15	Final inspection electrical & visual
Low Dk Organic Material	1	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	2	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	3	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
Very Low Dk PTFE / Ceramic	1	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	2	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	3	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
Very Low Dk PTFE / Polyimide	1	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	2	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	3	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok

The results of the lead-free reflow test show the performance for organic materials and as well as for PTFE filled materials. Overall, all boards passed 15 times lead-free reflow. We expected good performance because of the formation of Teflon materials having a strong Carbon – Fluor atomic bond (2 C,4 F and no H2 and O2).

Conclusions and Future Work

The material test vehicle successfully demonstrated the manufacturing of hybrid boards, comprising very low Dk materials (e.g. PTFE) in the same stack up with FR4. The reliability performance was comparable with homogeneous FR4 build ups.

The filter test vehicle demonstrated production of PCBs for high speed applications in a range of 42 GHz with organic raw material only. This concept with a homogeneous build up is an alternative to realize PCBs with both applications for high speed and fine pitch BGA. The cost of PCB manufacturing is not dramatically higher than for standard PCBs. No additional investment for specific desmear process (plasma treatment) equipment is necessary.

In future work, we will investigate the limits for organic based materials in homogeneous constructions and which opportunities of intelligent build up and design rules could be transferred to hybrid build up with FR4 / very low Dk materials. Another topic will be the investigation of other very low Dk / Df materials, like Liquid Crystal Polymer (LCP) materials due to the availability of very thin dielectric layers (50µm) and low moisture absorption for high speed applications.

References

[*] In Cooperation with MIDIMU, a European Consortium Project.

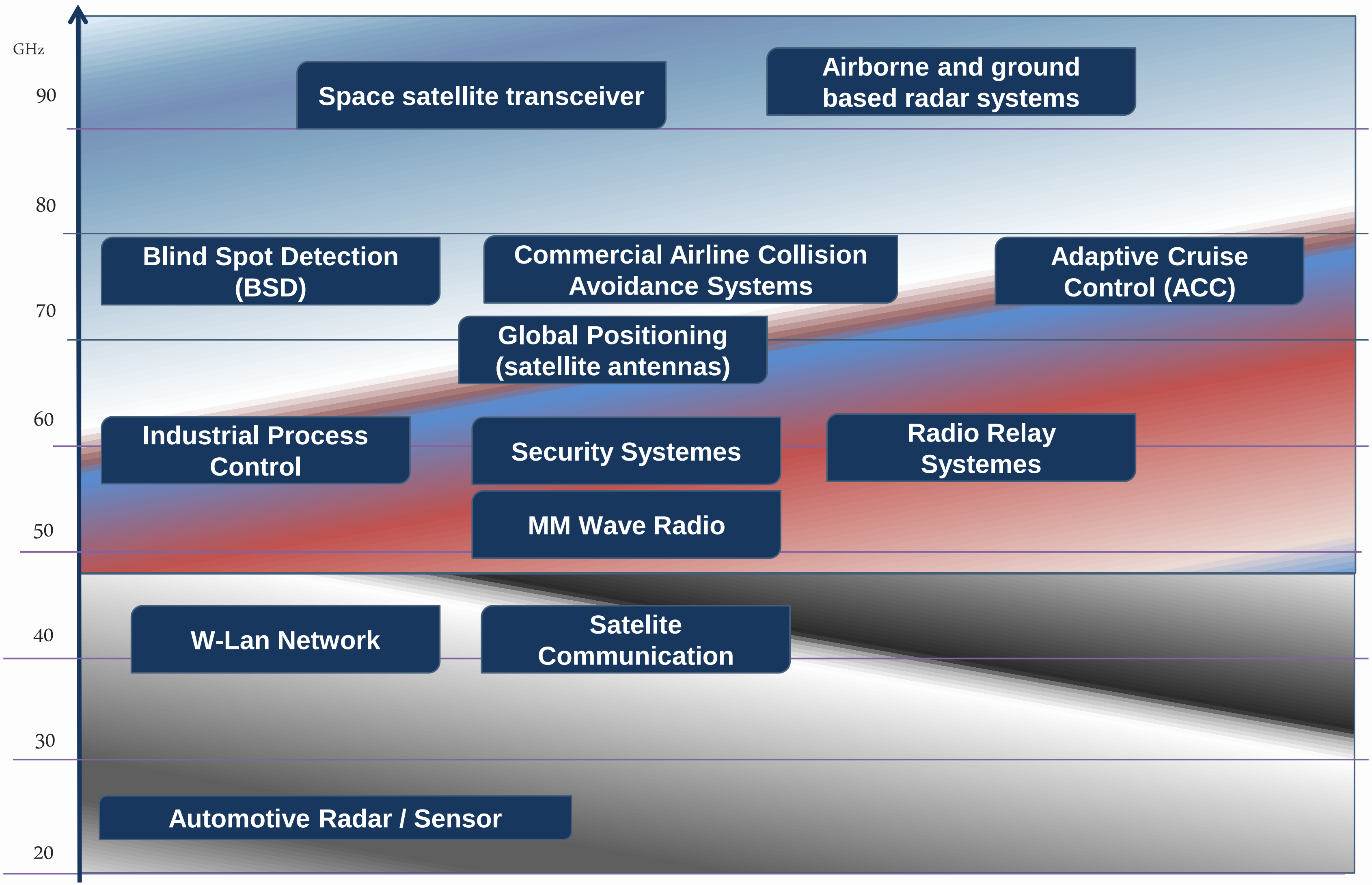
Alternative Concepts for High Speed High Frequency & Signal Integration into the PCB

AT&S
Erich Schlaffer

MIDIMU-HD

An European Consortium Project

High Speed Applications – our Motivation



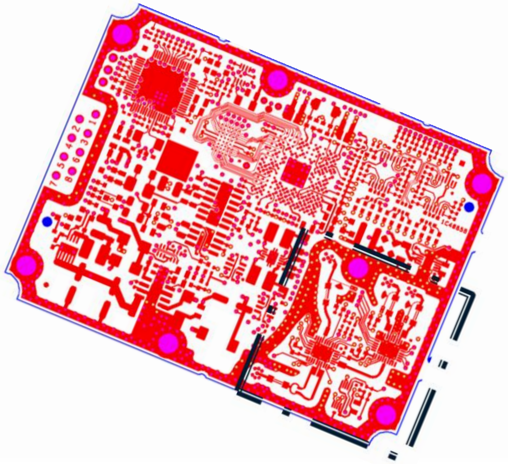
Concept

High speed

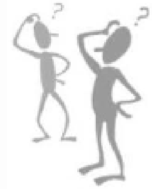
20 – 80 GHz

MIDIMU HD

RF 80



What´s MIDIMU ?



Mixed Microwave and Digital Multilayer
PCB for High Density Applications

MIDIMU-HD

AT&S	AUSTRIA
THALES	FRANCE
swerea IVF	SWEDEN
Lab-STICC	FRANCE
Panasonic ideas for life	AUSTRIA
PROTECNO CIRCUITS IMPRIMÉS	FRANCE
FLEXTRONICS SPECIAL BUSINESS SOLUTIONS	SWEDEN

Innovation:

- Integrated Filters with organic low Dk/Df materials
- Intelligent Design and Layer construction
- HDI, fine pitch BGA & RF application on same board
- Validation of the structure; assembly and repair process development
- Reliability Estimation

➢ Challenge: Development of a 42 GHz Filter & Fine Pitch BGA with organic Material

What's RF 80 ?

PCB Solutions for HDI & RF Application between 20 – 80 GHz

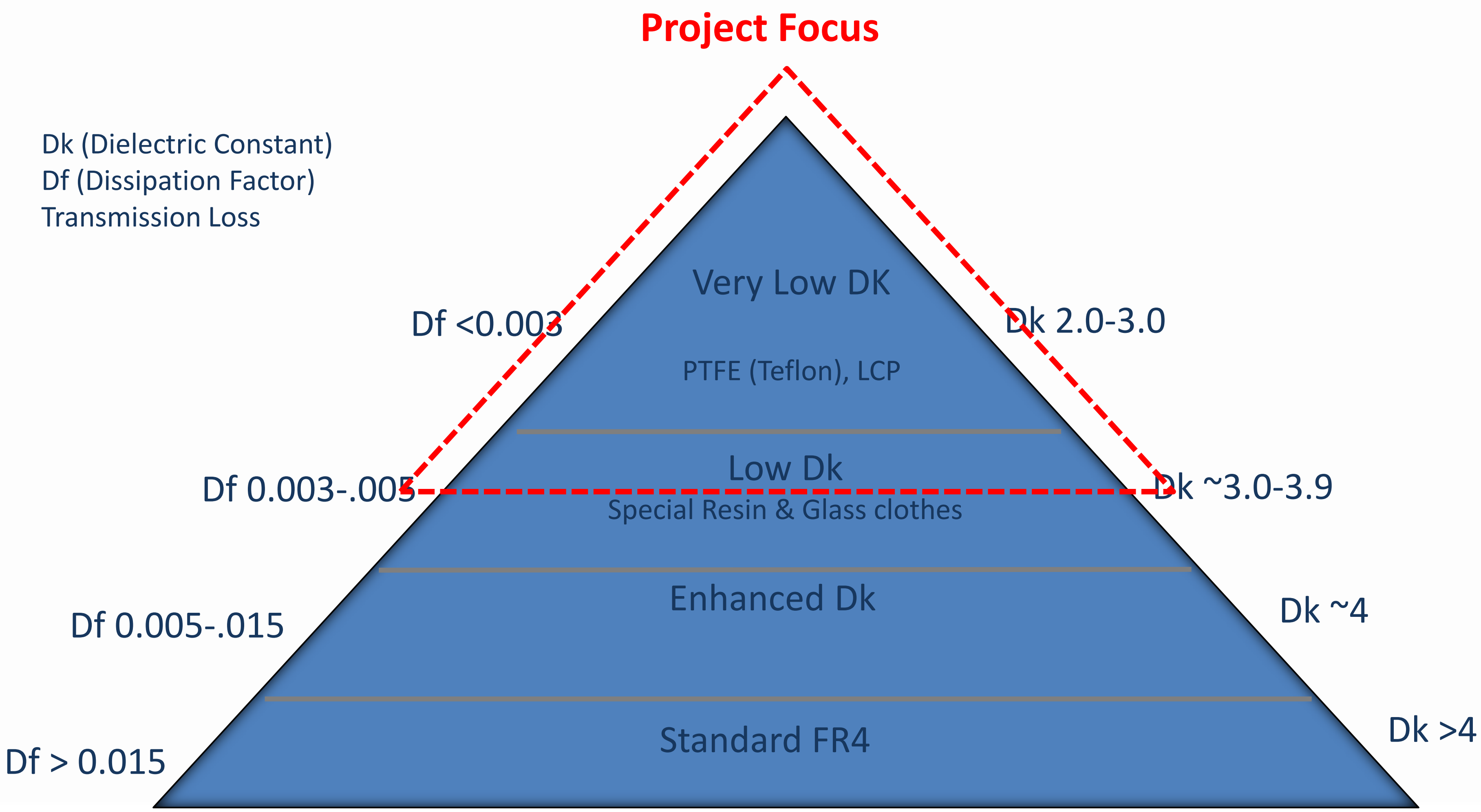
- HDI, fine pitch BGA & RF application on same board
- Materials with particulary High Speed properties (Low Dissipation factor)
- Printed Circuit Board Process Evaluation
  e.g: Plated Through holes, Solder Mask Adhesion…
- Evaluation of Structuring Process
  - Panel Plating
  - Pattern Plating
- Validation of electrical & RF performance
- Reliability estimation

➢ **Challenge: Process development & Optimization**

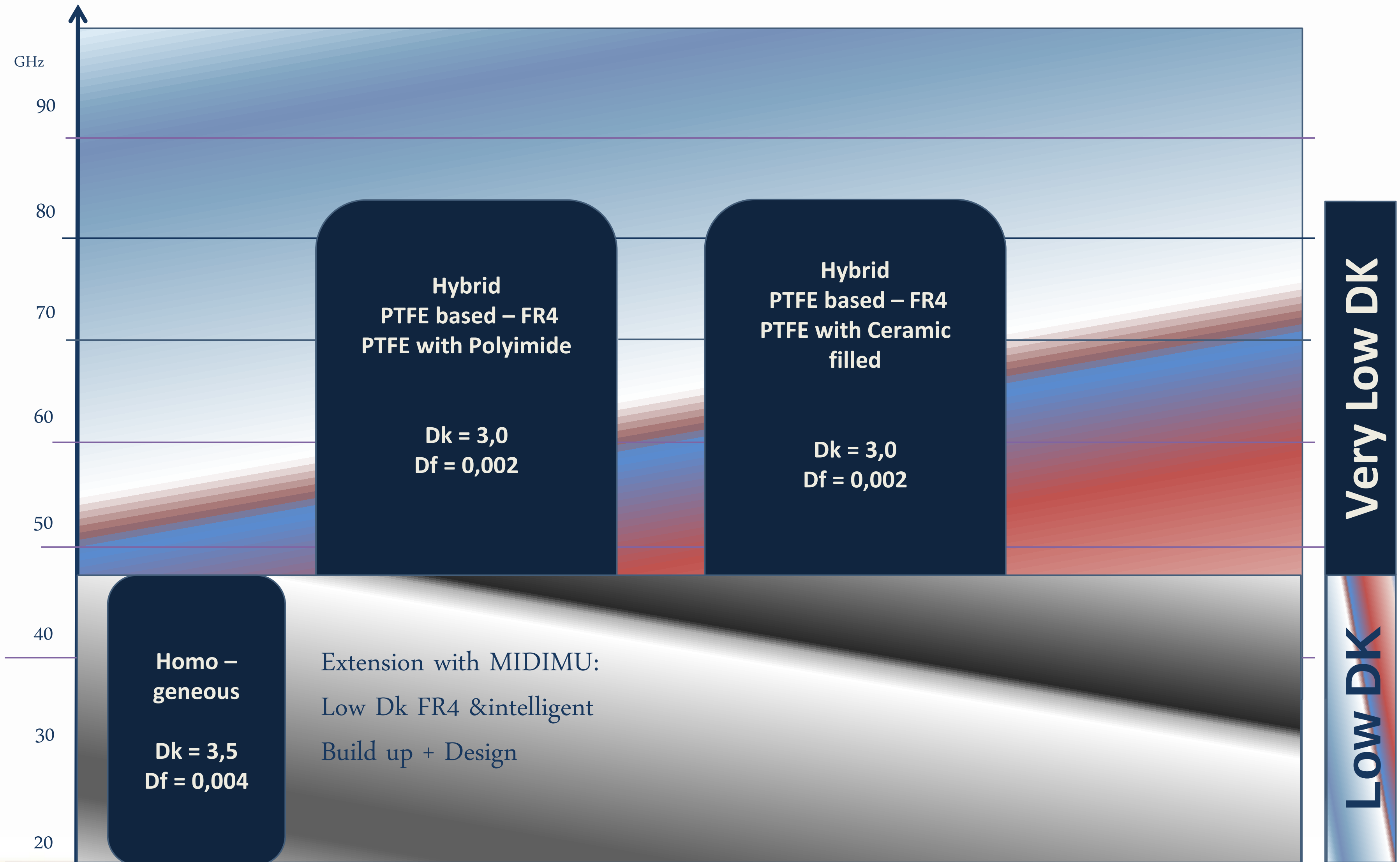
Material / Process / Technology optimized for High Speed Application

Material pyramide

Dk (Dielectric Constant)
Df (Dissipation Factor)
Transmission Loss



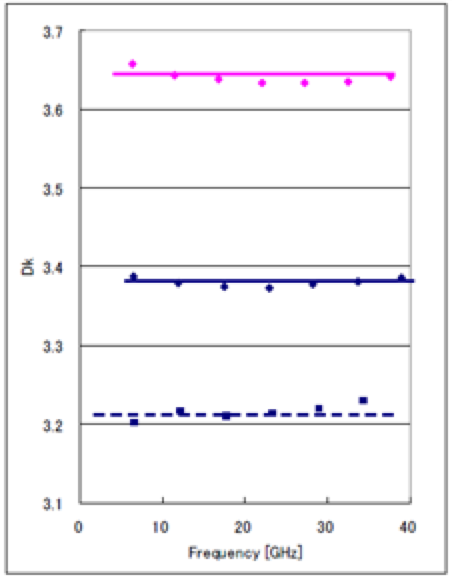
RF 80 Material Strategy

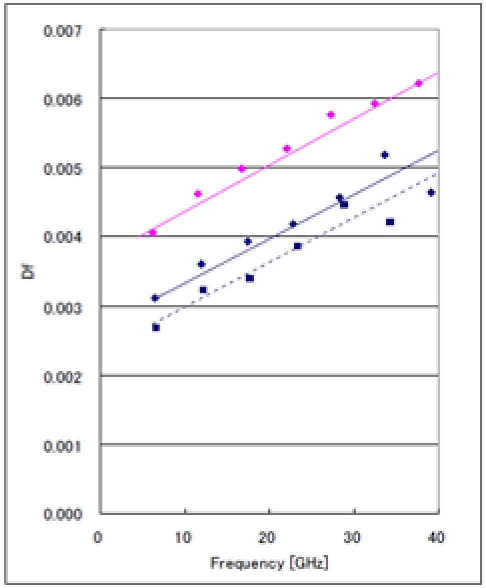


Materials

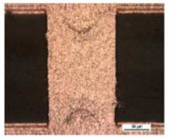
A) Low Dk / Df Material

Dk / Df = 3,5 / 0,004 @ 10 GHz
Organic Based Raw Material
Processing with Standard Processing possible
Application: Base Material for MIDIMU Demonstrator



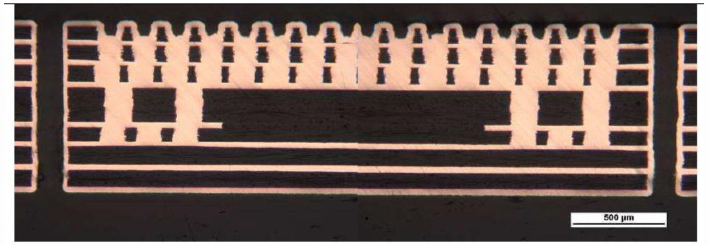


PTH with Via Filling



Stacked Laservias

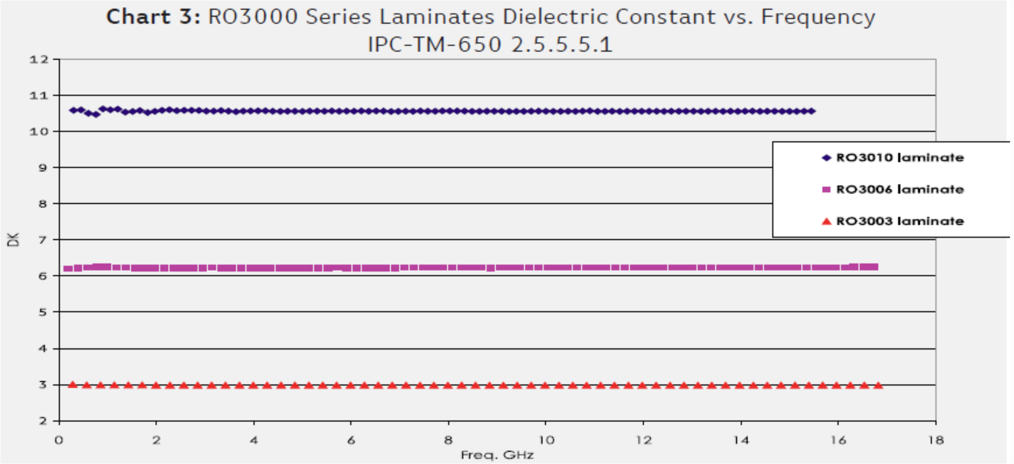
PTH´s



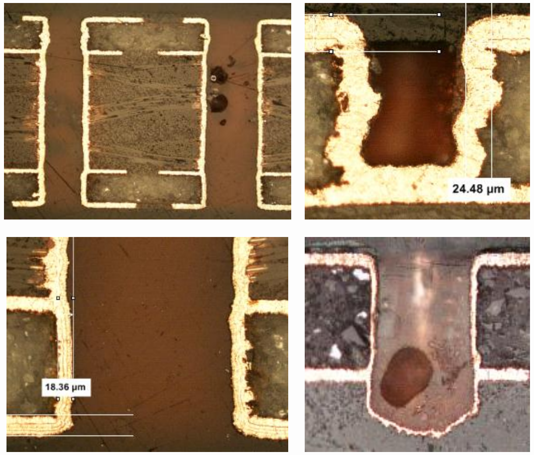
Materials

B) Very Low Dk / Df (PTFE with Ceramic filler)

Dk / Df = 3 – 10 / 0,0013 – 0,0022 @10 GHz
Ceramic filled Material
Particularly PCB Processing (e.g. Plasmatreatment)
Sensible Handlingsprocedure
Application: Saftey Car Systemes (77GHz)



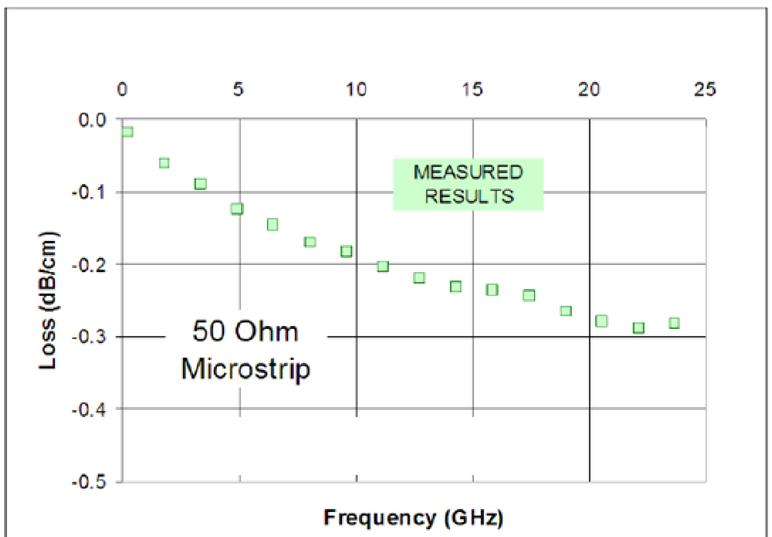
PTH + via Filling



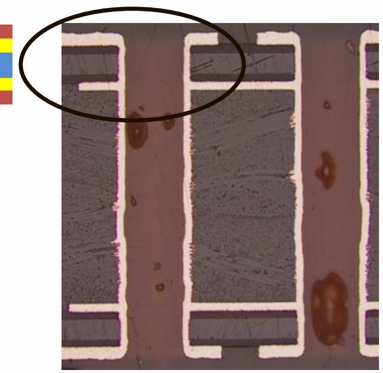
Materials

C) Very Low Dk / Df (PTFE with Polyimide)

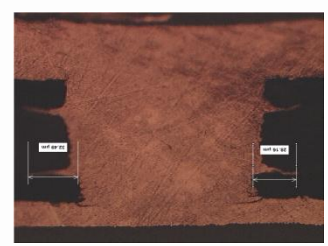
Dk / Df = 2,5 / 0,002 @10 GHz
Particularly PCB Processing (e.g. Plasmatreatment)
Sensible Handlingsprocedure
Application: RF / Medical Care / Rigid Flex

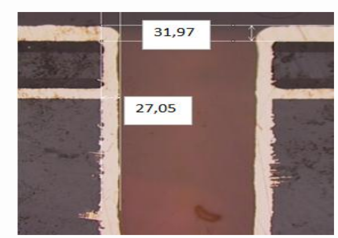


PTH´s



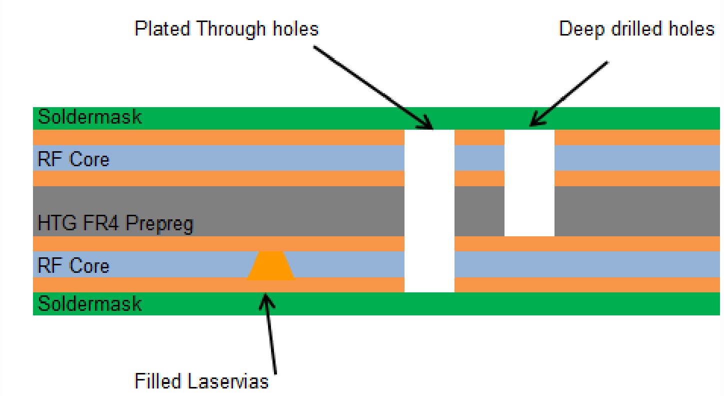
Stacked Laservias



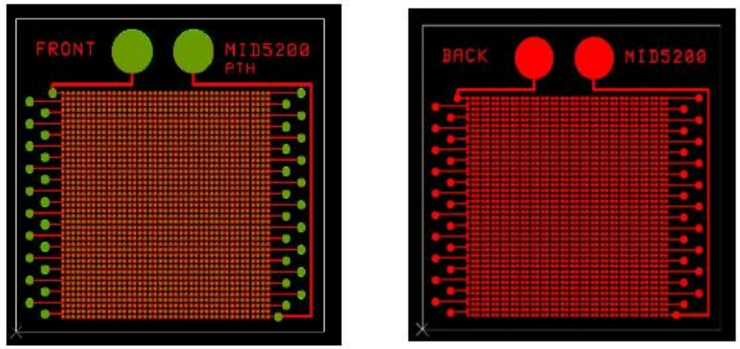


1) Test vehicle for Material qualification

High Speed Build up



Design



Specification

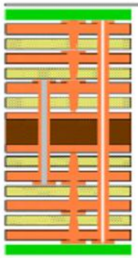
- Hybrid Stack up with FR4
- Mechanical holes: D = 250µm
- Laser Drill holes: D = 150µm
- Line Width: 75µm
- Space between Lines: 75 µm
- Soldermask adhesion
- Soldermask Annular Ring: 50µm
- Surface finishing: imm. Ni / Au

Target

- PCB Process finding
- PCB Process Qualification
- Reliability Testprocedure as for Standard PCB´s

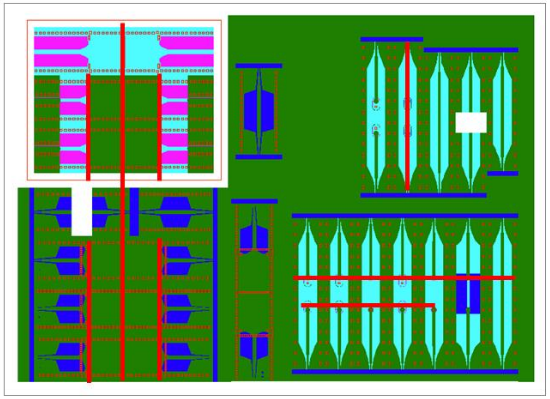
2) Test vehicle for Q Band Filter

High Speed Build up



Layer	Thickness (Millimeter)	Stackup Picture TopLayer layer_1 / layer_8	Family	Description	Type
sm1	0,0200		Prob 65 (Hal.Free)	Prob 65 Green	
layer_1	0,0450		Cu	18µ_d8 z5-8 + 38µm	SIGNAL - Foil
	0,0920		R-5670(K)	3313 (0100)	
layer_2	0,0200		Cu	18µ_d8 z5-8 + 13µm	SIGNAL - Foil
	0,0910		R-5670(K)	3313 (0100)	
layer_3	0,0450		Cu	18µ_d8 z5-8 + 38µm	SIGNAL - Foil
	0,0940		R-5670(K)	3313 (0100)	
layer_4	0,0150		Cu	18µ	SIGNAL
	0,1500		R-5775(K)	0150	
layer_5	0,0150		Cu	18µ	SIGNAL
	0,0940		R-5670(K)	3313 (0100)	
layer_6	0,0450		Cu	18µ_d8 z5-8 + 38µm	SIGNAL - Foil
	0,0910		R-5670(K)	3313 (0100)	
layer_7	0,0200		Cu	18µ_d8 z5-8 + 13µm	SIGNAL - Foil
	0,0920		R-5670(K)	3313 (0100)	
layer_8	0,0450		Cu	18µ_d8 z5-8 + 38µm	SIGNAL - Foil
sm2	0,0200		Prob 65 (Hal.Free)	Prob 65 Green	
	0,9940	**Total Thickness (Calculated)**			
	1,6000	**Over Mask (Customer)**	**+0,1600**	**-0,1600**	
	1,4840	**After Press (Customer)**	**+0,1484**	**-0,1484**	
	0,6800	SubAssembly layer_2 / layer_7 finished			
	0,4580	SubAssembly layer_3 / layer_6 finished			

Design



Specification

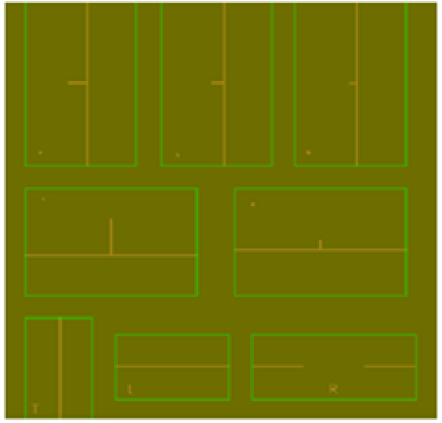
- Homogeneous Stack up with Low Dk / Df
- Eight Layer construction / Any layer
- Filled mechanical holes: D = 150µm
- Filled / Stacked Laser Drill holes: D = 150µm
- Line Width: 85µm
- Space between Lines: 85 µm
- Surface finishing: imm. Thin

Target

- Radio Frequency performance
- PCB performance
- Reliability

Material Characterisation

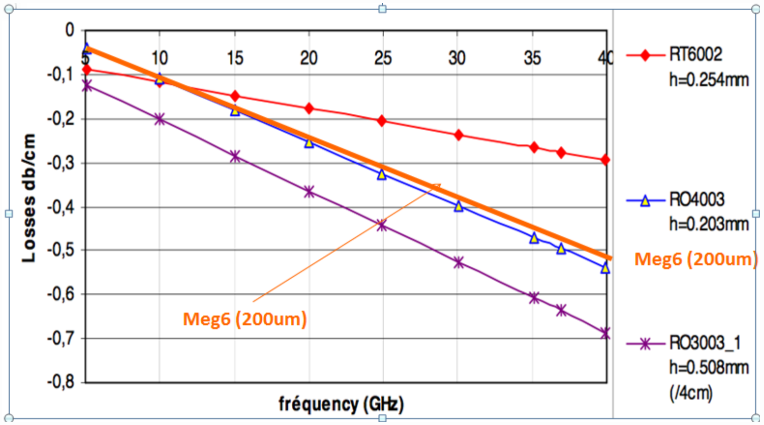
Specific Layout with different test pattern



ANRITSU Test Measurement

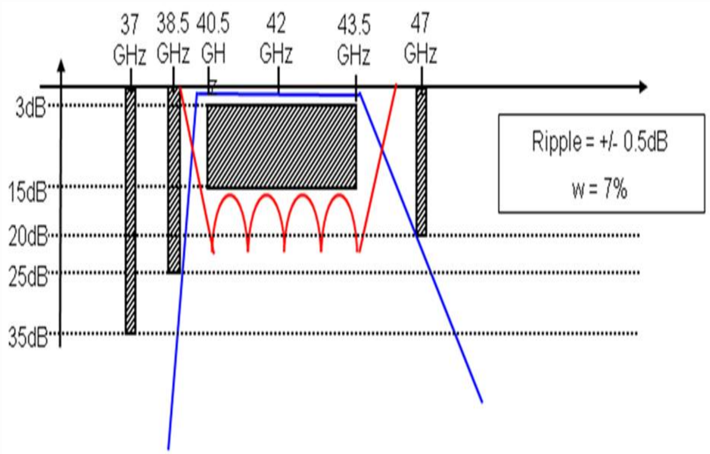
Results of this measurements

Dk, Df, Losses and Q Factor

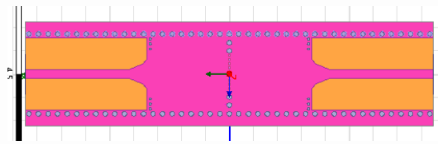


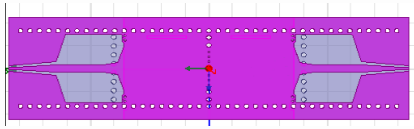
Design Simulation

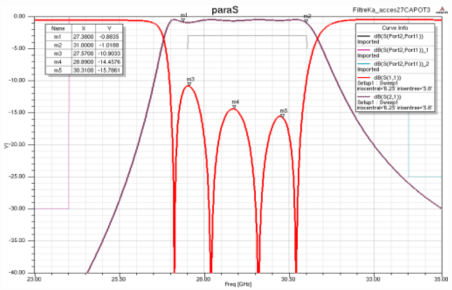
Specification

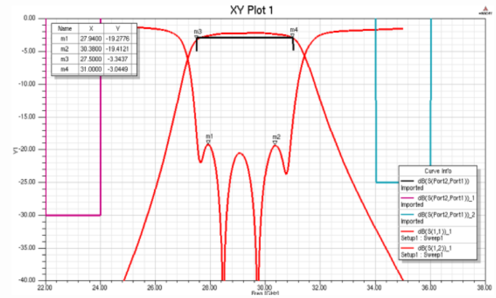


Design Variation / Simulation





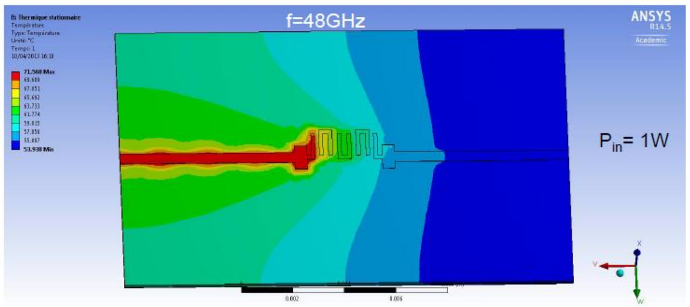


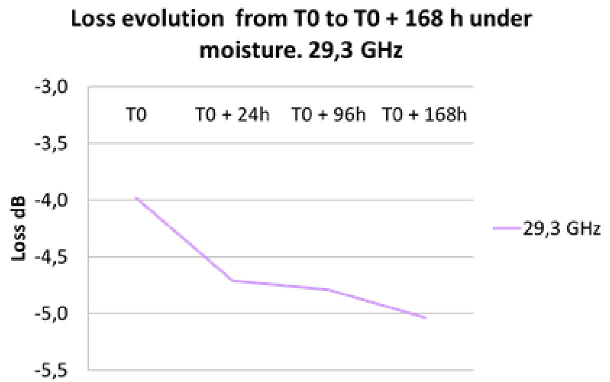


Investigation of thermal & moisture Aspects

Working with HFSS-ANSYS

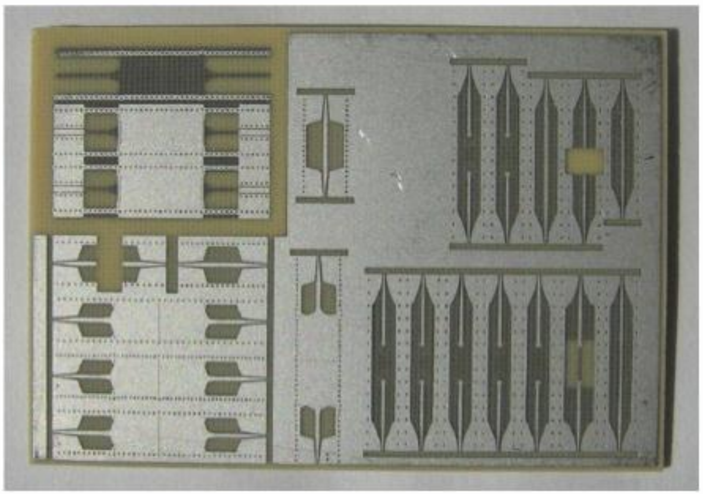
- Filter Elliptica, f=42.5GHz, h=200 um

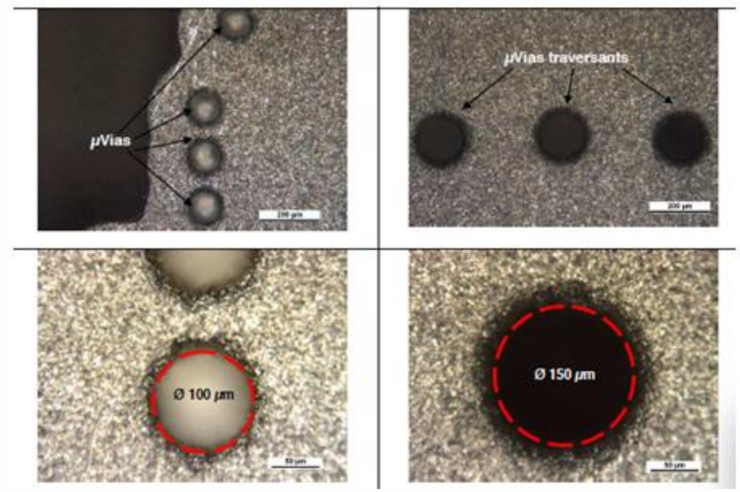




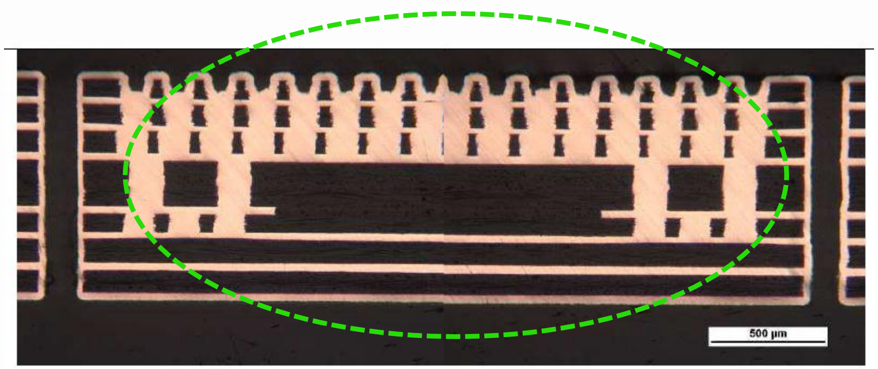
Manufacturing

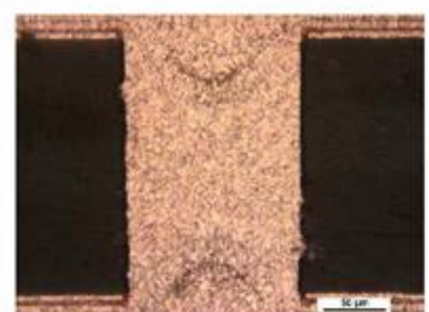
Filterboard Analyses





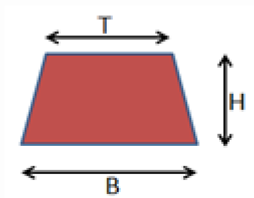
Cross Section





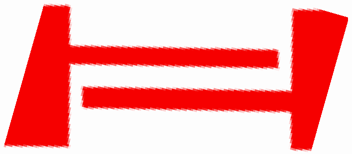
Validation of Structuring

Etch Factor

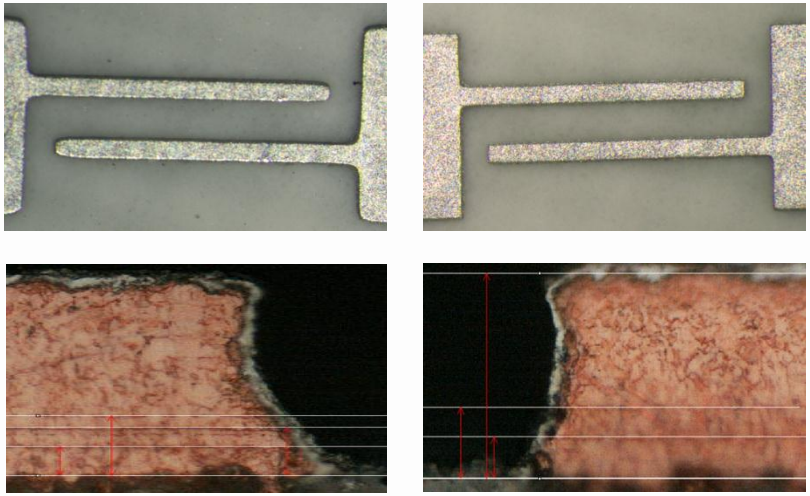


$$EF = \frac{2 \times H}{B - T}$$

EF = Etch Factor
H = Copper Height
B = Witdh Foot
T = Witdh Head



Customer Design / Manufacturing

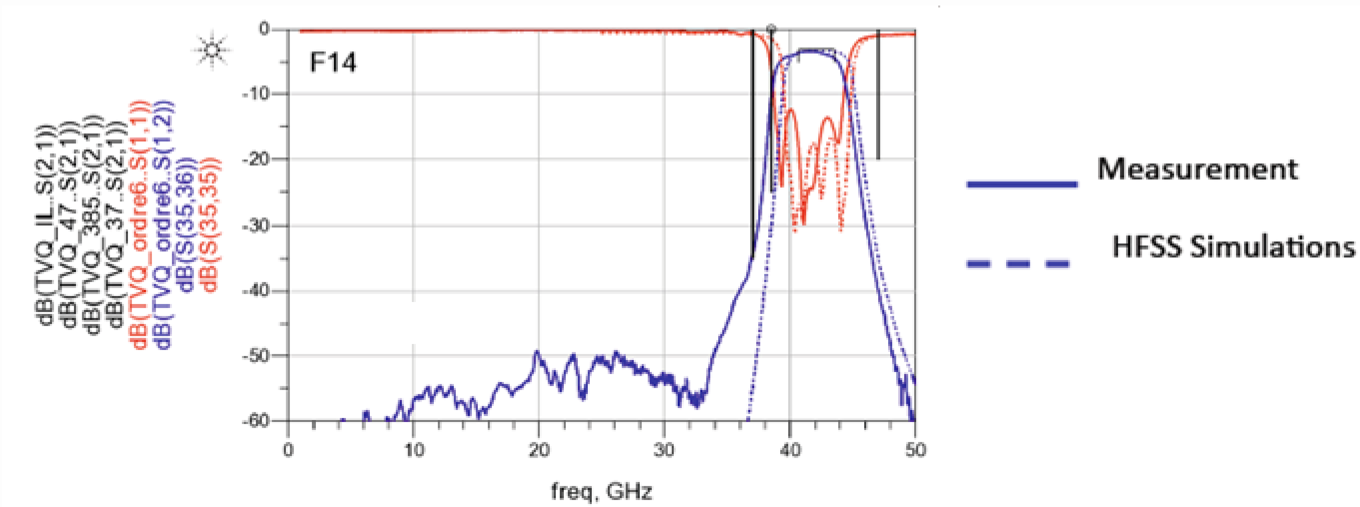


Investigation of Influence on the RF Behavior

Find best Conditions to reproduce RF critical Structure

Electrical & Radio Frequency Performance

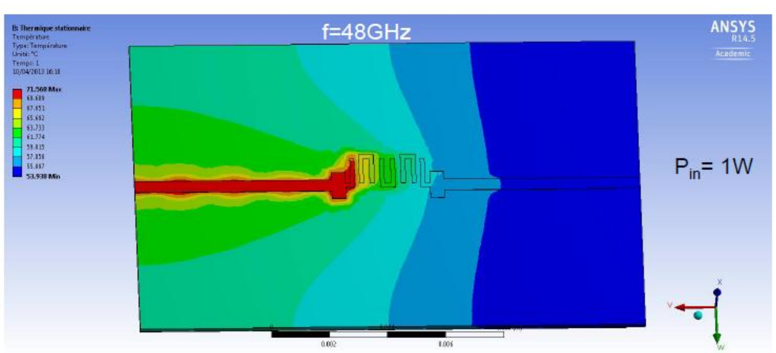
Filter measurements

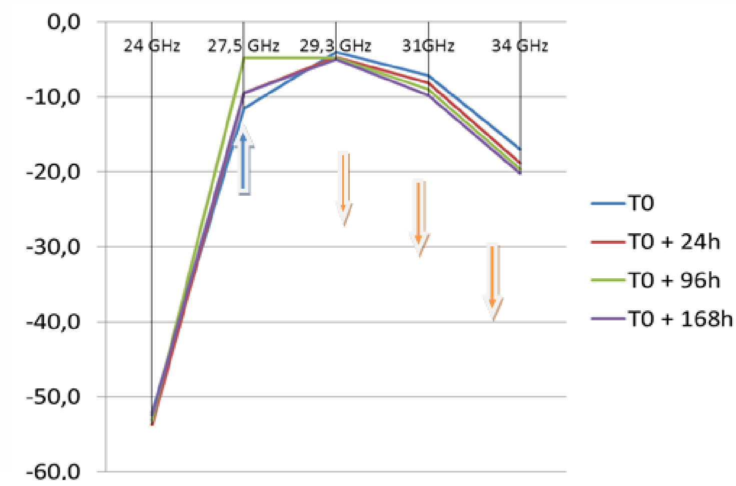


Thermal measurements / Moisture measurements

Working with HFSS-ANSYS

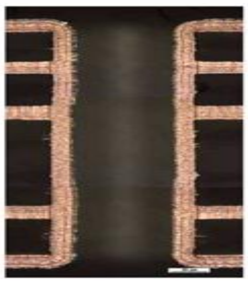
❑ Filter Elliptica, f=42.5GHz, h=200 um



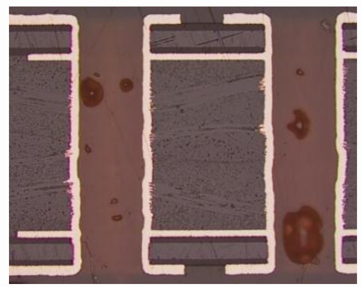


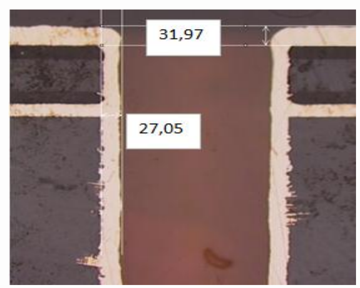
Cross Section Analysis

Low Dk / Df (organic based material)

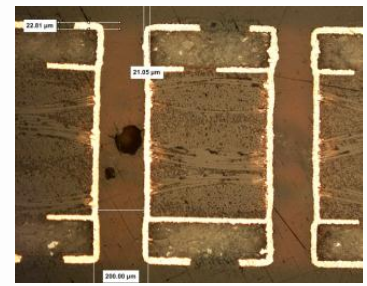


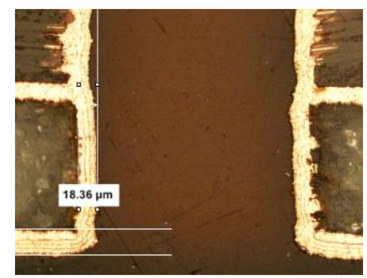
Very Low Dk / Df (PTFE / PI)

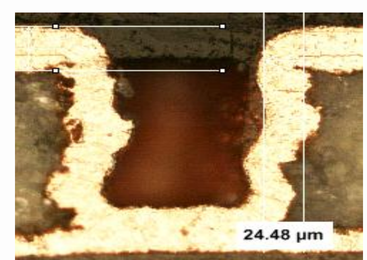




Very Low Dk / Df (PTFE / Ceramic)







Results Solder Float and Delamination Test

Material	Sample	Solder Float Test (10 sec @ 288°C)	Delamination Test 10 sec @ 270°C 60 sec @ 270°C
Low Dk Organic Material	1	ok	ok
	2	ok	ok
	3	ok	ok
Very Low Dk PTFE / Ceramic	1	ok	ok
	2	ok	ok
	3	ok	ok
Very Low Dk PTFE / Polyimide	1	ok	ok
	2	ok	ok
	3	ok	ok

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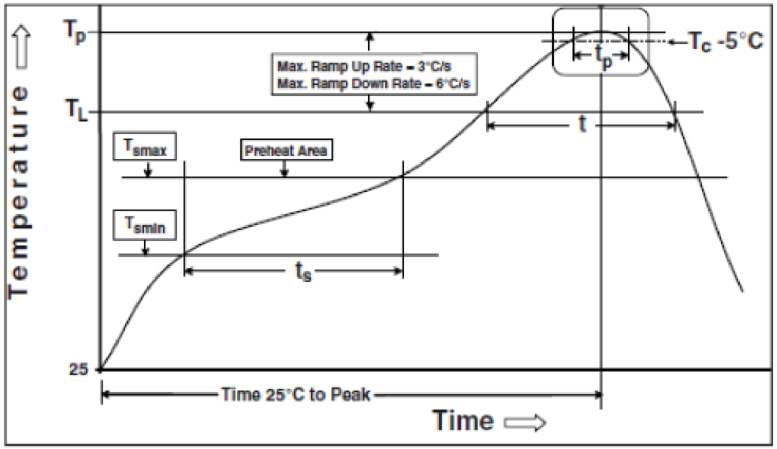
Results Lead Free Reflow Test



Pre-treatment	24h @ 125'C (+5/-0'C)
Pre-treatment	40h @ 60'C/60%RH
Reflow	Minimum 8 x Pb-free reflow

Material	Sample	Pre check electrical & visual	Drying 24h@125°C Humidification 40h@ 60/60	Standard Lead Free Reflow Profile 1	2	3	4	5	6	7	8	9	10	...	15	Final inspection electrical & visual
Low Dk Organic Material	1	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	2	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	3	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
Very Low Dk PTFE / Ceramic	1	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	2	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	3	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
Very Low Dk PTFE / Polyimide	1	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	2	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	3	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok

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Result Temperature Cycle Test

Material	Sample	Pre check electrical & visual	Temperature cycle test [cycles] 100	200	300	400	500	600	700	800	900	1000	Final inspection electrical & visual
Low Dk Organic Material	1	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	2	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	3	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
Very Low Dk PTFE / Ceramic	1	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	2	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
	3	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok
Very Low Dk PTFE / Polyimide	1	ok	ok	ok	ok	ok	ok	ok	ok	n ok	n ok	n ok	n ok
	2	ok	ok	ok	ok	ok	ok	ok	n ok	n ok	n ok	n ok	n ok
	3	ok	ok	ok	ok	ok	ok	ok	n ok	n ok	n ok	n ok	n ok

IPC-JESD22-A104B

Conclusion of Test vehicle 1

→ Positive manufacturing of Hybride Build up was demonstrated
(e.g. PTFE / FR4)

→ Performance of Reliability is comparable with homogeneous FR4 Build up

Conclusion of Test vehicle 2

→ Positive manufacturing of Homogeneous Build up with organic based material for 42GHz Filter was demonstrated
(e.g. Low Dk / Df)

→ Performance of 42 GHz Radio Frequency application meet the specification

Outlook

→ Find the speed (frequency) limits for organic based materials in homogeneous Layer construction

→ Identify Know How Transfer defindings of Design and manufacturing into Hybrid Build up (FR4 / very low Dk materials)

→ Investigation for LCP Materials(PTFE replacement)

Cost attractive (Material)
Low Moisture absorption
Thin Base Material (50µm)