Insertion Loss Reduction through Non-Roughening Inner-Layer Surface Treatments

Scott Hinaga
Staff Engineer, PCB Technology Group
Cisco Systems, Inc.
San Jose, CA 95134
Email: shinaga@cisco.com

Aleksei V. Rakov, Marina Y. Koledintseva, James L. Drewniak,
EMC Laboratory, Missouri University of Science & Technology
Rolla, MO 65401

Abstract
As channel speeds approach 25 Gbps, near the expected maximum bandwidth for traditional copper-based PCBs, every available tool to minimize total insertion loss in the board material system will need to be deployed. Material suppliers have devised low-Dk, low-loss dielectrics and fiberglass, as well as ultra-low-profile copper foils. However, one of the last remaining factors has not yet been quite so actively developed – the surface treatment applied by the PCB shop to the innerlayer cores prior to lamination.

In a previous paper presented at IPC, we described the effects of copper foil types, of varying levels of roughness, upon measured insertion loss of a stripline structure. We further showed the relative impact of different surface treatments (oxide and oxide alternative) which were then current in the industry. Recently, however, PCB chemical suppliers have begun offering new treatments targeted specifically at insertion loss and surface roughness minimization, whereas prior formulations were aimed at maximization of bond strength and prevention of pink-ring.

This paper builds upon our previous work by examining the insertion loss impact of such chemistry, holding constant the dielectric, test vehicle board design, and measurement technique used earlier. We are thus able to characterize the relative contribution of lower-roughness innerlayer treatment chemistry to loss reduction, as compared to conventional formulations.

Introduction and Background

In previous papers **[1-4]** we have addressed the topics of signal attenuation in transmission lines due to skin effect loss and surface roughness in copper conductors on printed circuit boards (PCBs), as this issue is of considerable consequence for designers and modelers of high-speed (>10 Gb/s) circuits. As demonstrated in **[1]**, the roughness profile of an inner-layer trace is influenced not only by the grade of copper foil used on the laminate core material, but also by the oxide or alternative-oxide inner-layer treatment process applied by the PCB fabricator. In this paper, we characterize the contribution to insertion loss due to roughness attributable specifically to the foil and oxide sides of the stripline conductor.

Samples and Measurement Method

Samples for the analysis consist of a 3-layer balanced stripline structure of 50Ω impedance, and 0.5-oz (18 μm) copper foil weight on all layers. The dielectric is a low-loss material (Panasonic Megtron 6) with a construction of 2x2116 glass style, 54% nominal resin content, on either side of the trace. The width of the traces was verified by micro-sectional analysis as within the range of 265±2 μm (top) and 273±3 μm (bottom). The length of the trace under test is 406 mm (16”). The PCB is equipped with four TRL calibration traces of lengths corresponding to frequency breakpoints of 0.281, 1.581, and 8.891 GHz, respectively, a THRU standard trace, and an OPEN standard trace, which is a stub half the length of the THRU trace.

The transition vias between the traces on layer 2 and the surface pads were drilled at 0.25 mm. At a stub length of only 0.2 mm, backdrilling to reduce parasitics was deemed unnecessary. Surface finish used on the external layers of the PCB is Electroless Nickel-Immersion Gold (ENIG), in order to minimize oxidation of the contact interface between the PCB and SMA connectors. As shown in **Table 3** below, the only intended variation between the sample sets was in the foil type and innerlayer surface treatment.

The foils used in this test were supplied by Circuit Foil, Inc. (Wiltz, LU) and were of the three types shown below in **Table 1**. Roughness (Rz) measurements were taken by the manufacturer on the specific manufacturing lots used in this test. As the reverse-treated RTF foil is textured on both sides, the Rz value applies to both surfaces, whereas the ED (electro-deposited) foils have negligible roughness on the 'shiny' side. Measurements on the HFz and HFi foils were taken by stylus profilometer, while those on the ultra-smooth ANP foil were additionally performed on a non-contact profilometer due to the Rz being below the resolution of the stylus.

Table 1
Foil types used in testing

Class	Foil Trade Name	Rz (µm)
RTF	HFz-B	4.2
ED	BF-HFi-LP2	1.8
ED	BF-ANP-PA	1.0*

*non-contact measurement – stylus measurement was 1.7µm

The innerlayer surface finishes were applied by chemical supplier MEC Co. (Amagasaki, JP) and were of the types shown below in **Table 2**. The V-Bond and EtchBond products are peroxide-sulfuric-based oxide alternatives which texturize the copper surface through micro-etching along the foil's grain boundaries. FlatBond is a new type of non-roughening innerlayer finish based on immersion tin with a silane-based adhesion promoter. Reduced Black Oxide is a traditional innerlayer surface treatment which has been in use in the PCB industry for some twenty years.

Table 2
Innerlayer surface treatment types used in testing

Type	Roughness (µm)
Reduced Black Oxide (RBO)	0.05 (Ra)
BO-series V-Bond (BO-0.5)	0.5 (Rz)
BO-series V-Bond (BO-1.5)	1.5 (Rz)
EtchBond (CZ8100)	1.5 (Rz)
Immersion Tin (FlatBond)	0.04 (Ra)

Note that the "V-Bond" finish was run under two different conditions of the peroxide-sulfuric microetch, resulting in 0.5 and 1.5 µm Rz measurements. Roughness measurements shown were provided by the supplier, with the measurements for RBO and FlatBond being expressed as Ra rather than Rz. Both terms can be derived from a common measurement data set, but differ in their statistical definitions (see, for example, **[6]**); as a result, the value of Ra is smaller than the value of Rz for the same surface.

A total of seven combinations of foil and surface treatment were prepared, as detailed in **Table 3**; for each such combination, three individual boards were measured. Loss values for each sample set shown under **Results** below are the average values of each triplicate measurement.

Table 3
Foil and innerlayer treatment combinations under test

Sample Set No.	Foil and Surface Treatment	No. of Samples
1	BF-HFi-LP2 + FlatBond	3
2	BF-HFi-LP2 + EtchBond	3
3	BF-HFi-LP2 + BO (0.5)	3
4	BF-HFi-LP2 + BO (1.5)	3
5	BF-HFi-LP2 + RBO	3
6	HFz-B + FlatBond	3
7	BF-ANP-PA + FlatBond	3

The measuring instrument used was an Agilent N5245A PNA-X vector network analyzer in two-port mode. Compression-fit SMA connectors (Molex P/N 73251-1850) were used to interface the PCBs to the VNA cables. Measurements were conducted under ambient conditions (20-25 ˚C, following stabilization of the VNA). It should be noted that the stripline structure of the test vehicle requires that the external layers be almost entirely metal-clad (exposed laminate represents <0.2% of the surface area). Furthermore, the traces under test are recessed from the edge of the PCB by 25mm or more. These design factors combine to isolate the dielectric nearest the test traces from variation due to absorption of moisture resulting from varying atmospheric humidity.

Following a four-point TRL calibration on each individual board, S-parameter measurements were taken over a range of 10 MHz – 20 GHz. For the purposes of this report, the specific values at 10 GHz were selected for analysis. 16 consecutive readings, each of 6401 individual points, were taken on each individual board, and the average of these 16 readings was used to generate the final S-parameter set for each board. As noted above, each of the seven sample sets consisted of three separate boards, and the values reported for each set were generated by averaging the readings from the three boards in each set.

Quality assurance for each measurement consisted of a causality-passivity check, and verification that the return loss $|S_{11}|$ was no worse than -20 dB at any point on the spectrum. The values of insertion loss $|S_{21}|$ were validated against previous Megtron 6 test boards of the same design and layer stack-up.

Measured Insertion Loss Results

The 3-board measurement averages for each of the sample sets are shown in **Table 4** below. The insertion losses shown are those of the entire 406mm traces under test, while the composite values of Df (dissipation factor) shown were extracted using Cisco's S3 Test Method algorithm described in **[1].** The flowchart of the S3 technique is given in **[4, Fig.1]**.

Table 4
Measured values of insertion loss at 10 GHz

Sample Set No.	Foil and Surface Treatment	|S21|, dB	Composite Df
1	BF-HFi-LP2 + FlatBond	-6.81	0.0063
2	BF-HFi-LP2 + EtchBond	-7.24	0.0072
3	BF-HFi-LP2 + BO (0.5)	-7.01	0.0068
4	BF-HFi-LP2 + BO (1.5)	-7.23	0.0071
5	BF-HFi-LP2 + RBO	-6.95	0.0065
6	HFz-B + FlatBond	-7.41	0.0076
7	BF-ANP-PA + FlatBond	-6.96	0.0065

Although incidental to the goal of this project, it was possible to use the S3 algorithm to extract the values of dielectric constant (Dk) for each sample set based on the phase component of the S-parameters.

The extracted values of Dk covered a range of 3.70 – 3.74 across the sample set, a very reasonable span in view of manufacturing tolerances (discussed below) and measurement error.

Discussion and Opportunities for Further Work

Total insertion loss on a single-ended stripline, in the form of $|S_{21}|$ as measured, is the sum of dielectric and conductor losses. In order to attribute the above measurement differences solely to variation in surface roughness, it is necessary to establish that other variables which contribute to dielectric and conductor loss are negligible within the sample set. In the case of dielectric loss, resin content (RC%) must remain constant, and when all samples within the set have the same layer construction (stack-up), dielectric thickness may be used as a proxy for RC%. Micro-sectional analysis of the sample boards performed as described in [5] showed that the core (CCL) material thickness fell within a span of 245±4 μm, while the pre-preg thickness spanned a range of 232±3 μm. In both cases, the levels of variation seen are well within standard manufacturing tolerances for PCBs and laminate.

In the case of conductor loss, variation in trace geometry contributes to variation in loss, and must be demonstrated negligible prior to attempting to characterize differences as due to surface roughness. The test traces of our sample set showed a range of 265±2 μm at the tops of the traces and 273±3 μm at the bottoms. Trace thickness fell within a range of 16±1.7 μm. Such levels of variation also fall well within standard PCB manufacturing tolerances.

Within the limits of reasonable manufacturing tolerances, the differences in the measured insertion loss values may be thus attributed to the differences in surface roughness between the sample sets.

As expected, among Sets #1, 6, and 7, in which the surface treatment (FlatBond) was held constant, the highest loss was seen on Set #6 which used the roughest (RTF-type) foil, measuring 0.60 dB greater in loss than Set #1. Results of sets #1 and #7 seemed to be inverted in that the stylus-measurement Rz of the ANP foil was slightly lower than that of the HFi. However, given the known difficulty in performing contact profilometry on ultra-low-profile foils, a difference of 0.1 μm must be regarded as within measurement error. A non-contact profilometry value of 1.0 μm was provided for the ANP foil; unfortunately, no corresponding measurement for HFi foil was available.

When the foil was held constant (Sets #1 through #5), a difference of 0.42 dB was observed between the best (#1) and the worst (#2) cases. Although this value may not seem large in absolute terms, within a large-form-factor router or switch chassis, total channel length (linecard-backplane-linecard) may reach 1 m (39.3”), for a corresponding loss delta of 1.03 dB, which would be significant at channel rates in the 25-28 Gbps range, given the expected SI margins involved.

It should be noted that our three-layer balanced single-stripline structure equally weights the roughness of the foil and oxide sides of the trace. In a dual-stripline layer structure (plane-signal-signal-plane) this weighting would no longer be equal. If this four-layer structure were to be constructed as Core-Prepreg-Core, the foil sides of the traces would contribute relatively more to the total channel loss due to the foil sides’ closer proximity to the reference planes. In the corresponding alternate construction, Prepreg-Core-Prepreg, this effect would be inverted and the contribution of the oxide sides would be greater. Characterization of dual-stripline structures through measurement of physical test vehicles would pose an interesting avenue for further study.

In the time since these measurements were performed, copper foil manufacturers have further evolved their product lines, releasing foils which are nearly completely profile-free (Rz <0.5 μm). In these products, a priming resin coat is applied to the foil as the primary means of adhesion between the foil and underlying pre-preg, since the profile is so low as to nearly eliminate mechanical adhesion between foil and pre-preg. In the future, these products may approach the theoretical lower bound of zero roughness, represented by mirror-bright foil. The data set presented here should be extended with corresponding measurements on such foils, both for comparison with earlier products and for validation of insertion loss models incorporating a surface roughness term.

Conclusion

Printed circuit board test vehicles using a 50-ohm balanced-single-stripline construction were manufactured using low-loss dielectric and several combinations of low-roughness copper foil and innerlayer surface finishes. Insertion loss measurements using the Cisco S3 test method were performed, with TRL calibration employed to de-embed connector and launch structure effects. With dielectric characteristics (thickness, resin-glass ratio) held constant, as well as the dimensions of the stripline trace, the measured differences in insertion loss could be attributed solely to the differences in surface

roughness of the stripline traces. In a subset of the test samples, the copper foil type was held constant with variation only in the innerlayer surface finish, thus allowing further differentiation as to the effect of the surface finish alone. The combination of lowest-roughness surface finish and foil demonstrated a reduction of 0.60 dB insertion loss on the 16" line at 10 GHz as compared to a combination of lowest-roughness surface finish and RTF foil. The combination of lowest-roughness surface finish and foil demonstrated a reduction of 0.42 dB on the 16" line at 10 GHz as compared to a combination of lowest-roughness foil and conventional alternative-oxide surface finish. While these insertion loss reductions are not large in magnitude, they can still be significant in the context of further minimizing total channel loss in a PCB, especially in large-form-factor systems in which the lowest-loss dielectric has already been deployed.

Acknowledgements

The author wishes to acknowledge Circuit Foil, Inc. and MEC Co. for provision of the copper foil and innerlayer surface finishing used in this study, Panasonic for provision of the Megtron 6 base material, and Toppan NEC Circuit Solutions for manufacturing of the test vehicle PCBs.

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Biographies

Scott Hinaga holds the position of Staff Engineer in Cisco's PCB Technology Group, and is responsible for investigation and characterization of new laminate materials. He holds a B.S. from Stanford University, joined Cisco in 2004 and has PCB manufacturing and engineering management experience dating back to 1985.

Aleksei V. Rakov received his M.S. degree (with highest honors) in RF Physics and Electronics from National Research University "Moscow Power Engineering Institute", Moscow, Russia in July 2011, and then joined EMC Laboratory of Missouri University of Science and Technology as a graduate student. He defended his M.S. thesis in Electrical Engineering in July 2013, and in September 2013 joined "Information Technology Laboratory" (Lintech), Moscow, Russia, as an engineer.

Marina Y. Koledintseva, Ph.D., has been a Research Professor at the Missouri University of Science and Technology, Electrical and Computer Engineering Department, since 2000. Before that she was a Senior Scientist and Associate Professor of Radio Engineering Department of National Research University "Moscow Power Engineering Institute", Moscow, Russia.

James L. Drewniak, Ph.D., since 1991 has been a Professor with the Missouri University of Science and Technology (MS&T), formerly known as UMR, Electrical and Computer Engineering Department. In 1995-2008 he was the co-director of the EMC Laboratory and the EMC Consortium. In 2002-2007 he was the Director of the Materials Research Center of the same University.

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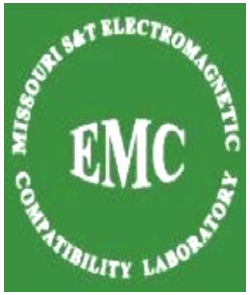
Staff Engineer, PCB Technology Group
Cisco Systems, Inc.
San Jose, CA 95134
Email: shinaga@cisco.com



Channel Speed Range – By Platform

Low ← Cost → High

IP Phone

Telepresence

<2 Gb/s

Small Router,
Blade/Rack Server

2-5 Gb/s

Enterprise and
SAN Switch

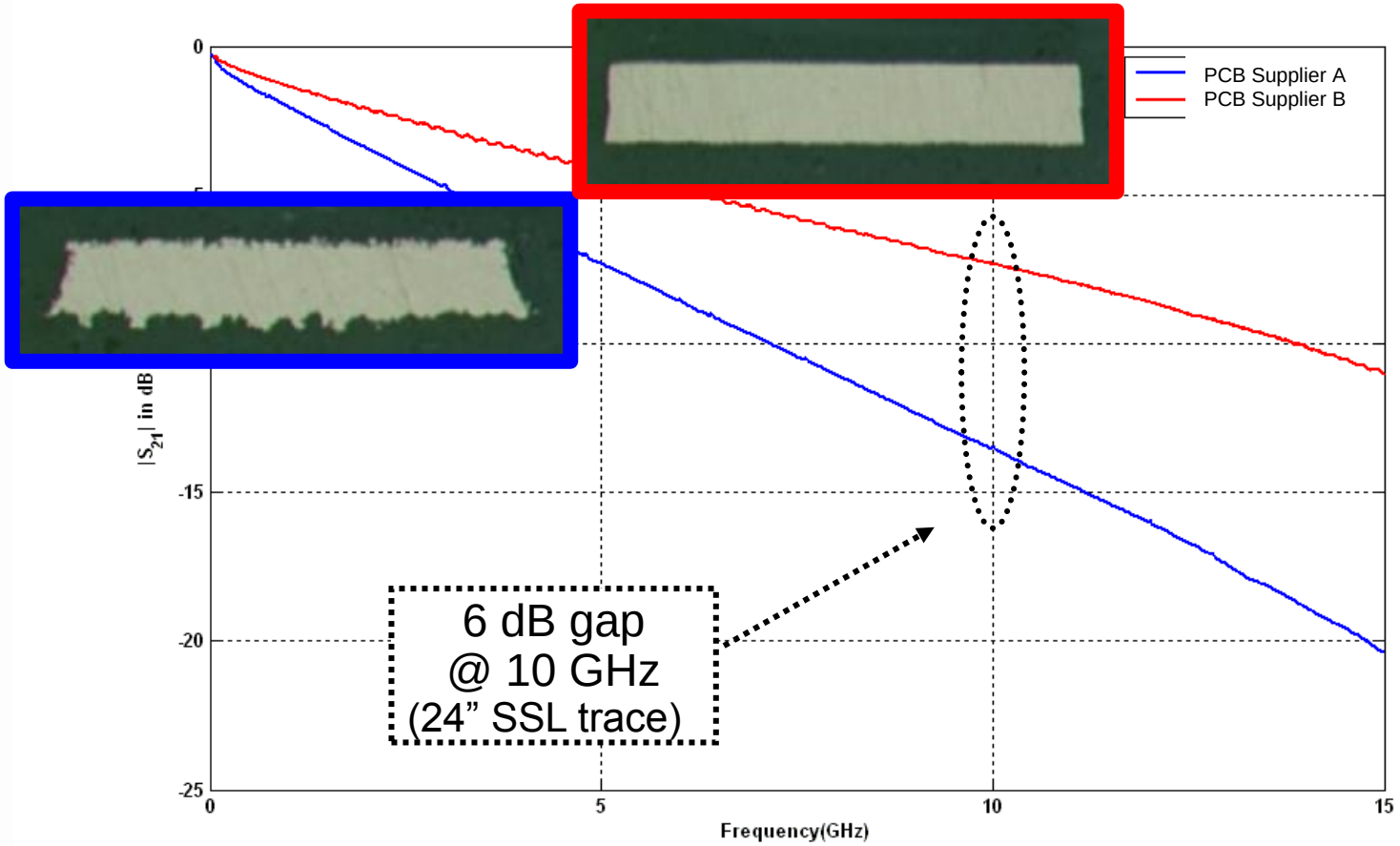
5-10 Gb/s

Edge Router
Core Router

10-25+ Gb/s

Lower ← **Channel Speed / Electrical Performance** → Higher

Real-Life Example – Impact of Cu Foil Rz

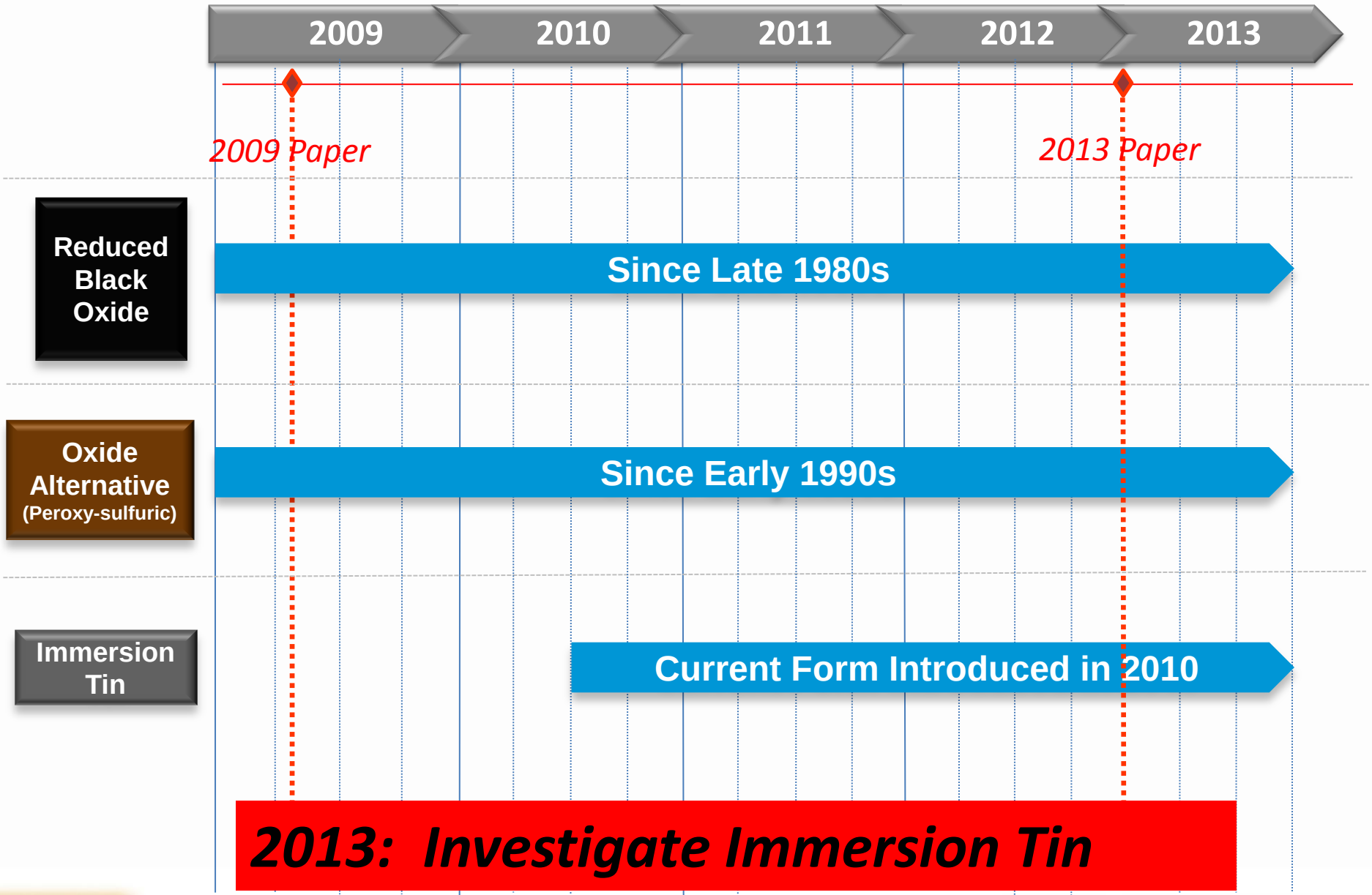


|S21| insertion loss of an SI test card built by two PCB suppliers, one with **rough** traces and one with **smooth**.

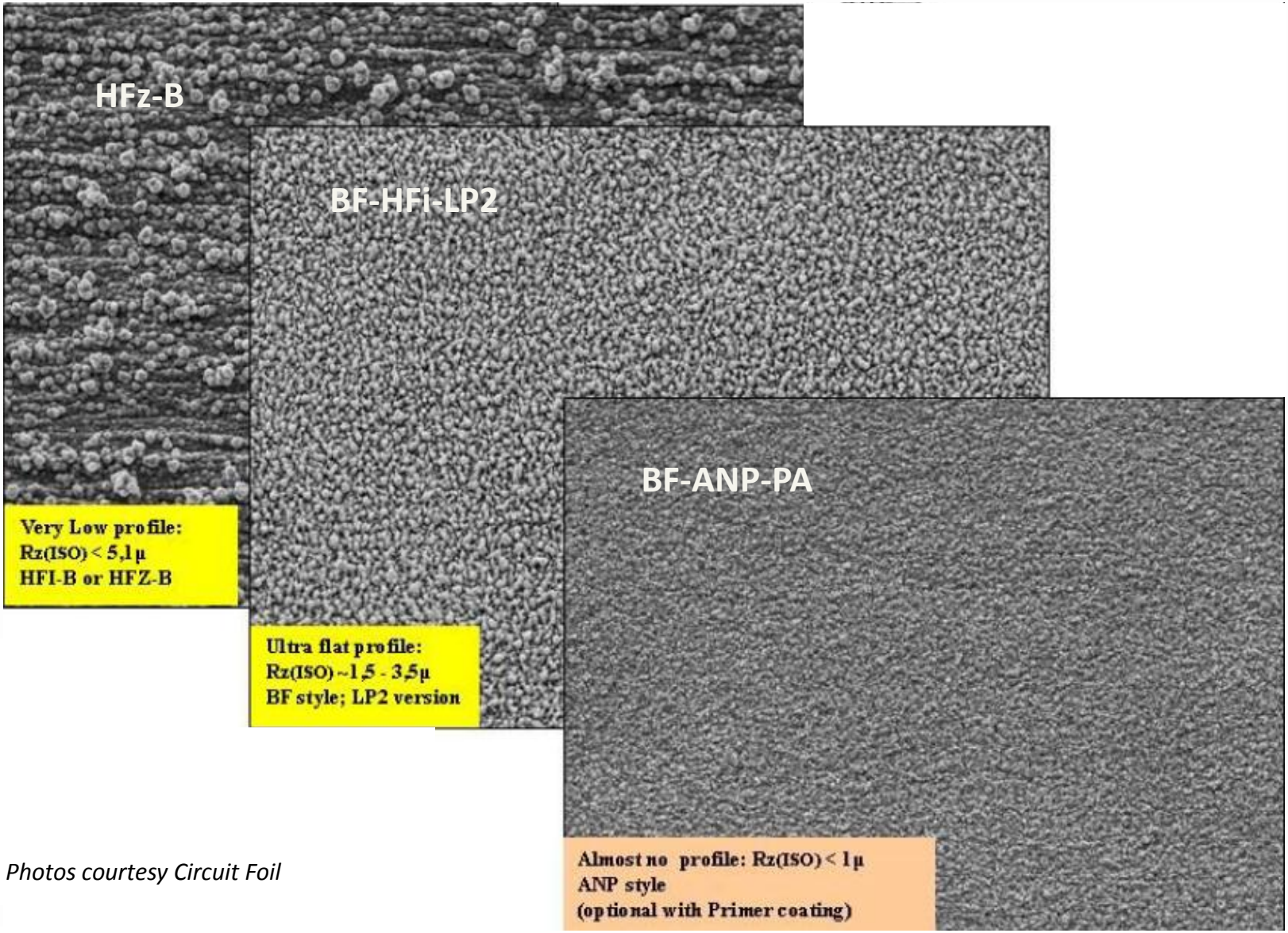
Inner-layer trace surfaces

The PCB shop applies an oxide coating to top and side surfaces to maintain bond strength. Rougher surface = stronger bond.

Bottom side of trace is textured by the copper foil maker who supplies the laminate manufacturer. This texture is formed during mfg. of the foil itself.

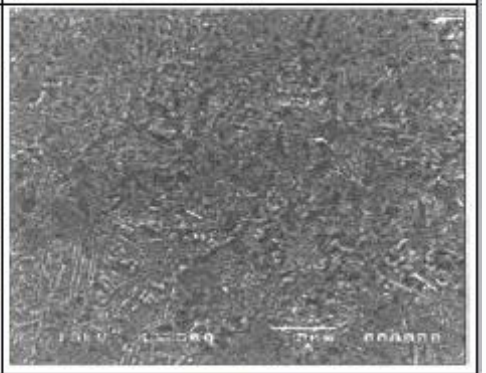

2009
2010
2011
2012
2013
2009 Paper
2013 Paper
Reduced Black Oxide
Since Late 1980s
Oxide Alternative (Peroxy-sulfuric)
Since Early 1990s
Immersion Tin
Current Form Introduced in 2010
2013: Investigate Immersion Tin

Copper foils used in study

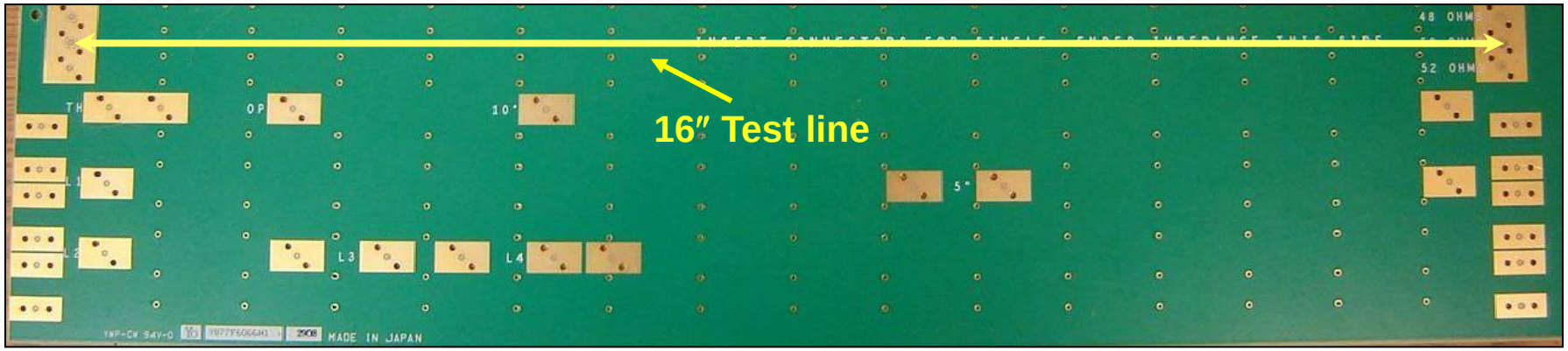


Photos courtesy Circuit Foil

Innerlayer Surface Finishes Used In Study

	Surface Roughening (CZ-8101:1um)	New Treatment (*FlatBOND*)
SEM X3,500		
Ra*(um)	0.27	0.04

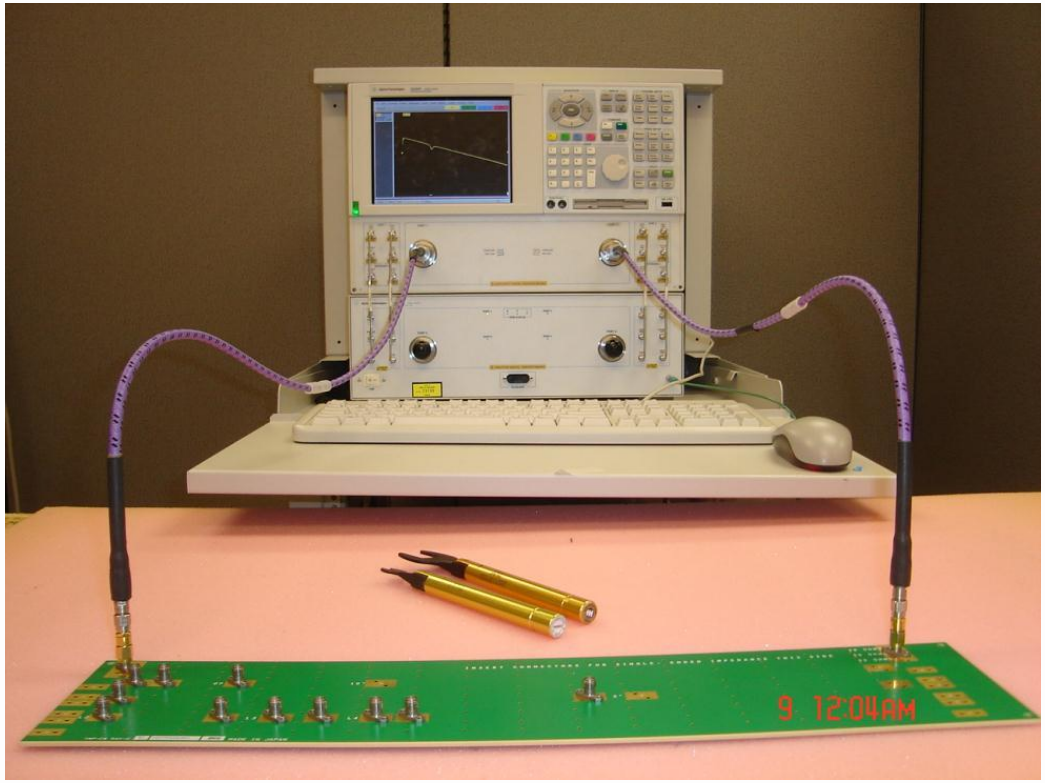
Photos courtesy MEC Co.



S3 TV Board

- 16” (406mm) balanced stripline, TRL cal pattern
- Launch thru low-loss SMA jacks (compression-fit)
- Megtron 6 material, ~50% RC on both sides (2x2116)
- Cu weight 0.5 oz. Line width 270 µm nominal
- Variables are base foil roughness and I/L treatment

S3 Testing Setup



2-port VNA: Agilent N5245A
Range 10 MHz – 20 GHz

Foil – Innerlayer Finish Testing

Calibration and measurement details

- No. of samples : 21
- Cal type : TRL
- No. of averages for calibration : 16
- No. of averages for measurement : 16
- No. of points : 6401
- Network Analyzer : Agilent N5245A

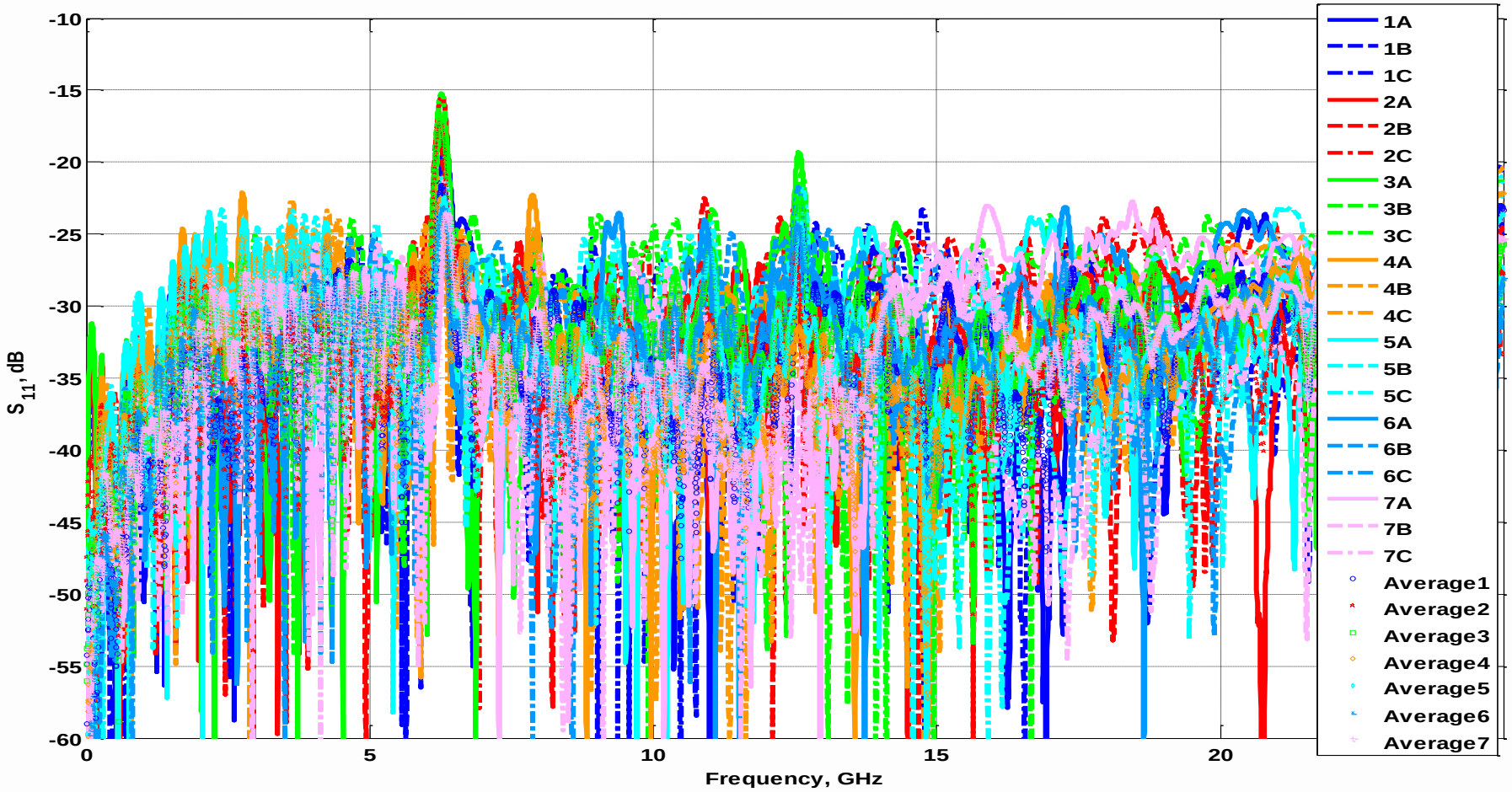
Foil – Innerlayer Finish Testing

Sample Identification

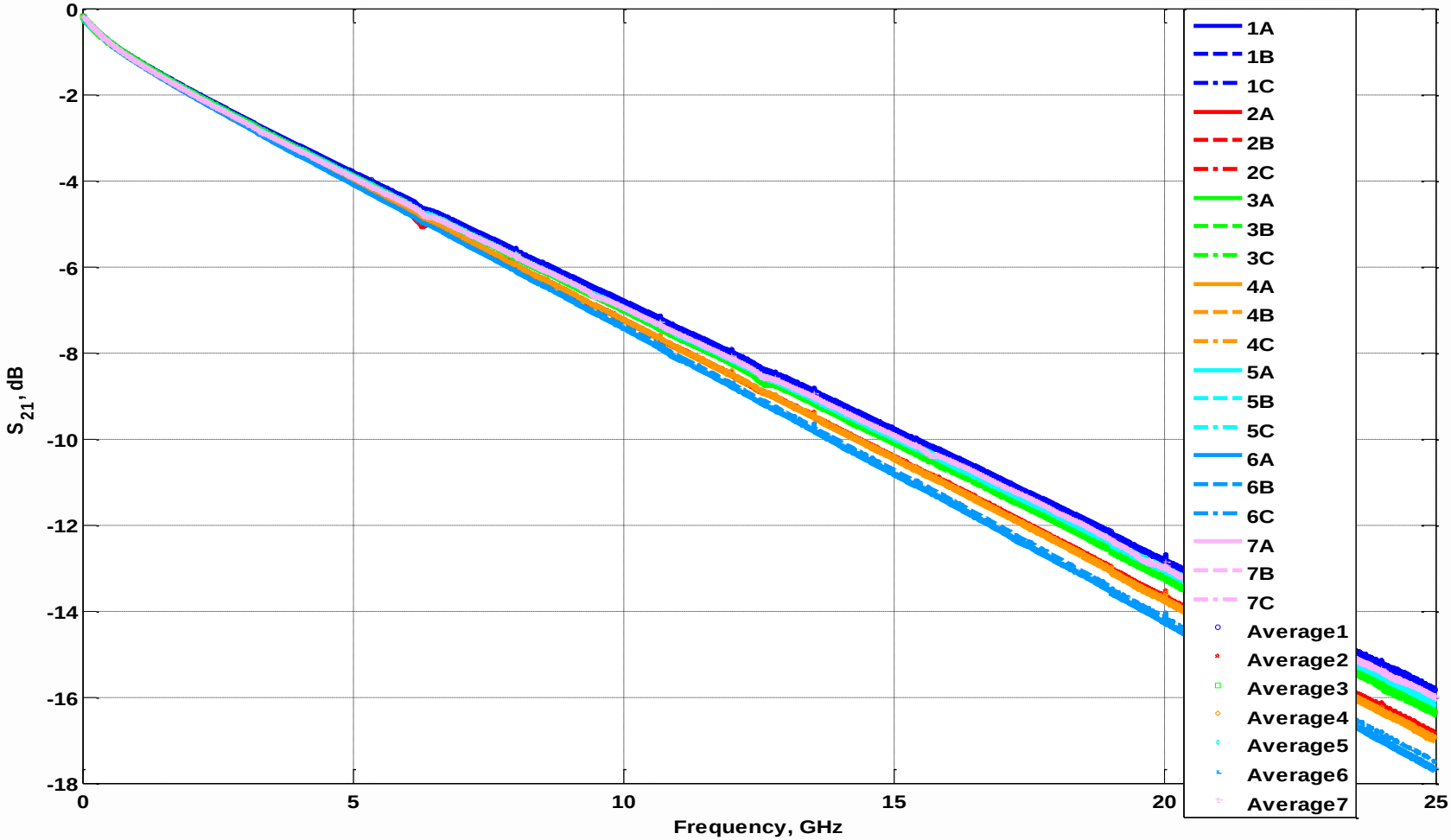
- No. 1 = BF-HFi-LP2 (1.8 µm Rz) + FlatBond (0.04µm Ra)
- No. 2 = BF-HFi-LP2 + CZ-8100 (1.5 µm Rz)
- No. 3 = BF-HFi-LP2 + BO-7770V (0.5 µm Rz)
- No. 4 = BF-HFi-LP2 + BO-7770V (1.5 µm Rz)
- No. 5 = BF-HFi-LP2 + RBO (Reduced Black Oxide, 0.05µm Ra)
- No. 6 = HFz-B (4.2 µm Rz) + FlatBond
- No. 7 = BF-ANP-PA (1.7 *[1.0*]* µm Rz) + FlatBond *[*non-contact]*

- Three identical samples for each of the 7 builds were tested. These were identified as 1A, 1B, 1C…7A, 7B, 7C. Structure is 50Ω single-ended stripline
- All Cu is H-oz. Actual thickness measurement 16 ± 1.7 µm
- Dielectric is Panasonic Megtron 6, 2 x 2116, 54% RC.
- Line = 16” length. Width (top) = 265 ± 2 µm, and (bottom) = 273 ± 3 µm
- Dielectric height (prepreg) = 232 ± 3 um, and (core) = 245 ± 4 µm

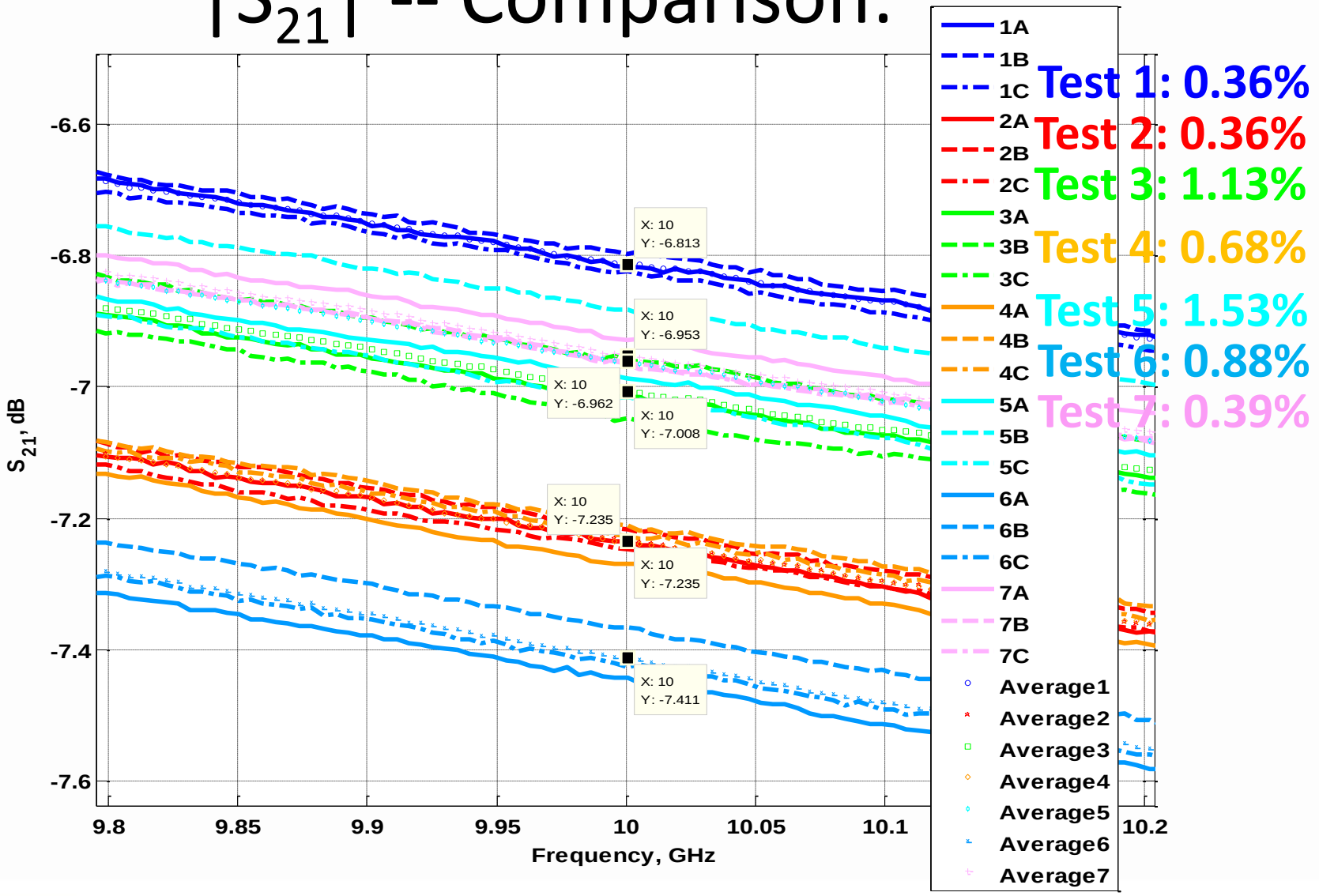
$|S_{11}|$ -- Comparison:



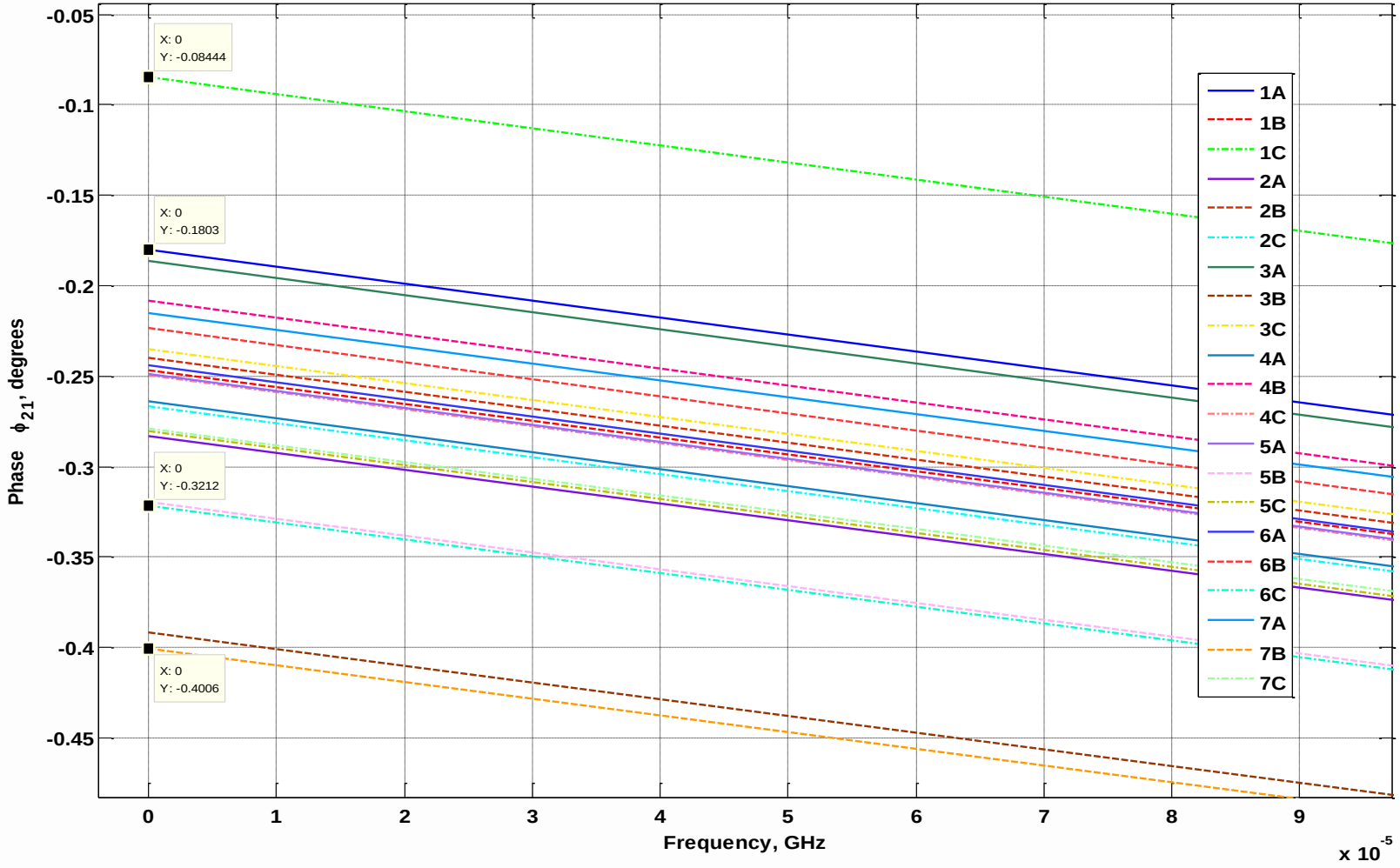
$|S_{21}|$ -- Comparison:



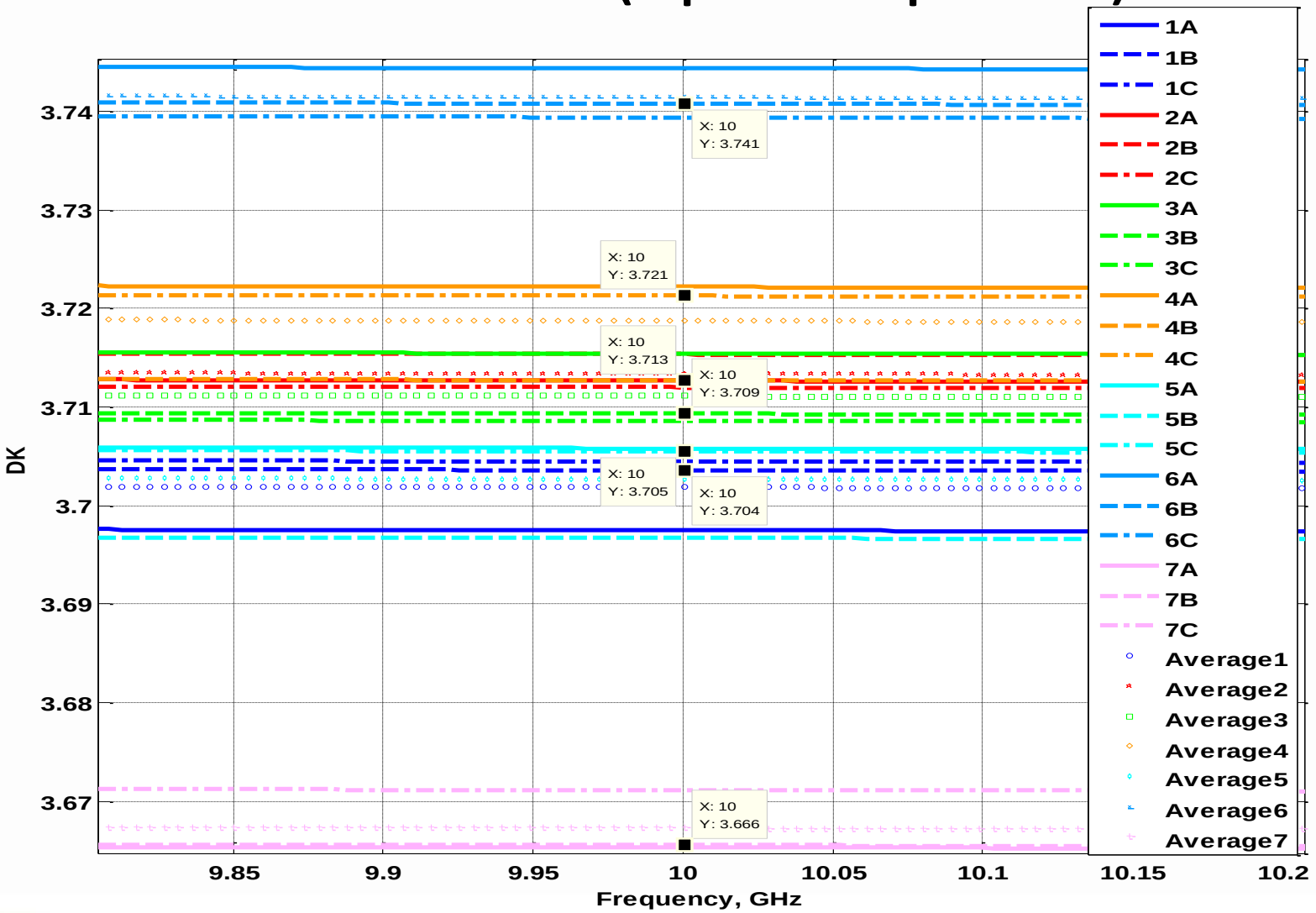
$|S_{21}|$ -- Comparison:



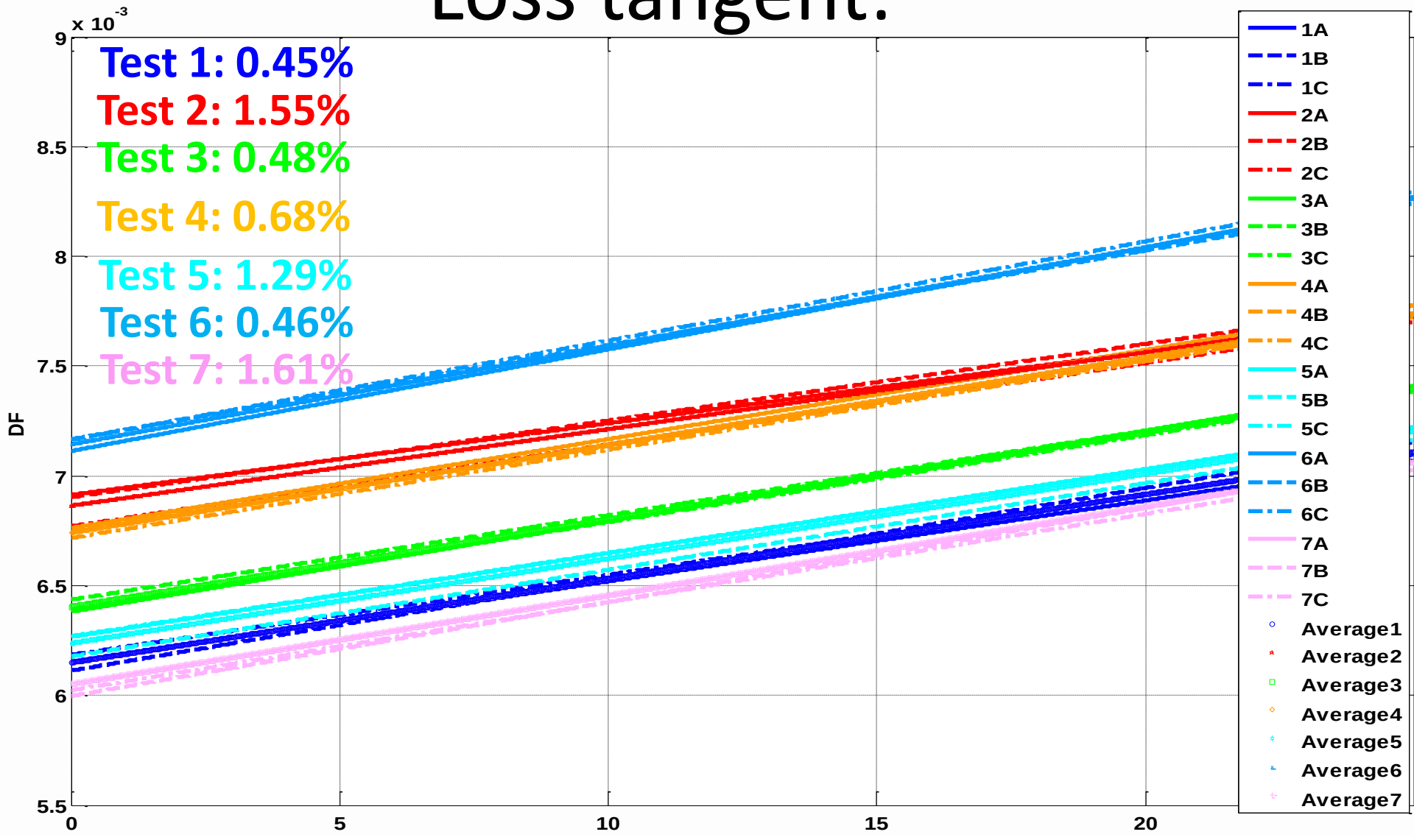
Phase (S_{21}) – Comparison:



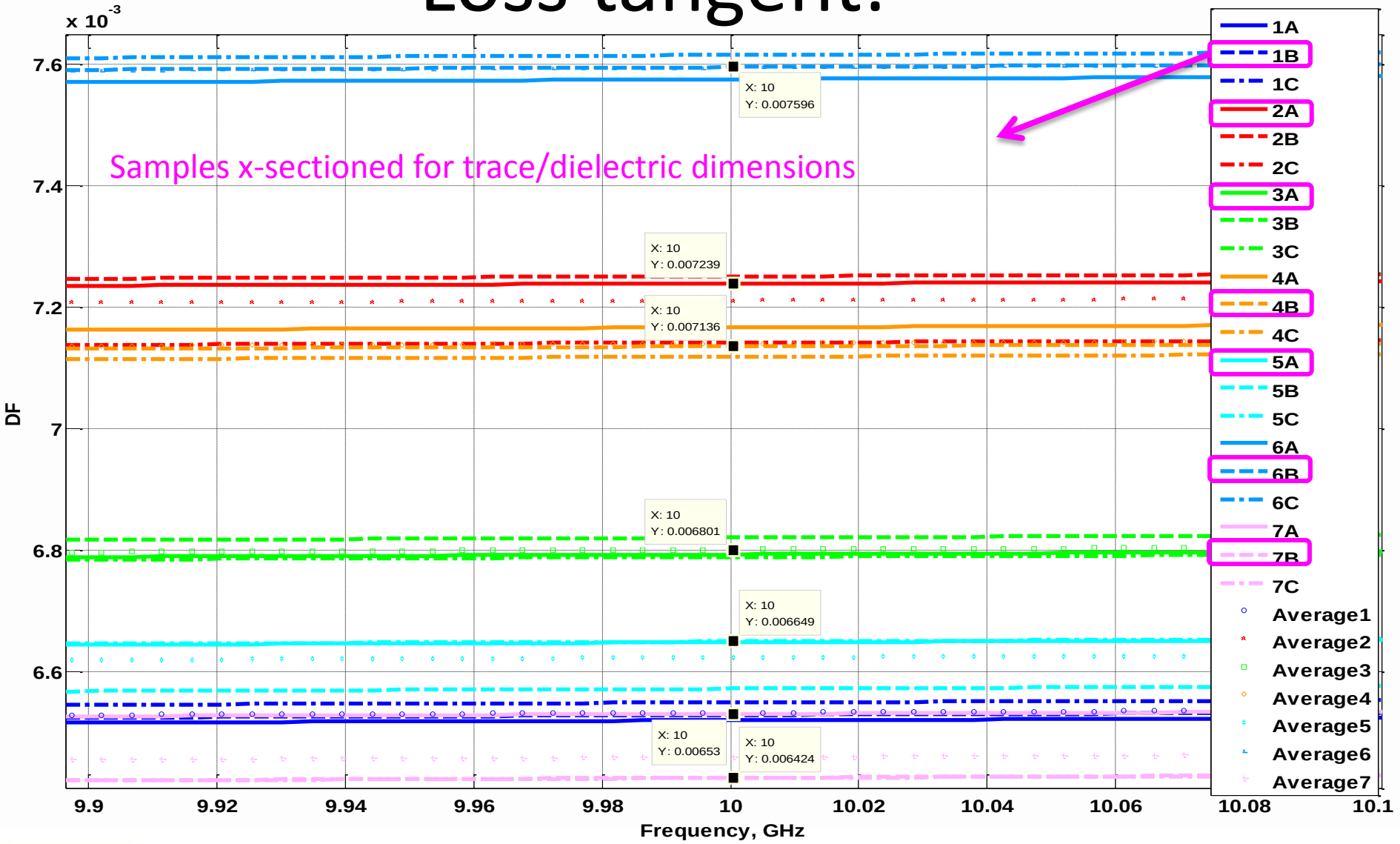
Dielectric Constant (Epsilon prime):



Loss tangent:



Loss tangent:



Summary Table of Results

No.	Identification	S21 (10 GHz)*	Df (10 GHz)
1	HFi / FB	-6.81	0.0063
2	HFi / CZ	-7.24	0.0072
3	HFi / BO-0.5	-7.01	0.0068
4	HFi / BO-1.5	-7.23	0.0071
5	HFi / RBO	-6.95	0.0065
6	HFz-B / FB	-7.41	0.0076
7	ANP-PA / FB	-6.96	0.0065

*Total Insertion Loss in dB, for 16" Test Line

Df values are **composite values** incorporating Conductor and Dielectric Loss. (Cisco S3 Test Method)

Note on Dk: Span of values across all samples was 3.70 – 3.74, (within margin of measurement error).

Conclusions

With I/L treatment held constant (runs 1, 6, 7), the largest differential is seen between BF-HFi (ultra-smooth foil) and HFz-B (RTF foil), amounting to a 19% delta in loss tangent.

With foil held constant (runs 1 through 5), the largest differential is seen between CZ-8100 and FlatBond, amounting to a 11% delta in loss tangent.

While less critical than specification of the foil roughness, potential loss tangent impact due to the choice of oxide treatment at the board shop is still significant.

Especially with Low-loss and Ultra-low-loss materials, it may be wise to control the oxide treatment by fab print specification, or by specific process line approval at the PCB suppliers.