APEX EXPO IPC
NEW IDEAS ... FOR NEW HORIZONS
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LAS VEGAS, NEVADA

The Role and Future of 2.5D IC Integration

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OBJECTIVE

The role and future of passive interposers (2.5D IC integration) for semiconductor IC packaging will be investigated.

Emphasis is placed on:

1. **The real applications of interposers**
2. **The recent advances of the build-up package substrates**
3. **Is interposer necessary for wide I/O 2 and HBM**
4. **Is interposer necessary for smartphones and tablets**
5. **Some recommendations**

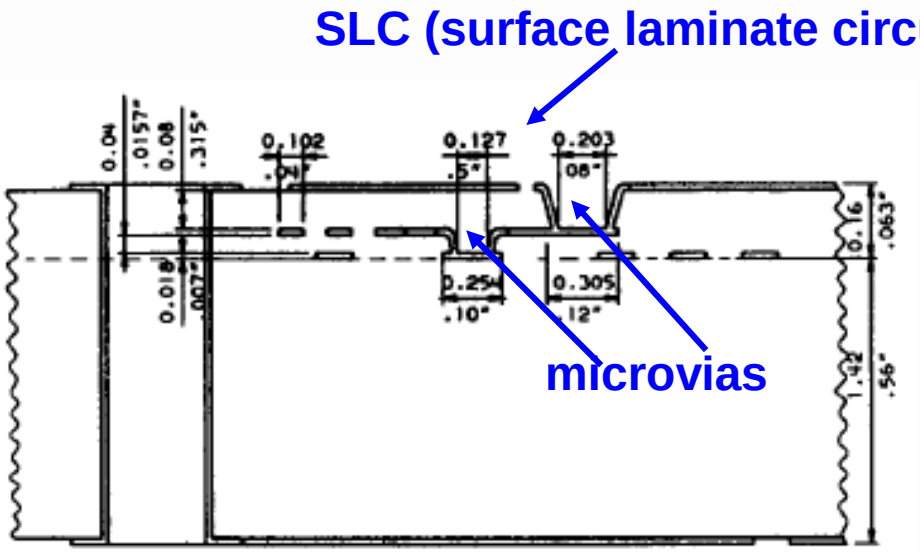
CONTENTS

Package Substrate with Build-Up Layers for Flip Chip Applications

Build-up Layer in Package Substrates

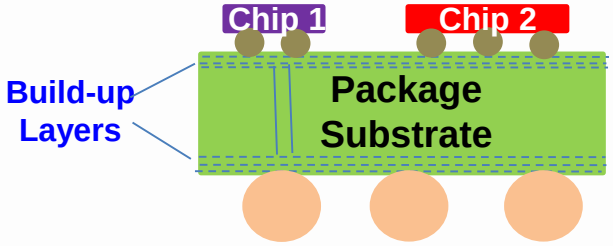
More than 20 years ago, Tsukada of IBM in Japan invented the SLC (surface laminate circuit) technology, which formed the basis of today's very popular low-cost organic package substrates with build-up layers vertically connected through microvias to support solder bumped flip chips.

1996 IBM Fellow

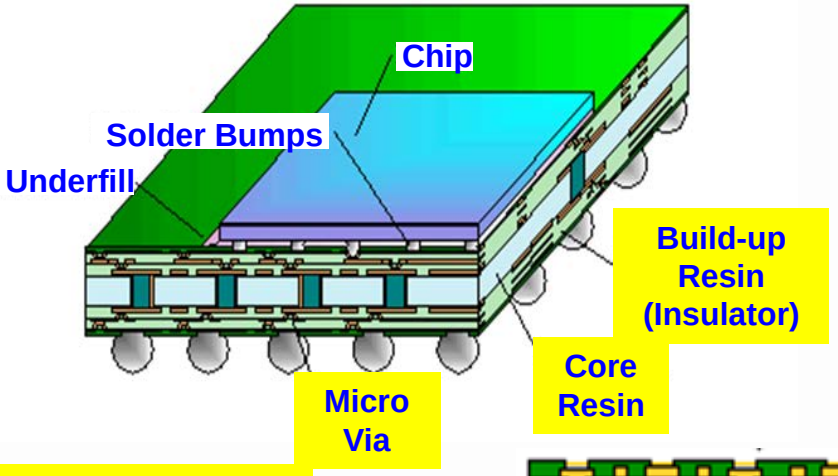


Tsukada, Y., S. Tsuchida, and Y. Mashimoto, "Surface Laminar Circuit Packaging", *Proceedings of IEEE/ECTC*, May 1992, pp. 22-27.

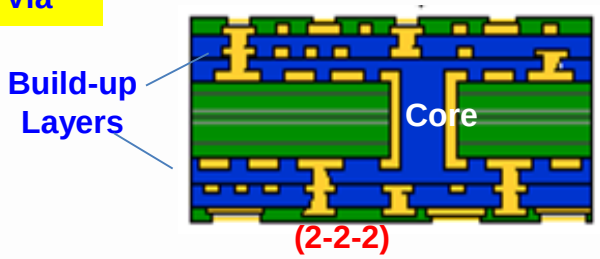
TODAY



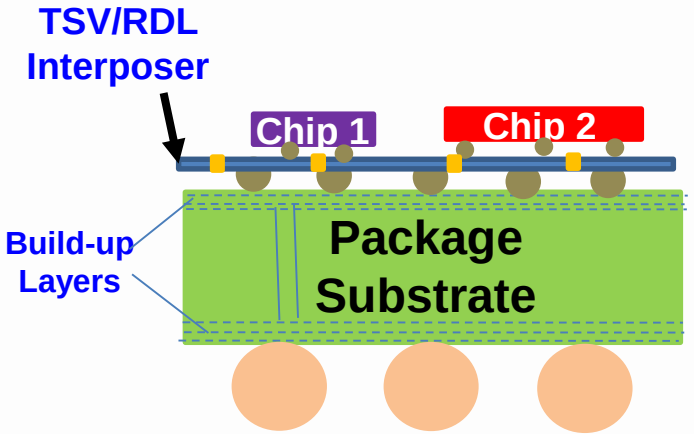
PBGA (Plastic Ball Grid Array)



8-build-up-layer (4-2-4) and 25μm line-width and spacing is more than adequate to support most of the chips!



TOMORROW

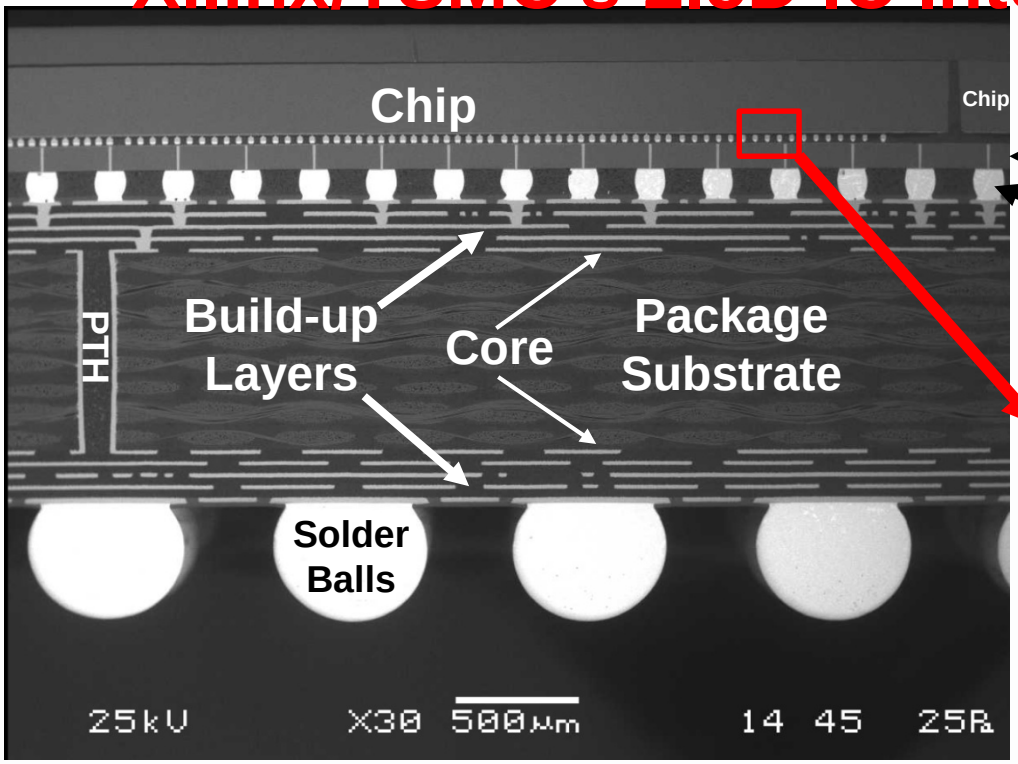


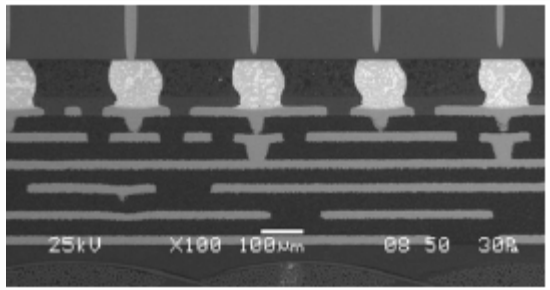
2.5D IC Integration (Interposer)

TSV/RDL Interposer is for:
- **Very High I/Os,**
- **Very High Performance,**
- **Very High Density,**
- **Very Fine Pitch, etc. applications.**

2.5D IC Integration (Interposer)

Xilinx/TSMC's 2.5D IC Integration with FPGA





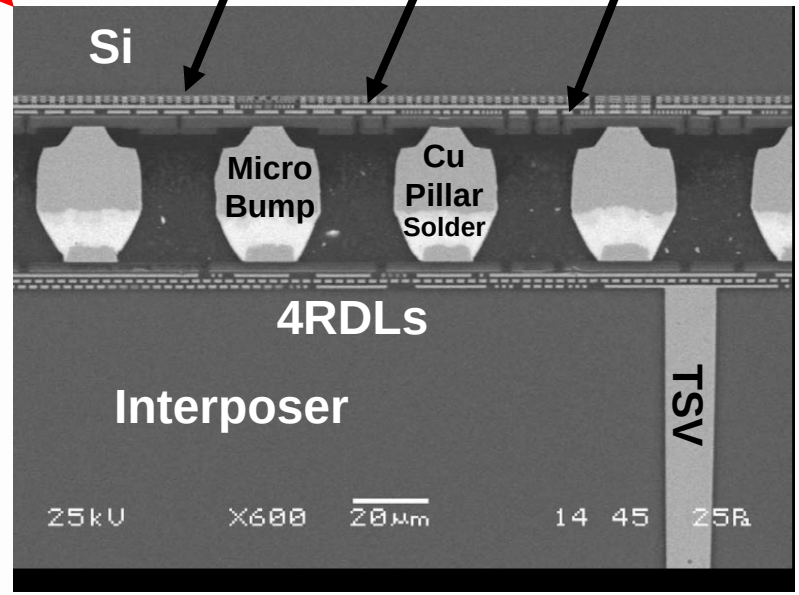
Interposer

C4 Bumps

Metal Layers

Metal Contacts

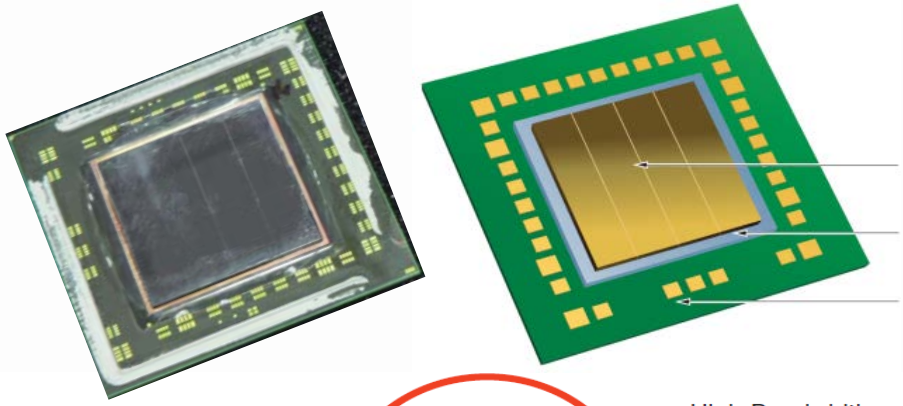
Devices (Cannot see)



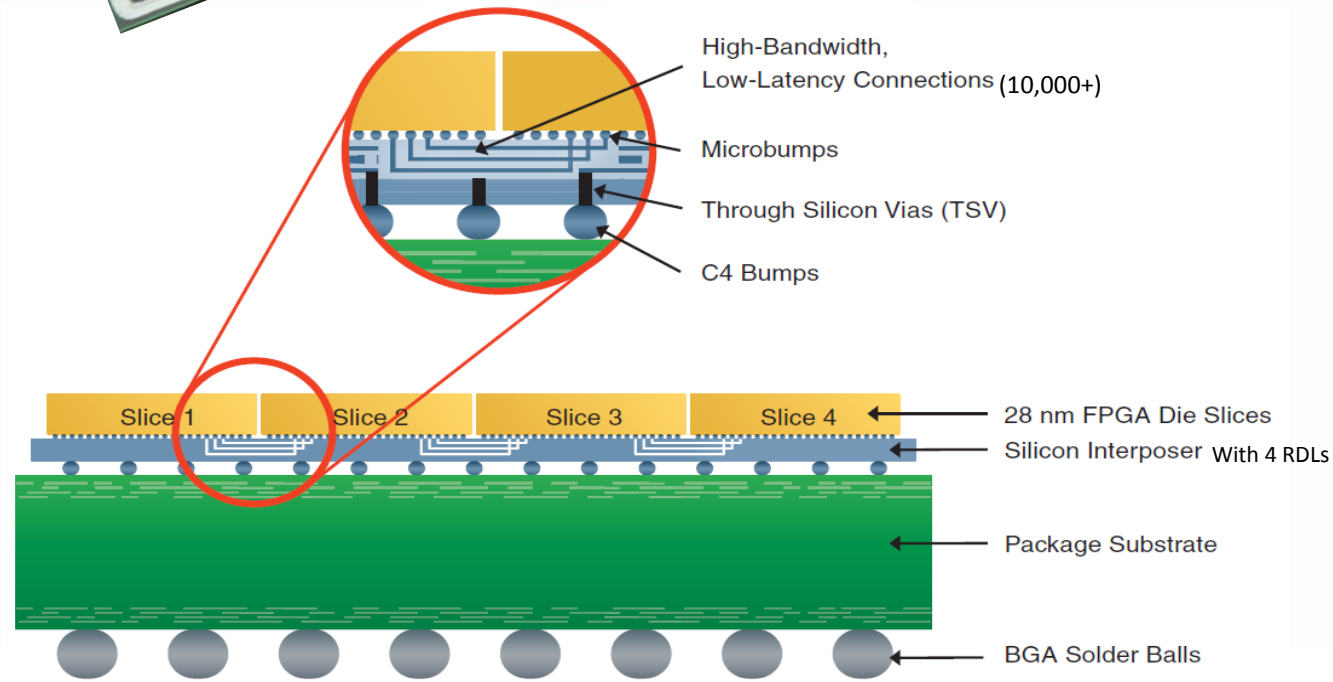
The package substrate is at least (5-2-5)

RDLs: 0.4µm-pitch line width and spacing
Each FPGA has >50,000 µbumps on 45µm pitch
Interposer is supporting >200,000 µbumps

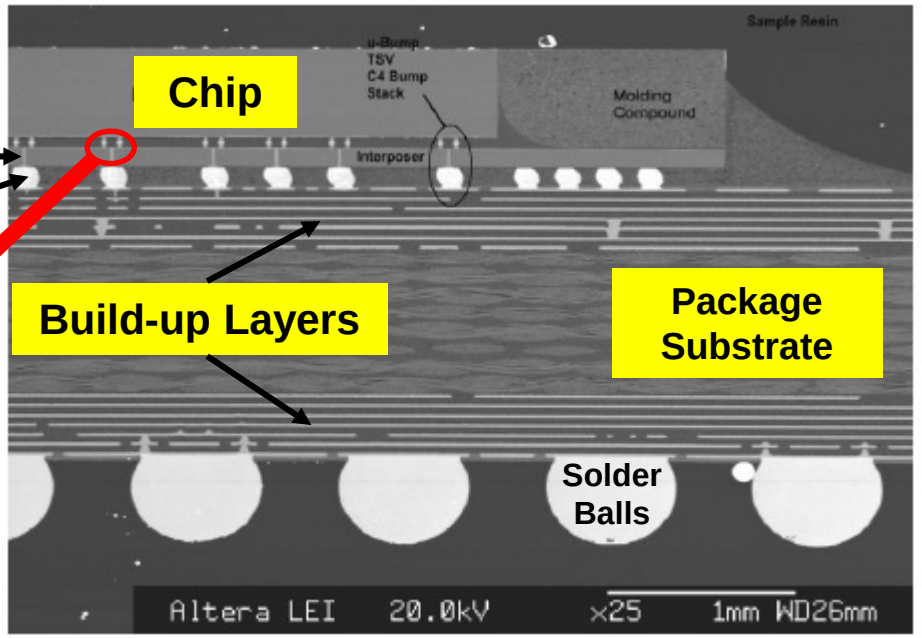
Xilinx's Passive Interposers with TSV and RDL for Wide I/O Interface in FPGA Products

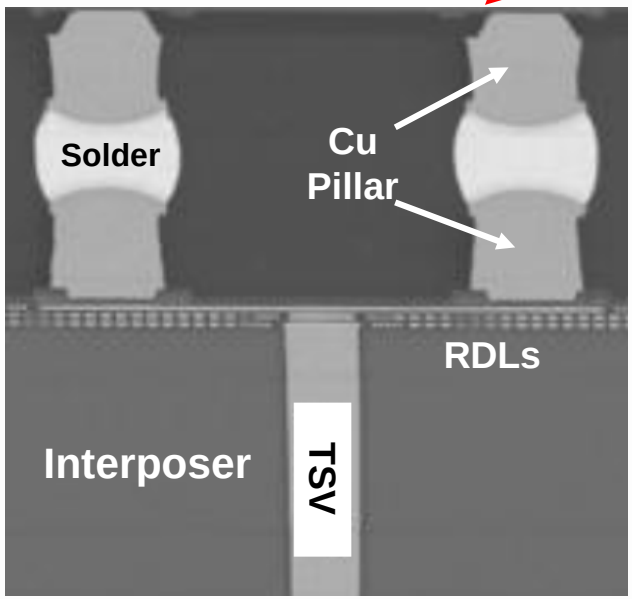


For better manufacturing yield (to save cost), a very large SoC has been sliced into 4 smaller chips (2011)

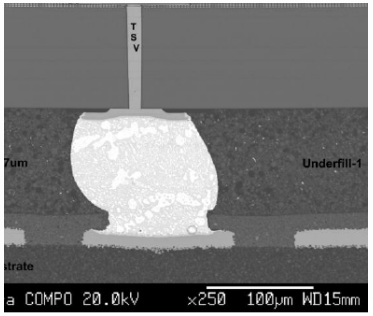


Altera/TSMC's 2.5D IC Integration with FPGA



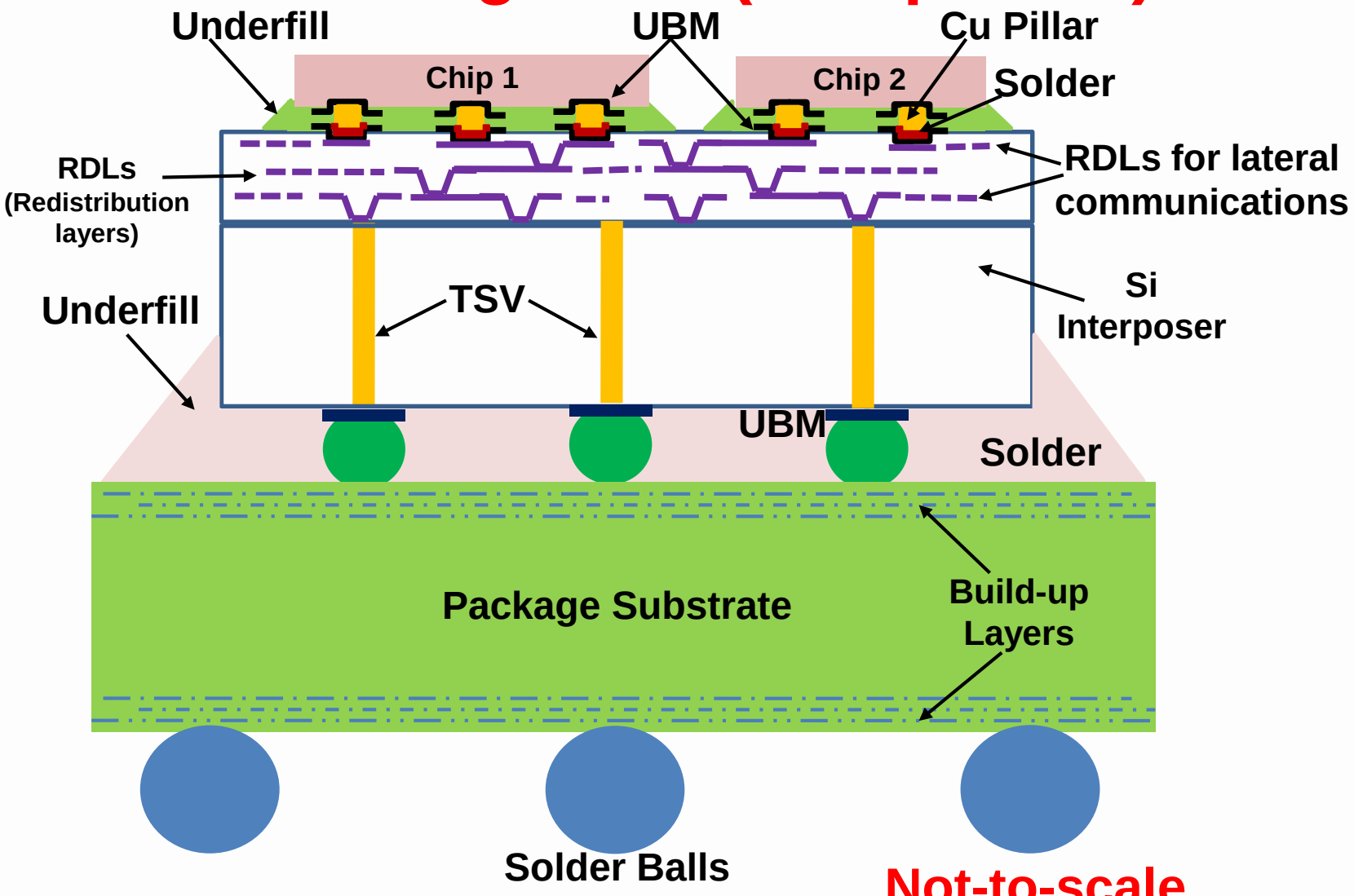


The package substrate is at least (6-2-6)

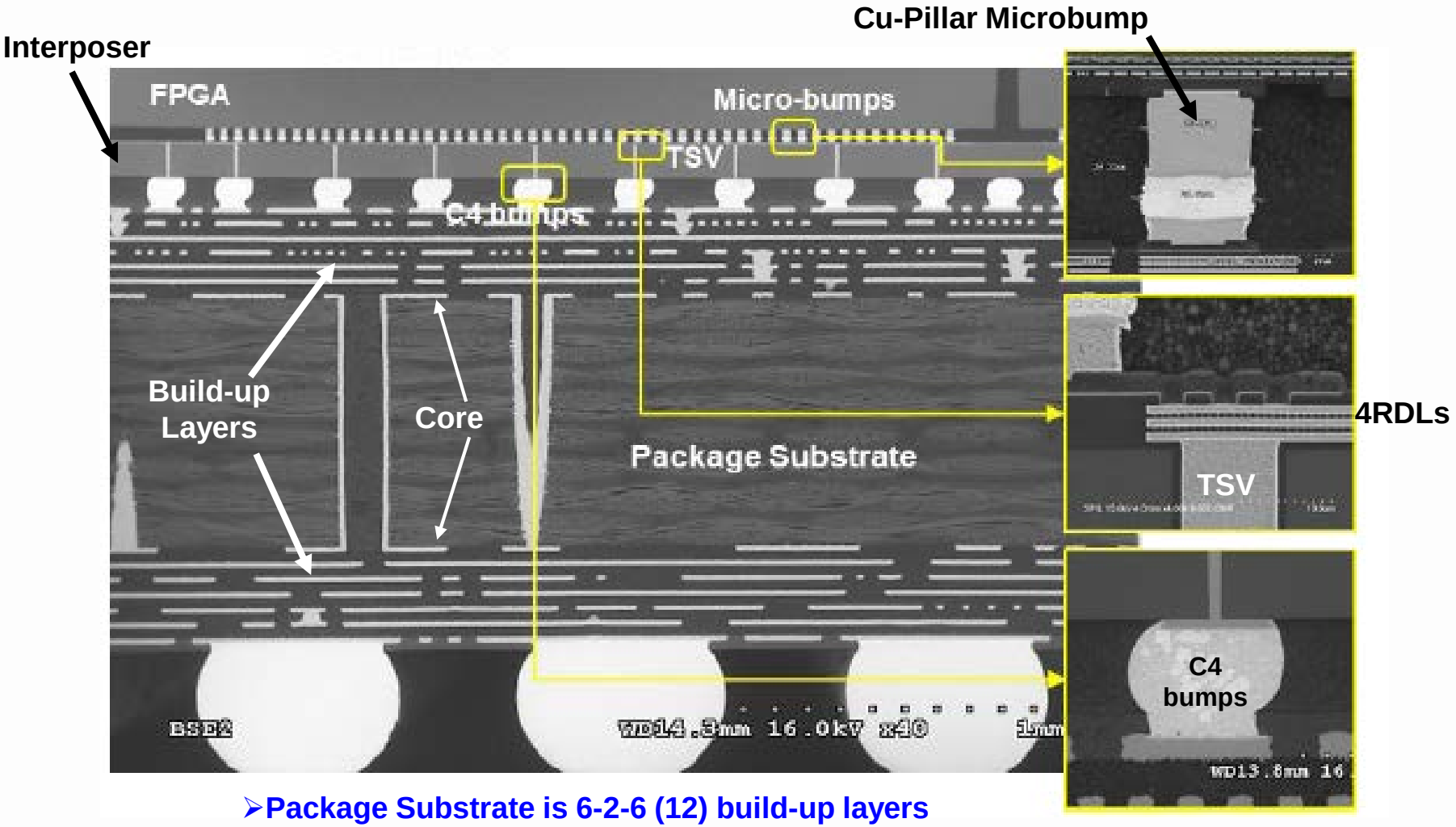


4RDLs on top of the interposer and there isn't any at the bottom

2.5D IC Integration (Interposers)



Xilinx/UMC/SPIL FPGA on Si Interposer on Package Substrate



- Package Substrate is 6-2-6 (12) build-up layers
- 200,000+ Cu-Pillar microbumps are at 45µm pitch
- 4RDLs are at (minimum) 0.4µm pitch

Thus, passive TSV/RDL interposers are for extremely fine-pitch, high-I/O, high-performance, and high-density semiconductor IC applications.

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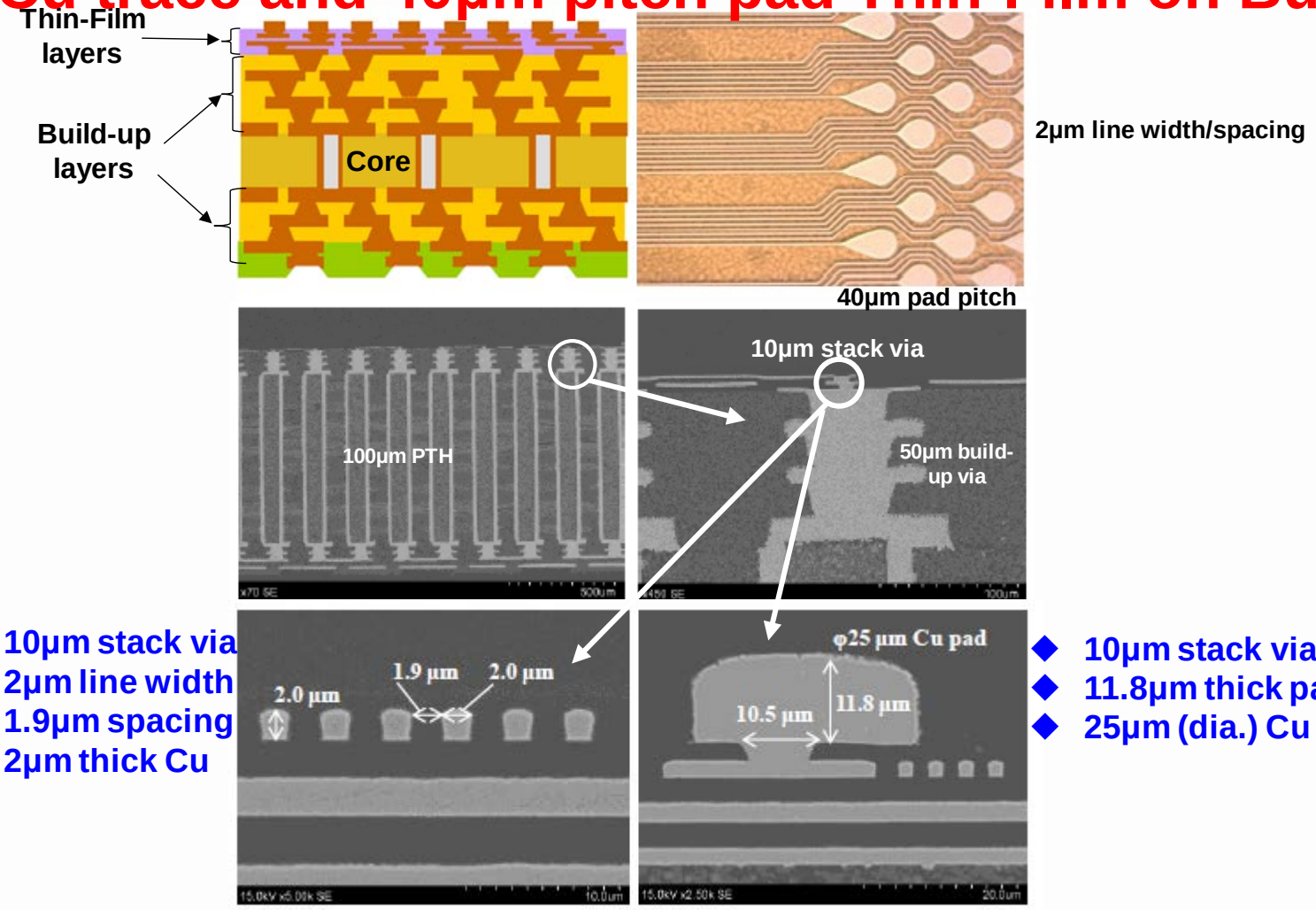
Recent Advances in Low-Cost Build-Up Package Substrates

Shinko's Test Vehicle 4+(2-2-3):
2µm Cu trace and 40µm pitch pad Thin-Film on Build-Up



- 10µm stack via
- 2µm line width
- 1.9µm spacing
- 2µm thick Cu

- 10µm stack via
- 11.8µm thick pad
- 25µm (dia.) Cu pad

Future Package Substrates

In general, a package substrate with 8-build-up-layer (4-2-4) and 25µm line-width and spacing is more than adequate to support most of the chips. Thus, interposers are not needed.

Also, in the past 3 years, Substrate Houses have been developing package substrates with high build-up layers (5-2-5) and fine (12-15µm) line-width and spacing.

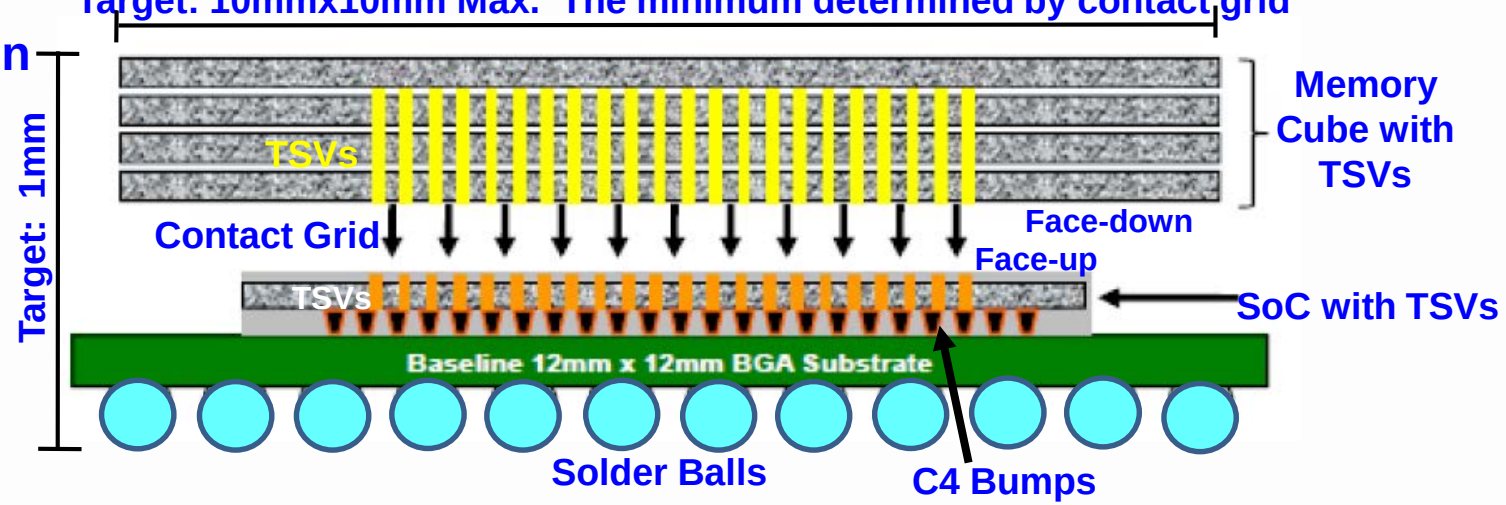
Recently, Shinko's thin-film layers on build-up layers can make 2µm line width and spacing and 40µm pad pitch.

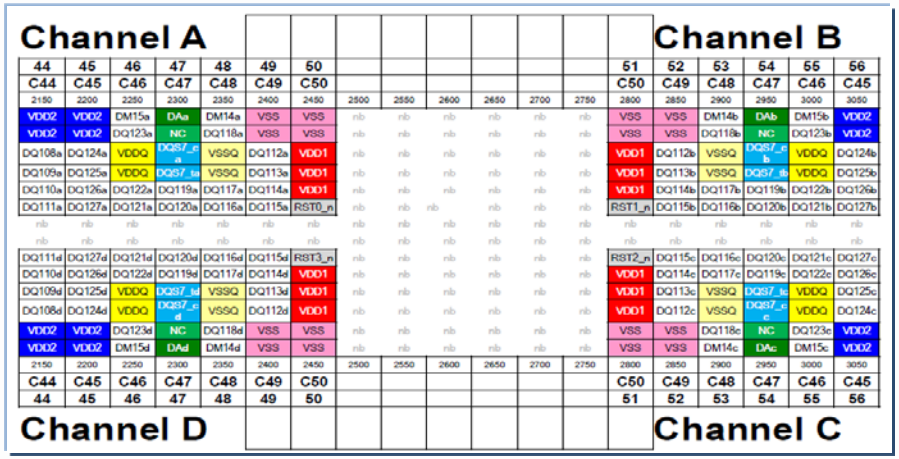
All these activities are keeping interposers away from volume production, except for very niche (such as extremely high-performance, high-density, and fine-pitch) applications.

3D IC Integration

Wide I/O Single Date Rate
JEDEC Standard (JESD229), December 2011

Micron's Suggestion

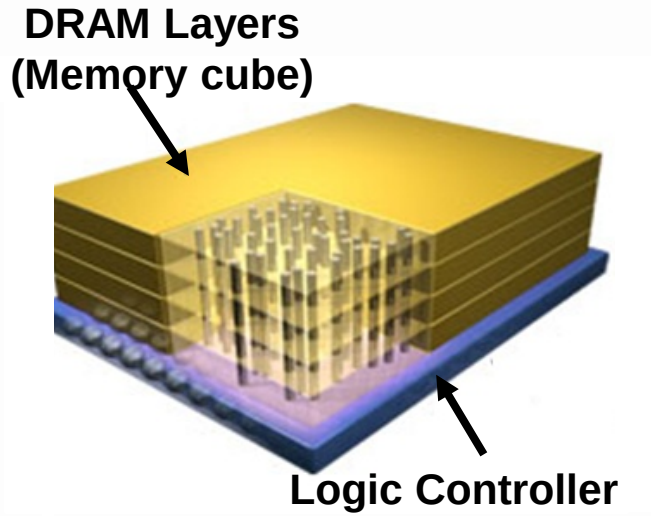




Hybrid Memory Cube (HMC)

The HMC consortium already has 8 members:

- Micron
- Samsung
- Altera
- ARM
- IBM
- Open-Silicon
- SK Hynix
- Xilinx

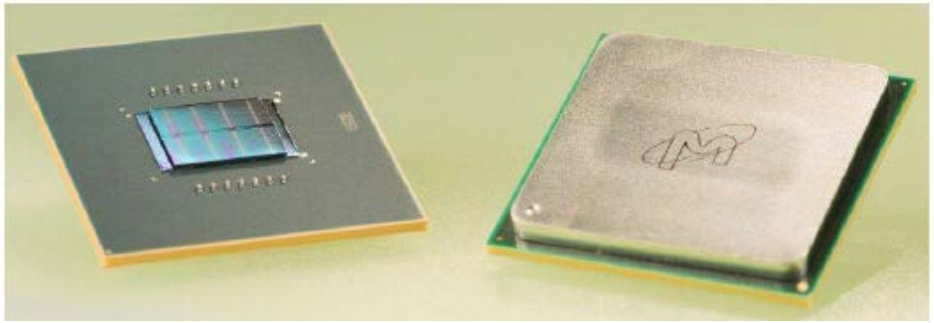


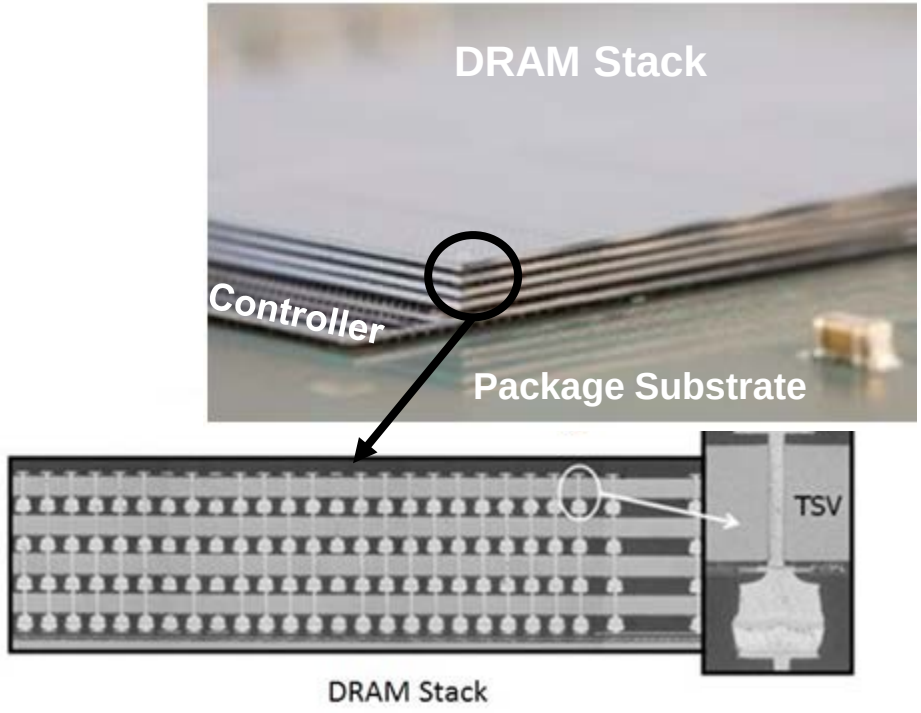
The SPEC was published on April 2, 2013 and is primarily targeted at:

More than 120 adopters!

- HPC (high performance computing)
- Networking
- Energy,
- Wireless communications
- Transportation
- Security
- High-end servers

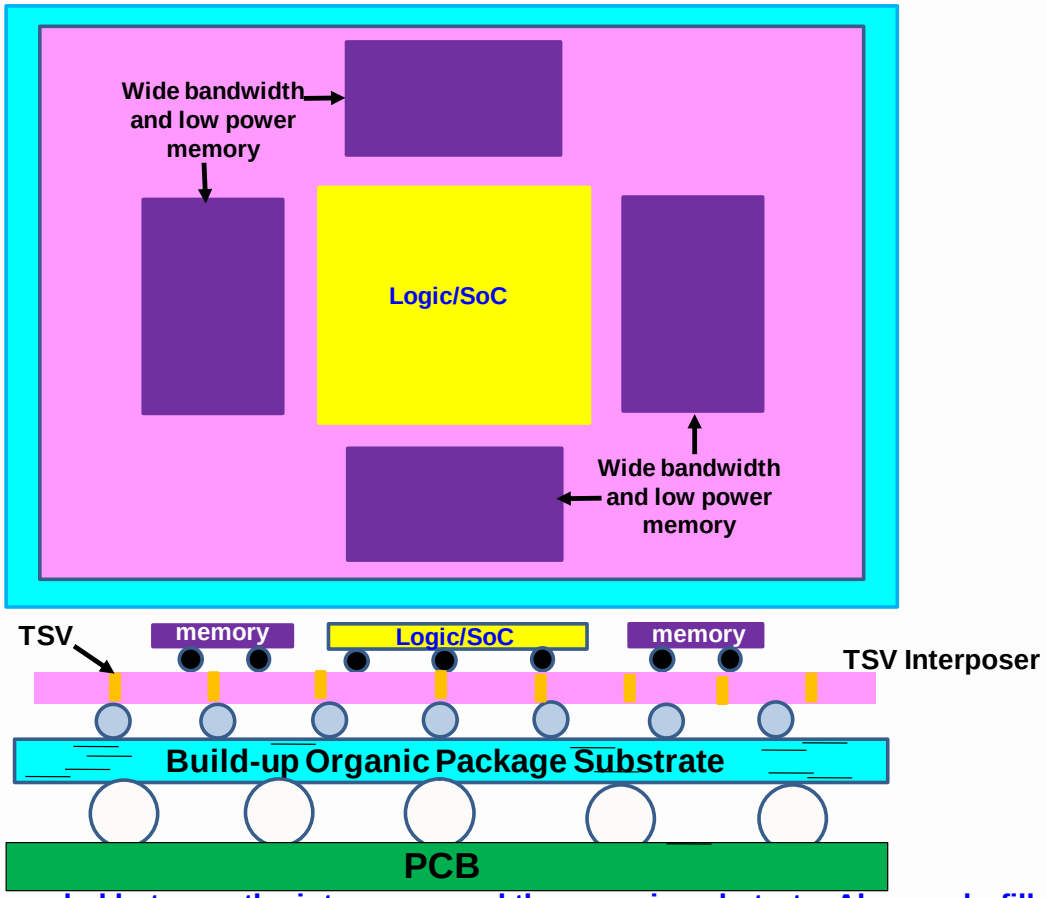
Micron's First HMC Sample Shipped in the Last Week of September 2013





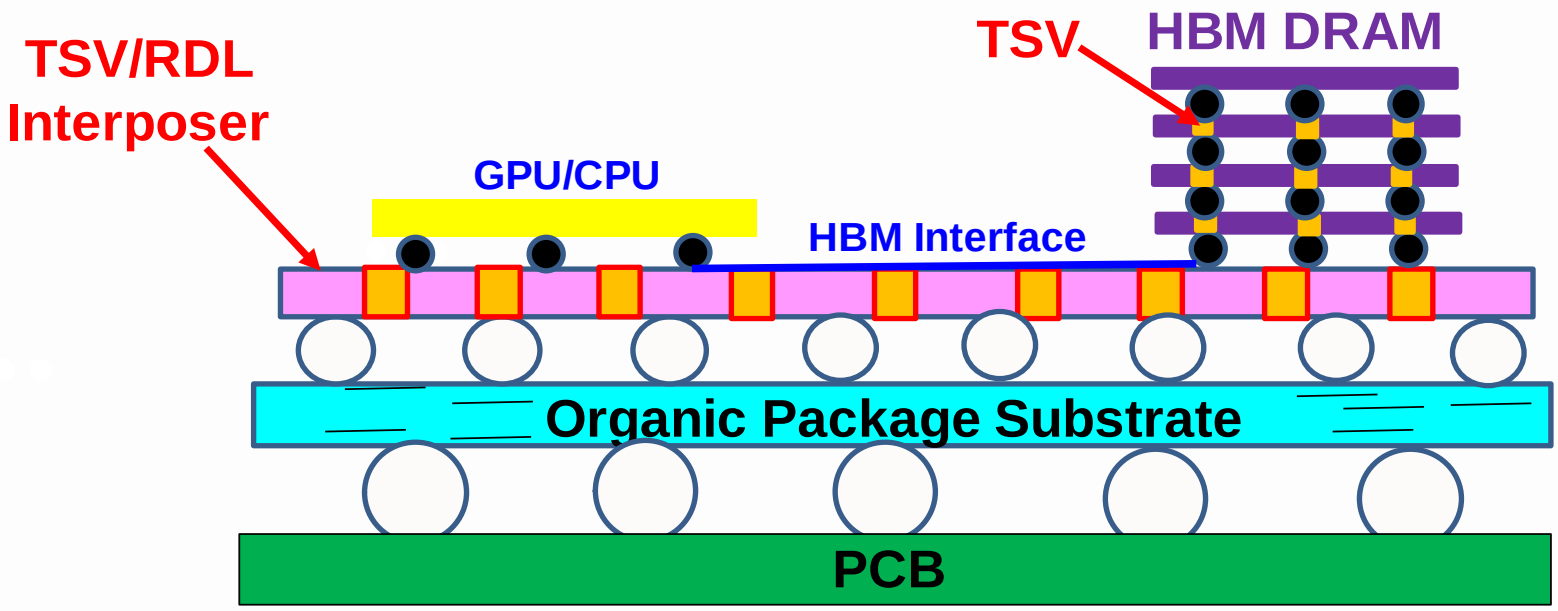
- The hybrid memory cube is a 4-DRAM (each one with 2000+ TSVs) on a logic controller (which size is slightly larger than the DRAMs) with TSVs
- The hybrid memory cube is on an organic package substrate.
- The TSV-DRAM is ~50-µm thick.
- The TSV-DRAM is with 20-µm (tall) Cu pillar + solder cap.
- The memory cube is assembled one DRAM at a time with thermal compression bonding.
- The heat dissipation is from 10W to 20W.
- TSV diameter ~ 5 to 6-µm.
- Volume production will be in next summer.

An interposer is supporting the Logic and memory chips side-by-side (Wide I/O 2)



Underfill is needed between the interposer and the organic substrate. Also, underfill is needed between the interposer and the Logic/SoC chip and the memory chips

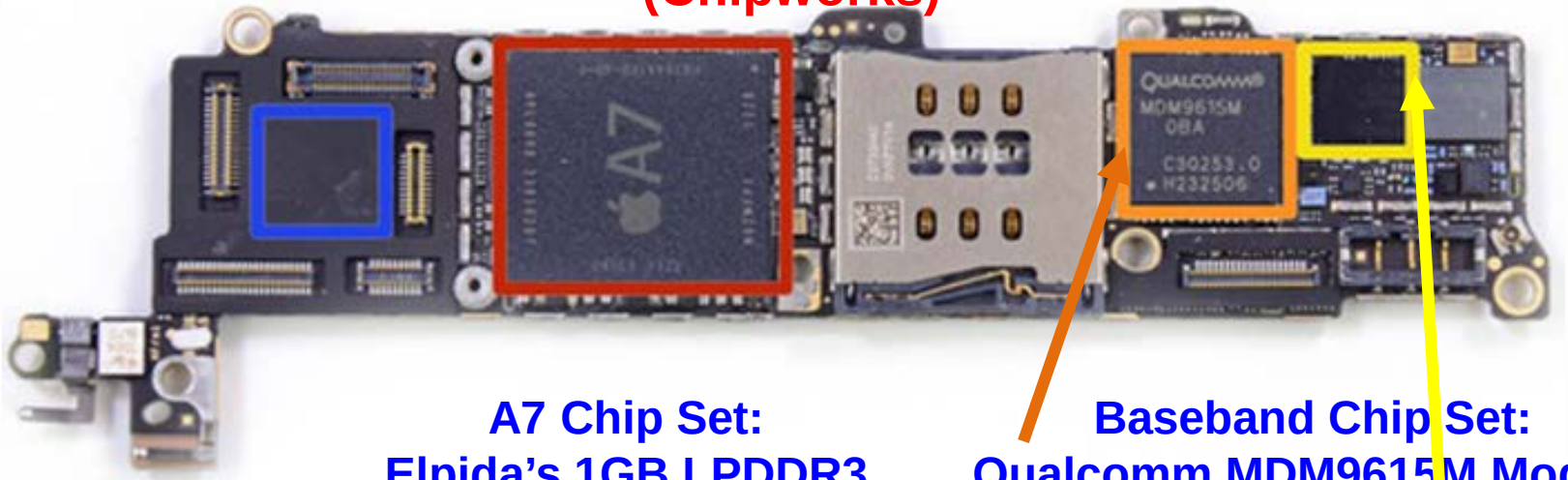
An interposer is supporting the HBM DRAM cube and the GPU/CPU side-by-side



Underfill is needed between the interposer and the organic substrate. Also, underfill is needed between the interposer and the GPU/CPU and the memory cube

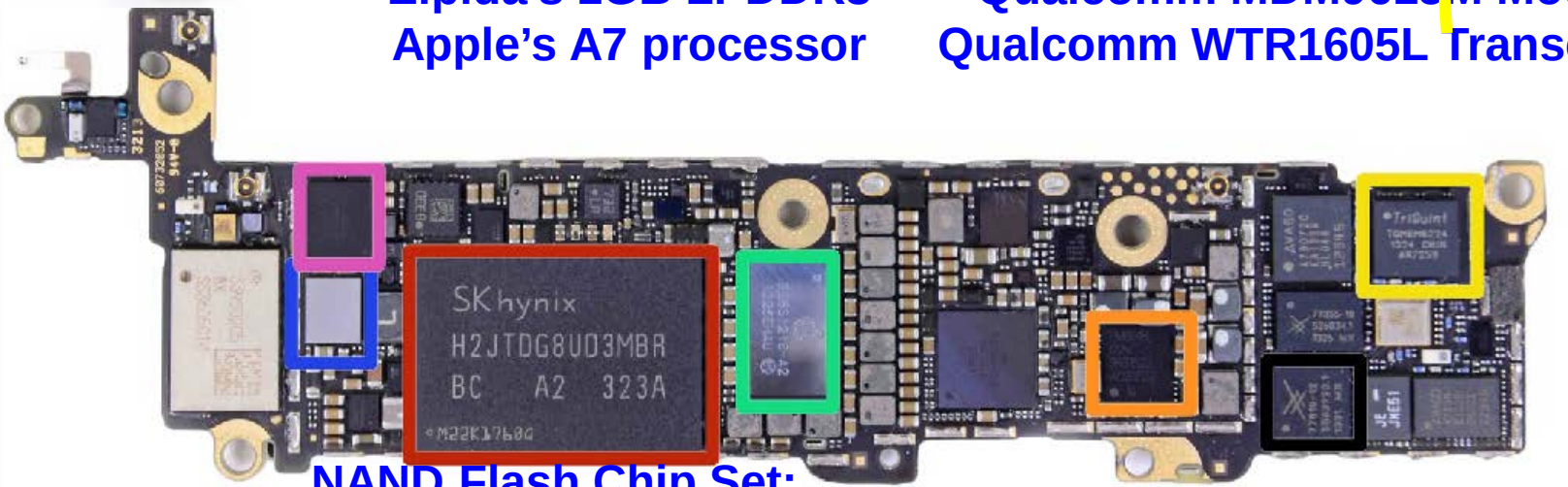
Will 2.5D/3D IC integration technologies be used in smartphones and tablets in the near future?

iPhone 5s: A7 Chip Set, Baseband Chip Set, and NAND Flash Chip Set (Chipworks)



A7 Chip Set:
Elpida's 1GB LPDDR3
Apple's A7 processor

Baseband Chip Set:
Qualcomm MDM9615M Modem
Qualcomm WTR1605L Transceiver

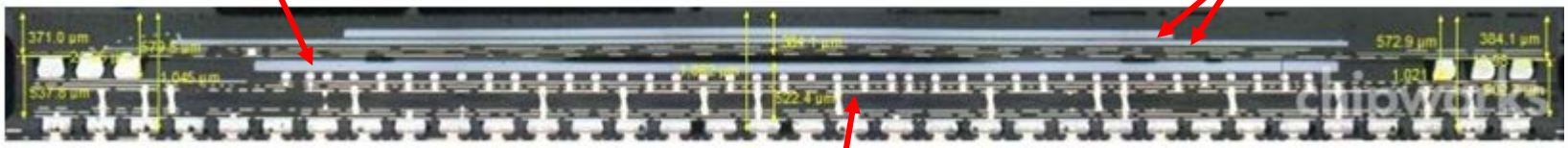


NAND Flash Chip Set:
SK Hynix's 16GB NAND Flash

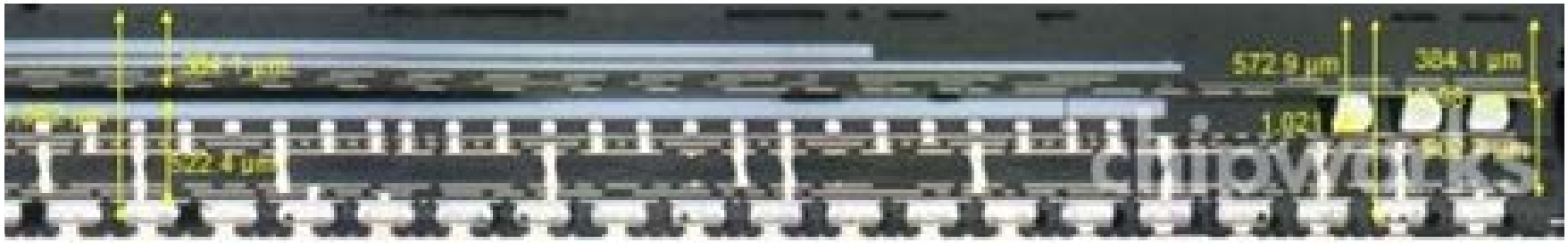
Cross Section of the PoP inside iPhone 5s (Chipworks)

Apple's A7 processor

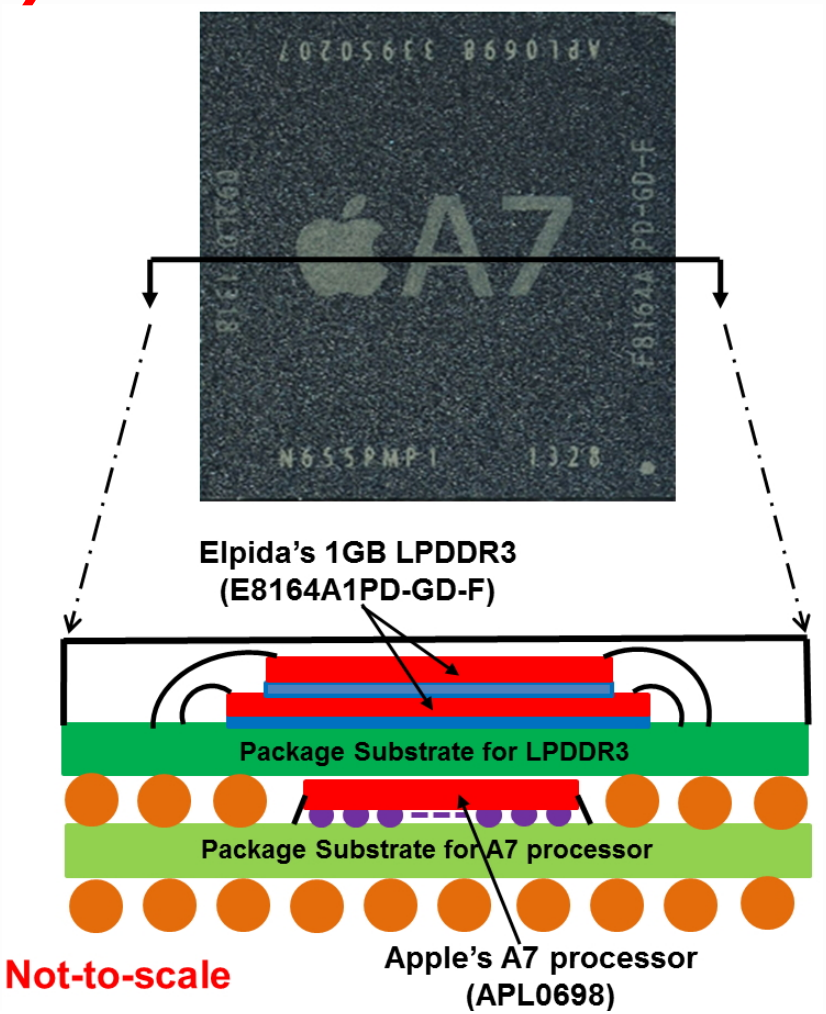
Elpida's 1GB LPDDR3



2-2-2 package substrate

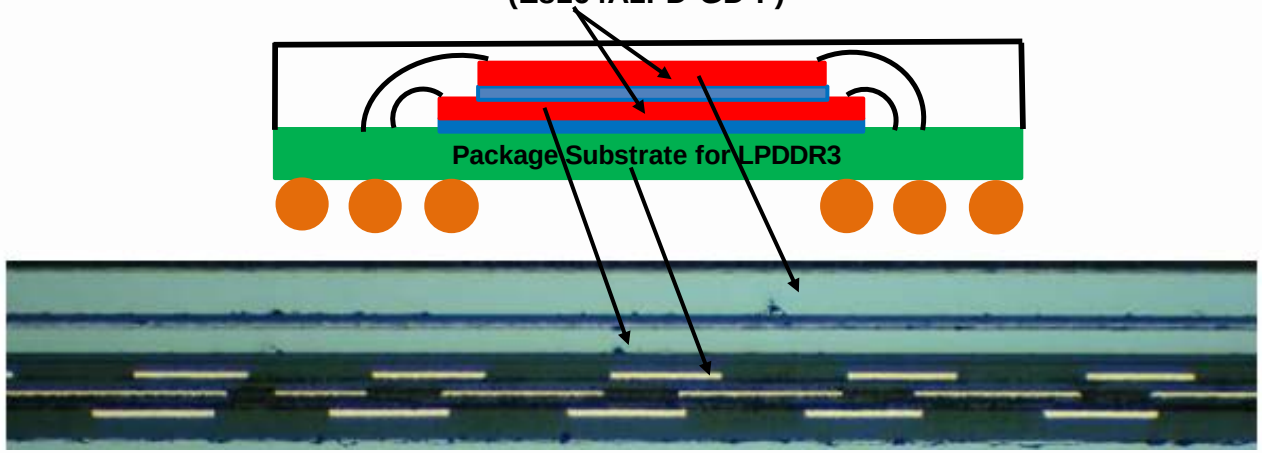


(Top) The top view of the A7 processor/memory PoP. (Bottom) Cross section view of the PoP

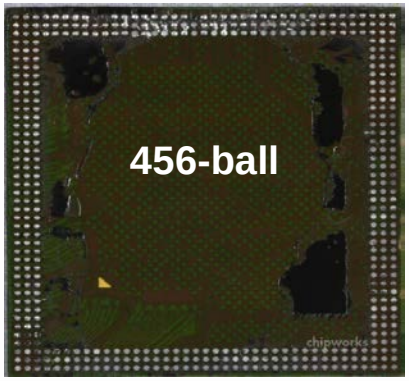


FBGA for the 1GB LPDDR3 mobile RAM chips (cross bonded with wires)

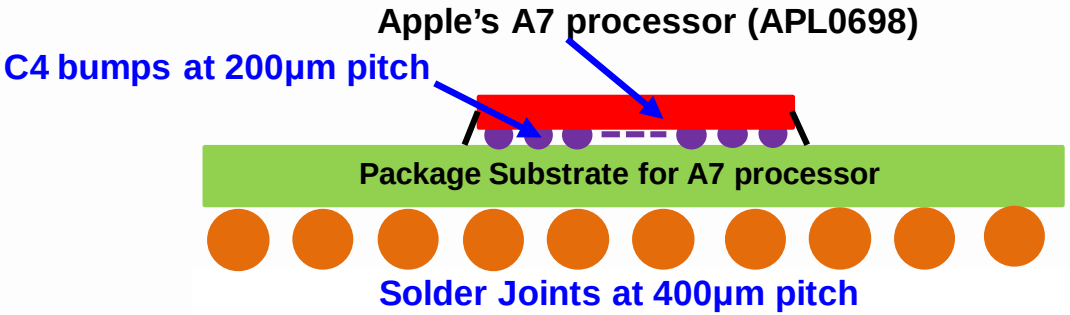
Elpida's 1GB LPDDR3 (Low-Power Double Date Rate – Type-3)
(E8164A1PD-GD-F)

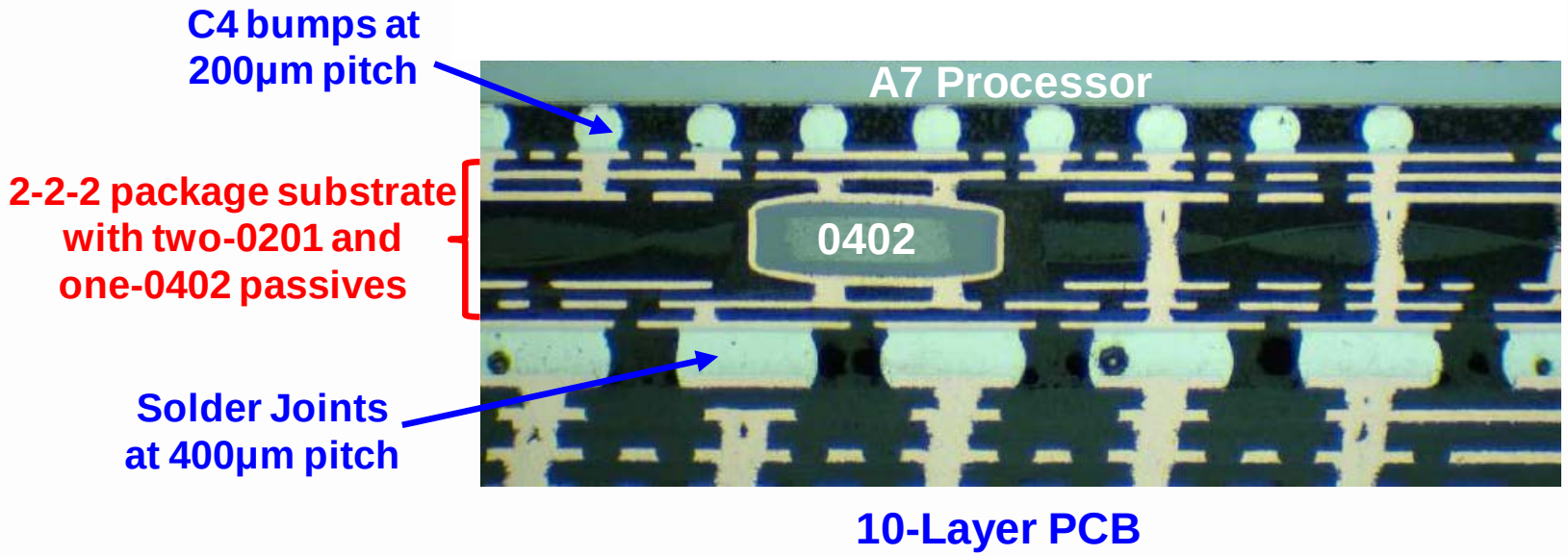


Core-less FBGA (Fine-Pitch Ball Grid Array)

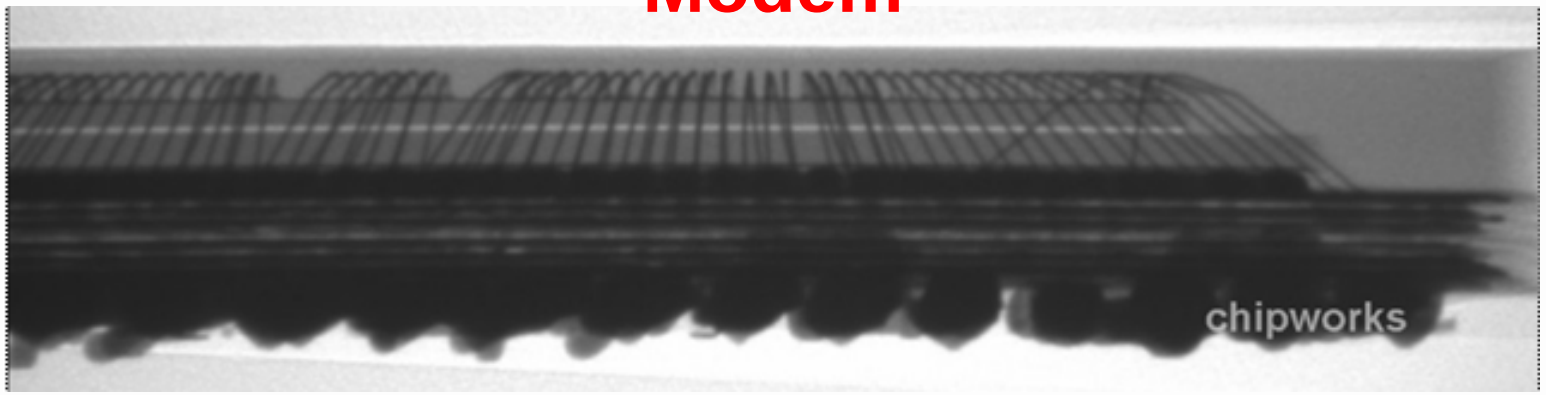


A typical cross section of the package substrate of the A7 processor



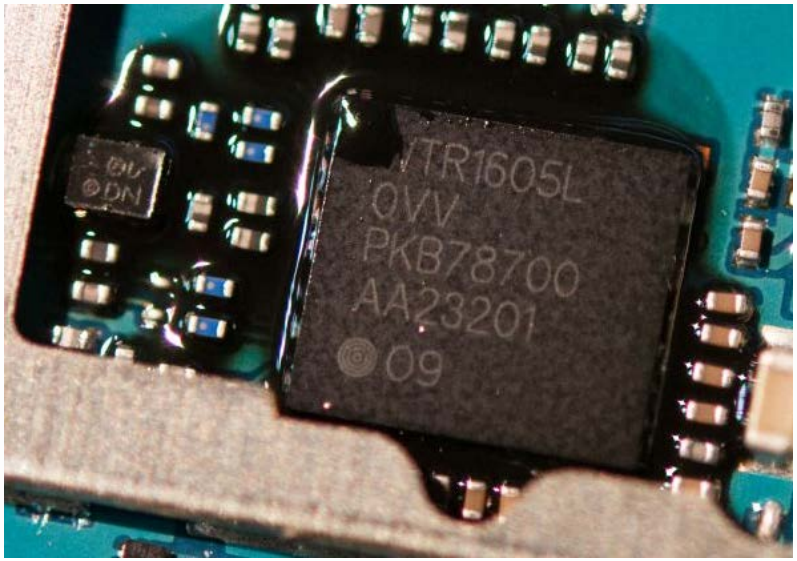


Qualcomm MDM9615 4G LTE (Long Term Evolution) Modem

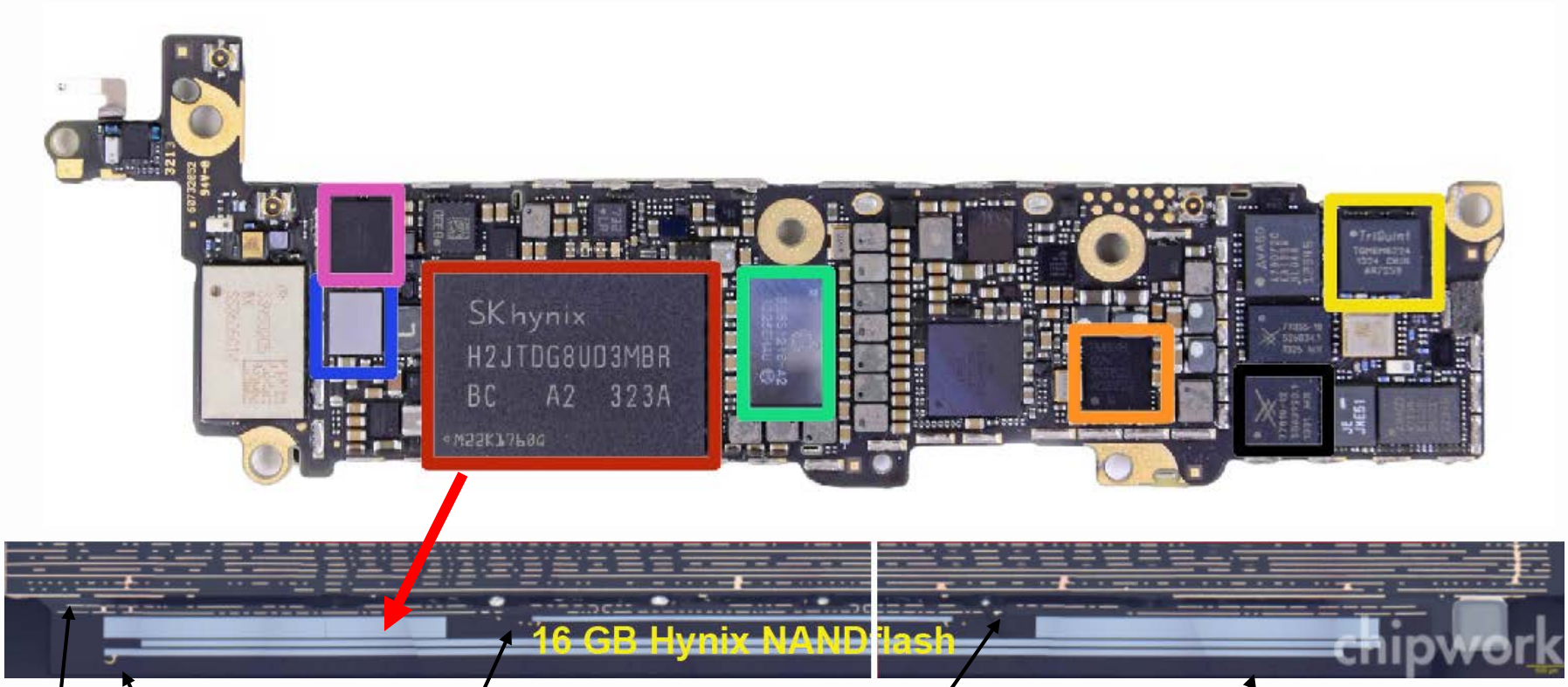


Qualcomm WTR1605L Transceiver

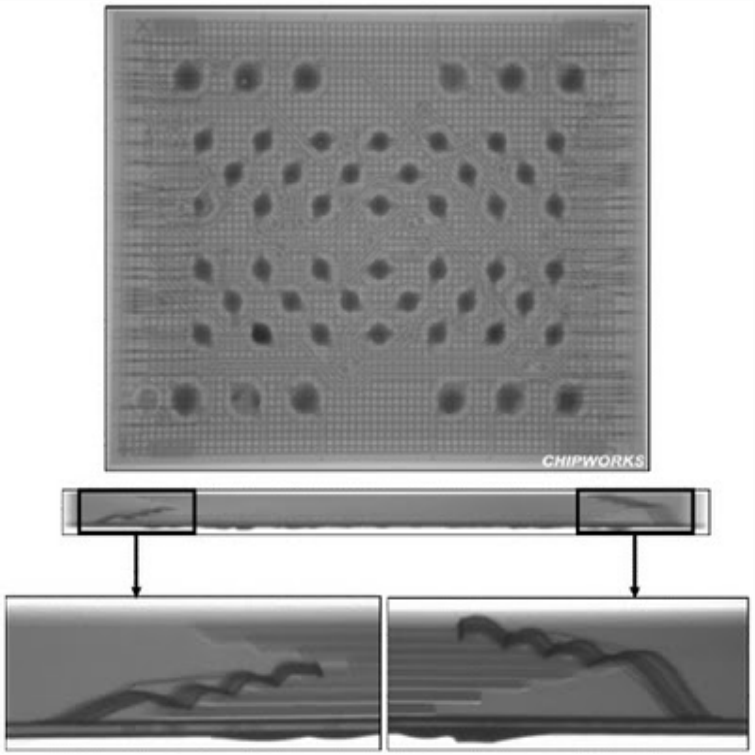
25mmx25mm
Wafer Level Package

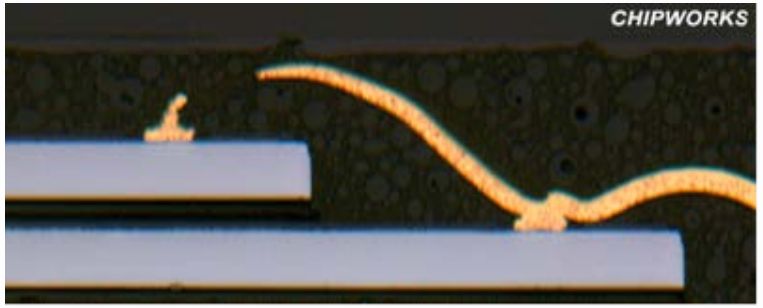


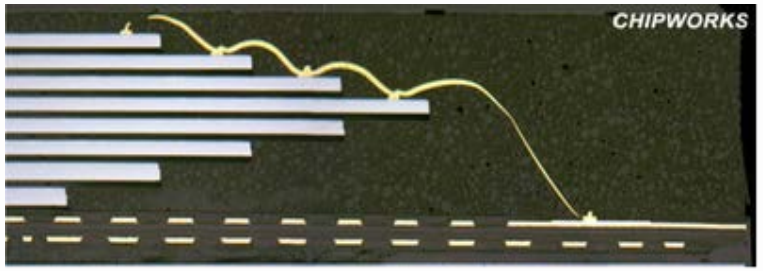
SK Hynix's MLC (Multi Level Cell) 128Gb (Gigabit) or 8GB (Gigabyte) NAND Flash in iPhone 5s



Samsung's Eight-Stack Flash Shows up in Apple's iPhone 4s



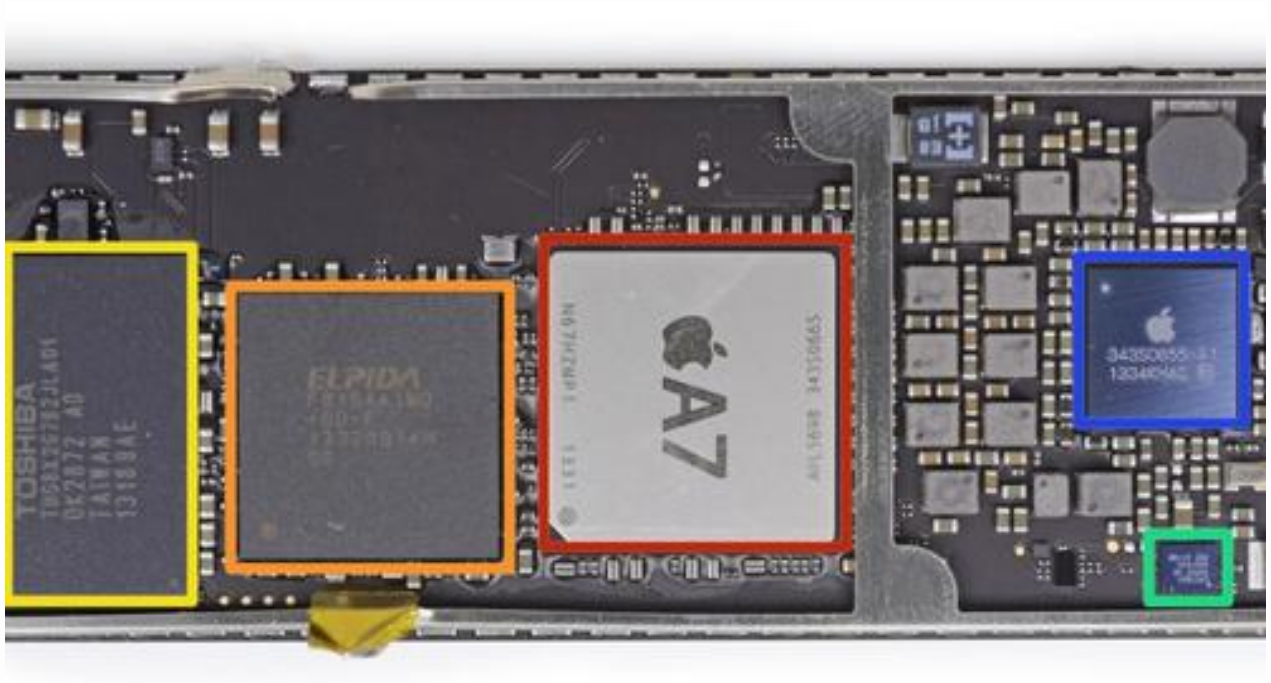




The package, including substrate, is ~0.93 mm thick, and the die stack is ~670 µm high. Die thicknesses vary from 55 – 70 µm, with the thickest die at the bottom.

Why iPad Air is the World's Thinnest Tablet?

(Apple dropped the PoP format and put the A7 processor package and the memory package side-by-side)



Summary and Recommendations

1.In general, interposers are for extremely high-I/O, high-performance, high-density, and fine-pitch semiconductor IC applications. Due to its wiring capabilities such as submicron metal line width and spacing, small via forming abilities such as 3μm or less via-diameter, and heavy/frequent/consistent use in the semiconductor IC industry such as infrastructure, a Si interposer is the choice!

2.Thin-film RDLs on top of the build-up package substrate with CMP (to perform the planarization) and stepper (to form the RDL pattern) technology invented by Shinko is the right way to go. The industry should strive to commercialize it.

3.Interposers for wide I/O 2 and HBM are not necessary. Build-up package substrates are adequate to support the side-by-side logic and memory chips without TSVs for wide I/O 2 and the DRAM memory cube with TSVs and GPU/CPU without TSVs for HBM. If not, then the thin-film layer on top of the build-up package substrate must be more than adequate to support them.

4.It ought to know that package substrate is a must (except the fan-out embedded wafer-level package). However interposer is an addition (to increase cost) and slows down the electrical performance. Try not to use the interposer unless the build-up package substrates are not adequate to support the very high I/O, high-performance, high-density, and fine-pitch chips. Now, with the thin-film RDLs on top of the build-up package substrate, the high-volume production of interposer will be pushed out even further.

5.The conventional packaging techniques such as the wire bonding, flip chip, build-up substrate, thin-film layer on build-up substrate, coreless substrate, wafer-level packaging, fan-out wafer-level packaging, 3D chip-stack by wire bonding, 3D PoP, etc. are more than adequate to support the semiconductor IC chips in high-end smartphone and tablet applications and TSV/RDL interposers are not necessary.

ACKNOWLEDGEMENTS

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