PCB Design and Assembly Process Development of 01005 Components with Lead Free Solder

Yueli Liu, Shaunte Rodgers, R. Wayne Johnson
Laboratory for Electronics Assembly & Packaging, Auburn University
162 Broun Hall/ECE Dept. Auburn, AL 36849

Abstract
The continuing demand for smaller, lighter multifunctional portable electronic products has driven the use of miniature components. To satisfy this demand, 01005 chip components are now commercially available. However the implementation for such tiny components into new products presents some design and assembly process challenges. In this study, a test vehicle was designed to investigate the effect of PCB pad design on assembly yield. Process capability of the 01005 test board manufacturing was evaluated. A Design of Experiments (DOE) was used to optimize the solder paste printing based on 3D solder paste inspection. Lead free solder was used for all assembly trials. Several tests were performed to explore the influences of process parameters on placement accuracy and reflow defects. Through the analysis of experimental results and post-reflow inspection for assembly defects, recommendations for PCB design and assembly processes are made.

Introduction
Due to the desire to make electronic products smaller and lighter, miniaturization and reducing spacing between components is the general trend in the electronics industry, particularly for handheld electronic products such as camcorders, cameras, cell phones and laptops. In fact, another driving force for smaller components is the increasing complexity of features and functions. Passive components occupy significant area on the PCB, especially for analog and mix-signal applications that use a larger number of passives compared to a typical digital system [1]. Reducing the size of the passive components and the spacing between them would increase the packaging density, and is an efficient way to miniaturize many electronic products.

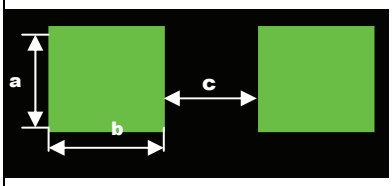
The second trend impacting the electronics industry is the switch to lead free solder in response to the RoHS and WEEE Directives in Europe, recycling laws in Japan and pending regulations in China and California. The wetting characteristics of lead free solders are different from eutectic Sn/Pb [2], and higher reflow temperatures are required.

Recently, 0201 components have been implemented in very high density applications such as mobile phones, blue tooth modules, and wireless LANs after extensive process optimization [3-10]. Resistors and capacitors are now being produced in the extremely miniaturized 01005 size (0.4mm x 0.2mm). However, the use of such a tiny component poses challenges for SMT assembly. The main factors affecting the 01005 assembly process can be divided into the following categories: PCB design, components, stencil, solder paste, PCB handling, printing, pick and placement, reflow and inspection [11, 12]. In order to investigate the effect of PCB design on assembly yield, a 01005 test vehicle was designed with different pad sizes, resistor-to-resistor spacing, shapes and orientations. Experiments were performed to optimize and characterize the solder paste printing, component placement and reflow processes.

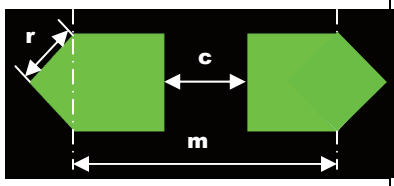
Test Vehicle Design
In order to optimize pad designs and evaluate assembly processes for 01005 components, a test vehicle was designed. The pad dimensions are shown in Table 1. Pad Size Type 1 is considered ‘nominal’. The pads were non-solder mask defined (NSMD). The other variables in the PCB design included: one laser drilled via in one of the two pads; a laser drilled via in both of the pads; no via in either pad; different resistor orientations (0^o, 45^o and 90^o); resistor-to-resistor spacing; and intentional solder mask misalignment.

Table 1. - Pad Dimensions (unit: mils).

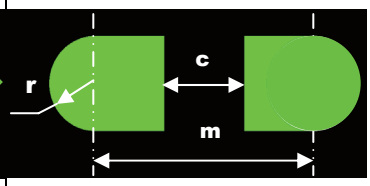
Pad Size Type	Pad Type	a	b	c	r	m	Stencil Area Ratio	
							3mil stencil	4mil stencil
Pad size 1, 100%	Rectangular	8.0	8.7	7.0			0.695	0.521
Pad size 2, 90%	Rectangular	7.2	7.8	7.0			0.624	0.468
Pad size 3, 110%	Rectangular	8.8	9.5	7.0			0.761	0.571
Pad size 4, 120%	Rectangular	9.6	10.4	7.0			0.832	0.624
Pad size 5, 130%	Rectangular	10.4	11.3	7.0			0.903	0.677
Pad size 6,	Home base 1			7.0	5.6	23.0	0.755	0.566
Pad size 7,	Home base 2			7.0	4.0	19.0	0.748	0.561



Rectangular



Home base 1



Home base 2

The test vehicle, shown in Figure 1, was a double sided, high T_g (T_g>170°C) FR-4 board with 9600 resistors sites, 8 CSP sites and 1 BGA site on one side. The pads had an immersion silver finish and were all non-solder mask defined (NSMD). The test board was 8.0" by 6.0" by 0.042" thick and replicated the basic test pattern in a 2 x 2 array. There are a total of 20 design groups located in each quadrant of the board: Seven groups (Pad Size Types 1-7, 5 pad spacings for each) with 90° orientation; Seven groups (Pad Size Types 1-7, 5 pad spacings for each) with 0° orientation; One group (Pad Size Type 1, 5 pad spacings) with 45° orientation; One Group (Pad Size Type 1, 5 pad spacings) with 0° and 90° orientation and a via in one pad; One Group (Pad Size Type 1, 5 pad spacings) with 0° and 90° orientation and vias in both pads; and One group (Pad Size Type 1) with 0° and 90° orientation,, solder mask intentionally shifted 2 mils along the length of resistor. Round global and local (a set for each quadrant) fiducials were also included in the design.

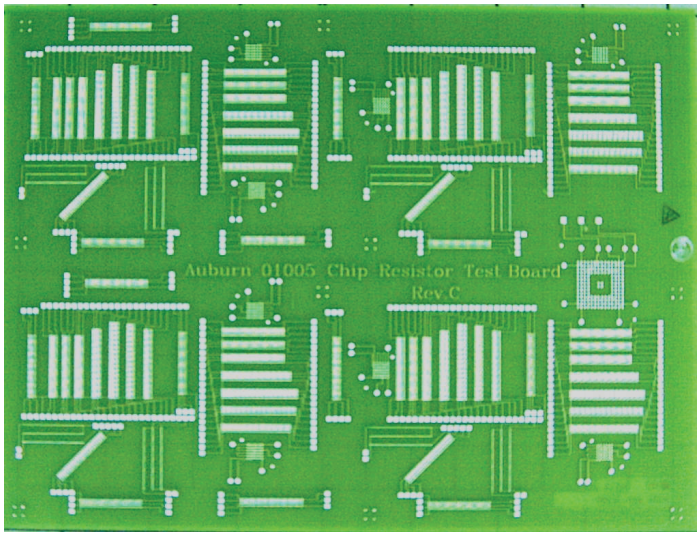


Figure 1 - 01005 Test Vehicle.

Process Capability Evaluation of Board Manufacturing

The board quality is important for reliable and consistent SMT assembly. To determine if the board manufacturing was capable, and if the boards met the specification limits, capability analysis was performed on the incoming boards. Five rectangular pad size designs and five different spacing designs were chosen for measurement. Fifty samples per board were measured for two boards. Based on the design specifications, the pad width and spacing tolerance was ±0.5mils. Process

capability analysis for normal distribution samples was conducted using Minitab 13.0. In this analysis, the process variation was measured by 6 standard deviations (+/-3□ on each side of the mean). For the pad dimension, the process capability statistics are summarized in Table 2, and one of corresponding capability histograms of the individual measurements overlaid with a normal curve based on the process mean and standard deviation is shown in Figure 2. Similarly, for the pad spacing, the process capability statistics are summarized in Table 3, and a corresponding capability histogram of the individual measurements is shown in Figure 3.

Table 2 - Process Capability Statistics of Pad Dimension (unit: mils).

	X1	Y1	X2	Y2	X3	Y3	X4	Y4	X5	Y5
Ave.	7.48	8.25	6.70	7.39	8.29	9.09	8.97	9.97	9.95	10.73
Std. Dev.	0.19	0.19	0.20	0.17	0.20	0.15	0.13	0.14	0.27	0.24
Design Target	8.00	8.70	7.2	7.8	8.80	9.50	9.60	10.40	10.40	11.30
USL	8.50	9.20	7.70	8.30	9.30	10.00	10.10	10.90	10.90	11.80
LSL	7.50	8.20	6.70	7.30	8.30	9.00	9.10	9.90	9.90	10.80
C_p	0.89	0.89	0.85	0.99	0.85	1.12	1.27	1.21	0.63	0.69
C_{pU}	1.82	1.70	1.71	1.81	1.73	2.05	2.87	2.27	1.19	1.46
C_{pL}	-0.04	0.08	-0.01	0.18	-0.02	0.20	-0.33	0.16	0.07	-0.09
K	1.05	0.90	1.01	0.82	1.02	0.82	1.26	0.87	0.89	1.13
C_{pK}	-0.04	0.08	-0.01	0.18	-0.02	0.20	-0.33	0.16	0.07	-0.09

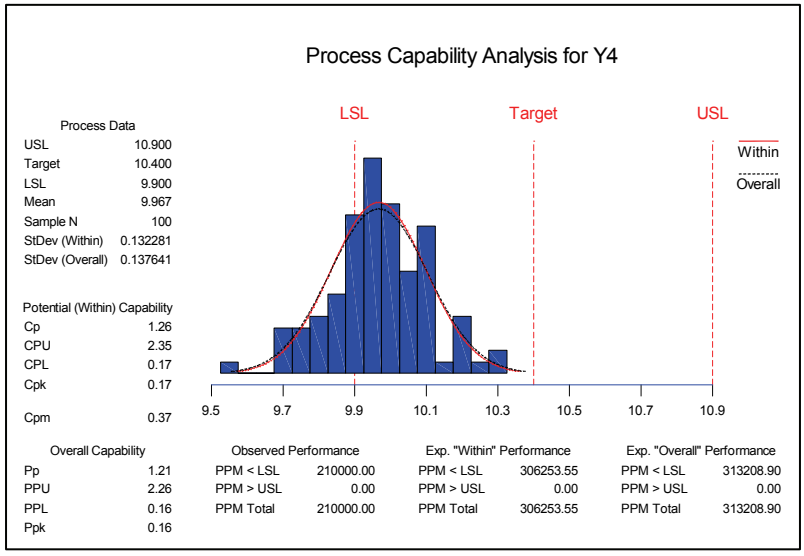


Figure 2 - Capability Histogram for Y4 (Pad Size 4).

From the statistical results in Table 2 and Figure 2, it is clear that the process for pad size is non-centered on the target, most of pads are smaller than target, and the whole normal distribution is shifted to the LSL (Lower Specification Limit). Nominally, the pads are ~0.5mils smaller than the design value. From the statistical results in Table 4 and Figure 3, it can be seen that the process for spacing is non-centered on the target. Most of the spacings are larger than target, and the whole normal distribution is shifted to the USL (Upper Specification Limit). For both pad size and spacing, the C_{pk}<<1, indicating the process capability did not meet the desired process specifications. A compensation factor was used in plotting the imaging artwork to address processing factors by the board manufacturer. However, due to the small spacing designed into the test vehicle, the amount of compensation that could be used was limited. In the subsequent discussions of assembly process optimization, the design values (not the actual value) of the pad and space will be used to describe the pads and spacings.

Table 3 - Process Capability Statistics of Pad Spacing (unit: mils).

	Spacing 1	Spacing 2	Spacing 3	Spacing 4	Spacing 5
Ave.	4.32	5.36	6.44	8.51	15.61
Std. Dev.	0.18	0.19	0.16	0.22	0.19
Design Target	4.00	5.00	6.00	8.00	15.00
USL	4.50	5.50	6.50	8.50	15.50
LSL	3.50	4.50	5.50	7.50	14.50
C_p	0.92	0.88	1.06	0.77	0.89
C_{pU}	0.33	0.24	0.13	-0.02	-0.19
C_{pL}	1.50	1.51	1.98	1.56	1.97
K	0.64	0.73	0.87	1.03	1.22
C_{pK}	0.33	0.24	0.13	-0.02	-0.19

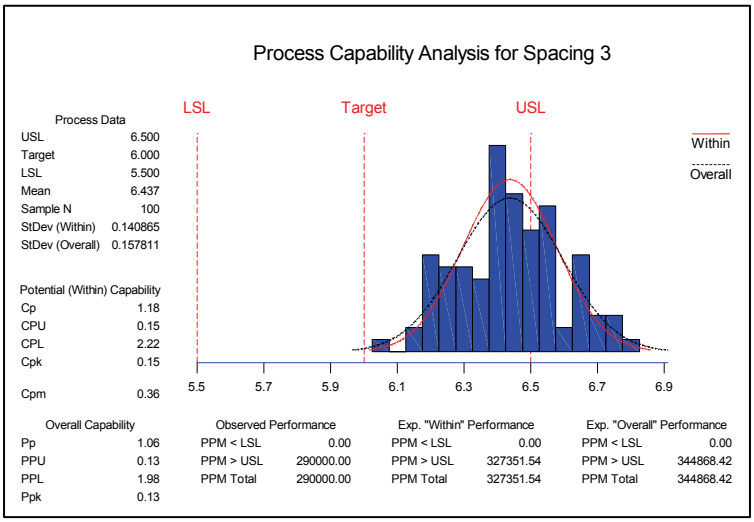


Figure 3 - Capability Histogram for Pad-to-Pad Spacing 3.

Direct laser imaging was used to define the solder mask. As shown in Figure 4, the solder mask could not be designed between the pads with spacings of 4mils and 5mils given a ±2mils solder mask alignment tolerance specification. The solder mask registration was very good.

Printing Optimization

Solder paste printing is a critical step in the SMT process, with the majority of SMT assembly defects related to this process step. In this project, four main factors were investigated: stencil thickness, squeegee pressure, squeegee speed and stencil-board separation speed. The factors and levels are shown in Table 4, with the corresponding Taguchi's L8 OA shown in Table 5. For each DOE run, 3 boards were printed with a fully automated MPM AP printer using a metal squeegee blade and then inspected with a 3D solder paste inspection system (MVT SP-1). The solder paste height and volume data of 20 reference designators for Pad Size Type 5 (130%) were collected for analysis.

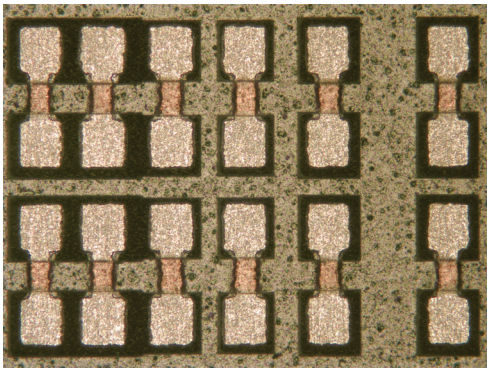


Figure 4 - Photograph of Pads and Solder Mask Showing Lack of Solder Mask between Pads with 4 mil and 5mil spacing. The other pad spacings are 6mils, 8mils and 15mils.

Table 4 - Factors and Levels for 01005 Printing DOE.

Factors	Level 1	Level 2
A: stencil thickness	3mils	4mils
B: Printing Speed	1in/sec	2in/sec
C: Squeegee Pressure	10lb	14lb
D: Separate speed	0.01in/sec	0.025inch/sec

Table 5 - Taguchi's L8 OA for Printing DOE.

Run No.	A	B	C	D
	Stencil thickness	Printing speed	Squeegee pressure	Separate speed
1	1	1	1	1
2	1	1	2	2
3	1	2	1	2
4	1	2	2	1
5	2	1	1	1
6	2	1	2	2
7	2	2	1	2
8	2	2	2	1

The solder paste used in this test was Kester EM907 SAC305 (96.5%Sn/3% Ag/0.5%Cu) lead-free solder paste with 88.5% metal content and Mesh 400. Two electroformed stencils with 3mils and 4mils thickness were tested in this experiment. The aperture shape was the same as the pad shape, and the ratio of aperture to pad size was 100%. The area ratio (AR), defined as the ratio of the opening area of the aperture to the wall area of the aperture, were calculated and are given in Table 1.

Before running the tests, the 3D solder paste inspection system was calibrated. 3D solder paste inspection results after calibration are shown in Figure 5. A Gage R & R (Gage Repeatability & Reproducibility) study was conducted. Variability of reproducibility is due to differences between more than one gage/operator combination. Variability of repeatability is due to differences in successive readings by a single gage/operator combination. The Gage R&R results are shown in Figure 6 based on solder paste Height and Volume response. Since there was only one gage/operator combination, the variability of reproducibility is 0. It can be seen that most of the variation is due to differences between parts. The Gage R & R result based on height response was 7.5% and the Gage R & R result based on volume response was 9.83%. Both measurement errors of the gage are less than 10% of the measurements of the product characteristic, which indicates this inspection machine is capable and appropriate for 3D solder paste inspection.

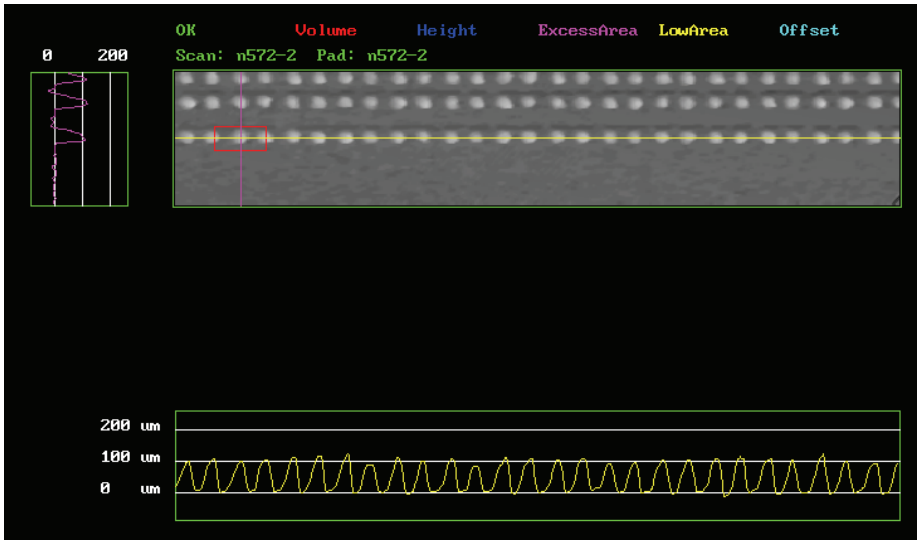


Figure 5 - 3D Solder Paste Inspection Using the MVT SP-1 after Calibration.

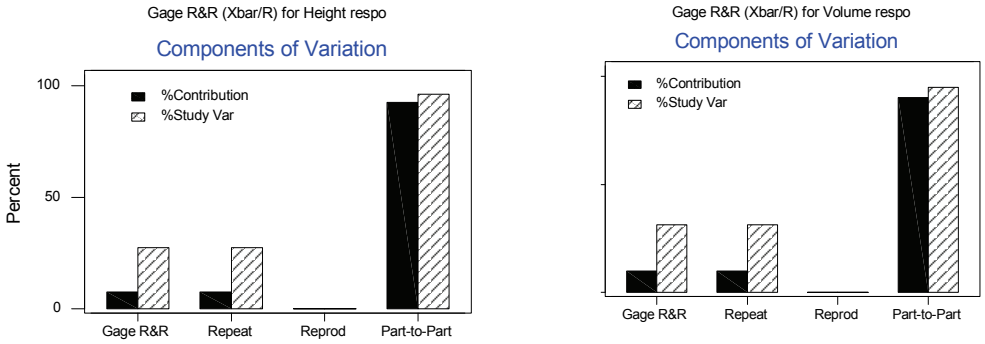


Figure 6 - Gage R&R for Height and Volume Response.

Figures 7 and 8 show the Taguchi DOE analysis results. Figure 7 is the main effect plot for means based on solder paste volume transfer efficiency. Volume transfer efficiency (volume of solder paste transferred/volume of stencil aperture) was used to normalize the difference in solder paste volume due to stencil thickness. From Figure 6, only the stencil thickness had an obvious effect on volume transfer efficiency. The stencil with 3mils thickness has a better transfer efficiency (more than 95%) than the stencil with 4mils thickness (72%), which correlates with area ratio, since the area ratio has the biggest impact on transfer efficiency and repeatability of the solder paste deposits [12]. The 3mils stencil with a Pad Size Type 5 has a higher area ratio (0.903) than the 4mil stencil (0.677). Usually an area ratio of ≥ 0.66 is considered acceptable in the industry [13]. The separation speed had a slight effect; quicker separation contributed to higher transfer efficiency. Printing speed also has a minor effect, while squeegee pressure had an insignificant effect on transfer efficiency.

Further examination of the DOE results by analysis of variance on the S/N ratio is shown in Figure 8. Here, the experiment was conducted with "nominal is the best" quality characteristic. A higher S/N ratio is preferred because a high value of S/N implies that the signal is much higher than the uncontrollable noise factors. The optimal print parameters can be identified based on the S/N ratio plot. The optimal printing parameters were - stencil thickness: 3mils, printing speed: 2 in/sec, squeegee pressure: 14lb, separate speed: 0.01in/sec. Figure 9 shows the printing performance using optimized printing parameter setting.

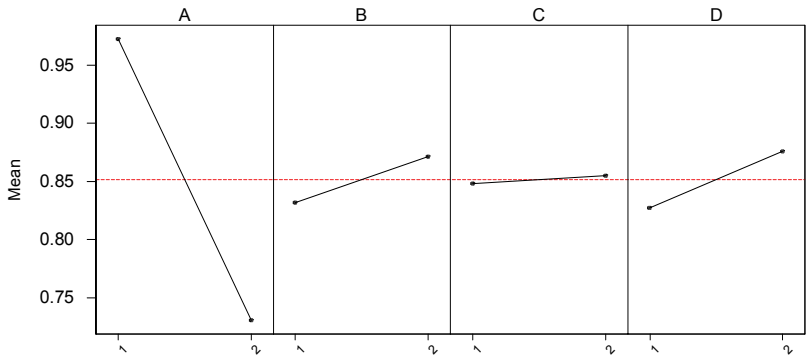


Figure 7 - Main Effects Plot for Means Based on Volume Transfer Efficiency.

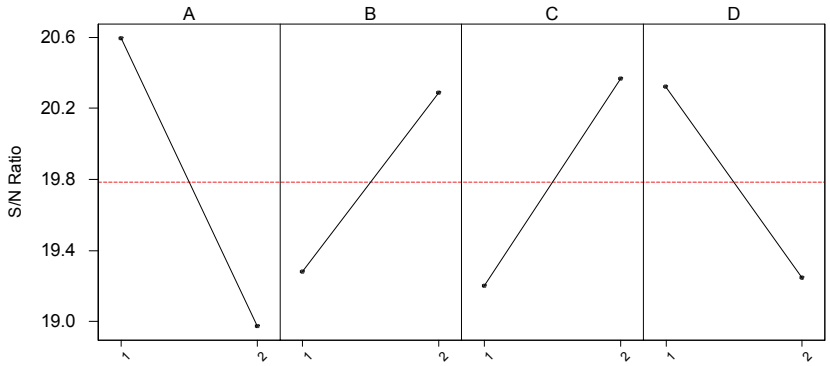


Figure 8 - Main Effects for S/N Ratio Based on Volume Transfer Efficiency.

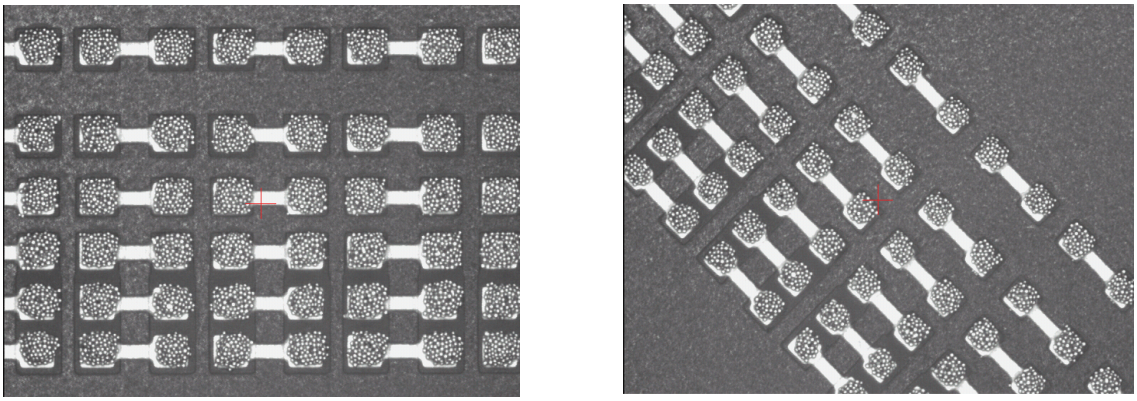


Figure 9 - Printing Performance Using Optimized Printing Setting.

Figure 10 shows process the capability index (C_p) comparison for different pad size types for the two stencils based on the optimal printing settings. The 3mil stencil is more process capable and robust than the 4mil stencil, which confirms the above DOE results. Similarly the bigger pad size types with higher area ratio have larger process capability indices. The 3mils thick stencil was used for all subsequent assembly experiments.

Placement Accuracy Evaluation

The typical size of the 01005 resistor was 0.38mm x 0.18mm with a termination width of 0.08mm. 01005 components are supplied in regular 8mm tape and reel with 2mm pitch between pockets. There were two common orientation defects in as-received components in tape & reel as shown in Figure 11; edge-standing and upside-down components. Sometimes edge-standing components damaged the nozzle tip during pick and place of the component. Edge-standing components may also be placed since the width and thickness of these tiny components are similar and the difference may not be discerned by the pick and place vision system. Upside-down components have the appropriate length and width dimensions and will typically not be rejected by the pick and place vision system.

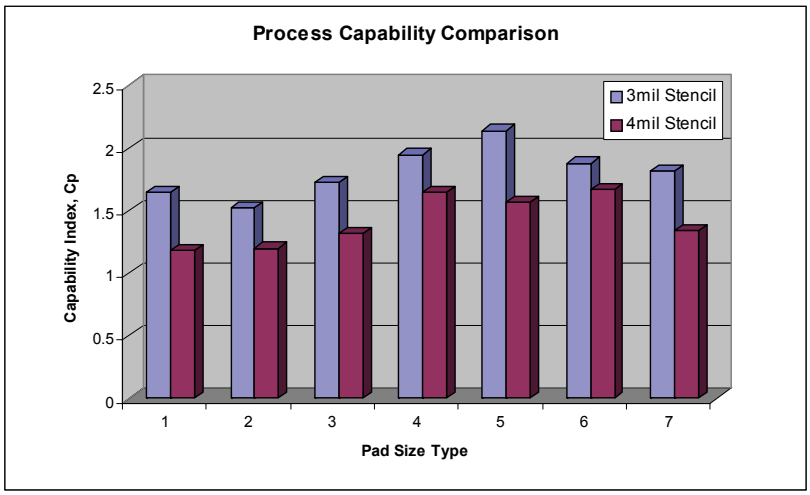


Figure 10 - Process Capability Comparison for Two Stencils and Different Pad Size Types.

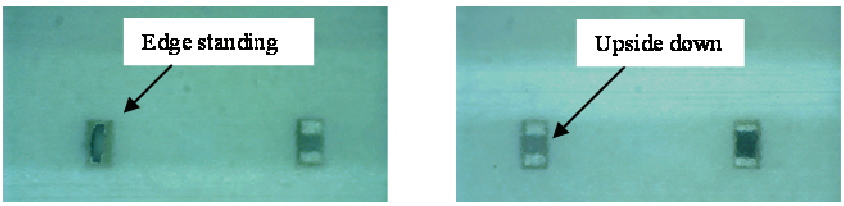


Figure 11 - Two Common Orientation Defects in As-received 01005 Components in Carrier Tape.

The 01005 components were placed with an Assemble on ACM Micro[1] pick and placement machine. A new nozzle body and tip were specially designed for 01005 placement. The diameter of the nozzle tip was 0.38mm and the opening of the tip was 0.14mm. The maintenance of such a tiny and precise tip is very important. Once the tip is worn out or not flat enough, it will have an obvious effect on the placement performance. Feeder precision is sensitive for consistent pick performance.

The objective of the placement tests was to compare the placement to pad accuracy when using 2 or 3, local or global fiducials. Four tests were performed based on: 2 round global fiducials, 3 round global fiducials, 2 round local fiducials and 3 round local fiducials. The distances X1, Y1, X2 and Y2 shown in Figure 12 were measured to calculate the component's centroid offset and rotation relative to its associated pads. The Centroid Offset (CO) was calculated as:

$$CO = \sqrt{(\Delta x)^2 + (\Delta y)^2}$$

The measured offsets combine PCB accuracy and machine placement accuracy. Two boards were run for each test and 25 components were randomly selected for measurement. The calculated offset and rotation data were analyzed using the statistics software Minitab 13.0. Table 6 lists the mean and C_{pk} for all combinations. The C_{pk} values were calculated with a centroid USL and LSL of $\pm$2mils and a rotation USL and LSL of $\pm 5^{o}$. From this data, it can be seen that using 3 local fiducials results in the best placement to pad accuracy. Local fiducials better accommodate area variations within the PCB caused during the PCB manufacturing process such as PCB stretch and over/under etch during processing. All subsequent assemblies used 3 local fiducials for placement.

[1] Assembleon's AQ-2, successor of the ACM Micro, should perform better in 01005 placements because of higher resolution cameras that can detect edge-standing and missing 01005 components. The AQ-2 was not available to Auburn University during this study.

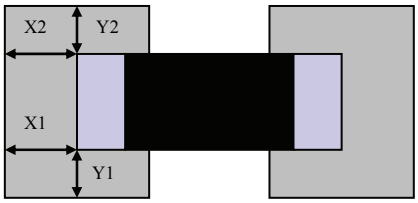


Figure 12 - Schematic of Distances X1, Y1, X2 and Y2.

Table 6 - The Means and C_{pk} for Placement Accuracy Evaluation.

Fiducial	Centroid Offset, (mm)			Rotation, (Degree)		
	Orientation	0	90	Orientation	0	90
2 Global Fiducials	Mean	0.024	0.023	Mean	-0.90	0.55
	C_{pk}	0.93	1.45	Cpk	1.03	1.21
3 Global Fiducials	Mean	0.026	0.022	Mean	-1.052	-0.206
	C_{pk}	0.98	1.54	Cpk	1.41	2.25
2 Local Fiducials	Mean	0.011	0.026	Mean	-1.129	0.34
	C_{pk}	2.18	1.87	Cpk	1.81	2.13
3 Local Fiducials	Mean	0.014	0.018	Mean	0.643	0.521
	C_{pk}	2.21	2.32	Cpk	2.08	3.12

Reflow

Reflow was carried out in a Heller 1800 reflow oven. Two reflow profiles, a quick-ramp and a soak profile shown in Figures 13 and 14 were used for lead free soldering. Initially, one board was reflowed in air; however, the wetting was not satisfactory. Individual solder spheres could be seen under the microscope.

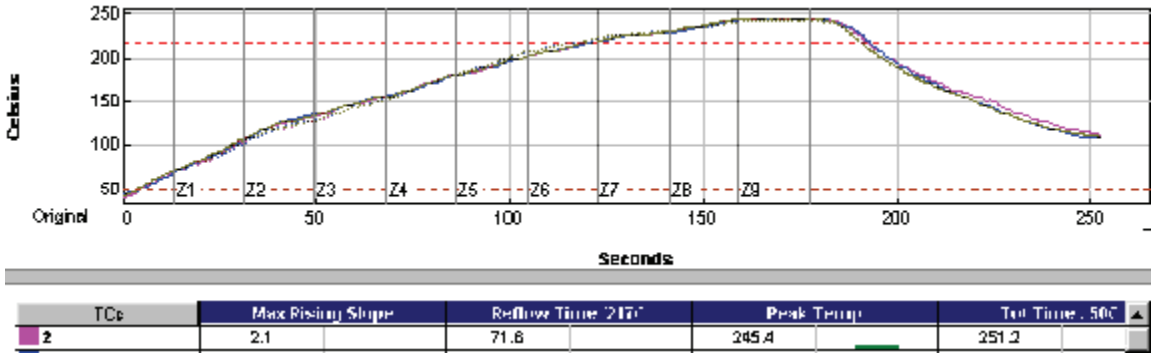


Figure 13 - Lead Free Quick-ramp Reflow Profile.

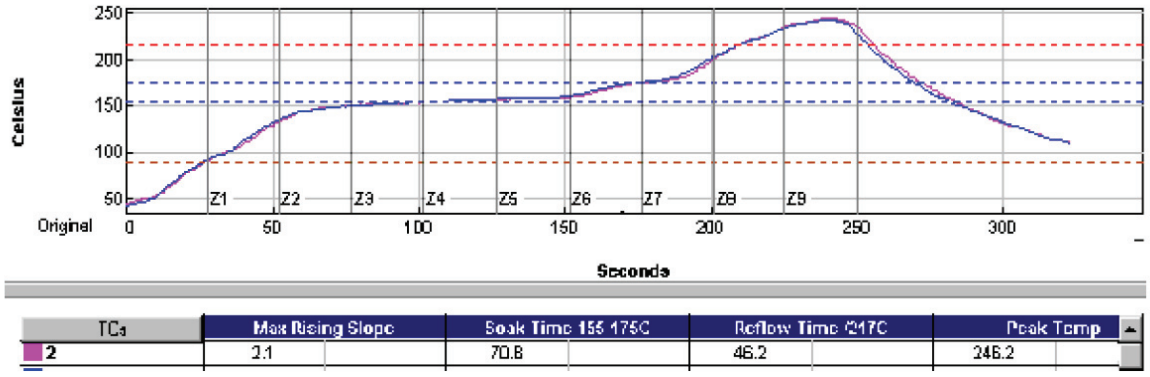
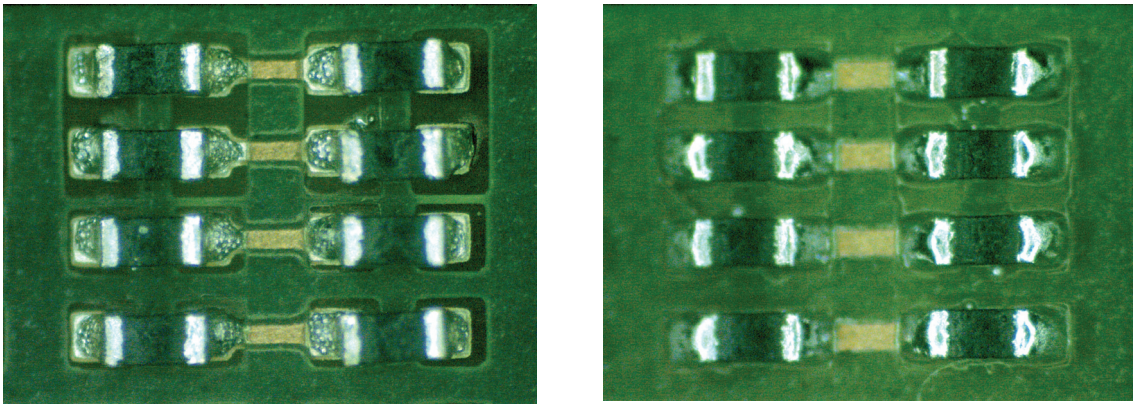


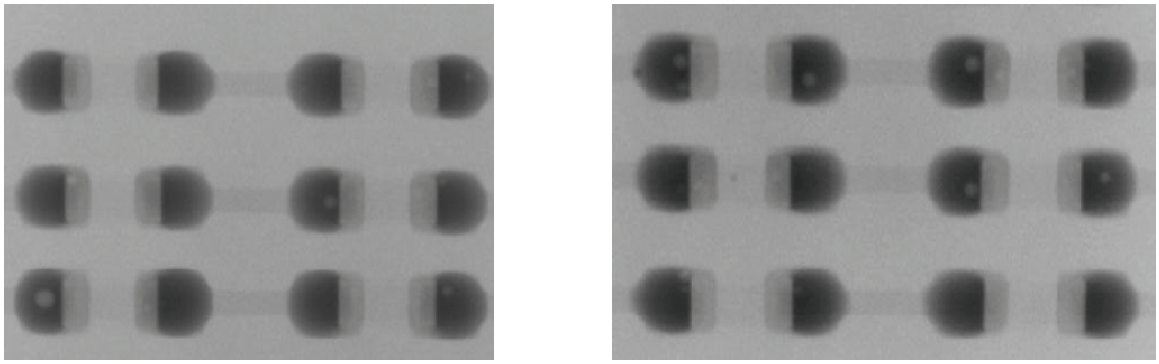
Figure 14 - Lead Free Soak Reflow Profile.

The 01005 solder paste deposits are so small that most of the solder alloy is exposed to the reflow atmosphere, which can lead to surface oxidation in an air environment. Subsequently, nitrogen was used for reflow and good wetting was observed. Figure 15 shows the wetting performance comparison between air and nitrogen reflow atmospheres. Nitrogen was used for all subsequent assemblies. Solder joints reflowed using the two reflow profiles were x-rayed. Figure 16 shows typical x-ray images. Both profiles resulted in some voiding, primarily in the fillet, but also under the resistor terminals.



(a) Reflow in air (b) Reflow in nitrogen

Figure 15 - Wetting Comparison in Air (a) or Nitrogen (b).



(a) (b)

Figure 16 - X-ray of Solder Joints for Ramp (a) and Soak (b) Profiles in Nitrogen.

Post Reflow Inspection

After reflow, all of the boards were inspected using a VISCOM PCB inspection machine, and the number of defects was collected. Defects observed after reflow included bridging, tombstone, edge-standing parts, missing parts and upside-down parts. There were a total of 2296 defects out of 28920 resistor placements, i.e. 7.94% defect rate. This includes all combinations of pads, spacings, reflow profiles, orientations, and vias-in-pad. Table 7 lists the defect distribution in all samples. Figure 17 shows the defect distribution for all defects. Bridging and tombstones are the primary defects (68%). Figure 18 illustrates the common defects.

Table 7 - Defect Distribution in All Samples.

Defect	Bridging	Tombstone	Edge-standing	Missing Part	Upside down	Sum
Sum	1086	485	416	245	64	2296
Percentage	3.75%	1.68%	1.44%	0.85%	0.22%	7.94%

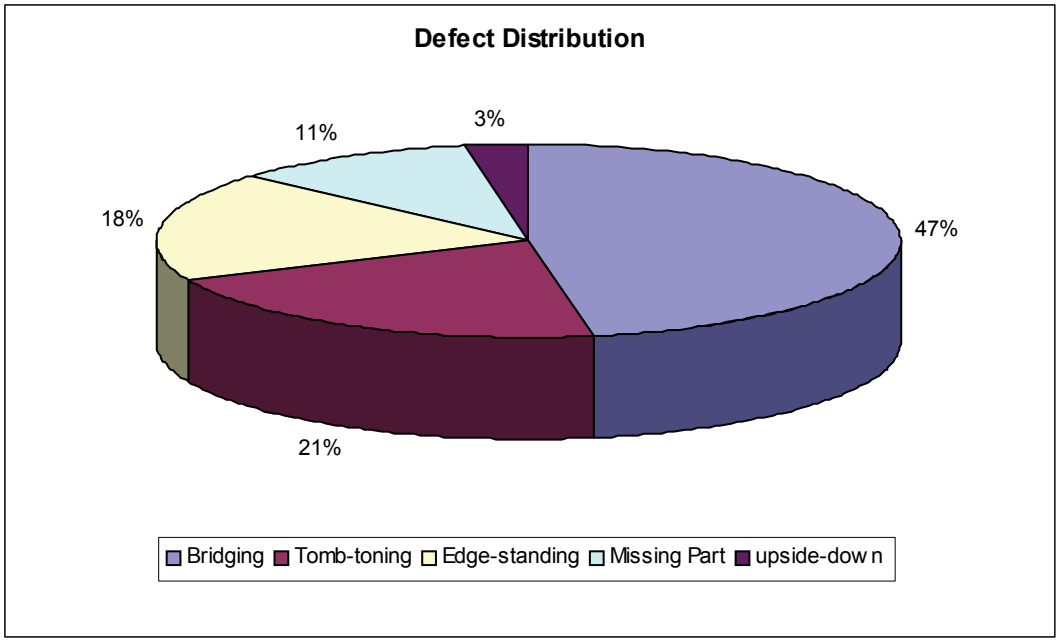


Figure 17 - Defect Distribution for all Build Combinations.

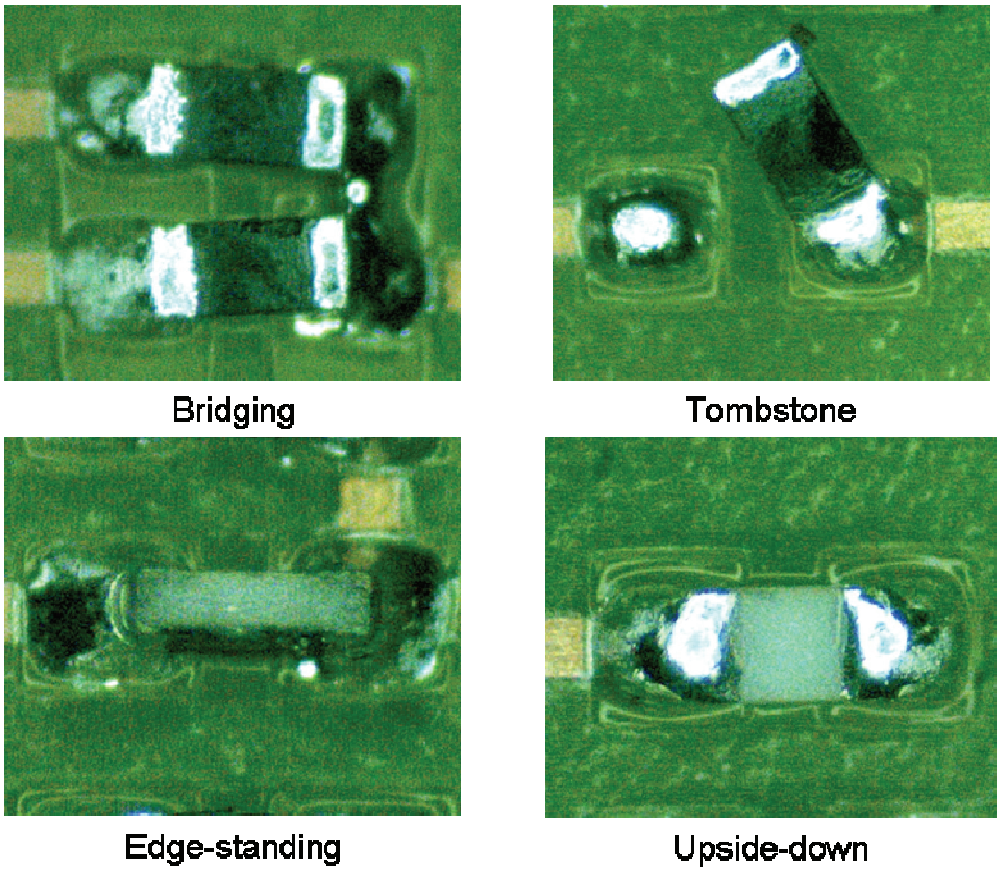


Figure 18 - Example of Different Defects.

Bridging - 90.3% of the bridging occurred in the Space 1 (4mils pad-to-pad) group and 9.7% of the bridging was in the Space 2 (5mils pad-to-pad) group. As previously noted in Figure 4, there was no solder mask patterned between the pads at these tight spacing. There were no bridges for pad-to-pad spacing of 6mils or greater. Figure 19 shows the bridging defect rate comparison for different pad size types. The percent Defect Rate is calculated as the number of defects per category/total number of components assembled per category x 100%. It can be seen that larger pad sizes resulted in more bridging for rectangular pads and the home base design had more tendency for solder bridging than the rectangular pads. A minimum of 6mil pad-to-pad spacing for parallel resistors is recommended for 01005 chip resistors.

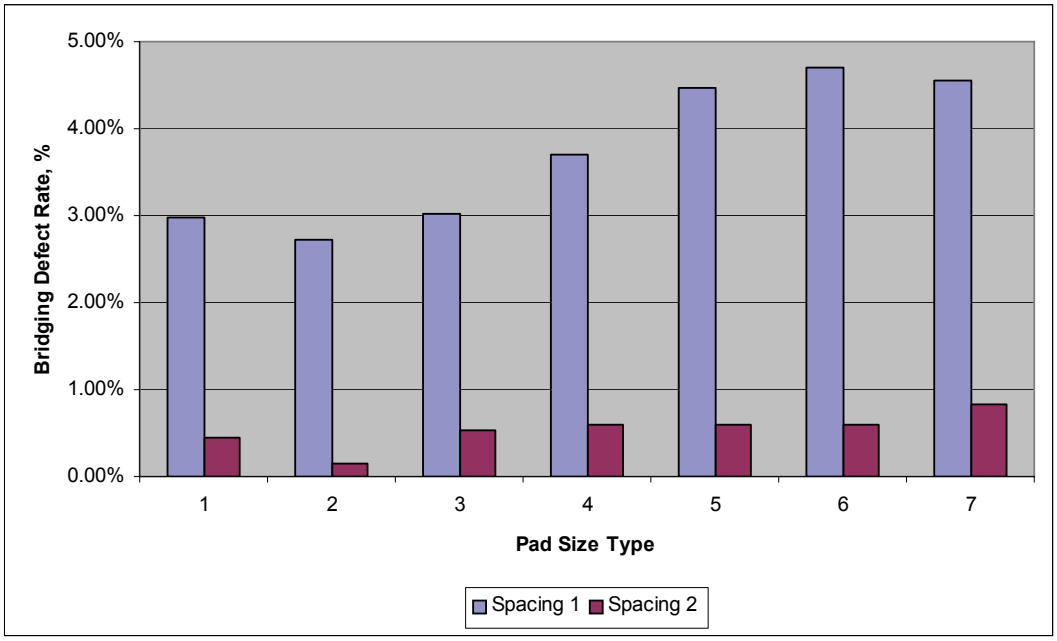


Figure 19 - Bridging Defect Rate Comparison for Different Pad Size Types.

Tombstones - Figure 20 shows the influence of pad-in-via design on tombstones for Pad Size Type 1 (100%) pads. As expected, the via-in-pad design significantly increased the likelihood of tombstones, with a via in only one of the two resistor pads being somewhat worse.

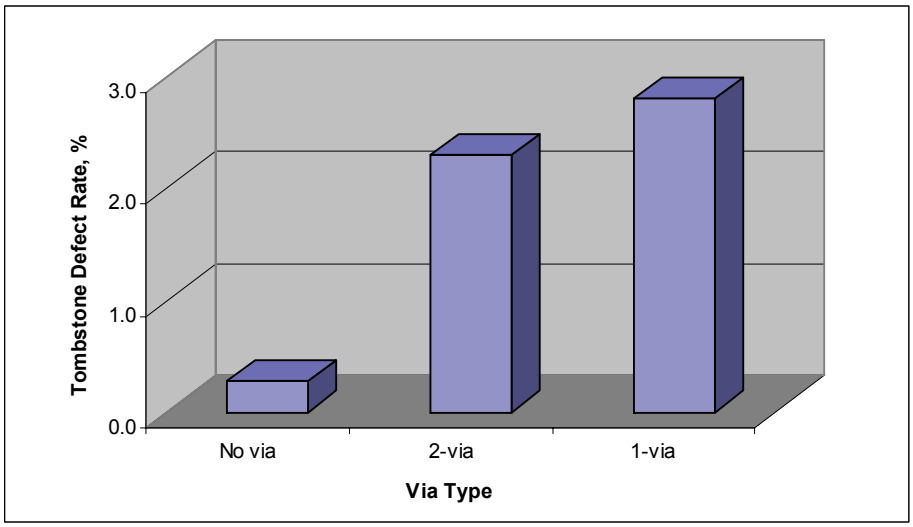


Figure 20 - Tombstone Defect Rate Comparison for Pad Size Type 1 with and without Vias-in-Pad.

Figure 21 plots the effect of the reflow profiles on tombstone defect rates. The data includes all pad size types and resistor orientations. The direct ramp-to-peak profile is significantly better than the soak profile.

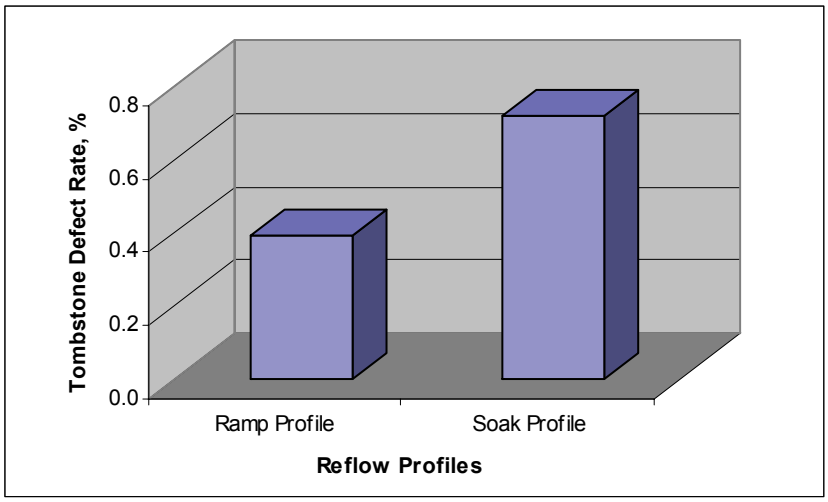


Figure 21 - Tombstone Defect Rate as a Function of Reflow Profile.

Figure 22 plots the tombstone defect rate as a function of resistor orientation for Type 1 Size Pads (100%). It includes data for both reflow profiles. Resistor orientation has little effect on tombstones.

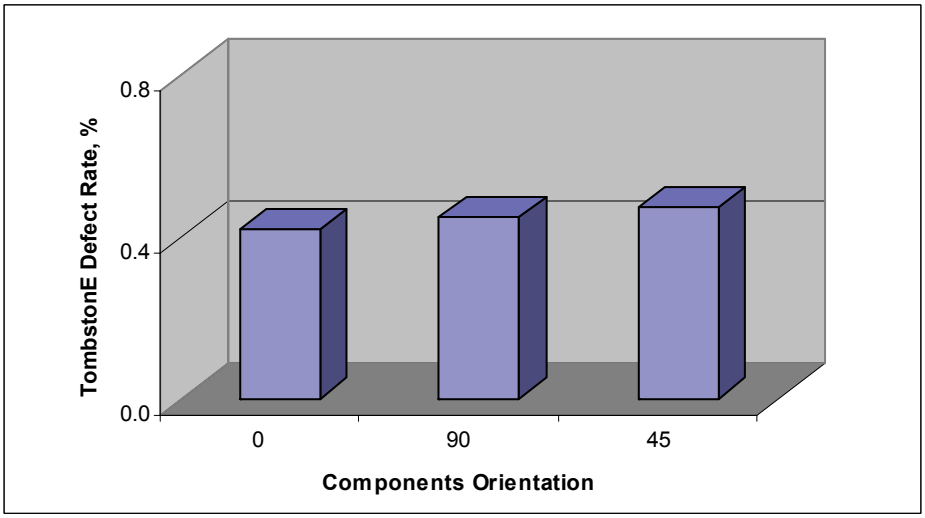


Figure 22 - Tombstone Defect Rate as a Function of Resistor Orientation for Type 1 Size Pads.

Figure 23 plots the effect of pad size type on tombstone defect rates. The data includes both 0^o and 90^o orientations and both reflow profiles. Increasing the pad size (and volume of solder) has a significant impact on the tombstone defect rate. With the ramp profile, 0^o and 90^o orientation and the Pad Size Type 2 (90%), the tombstone defect rate was 0% for 1200 resistors placed.

Figure 24 compares the tombstone defect rate for pad size Type 1, no via pads with an intentional solder mask shift of 2mils in the resistor length direction. $\pm$2mils was the solder mask design tolerance. Shifting the solder mask unbalances the solderable copper area: pad only on one end and pad plus 4mils of trace length on the other. Solder mask misalignment increased the tombstone defect rate.

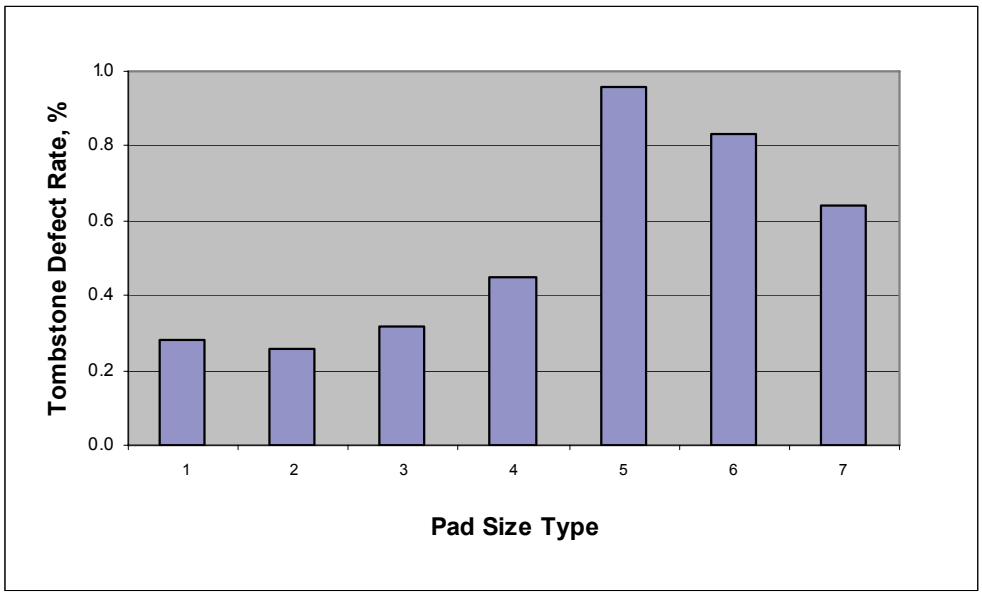


Figure 23 - Tombstone Defect Rate as a Function of Pad Size Type.

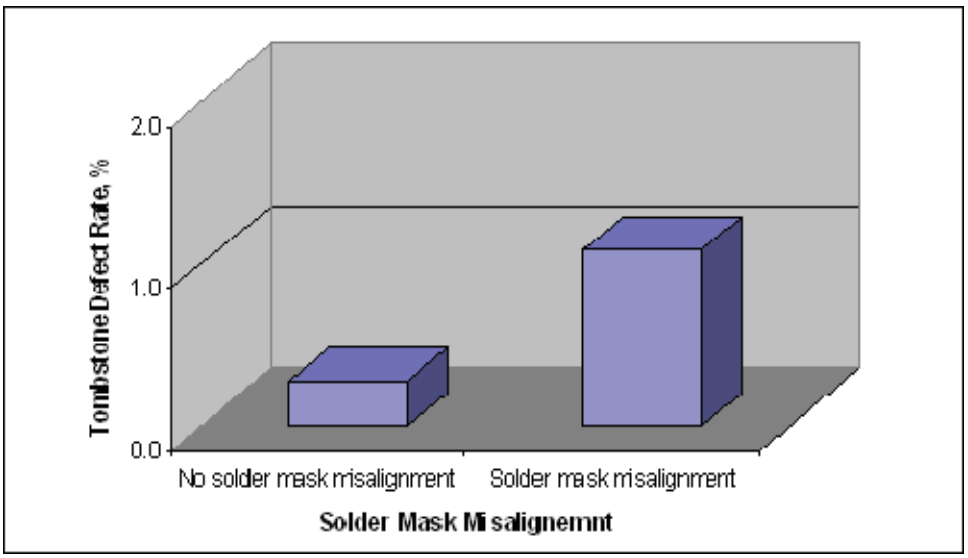


Figure 24 - Tombstone Defect Rate as a Function of Solder Mask Misalignment for Pad Size Type 1.

Missing Parts - Due to the small size of the nozzle tip opening and the component, vacuum sensing could not be used to verify part pick-up. After the nozzle became worn, the surface of the tip became shiny and the vision system would occasionally recognize the shiny tip as the small 01005 component. Tip wear must be properly monitored to avoid missing parts.

Edge-standing and Upside-down Components - As mentioned in the placement section, upside-down and edge-standing defects were caused by part orientation in the as-received tape. Given the symmetry of the part, the vision system could not consistently detect edge-standing components and could not detect upside-down components. Upside-down components are likely not an issue as bulk feeding is often used for larger chip components and up or down orientation is not a concern. Edge-standing parts should be addressed in the taping system.

Conclusions

01005 chip resistors placement has been studied. The board manufacturer did not maintain the design tolerance of $\pm$0.5mils, the pads were all approximately 0.5mils below design dimensions. An electroformed, 3mil stencil yielded a robust paste printing process and higher C_p indices compared to a 4mil stencil. Nitrogen reflow was required to achieve good solder

wetting due to the high surface-to-volume ratio of the solder deposits. With regard to bridging defects, no defects were observed if the pad-to-pad spacing for parallel resistors was 6mils or larger. Rectangular pads with no vias-in-pad and designed at 90% of nominal pad size (Pad Size Type 2) produced no tombstones in 1200 placements with the ramp profile, independent of 0^o or 90^o resistor orientation. A larger sample size for this combination should be run to determine ppm defect rates. Given the undersized pads on the actual board, the 90% pad average width was 6.7mils (versus a design value of 7.2mils) and the measured width of the 01005 chip resistor was 7.1mils. Thus the pads were slightly smaller in width than the chip resistor. The reliability of the solder joints with this pad size should also be evaluated.

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