Thin Sn over Ni: A Practical and Effective Whisker Mitigation Strategy for Leadframe

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Abstract
As the electronic industry shifts to lead-free manufacturing, Sn whisker remains a key reliability concern. Several whisker mitigation strategies have been adopted by the component manufactures, but not without controversy and heated debate. In this paper, we will describe an innovative whisker mitigation approach for leadframe application. This approach can be viewed as a drop-in replacement for the SnPb surface finish and can be introduced without significantly modifying the current leadframe plating line process. Our investigations demonstrated superior whisker resistance of utilizing "thin tin over nickel" compared to other whisker mitigation strategies practiced in the industry.

Introduction

As RoHS will take effect on July 1, 2006, the lead-containing surface finishes have to be eliminated from most electronic components and devices. While precious metal surface finishes involving Au and Pd may be used for high-reliability products, pure Sn will be the preferred surface finish for most of the consumer electronics. Unfortunately, the electroplated Sn is known to be prone of spontaneous whisker formation, which can cause short in the electronics circuit and presents a reliability risk. Despite of extensive R&D in industry, academia and government national labs, whisker formation remains a concern of the long-term reliability for many products. Several approaches have been proposed for minimizing whisker formation, among which the Ni barrier layer and post-plating bake have received the most acceptance by the electronics industry[1-3]. For instance, E4 (Infineon, Philips, ST Microelectronics and Freescale) has chosen ~10 μm Sn with $150^{o}C$ baking for 1h immediately after plating as the leadfree component finish. On the other hand, several companies including Agere has decided to use Ni underlayer, where typically ~10μm Sn is plated over Ni/substrate. Both approaches have showed various degree of success in minimizing whisker formation at various aging conditions. However, thermal cycling has consistently produced whisker formation in most instances, which has been attributed to the thermal mechanical stress generated due to the CTE mismatch between Sn and substrate during thermal cycling.

In this paper, we will demonstrate a new approach, where a combination of thin tin (ca. 1 to 2 µm) with a Ni barrier layer (typically 1 to 2 µm) over common leadframe and connector substrates is used to minimize whisker formation under stringent thermal cycling as well as isothermal aging conditions. Compared to the two currently accepted whisker mitigation strategies in electronic industry, thin Sn over Ni has better whisker performance and lower overall cost. Rational of using thin Sn over Ni and results from lab whisker testing as well as field trial will be presented.

General background information on tin whisker and mitigation strategy

It has been widely accepted that the compressive stress is the driving force for the whisker formation[1-9]. The attempt by the deposit to relieve the compressive stress through recrystallization and grain growth results in whisker formation. Consistent with this notion, it has been also demonstrated that the tin film under tensile stress does not grow whiskers[3, 7-9]. The most effective way for minimizing whisker formation is eliminating all pathways that generate compressive stress. If a tensile stress could be created and maintained in the tin film throughout the lifetime of the devices, whisker formation would be eliminated.

There are several pathways for stress formation in electroplated Sn films: residual stress generated during plating, applied mechanical stress (e.g. mechanical deformation), stress formation due to interfacial reactions between Sn layer and Cu substrate, stress due to CTE mismatch between Sn layer and substrate during thermal cycling. More recently, it was also demonstrated that corrosion can also leads to stress and therefore whisker formation. In most cases, both plated stress and mechanical stress due to trim-and-form in the leadframe production are a "one time" event and therefore have a much smaller effect on the continuous growth of whisker compared to stress due to CTE mismatch and interfacial reactions. In some of the connector applications, a continuously applied mechanical stress is sometime present, which can lead to severe whisker formation. However, for the majority of electronic devices, especially leadframes, the main pathways for stress generation (whisker formation) are the stress due to intermetallic formation and thermal mechanical stress due to CTE mismatch. While the stress due to intermetallic formation can be effectively dealt with Ni underlayer or post-plating bake, the thermal mechanical stress remains problematic for many electronic devices.

As discussed briefly above, Ni-underlayer and post-plating bake have received most acceptances within the electronic industry among various whisker mitigation strategies. Ni under-layers have been shown to be effective in practically eliminating whisker formation both at room temperature and 50^{o}C. This has been attributed to the suppression of Cu diffusion into Sn and therefore eliminating the associated compressive stress formation in Sn film. However, when Sn/Ni couples are subjected to thermal cycling, whisker formation is observed. This has been attributed to the thermal mechanical stress generated due to the CTE mismatch between Sn and Ni/Cu substrates. Similar to Ni-underlayer, post-plating bake deals with stress due to intermetallic formation but not thermal mechanical stress due to CTE mismatch. It has been postulated that a smooth and homogeneous Sn-Cu intermetallic layer with minimal stress is formed during the post-plating bake. Any stress generated is most likely also released during the thermal bake. The intermetallic layer will then serve as a barrier layer for further Cu diffusion during the lifetime of the device. However, as in the case of Ni-underlayer, the thermal mechanical stress due to CTE mismatch can still be generated, if the device is subjected to a temperature fluctuation.

Pure Sn has one of the highest linear thermal expansion coefficients ($22X10^{-6}K^{-1}$). Cu and Ni, on the other hand, have much lower linear thermal expansion coefficients ($16.5X10^{-6}K^{-1}$ and $13.4X10^{-6}K^{-1}$ respectively). When Sn is plated over Cu or Ni and subjected to thermal cycling, the Sn coating will expand or contract differently as the Cu or Ni sub-layers. During the heating stage, Sn will expand more than Cu or Ni substrate, which will impose a compressive stress on the Sn film. During the cooling cycle, on the other hand, Sn will contract more than Cu or Ni, which will add a tensile stress to the Sn film. Therefore, during thermal cycling, Sn will be subjected to alternating compressive-tensile stress cycles. The compressive stress in the heating-up cycle is believed to be the cause of whisker formation during thermal cycle test. Clearly, a different approach than simply using Ni-underlayer and post-plating bake has to be developed to deal with the thermal mechanical stress generated by the CTE mismatch during the thermal cycling.

Why Thin Sn over Ni?

Recently, our thermal cycling experiments have repeatedly demonstrated that 3μm Sn over a Ni barrier layer (1.5 to 2μ) exhibited significant less whisker formation than 10μm Sn over the same Ni layer. This result is in strong contrast to Sn film plated directly over Cu, where thick Sn typically shows less whisker formation compared to thin Sn[1]. This difference can be readily understood if one look at the difference in the interfacial reaction between Sn-Cu and Sn-Ni. At both interfaces, there is a significant intermetallic formation as well as interdiffusion. However, the difference is that Sn is the slow diffusing species at Sn-Cu interface, while Sn is the fast diffusing species at Sn-Ni interface. For Sn over Cu, there is more Cu diffusing into Sn than Sn into Cu, which leads to excessive materials in the Sn layer. For Sn over Ni, on the other hand, Sn diffuses faster into Ni than Ni into Sn, which results in a material deficiency in the Sn layer. Consequently, the difference in the diffusion rate at the two interface leads to a compressive stress (excessive materials) in Sn layer for Sn/Cu and a tensile stress (material deficiency) in Sn layer for Sn/Ni. This stress is localized in the Sn layer close to the interface and decreases with the distance from the interface, as schematic illustrated in Figure1 for Sn-Cu. For a 10μm Sn film for instance, the first 5μm Sn layer from the surface, which is far away from the interface, is hardly affected by the intermetallic formation at the interface initially, while a compressive stress will develop quickly in the first 1μm Sn layer close to the interface. Therefore, a thick Sn film has a lower average stress than a thin Sn film. For Sn plated directly over Cu, the compressive stress decreases with increasing Sn film thickness, and consequently there will be less whisker formation for a thick Sn film than a thin Sn film. For Sn/Ni, the tensile stress decreases with increasing Sn film thickness. Since tensile stress will hinder whisker formation and can cancel out some of the compressive stress generated during thermal cycling. Therefore, a thin Sn film over Ni will show higher whisker resistance than a thick Sn film during thermal cycling test.

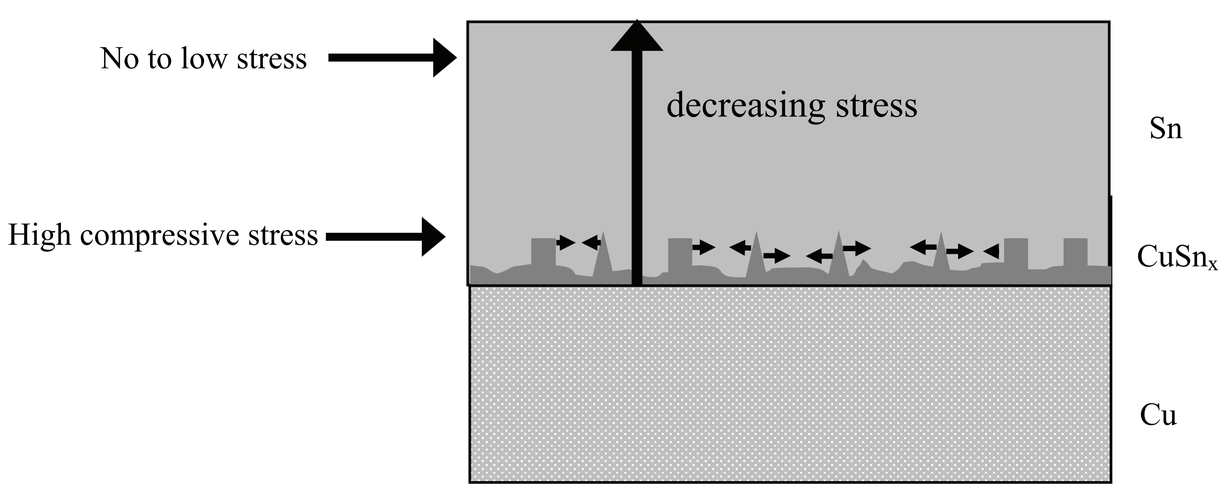

Figure 1 - Schematic Drawing of Stress Gradient Formed in an Sn layer due to the Interfacial

Experimental Results

In order to test the idea that thin Sn over Ni is more effective in minimizing whisker formation than thick Sn over Ni, we have designed a whisker test matrix consisting of 0.5□, 1□, 2□, 3□ and 10□ Sn plated on 2□ Ni over Cu C194 alloy. The samples were aged at room temperature for 40 days to allow Sn-Ni inter-diffusion and the build-up of tensile stress. The stress was measured using x-ray diffraction (D8 Discover diffractometer system with GADDS by Bruker Analytical X-ray Systems, Inc.). To achieve high accuracy on the lattice constant measurement, Cr-radiation was used. The strains were measured at 19 different angles from -45^o to 45^o for the diffraction peak (312) at 2□=143.8^o. The sin^2□plot method is used to calculate the stress in the coating. Please note that the stress measured is an average value of area covered by x-ray beam (diameter=0.5mm) to a depth of 1 to 2 microns.

Figure2 plots stress vs film thickness, and as can be seen from the curve, 0.5□ Sn is highly tensile stressed, which decreases with increasing Sn film thickness and becomes compressive at a thickness of 3 microns. This result is in perfect agreement with the explanation proposed above.

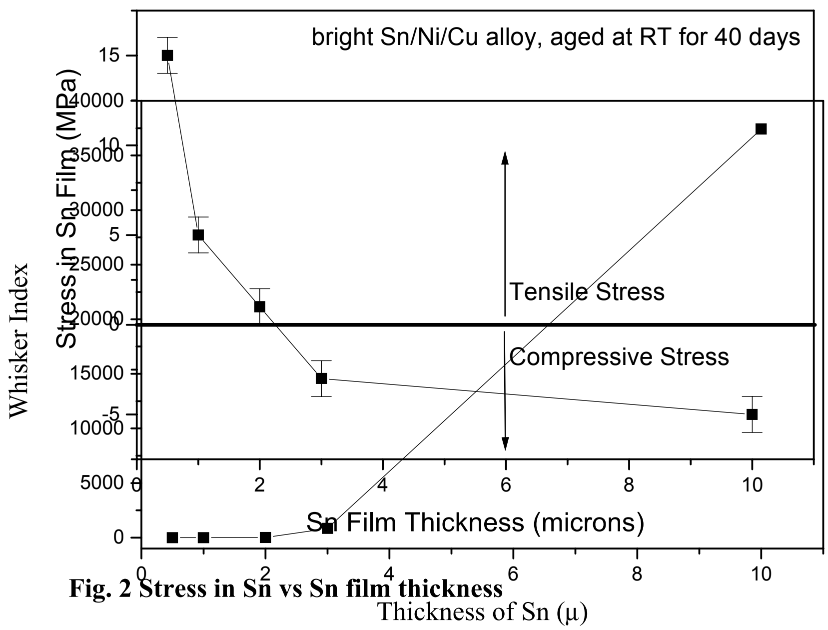

Fig. 2 Stress in Sn vs Sn film thickness

Fig.3 Whisker Index

To further test the effect of Sn film thickness on whisker formation, the samples were subjected to 1000 thermal cycles using the condition suggested by NEMI (One Cycle: -55°C/10min & 85°C/10min, Air to Air). In Figure3, tin whisker index is plotted versus tin film thickness. As we can see from Figure3, 10□ Sn plated over Ni showed a large number of whiskers after 1000 cycles. 3□ Sn showed some whisker formation, but much less than 10□ sample. Most interestingly, 0.5□, 1□ and 2□ Sn films showed no whisker formation after 1000 thermal cycles. Using thin Sn films over a Ni under-layer effectively eliminates stress formation due to the interfacial reaction as well as minimizes the effect of thermal mechanical stress due to CTE mismatch.

This result is also confirmed by data collected from samples plated in a production environment. Two different types of assembled components were tested. The components were plated with LECTRO-NIC Ni for a ductile and oxidation resistance underlayer and Sn films. The leadframes were trim-and-formed and some of the samples were subjected to two different simulated reflow conditions. Then, the as-received and reflowed samples were subjected to thermal cycling test using the condition suggested by NEMI (One Cycle: -55°C/10min & 85°C/10min, Air to Air). Tab. 1 summarizes the samples tested in this matrix.

Table 1 Sample Matrix

Sample	Component	Ni Thickness	Sn Thickness	Reflow condition
1	A	2□m	2□m	
2	A	2□m	3□m	
3	B	2□m	2□m	
4	B	2□m	3□m	
5	A	2□m	2□m	215^{o}C for 5 min.
6	A	2□m	2□m	260^{o}C for 2 min

Whisker observations were performed after 1000 and 2000 cycles aging. Figs 4, 5 and 7 summarize the results after 2000 cycles thermal cycling test. No whiskers were observed on any of the 6 samples after 1000 and 2000 cycles thermal cycling test except sample 4, which showed tiny whiskers after 2000 cycles whisker test. Close inspection shows that the whisker is only observed in the scratched area, apparently due to local mechanical stress. Interestingly, additional aging of the sample at room temperature for two months does not cause the whisker to grow further, as demonstrated in Fig 6. These results demonstrate again the superior whisker resistance of thin Sn over Ni even under thermal cycling condition.

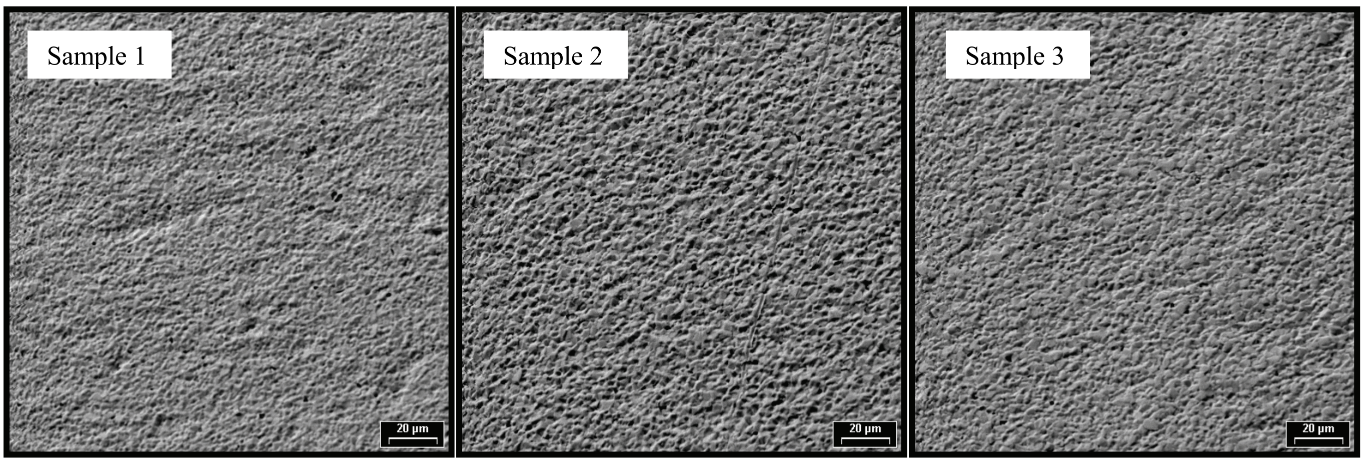

Figure 4 -SEM Images of Samples after 2000 Cycles Thermal Cycling Test

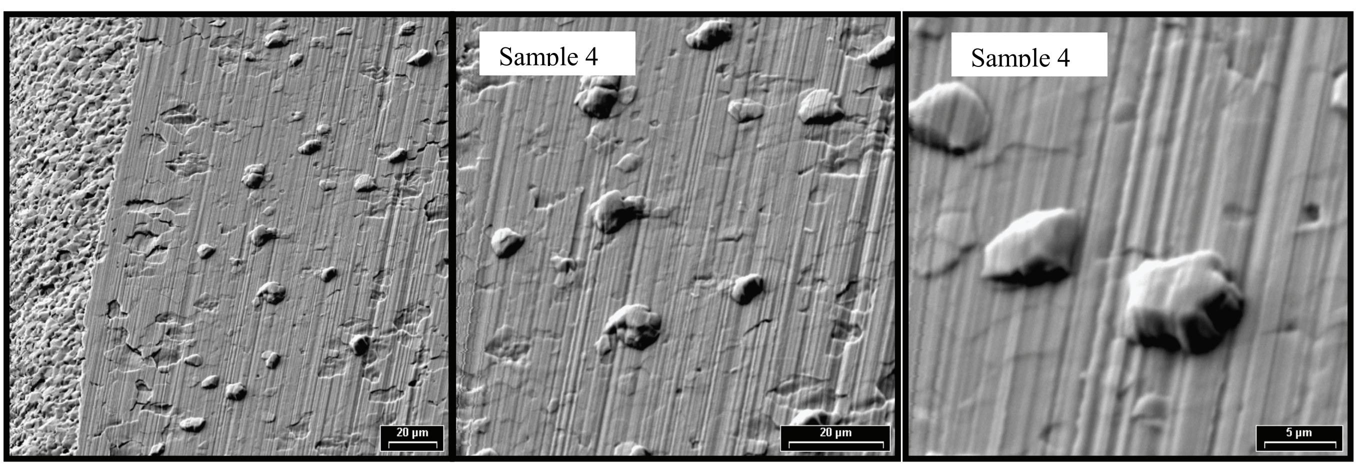

Figure 5 - SEM Images of Sample 4 after 2000 Cycles Thermal Cycling Test

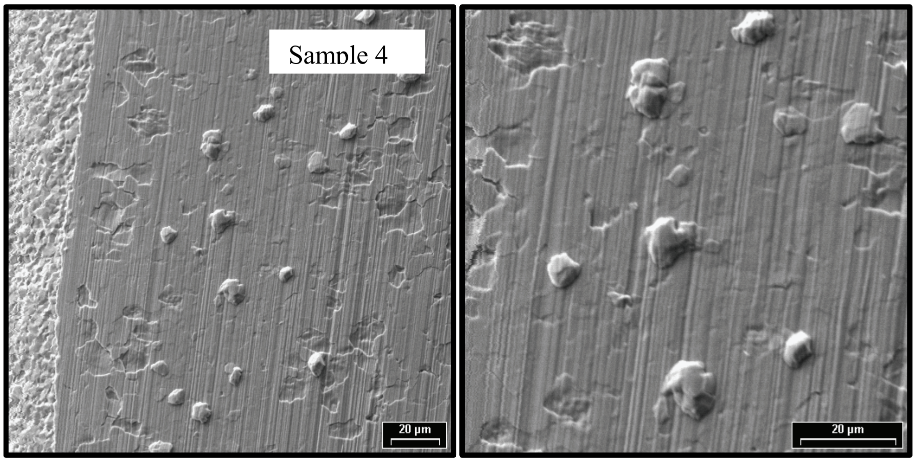

Figure 6-SEM Images of Sample 4 After 2000 Cycles Thermal Cycling and 2 Months Aging at Room Temperature

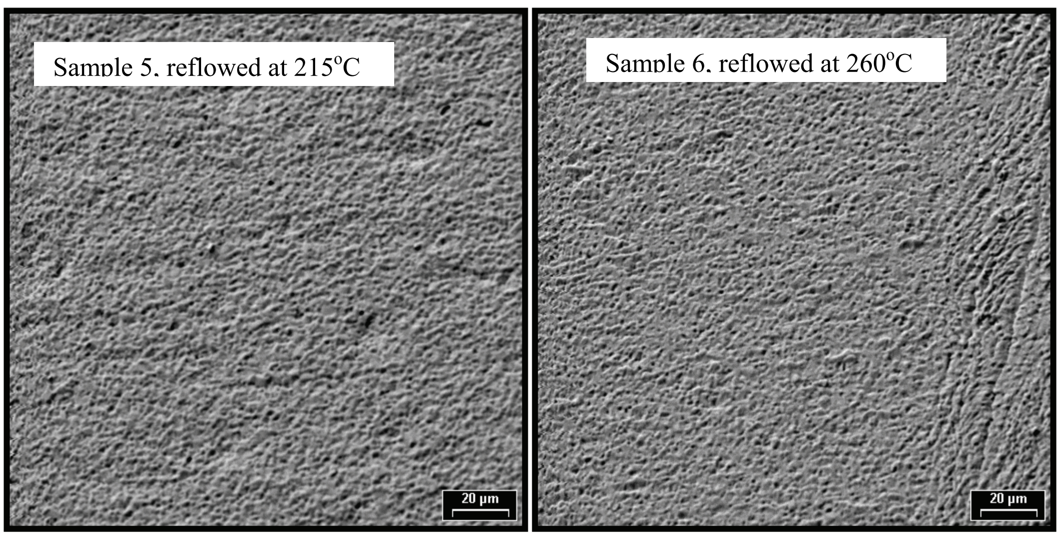

Figure 7 - SEM Images of Samples 5 and 6 After 2000 Cycles Thermal Cycling Test

Solderability

With decreasing tin film thickness, the solderability becomes a concern and needs to be evaluated. The “Dip-and-look” is a convenient test commonly used in industry to assess the solderability by evaluating solder coverage.

In order to test the solderability of the thin Sn, samples with various Sn thicknesses were aged at 85°C/85%RH for 8h. Tab.2 summarizes “Dip-and-look” test results for various Sn films from 0.5□ to 10□ performed on flat samples as well as sample after 90° bending. As can be seen from Tab.2, all the samples without bending passed solderability even with non-active flux. The bent samples showed slightly worse solderability. However, Sn film as thin as 1□ still passed the solderability test. If mildly activated flux is used, 0.5□ Sn film also passed.

Table 2 - Dip-and-Look Test After 8h Steam Aging

	R type NA flux		R type MA flux	
	Bent area	Flat area	Bent area	Flat area
10μm Sn	Pass	Pass		
3μm Sn	Pass	Pass		
2μm Sn	Pass	Pass		
1μm Sn	Margin	Pass	Pass	
0.5μm Sn	Fail (nw)	Pass	Pass	

Dip-and-look test condition: Sn63Pb37, 245°C

In some of the component manufacturing, the component needs to be baked for removing the moisture. To simulate those processes, samples were heated for 2 hours at 175^{o}C before steam aging and solderability test. These results are summarized in table 3. Again, samples thicker than 2μm have passed solderability test. These results demonstrated that thin Sn films plated over a Ni-underlayer provide adequate solderability protection.

Table 3 - Dip-and-Look Test after 2h Aging at 175^{o}C and 8h steam Aging

	R type NA flux		R type MA flux	
	Bent area	Flat area	Bent area	Flat area
3μm Sn	Pass	Pass	Pass	Pass
2μm Sn	Pass	Pass	Pass	Pass
1μm Sn	Non-wetting	Pass	Non-wetting	Pass
0.5μm Sn	Non-wetting	Non-wetting	Non-wetting	Non-wetting

Dip-and-look test condition: Sn63Pb37, 245°C

Is It Cost Effective And Practical To Use Thin Sn Over Ni?

Traditionally, leadframes are plated with 8 to 15 μm Sn or SnPb for solderability and corrosion protection. A typical plating line set up is illustrated in Figure 8. To achieve the required Sn thickness; three plating tanks are typically needed.

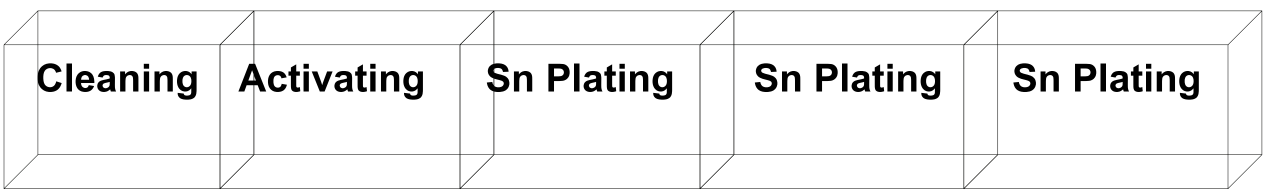

Figure 8 - Production line set up for traditional leadframe plating

If one uses Ni-underlayer for whisker reduction, an additional tank for Ni plating has to be added to the plating line, which requires extra floor space and longer plating time. This means an increased production and material cost as well as a decreased production throughput. However, for thin Sn over Ni, one can simply replace two Sn tanks with the Ni tank, since less than 1/3 of the traditional Sn thickness (`~10mm) is needed for the thin Sn technology (~2μm). This is illustrated in Figure9.

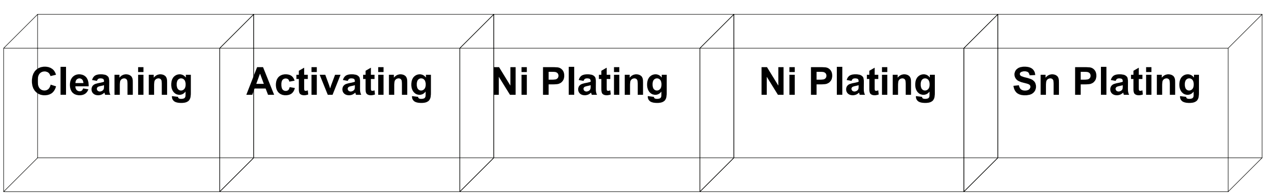

Figure 9 - Plating line set up for thin Sn over Ni technology

Clearly, thin Sn over Ni can be viewed as a drop-in replacement for the current SnPb. It provides superior whisker prevention, adequate solderability protection, reduced material cost and increase throughput.

IV Summary

The thermodynamic driving force for Sn whisker formation is compressive stress. The most effective strategy for eliminating whisker formation is to avoid the compressive stress. Both Ni-underlayer and post-plating bake effectively deal with the stress due to the intermetallic formation but provide no protection against thermal mechanical stress due to CTE mismatch. Thin Sn films (0.5 to 2□) plated over a Ni barrier layer utilizes the tensile stress generated in the Sn film to compensate the thermal mechanical stress generated due to the CTE mismatch and provides an effective means to deal with both stresses due to intermetallic formation and CTE mismatch. Furthermore, it can be viewed as a drop-in replacement for the current SnPb surface finishes at a reduced material and production cost.

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