Equalized Metal Distribution Will Improve High-Speed PCB Performance

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Abstract
During the design phase of a project, distribution of metal on the external layers of printed circuit boards is not a consideration. System designers concentrate on implementing the required logic. PCB designers have to satisfy many electrical and mechanical constraints and they do not lay out boards to provide an even distribution of metal on external layers. This creates a difficult problem for the fabricator, who tries to evenly plate a board with uneven metal distribution. In high-speed boards, uneven plating creates uneven impedance and circuit timing margins are decreased, negatively affecting a circuit board's performance.

In a plating tank, plating current is essentially constant across an entire panel being plated and all of the plating current must be absorbed. Pads and tracks in an area of a board with low metal density will be plated more than the same pads and tracks in an area of high metal density.

If a track originates in an area of high metal density and traverses an area of low metal density, its cross-section area will change due to uneven plating. A change in cross-section area will produce a change in impedance and part of a signal traveling along the track will be reflected. Reflections will cause a reduction in pulse amplitude, plus an increase in rise- and fall-times. This will reduce circuit timing margins and may be the difference between a high-speed board working or not working.

The best method of avoiding tracks with varying impedance is to equalize the metal distribution on external layers. Using statistical analysis, the mean metal distribution is computed and thieving only added to areas below the mean to bring them up to the mean. This provides a more even distribution of metal across a board, which will lead to better performance of high-speed boards. Equalized plating will also make a board flatter, improving assembly yields.

The Problem
The first step in designing a digital system is to develop logic equations to meet the system requirements. During the logic design phase, the emphasis is on implementing equations correctly. When a clock pulse occurs, pulses are assumed to change state instantaneously with zero rise- and fall-times. In a high-speed board, rise- and fall-times are very short but they are not zero.

Once the logic equations are correct, a PCB must run at the speed specified by its design.

We live in an analog world and digital circuitry converts an analog voltage into a 1 or 0. Digital circuitry has a band as shown in Figure 1. The height and width of the band depends on the circuitry. A voltage above the band at clock time is a solid one. Voltages below the band are a solid zero and voltages in the band are a maybe: they may be a 1 or they may be a 0.

Note: Drawings are not to scale. Artistic license has been taken to illustrate the concept.

Clock pulses propagate signals through digital circuitry. When a clock pulse occurs, outputs of logic elements are advanced to the input of the next logic elements as determined by the equations. When the clock pulse occurs, the voltage level for each signal is determined

For a signal going from 0 to 1, the timing margin is the amount of time from when the voltage level rises above the band, which means it is a solid 1, until the clock occurs, the light-blue line in Figure 2. The width of the red line represents the timing margin for this signal. The wider the circuit timing margins, the faster a board can run. When timing margins are too small, temperature, humidity, vibration, low battery voltage and other phenomena may cause pulses to slip from solid 1s and 0s to maybes. With boards running at a gigahertz and faster, it does not take much to degrade system performance.

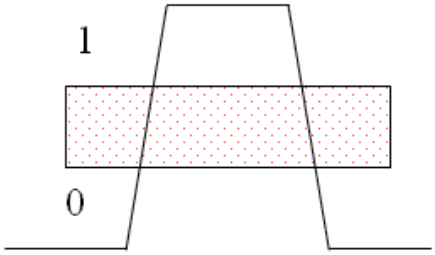

Figure 1 - Digital Circuitry with a Band

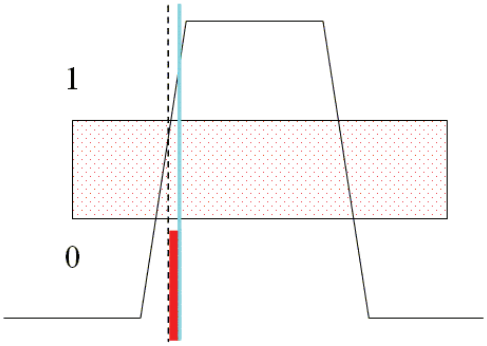

Figure 2 - Timing Margin is the Amount of Time from when the Voltage Level Rises Above the Band, the Clock Occurs, and a Light-blue Line Appears. The Width of the Red Line Represents the Timing Margin for This Signal

For maximum power transfer, the output impedance of the source circuit has to match the input impedance of the load. When the frequency is greater than 40 MHz, the board becomes a circuit element and tracks behave like transmission lines. Output impedance of the source must now equal the impedance of the board, which must equal the input impedance of the load. The impedance of a transmission line is comprised of resistance plus distributed inductance and capacitance and has characteristic impedance at its clock frequency.

Z = R + L + 1/C

Resistance is proportional to the length of a track and inversely proportional to the cross-section area of the track.

R = ρ x Length / Area

Where **ρ** is resistively and Area is cross-section area. When the cross-section area changes, the resistance changes, which changes the impedance. This will cause a portion of a signal to be reflected. Terminating resistors are widely used to correct impedance mismatches between a source and a load; however, terminating resistors are no help when a track itself has a change in impedance.

Figure 3 shows the input and output of a two-input AND gate. If both of the pulses are a 1 when the clock pulse occurs, the output is 1. One of the input signals originates on the same chip as the gate and the other signal travels across the board. As shown in Figure 4, the input to the track was a solid one, but as the signal travels across the board, it encountered a mismatch in impedance due a change in cross-section area, which was caused by an unevenly plated track. When it arrives at the gate, it is a maybe.

In a plating tank, plating current is essentially constant across an entire panel and must be high enough to plate the high density areas. The panel must absorb all of the plating current. Due to there being less metal to be plated, the portion of the track in the low-density area will have to absorb more plating current than the portion in the high-density area, resulting in changes in the cross-section of the track. As a pulse travels along this track (Figure 4) and encounters the change in impedance caused by the change in cross section area, a portion of the signal will be reflected, increasing its rise- and fall-times and decreasing the amplitude.

In Figure 5, when the clock pulse arrives, the signal OnChip is well above the band and is a definite one, as it was designed to be. The signal CrossBoard has not risen high enough to be a logical one. If the CrossBoard signal rises into the Maybe Band, sometimes there will be an output and sometimes not. This ambiguity is repeated with every other track that has a change in

cross-section area and the system's overall performance is degraded. This might mean a computer display is not as crisp as it could be, the range of a wireless device will not be as far, the system is more sensitive to low battery voltage, a missile will hit its target only 7 out of 10 times or maybe a collision warning radar occasionally misses a potential threat.

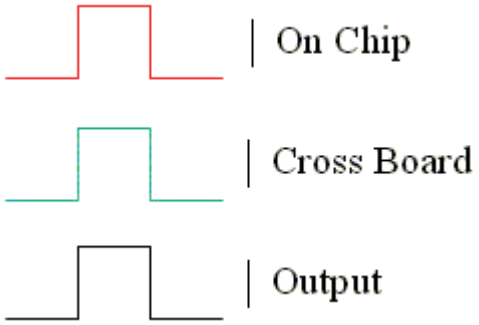

Figure 3 - Input and Output of a Two-input AND Gate

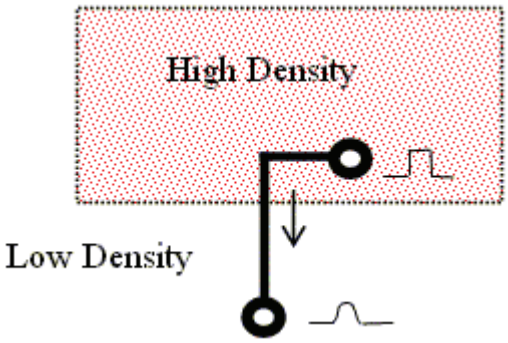

Figure 4 - The Input to the Track was a Solid One, but as the Signal Travels Across the Board, it Encountered a Mismatch in Impedance Due a Change in Cross-section Area. This was Caused by an Unevenly Plated Track.

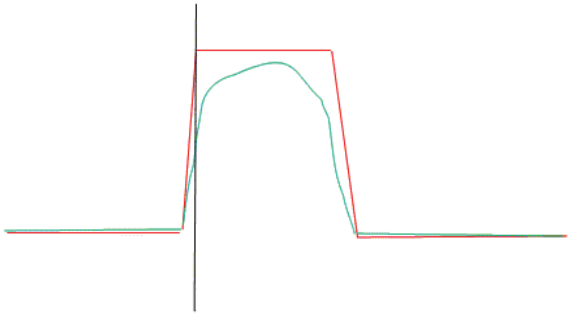

Figure 5 - When the Clock Pulse Arrives, the Signal OnChip is well above the Band and is a Definite one, as it was Designed to be

Solution

The solution is to post-process a design and equalize the metal distribution across the board. Statistical analysis is used to analyze a design and the mean metal distribution computed. Thieving, metal not part of the circuitry, is only added to areas whose density is below the mean to bring them up to the mean.

When a board is plated, the amount of plating is determined by the chemical bath, the amount of time the board is submerged in the tank and the level of plating current. To plate a panel, the current and time must be high enough to plate the areas of highest metal density. Figure 6 shows the top layer of a board and Figure 7 the density map for the top layer. The brighter the color, the higher the metal density.

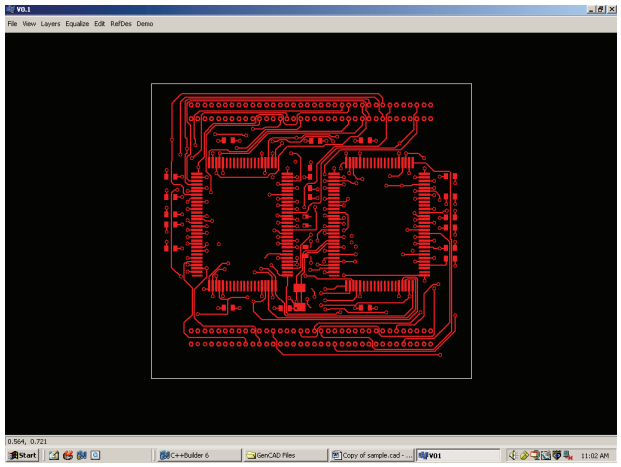

Figure 6

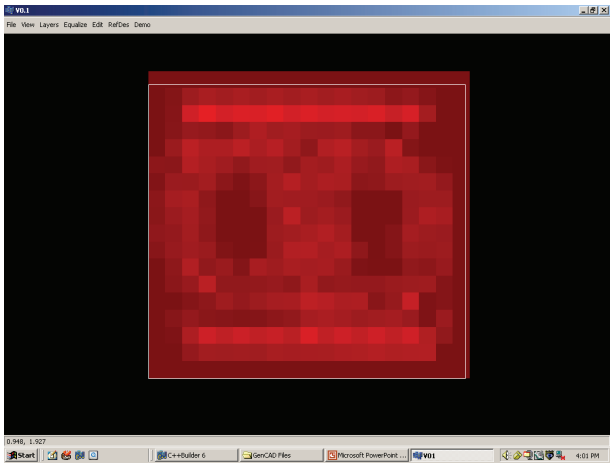

Figure 7

When the board shown in Figure 6 is plated, pads and tracks in the darker areas of the board will absorb more plating current than pads and tracks in the brighter areas. If a track traverses areas of varying density, its impedance will change due to the track's cross section changing.

Conclusion

It is difficult to design a printed circuit board that will run at or above a gigahertz and get it to work. As circuit speeds increase, things that didn't matter are now critical. Distribution of metal on the external layers of a printed circuit board is now an issue. Uneven metal distribution will lead to uneven plating, which leads to uneven impedance. Tracks whose impedance changes as a signal transits the track will cause reflections and reduce circuit timing margins.

Statistical analysis can determine the mean metal distribution of a board design. Adding thieving only to those areas of the board below the mean to bring them up to the mean will result in more even plating. This will lead to more even impedance which will lead to wider timing margins and improve the board's overall performance, allowing it to run faster.

Boards with even plating will also be flatter.