New Laminates for High Reliability Printed Circuit Boards

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Abstract
The challenges for today's PCBs are many, including higher assembly temperatures and higher device heat transfer temperatures; faster clock cycles and higher bandwidths; higher component density; lower noise margins and high current carrying requirements; while maintaining or improving cost/performance ratios and increasing assembly yields and field life.

This paper presents the work in Teradyne to characterize and qualify new printed circuit board ("PCB") dielectric substrates (a.k.a. "laminates") to meet the requirements of lead-free assembly, while providing more reliability and flexibility to design engineering. The paper provides details on: A) the drivers and the objectives of the program; B) some key properties of the laminates selected for testing; C) the tests and the results; and D) some discussion and conclusions.

Introduction
Challenges facing board design that are here now, or soon will be, include:

- A "Lead-free" assembly ("LFA") process that will be on average 30 to 40 °C higher than current eutectic soldering profiles; experimentation has shown that most of the currently available "standard" FR4s will not survive repeated exposures to these temperatures.

- A relatively new test, Thermal Decomposition Temperature (T_d), has been adopted in an attempt to correlate a laminate's response to heat to the reliability of the holes in that laminate after exposure to repeated, extreme temperatures. Does this new test predict LFA compatibility?

- New device packages are trending to finer hole-to-hole pitch, less than 1.0 mm, with smaller plated-through-holes (PTHs) required to route out of these devices. Experiments have shown that reduced spacing between hole walls can lead to Conductive Anodic Filament (CAF) growth failure; and there are ample studies of decreasing yields as aspect ratios increase, the by-product of smaller vias.

- At the same time, the lead count on fine pitch parts is remaining high or even increasing. Frequently the board height is fixed by the board to board pitch in the system. More I/O requires more route layers, but a fixed package height means that the distance between layers must shrink. Single-ply dielectric openings are now the norm.

- There is evidence, although not a library of reference results, that higher hole density in tight patches reduces some laminates' ability to withstand high soldering temperatures. This could be as a result of the increase in local "damage" by a high concentration of drill hits, or an increase in temperature transfer as a function of the sum of the via diameters introducing more heat to the center of the board in a small area, or both; alone or in combination with other effects – but the end result is that these high hole density regions are more susceptible to damage from thermal excursions.

- Reduced spacing between layers means that for the same impedance either the tracks need to shrink or the dielectric constant (E_r) of the material needs to be lower. Shrinking lines can be a problem for both fabrication yields, and for the application: too thin a line has higher resistance and greater loss. Lower Er materials which are reliable and cost competitive are highly desirable.

- Lower supply voltages and noise budgets require lower Power Distribution System (PDS) impedance. Thinner separations between power and ground reduce impedance and dampen resonances. Dielectric cores of 0.025 mm [0.001"] are now qualified and commercially available. Thinner dielectrics of 0.012 mm [0.0005"] are now in early pilot production.

- Higher bandwidths of 3 to 10+ Gbit/sec will require materials with lower dielectric loss (D_f; loss Tan) to reduce signal attenuation so that we can get a useful signal over the length of our boards. In addition, lower loss tangent reduces jitter. Again, materials for higher electrical performance which are reliable and cost competitive are highly desirable.
- The devices have faster clock rates and higher frequencies. A lower E_r material will minimize timing error by having a faster propagation delay.

- In general, the market requires ever improving quality and reliability, reduced cost and increased function in a fixed or shrinking volume (densification).

Our historical approach to laminate selection in Teradyne had been to rely on product engineering to identify and select materials for use in their PCBs. While those PCBAs were verified electrically in Design Verification Testing ("DVT"), the base materials had not had any reliability testing.

There had been no repository of test data for other engineering groups to leverage; and there were no formal controls to remove unsuitable materials from the design stream. On the other hand, this approach is fast, as it relies on laminators' statements of suitability and performance rather than on an extended build and qualification test process.

Unfortunately, as our designs had become more demanding, we had occasional problems in ramping some products to volume and also in field reliability.

- These problems were analyzed, and some were attributable to the laminate.
- There were occasions when the laminates, for one reason or another, could not be processed into the final construction desired, causing product delay while the board was redesigned around a laminate change.
- Last, there had been assemblies with a high occurrence of burning or charring after approximately 1 year in service.

After reviewing the material sets currently in use in Teradyne, we found the following deficiencies:

- They would not be compatible with lead free assembly processes; and/or
- They have limited design flexibility; and/or
- They are a single source solution; and/or
- They had not been qualified by reliability testing.

Our objective was to identify and qualify alternate materials that would provide:
- equal or better quality or cost than current materials while
- providing increased design options or
- improved printed circuit board performance at three design points.

Project Overview
We reviewed data sheets and technical brochures then selected materials which purported to deliver two or more of the following as compared to our current materials' suite:

A. Improved thermal performance for enhanced reliability after "Lead-Free" assembly processing;
B. Improved electrical performance, such as lower attenuation, or lower propagation delay, or lower inductance;
C. Improved reliability: longer PTH lifetime and/or lower CAF propensity;
D. Reduced total delivered cost;
E. Improved design flexibility or facilitation of increase in design densification.

New materials were selected for each of three performance points along with a "control" or baseline material from our current material set for each of these segments.

1. "Standard" high temperature epoxy laminates [Dk > 4.0]; [Df > .03]
2. High speed digital [Dk > 3.5 < 4.0]; [Df > 0.003 < 0.03]
3. Higher frequency and microwave [Dk < 3.5]; [Df <.003]

We also developed a qualification process and a Test Vehicle; the test plan, including the procedures, the sample sizes and testing service requirements etc.; and proposed the acceptability requirements.

The Materials
Some of the laminates selected for the first round of testing are listed it Figure 1**,** along with some key properties.

Material	Tg [°C]	Dk	Df
A	165	4.4	.015
B	170	4.1	.020
C	180	3.7	.008
D	200	3.7	.009
E	170	3.7	.010
F	170	3.9	.023
G	170	3.43	.010
H	193	3.7	.009
I	?	3.5	.005
J	280	3.48	.0037

Figure 1 - Laminates in Study - Tg, Dk, and Df values
As Listed on Respective Data Sheets, Where
Tg = Glass Transition Temperature;
Dk = Dielectric Constant;
Df = Dissipation Factor

The Test Vehicle
The test vehicle is a collection of coupons fully occupying the usable area of an 457 x 610 mm [18 x 24"] panel. The construction is 24 layers, of which 12 are plane layers. Signal layers are 17 micron [0.5 oz. copper/sq. ft.] and 35 micron [1.0 oz.]; plane layers are 17 micron, 35 micron, and 70 micron [2.0 oz. copper/sq.ft.]. There are single-ply and dual-ply prepreg fill sections; glass styles are 106 and 1080. The thinnest core is 0.075 mm [0.003"] nominally. The total overall thickness is 3.175 mm [0.125"] nominally. The smallest through drill is 0.025 mm [0.010"], with a drilled aspect ratio of approximately 12.5:1. The smallest blind via is 0.15 mm [0.006"], with an aspect ratio of approximately 0.5:1.

The Tests
The selected tests were chosen with an emphasis on reliability, especially suitability for and reliability after "Lead-Free" assembly process reflow cycles. LFAs, which have no lead in the solder paste, on the device lead, or on the circuit board, will need to be reflowed at temperatures higher than currently required for eutectic solder. The exact temperature will vary as determined by the selected paste composition and the mass of devices, but all the leading pastes in contention for LFA will require a 30 to 45 °C higher peak temperature.

Thermal Decomposition
A test called Thermal Decomposition Temperature (ASTM Title: "Standard Test Method for Rapid Thermal Degradation of Solid Electrical Insulating Materials by Thermo Gravimetric Analysis") is now being used in an attempt to quantify a measurable property of the laminate which would correlate with thermal stability at higher reflow temperatures. This test is a measure of the temperature at which 5 % weight loss occurs in the sample based on the weight after a 150 °C for 15 minute hold then a ramp to 800 °C at a rate of 5 °C/minute.

"The surface area of the test specimen will affect the results. If two specimens of the same material are tested, one with a large surface area and one with a small surface area, both of the same mass, the specimen with the smaller surface area will normally lose weight at a slower rate."[1]

Early studies indicate that laminates with T_d's below approximately 340 °C are not thermally robust at LFA process temperatures.[2]

Highly Accelerated Thermal Shock Test ("HATS")
Those materials with high Thermal Coefficients of Expansion (TCE) values in the z-axis combined with lower Glass Transition Temperatures (T_g; the temperature at which the epoxy becomes soft or fluid) will have a high rate of expansion of the material, especially at temperatures above the T_g of the laminate system. That expansion will stretch the copper plating on the hole walls; the more the hole expands and contracts under heating and cooling, the higher the failure rate of the hole from cracks in the copper initiated and then aggravated by the movement of the laminate. An example of the copper along a hole wall which was cracked by repeated high material expansion and contraction is shown in Figure 2.

To determine the propensity to fail after LFA processing, coupons (Figure 3) with daisy chained through vias (0.25 mm [0.010"]; 0.30 mm [0.012"]; and 0.35 mm [0.0135"]), and blind vias (0.15 mm [0.006"]) were subjected to either 0, 4 or 6 reflow cycles at 260 °C then monitored for resistance changes over 500 cycles at +145 °C to -40 °C air temperature (air-to-air

thermal cycle test). This test, called Highly Accelerated Thermal Shock, uses a single chamber (Figure 4**)** in which high volume hot and cold air alternately pass stationary samples, providing rapid thermal transfer. The samples are fixtured to a high-speed precision resistance sampling network, allowing continuous monitoring of the samples during the temperature cycles, commonly run to 500 cycles (although 1000 cycles or cycle-to-failure are also options).[3]

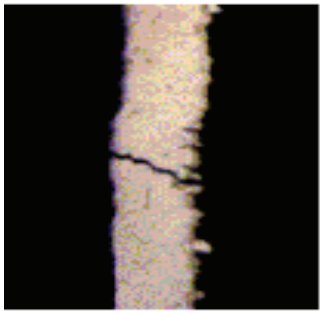

Figure 2 - Copper Along a Hole Wall which was Cracked by Repeated High Material Expansion and Contraction

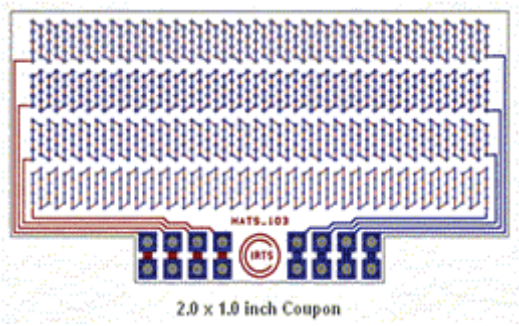

Figure 3 - HATS Coupon

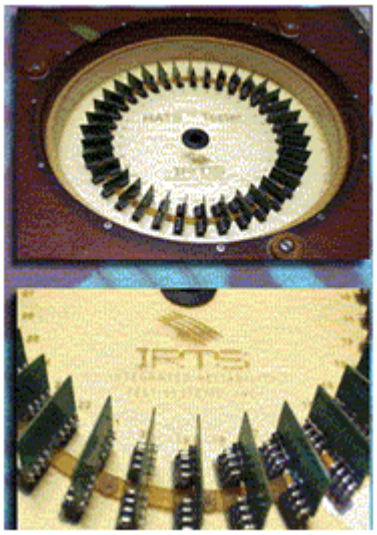

Figure 4 - HATS Test Head Loaded with Coupons (Top View and Close Angle)

Interconnect Stress Test (IST)

Another set of coupons (Figure 5) with daisy-chained 0.25 mm [0.010"] and 0.35 mm [0.0135"] drilled diameters was subjected to 0, 4 or 6 reflow cycles at 230 °C in the conditioning mode of the IST system then cycled from room temperature, ~ 25 °C, to +150 °C until failure [note: this is the "standard" IST test, not the higher temperature "Lead Free" processing conditioning and testing temperatures test recently derived (ref: 260 °C condition and "above Tg" for run time).

This test is an IPC approved accelerated stress test (IPC TM 650 Method 2.6.26) for the assessment of plated through holes and inner layer to PTH barrel connections. Current introduced into the hole initiates heat at the interface of the innerlayer to the copper barrel. The IST system continuously monitors the nets and records the relative changes in resistance of both the

barrel and the internal layer connections. The integrity of the interconnect can thereby be quantified by creating cyclic strain within the interconnect; this strain accelerates the inherent failure mechanisms that could cause the product to fail in the end use environment.[4]

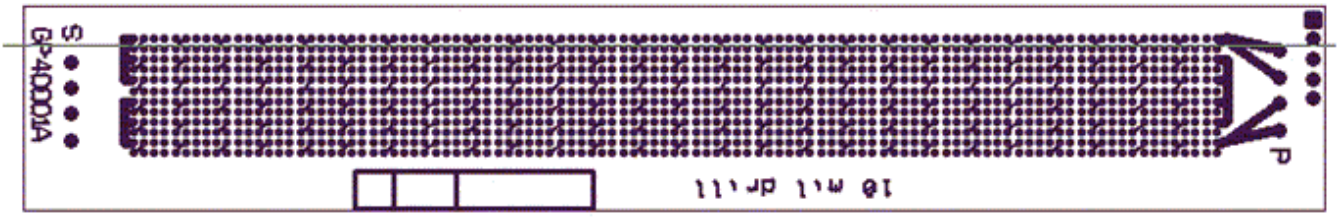

Figure 5 - IST Coupon

Conductive Anodic Filament (CAF) Resistance Test
A newer test, done more often today, is the Conductive Anodic Filament resistance test (IPC TM 650 Method 2.6.25). CAF is defined by this specification as: "the growth of metallic conductive salt filaments by means of an electrochemical migration process involving the transport of conductive chemistries across a nonmetallic substrate under the influence of an applied electric field, thus producing Conductive Anodic Filaments" (Figure 6). This test method provides a means to assess the propensity for CAF growth, a form of electrochemical migration within a printed wiring board.

The test sets up a bias between isolated elements in the design and then tests for leakage or shorting at 85 ± 2 °C [185 ± 3.6 ° F] and 87 +3/-2 % relative humidity. The test is commonly run to 500 hours under voltage and then stopped. The percent failure rate at 500 hours for each of the varying PTH-to-PTH in-line spaces are usually the results of interest. "Generally PWB processing has the greatest impact on reduced CAF resistance at smaller plated-through hole-to-plated-through hole (PTH-to-PTH) spacings, while the laminate material has the greatest impact at larger PTH-to-PTH spacings. However, the laminate material used can also affect the extent of fracturing and copper wicking near a PTH."[5]

We tested for CAF resistance between blind vas; between through-hole vias at decreasing hole-wall to hole-wall spacings; between planes, both through cores and through the prepregs between adjacent cores; and plated-through hole to copper plane across clearances. The test was run with 25 % of the samples at 10 V bias; 50 % at 48 V bias; and the remainder at 100 V bias.

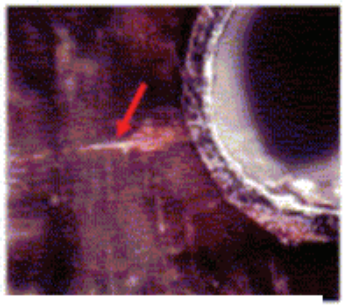

Figure 6 - CAF(Photo Courtesy ofArlon Co.)

Other Tests
Other tests performed for this investigation are listed below. "IPC TM 650" is the IPC Test Methods Manual; the Method x.x.xx is the specific test; the description of the test is a synopsis of the language from the Scope section of the Method.

- "T260 minutes" (IPC TM 650 Method 2.4.24.1) This test determines the time to delamination of laminates and printed boards through the use of a thermo mechanical analyzer (TMA; measures dimensional change within a thermal range). The time to delamination is defined as the time from the onset of the isotherm to failure, which is any event or deviation of the data plot where the thickness is shown to have irreversibly changed. The isotherm temperature is 260 ° C.

- "T288 minutes" (IPC TM 650 Method 2.4.24.1): The isotherm temperature is 288 °C.

- D_k @ 1.0 GHz (IPC TM 650 Method 2.5.5.9): This test determines the permittivity (dielectric constant or E_r) of printed wiring materials at various frequencies from 1.0 MHz to 1.5 GHz using a using a narrow sweep of frequency around the target or desired frequency. The test method is built around the capability of currently available materials analyzers,

which use a capacitance method to determine permittivity, such as the Hewlett-Packard Impedance Material Analyzer, model 4291A, or equivalent. (This test method is not intended for low loss materials).

- D_f @ 1.0 GHz (IPC TM 650 Method 2.5.5.9): same as D_k.

- T_g by TMA (IPC TM 650 Method 2.4.24): This test is designed to determine the Glass Transition Temperature of the dielectric material by use of Thermal Mechanical Analysis.

- Dielectric Withstanding Voltage (IPC TM 650 Method 2.5.7 @ 500 V {a.k.a.: HiPot}): This test consists of the application of a voltage higher than the rated voltage for a specific time between mutually isolated portions of a PWB or between isolated portions and ground; used to prove that the PWB can operate safely at its rated voltage and withstand momentary over potentials due to switching, surges and other similar phenomena.

- Copper Peel Strength (IPC TM 650 Method 2.4.8 Conditions A, B and C): This test is designed to determine the peel strength (in units per square area; i.e.: lbs./sq.in.) of the metal cladding to the base laminate in the following conditions: "as received", after thermal stress, and after exposure to processing chemicals; also to evaluate the base laminate for obvious degradation after test.

- Solder Floats (IPC TM 650 Method 2.6.8 (3 x @ 288 °C) and (6 x @ 288 °C) and (3 x @ 260 °C) and (3 x @ 260 °C): This test is designed to determine the thermal integrity of laminates using exposure to solder.

- Microsection PTH Quality Evaluation to IPC 6012 B: Qualification and Performance Specification for Rigid Printed Boards. The evaluation of the plating integrity, laminate integrity, quality and workmanship (e.g.: drilling; registration) of the plated through hole in the laminated and plated board.

Experimental Results

A word of caution regarding the results: many of these materials were manufactured well over a year ago given the lag time between designing the project, developing the test vehicle, ordering and building the materials, and running the testing. Tests such as CAF take about 6 weeks when shipping and queue is added to the actual test time; the CAF testing was run somewhat in parallel in that we could get up to 3 materials tested at one time; after that they had to queue for the next opening. Most of the testing was completed by or before August 2005. The data took some time to analyze and summarize; and that step finished in September-October of 2005. The deadline for this paper was October 31, 2005.

At least a few of these materials have seen changes from their original introduction. The test results provided ample information for a feedback loop for improvement, in addition to any other data which the laminators were also collecting simultaneously. These data are still a valid indication that perfecting laminates for LFA is in the early stages, and that most if not all the available laminates have room for improvement. In addition, the data points to areas for further investigation which would hopefully enhance our industry's understanding of the mechanisms involved in the development of the different failure modes, and suggest changes to eliminate or mitigate those weaknesses.

The initial plan was for 12 materials to start into the project: 4 in the first category (low end), 5 in the second (mid range), and 3 in the third category (high end, very low loss). Twelve sets of materials were ordered and started; 3 did not make it through PCB fabrication having problems with either lamination or drilling. Two of the 3 were restarted (one of them multiple times) and the effort on one of those 3 was discontinued. Nine materials moved into the testing phase. Of those 9, only 8 were tested as 1 was found to be badly delaminated and not worth the cost to test. We therefore had results on 8 materials. One of the 8 tested had serious problems and replacement material was provided. That replacement material was put on a "fast track" to catch up, and so we had two sets of data on that material: a "before" and an "after the changes" data set. That material may be shown with "before" or "after" or both data; the section will indicate which value is shown.

T_g, D_k, D_f Results

The measured values are recorded in Figure 7, alongside the data sheet values; where the box is blank, that test not yet been done on that material. A couple of observations can be made: actual T_g value can be different by as much as 9 degrees from the data sheet, or approximately 5.5 %; however, as a group, the average difference is ± 6 degrees or approximately 3.5 %.

D_k and D_f measured values tend to differ quite a bit from the manufacturer's data sheets; and, at least in this study, are less than stated. We speculate that the principal reason for the difference is that the bare laminate test specimen is not representative of a multilayer board. The usual laminate specimen, as described in the test method, is 1.0 mm (0.039") thick, and so is usually made from "thick" glass styles with a low percentage of resin. These tests were done on a 3.175 mm, 22 layer, PCB having many sections of resin-rich "106" and "1080" glass fabrics.

The measured data is labeled "Effective D_k" (Eff D_k) and "Effective D_f" (Eff D_f). When fabricators calculate impedance; their models are based on empirical readings not the specification sheet values, hence the term "effective".

	Laminators' Data			Measured Data		
Material	T_g	D_k	D_f	T_g	Eff D_k	Eff D_f
A	170	4.4	.015	177	3.99	.014
B	170	4.1	.020	174	3.7	.013
C	180	3.7	.008	178	3.32	.006
D	200	3.7	.009	201	3.43	.006
E	170	3.7	.010	178	3.53	.006
F	170	3.9	.023	161	3.75	.019
G	170	3.85	.015	163	3.43	.010
H	193	3.7	.009	188	3.36	.006
I	200	3.5	.005			
J	280	3.48	.0037			

Figure 7 - Measured Data and Spec Data

T_d, T260, T288

Figure 8 shows the T_d, T260 and T288 data; together these ought to provide a basis to predict the laminates' thermal stability at the higher temperatures of LFA processing. Correlation data is still minimal, but early studies indicate that a material should have a T_d of at least 340 °C [4] and the "higher the T288" the better.

A couple of words are in order regarding the thermal stability test results. First, the specification sheet data is not listed, as was the case for the T_g, D_k, and D_f for principally two reasons: 1) not every laminate reported each of these values, and 2) there was not good correlation.

The other concern was the apparent lack of correlation between the TMA and the TGA data for each laminate. See Figure 9 for a chart illustrating the concern. We had anticipated that laminates that had high T288 values (TMA testing) would also have high T_d values (TGA testing) – but they don't, or at least, not in this test. Looking into the tests further, and after discussion with some laminators, we decided that there was not enough standardization in either setup of the test and/or interpretation of the results, especially for TMA. The thickness and composition of the sample is a variable; e.g.: an 0.71 mm [0.028"] core that is 54 % resin, vs. a 3.175 mm [0.125"] multilayer which is 65 % resin. The following is taken directly from IPC-650 TM Method 2.4.24.1 Subject, Time to Delamination (TMA Method): *"5.3 Evaluation - The time to delamination is determined as the time from the onset of the isotherm to failure. Failure is any event or deviation of the data plot where the thickness is shown to have irreversibly changed. ... Report the Time to Delamination as determined in 5.3. Report the time at which any other plot event has taken place which was not determined to be irreversible."*

The same material, from the same build lot, tested one day apart was reported at 8.9 minutes and 41.2 minutes – determining the occurrence of an "irreversible" event is very subjective as the indication of an "event" tends to be more subtle than the example chart in the test method would suggest.

For T_d by TGA, the following is taken from IPC-TM 650 Method 2.3.40 Subject, Thermal Stability, *"Scope: This test method establishes a procedure for determining the thermal decomposition temperature of organic films using thermo gravimetric analysis (TGA). Samples may vary nominally between 2 and 20 mg.* And: *The surface area of the test specimen will affect the results. If two specimens of the same material are tested, one with a large surface area and one with a small surface area, both of the same mass, the specimen with the smaller surface area will normally lose weight at a slower rate*. Then: *Record the temperature at which 5 % additional weight loss occurs based on the weight after the 150 °C hold.*"

The reported 5 % weight loss can occur rapidly after the onset of weight loss or slowly. The temperature, at which weight change first occurs, onset, can also be quite different between materials. It is important to see the thermal plots, not just be given the 5 % temperature. The 5 % might occur at approximately the same temperature for two laminates, but if one material's onset to change is at a lower temperature will it incur more damage with each reflow cycle? There is still more work to be done to standardize T_d testing and to correlate values to real-world results.

	Measured Data		
Material	T_d (°C)	T260 (mins)	T288 (mins)
A	?	14.38	1.34
B	379	16.12	1.3
C	362	17.5	1.28
D	376	27.5	1.92
E	354	29.5	4.36
F	346	30.9	17.4
G	353	60	21.4
H	334	54.9	23
I			
J			

Figure 8 - Thermal Stability Data

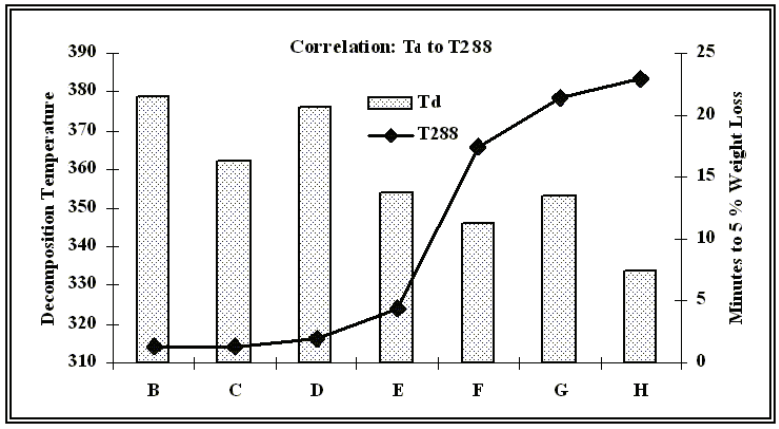

Figure 9 - Thermal Stability Test Correlation

Hats

Highly Accelerated Thermal Shock test results were mostly as expected, but with one surprising finding. Some materials appeared to be more reliable than others after multiple exposures to high temperatures, with reliability interpreted as an increasing number of cycles to failure. Via size and type seemed to impact the number of cycles to failure, although not dramatically. What was surprising is that the number of thermal preconditioning cycles corresponding to lead-free assembly cycles showed less effect than anticipated.

In Figure 10, from left to right, are the materials' average cycles to failure after 1 cycle at 215 °C, 4 cycles at 260 °C, and 6 cycles at 260 °C. As can be seen, there is not an obvious or large degradation based on preconditioning. Since all the materials involved in this investigation were self-described as "Lead-Free Process Compatible" (or "Capable"), one explanation might be that they have a flat response to temperatures up to 260 °C for up to 6 exposures – suggesting that either they can or can't make it to this target. This aspect is intriguing and would suggest further study, for instance: increasing reflow cycles until each material starts to show decreasing cycles with increasing reflows; and/or increasing reflow temperature as an input to differentiate the materials at a constant number of cycles.

Figure 11 shows the Average of Cycles for each material by each via size and type: 0.15 mm blind [0.006"]; also 0.25 mm [0.010"], 0.30 mm [0.012"], and 0.35 mm [0.0135"] through vias. Blind microvias are particularly robust, in general, going to 500 cycles for all materials. The two materials where the blind vias averaged approximately 300 cycles exhibited other fabrication effects which could account for those lower cycles to failure numbers.

There is some general lowering of cycles to failure by decreasing via size, but not that dramatic. The very low, 113, cycles for the 0.25 mm through via on material "G" is thought to be a fabrication induced weakness, since that material did not show a tendency to significantly lower (or even lower at all) cycles from 0.35 mm to 0.30 mm.

There was one material standout – "H" went 500 cycles for all via sizes and all reflow conditions (see the top most bar for 0.25 mm [0.010"] hole); and there were 2 extremely good materials, "D" and "A", which were close to but not quite "perfect" (see 2 right hand bars on every run). In all, 6 of the 8 materials could pass 300 HATS cycles for all holes and all preconditions.

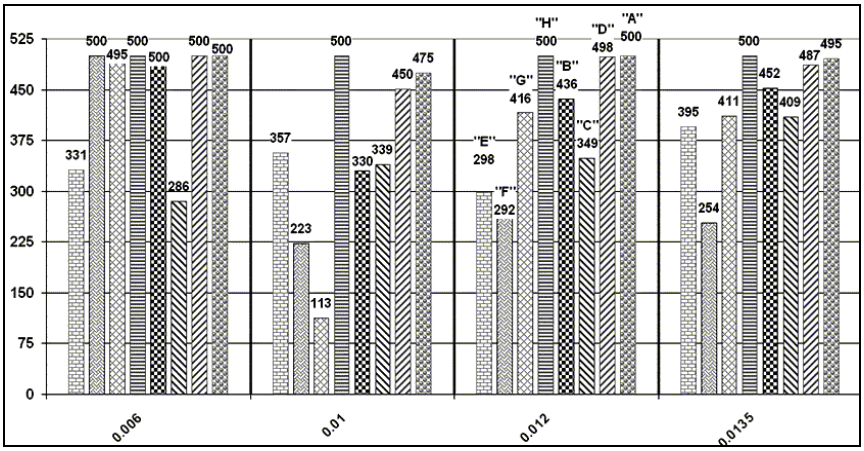

Figure 10 – Average of HATS Cycles for Each Material by Preconditioning for all Vias

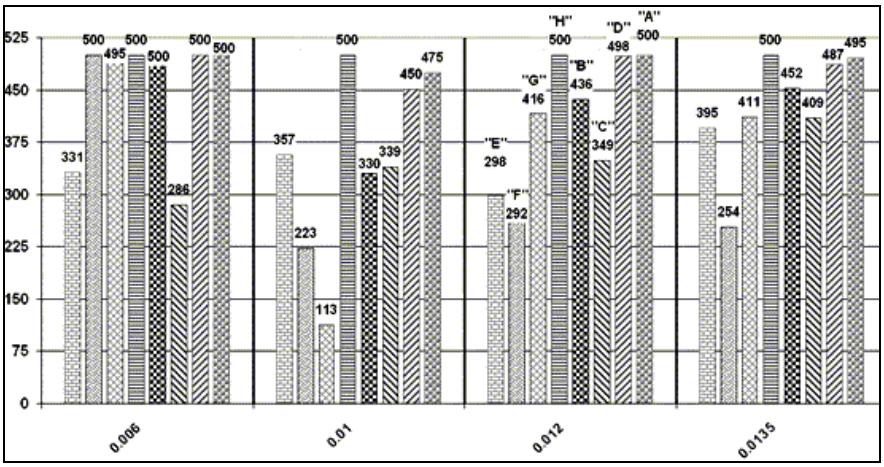

Figure 11 – Average of HATS Cycles for Each Material by Via Size for all Preconditions

IST

Interconnect Stress Testing is comparable to air-to-air thermal (chamber/oven) shock (IPC TM 650 Method 2.6.7: Thermal Shock and Continuity Test). Since it is current induced strain, it is particularly sensitive to failures due to copper plating and adhesion, in addition to the expansion characteristics of the laminate. The coupon is monitored at "Power" and "Signal" connections. Signal failures can be barrel cracking or innerlayer separation (separation between the edge of the copper foil and the copper barrel); failures at Power are usually attributable to processing and not material characteristics. Figure 12 shows the Average and Standard Deviation for all the materials which were IST tested. There is clear differentiation between these materials. There is no industry-wide accepted number of cycles that is considered passing for IST; that number can and does vary OEM to OEM and even design to design. Usually, however, 300 cycles after preconditioning is considered acceptable.

Note that the laminate second from the right, while having a good number of cycles, has a very high and unacceptable standard deviation. Like all of these reliability tests on finished product, it can sometimes be difficult to assign cause; however whenever there is a non-bell shape response, there are usually secondary factors contributing to the second curve. Each of these materials was analyzed for response as a function of reflow preconditioning cycles, and some example plots are shown in Figures 14 to 16. In the plot in Figure 13 the 4 low readings that are circled are all at Power connections. After 4 conditioning cycles 3 coupons went all 1000 cycles while 1 coupon failed at 253 cycles; after 6 conditioning cycles 2

coupons went all 1000 cycles while 2 coupons failed at 84 and 36 cycles. If we attribute those failures to sample processing and not inherent material capability (or all the samples would have consistent failure response rates), then the mean cycles to failure for that material would improve from 713 to 982; and the standard deviation would improve from 415 to 43.

This is the material mentioned in Section 5.0, which was built and tested twice. The second time the IST results were: 1000 average cycles (100 % passing) and 0 cycles standard deviation (100 % passing).

A few materials showed relatively little response to the number of preconditioning reflow passes, while one material in particular showed a clear weakening of the material with increasing reflows. The solid line in the plots in Figures 14 to 16 is the trend line for all the "maximum number of cycles" by via size and preconditioning cycles.

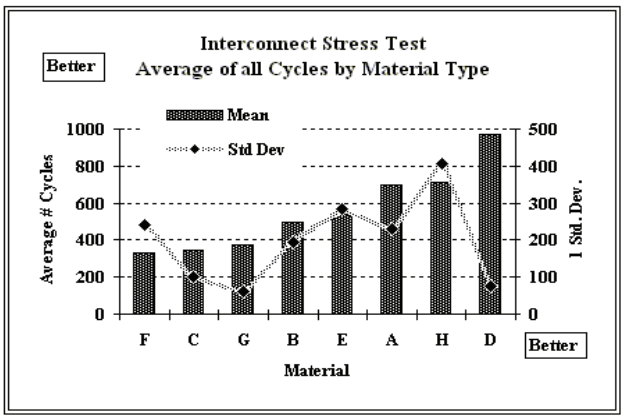

Figure 12 - IST Mean Cycles & S.D. for All Conditions by Material

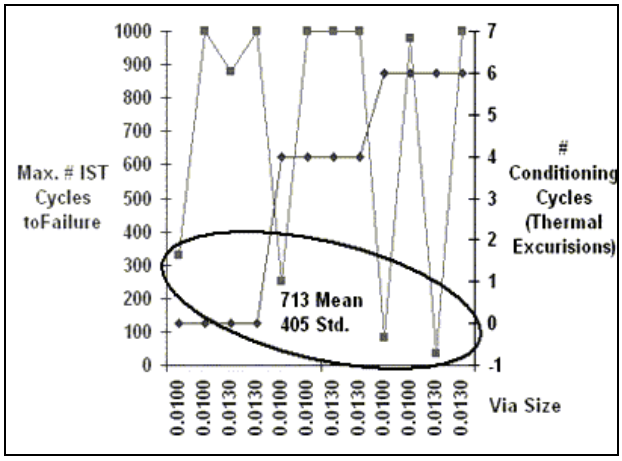

Figure 13 - Material "H" Showing Bimodal Response, not Reflow Dependent

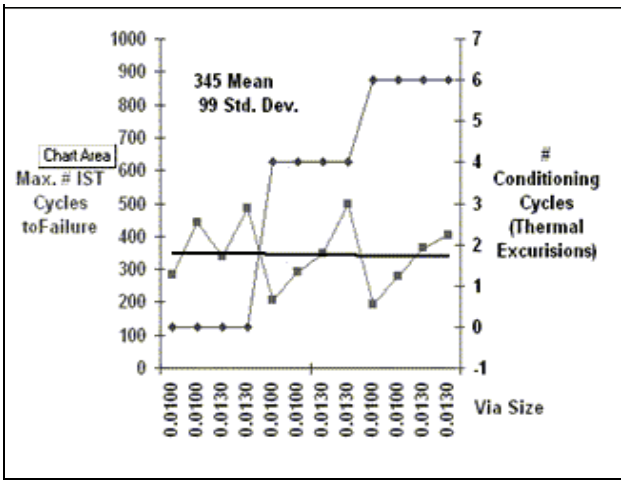

Figure 14 - IST results for "C"

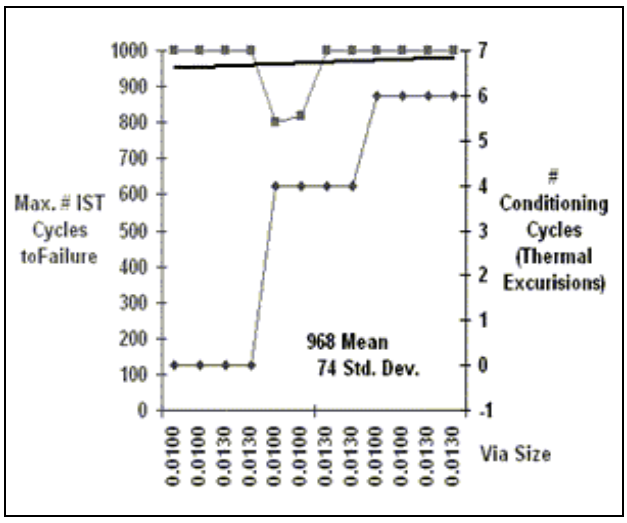

Figure 15 - IST results for "D"

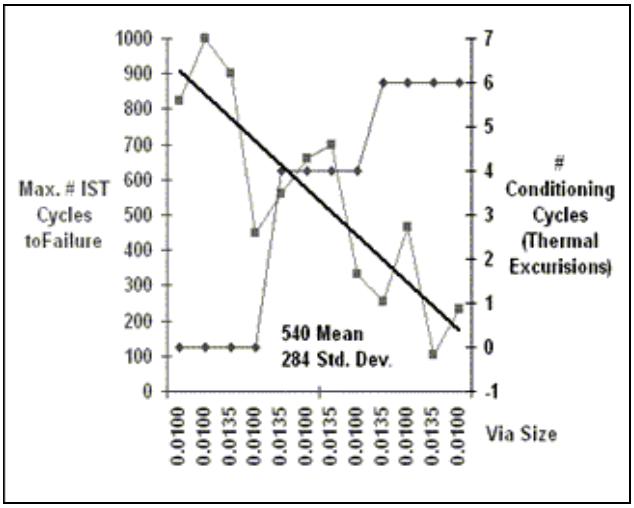

Figure 16 - IST results for "E"

CAF

Conductive Anodic Filament Formation Test is another fairly new test, only recently standardized. This is Teradyne's second foray into a major CAF test undertaking, so we have some background in the limitations and interpretation of the data. There is a growing list of studies with data on CAF results; however there is not yet enough information to make valid comparisons

between tests or to predict test outcomes. Also, results should always be analyzed before conclusions drawn because CAF testing is susceptible to false fails due to extraneous factors. Prominent trends, however, yield useful information.

Blind Microvia CAF - We tested Blind Microvia Wall-to-Wall with a 0.10 mm [0.004"] via in a 0.25 mm [0.010"] pad. Distance varied from 0.25 mm [0.010"] to 0.41 mm [0.016"]. For each material we tested 640 microvia to microvia spaces; a total of 5,120 spaces for the 8 materials.

Laser-formed microvias were far less likely to grow CAF, in this test, than through-the-board vias. There were no failures at 0.35 mm [.014"] or greater spacing at any voltage; 1 material had 1 coupon fail at 0.30 mm [.012"] separation and 48 volts; and 4 materials (of 8) had 2 coupons fail at 0.28 mm [.011"] separation and 100 volts.

Z-axis Plane-to-Plane CAF - For plane-to-plane CAF testing we had 23 dielectric spaces tested per board times 8 boards, so 184 Z-axis tests for each material; a total of 1,472 Z-axis tests for the 8 material sets. Twenty-five percent were tested at 10 volts; 50 % were tested at 48 volts; the remaining 25 % of structures were tested at 100 volts.

There were 3 failures: one material at Layer 1 to Layer 2 at 48 V after 500 hours; and two for another material also for Layer 1 to Layer 2: one after 144 hours at 48 V and the other after 264 hours at 100 V. Since Layer 1 is involved, it is possible that the failure is not due to CAF, but to surface insulation resistance breakdown. If there were residues on the surface after attaching the connections, those may have grown a filament. The CAF coupon is specified as “without soldermask”, so that is a distinct possibility. Since Layer 24 to layer 23 is the same as Layer 1 to 2, we should expect to see some failures across that dielectric if the spacing and the single ply of prepreg were the root cause of the CAF; but all the failures had Layer 1 in common, and Layer 1 is where the connection is soldered, a special cause, so we concluded that layer-to-layer CAF is effectively non-existent.

PTH to Plane CAF -Figure 17 is a depiction of the PTH-Wall-to-Copper Plane CAF coupon.[6] Using an ohm meter the technician determines the first hole in the series which is not shorted to the plane; this hole is the “first hole”. The “first hole” is determined for every coupon, effectively negating misregistration, or “zeroing” the coupon. The clearances tested were “first hole” plus 0.076 mm [0.003"], “first hole” plus 0.10 mm [0.004"], and “first hole” plus 0.127 mm [0.005"] for 3 layers; in addition, for one of those layers, the test included “first hole” plus 0.15 mm [0.006"] and “first hole” plus 0.178 mm [0.007"]. Example: if a coupon was shorted at the 0.81 mm [0.032"] clearance but not the 0.84 mm [0.033"] clearance, then that coupon would be wired to test the 0.91 mm [.036"] (“first hole” + 0.003"), the 0.94 mm [0.037"], and the 0.97 mm [0.038"], possibly up 1.02 mm [to 0.040"]. For each material there were 88 PTH to Plane CAF tests; 22 were run at 10 V, 44 at 48 V, and 22 at 100 V.

This test was interesting in that clear differentiation between conditions, both distance and voltage, and materials was seen. One obvious purpose of such a test was to determine if we could “shrink” clearance sizes without compromising reliability, assuming that registration or “no breakout” could be maintained. These clearances tested are smaller than we typically use. The data show that to reduce the clearances would potentially introduce more risk to the design. The data is by clearance size, so annular ring is ½ the value. The materials are, from left to right: F, G, E, H, B, C, D, A. See Figures 18 – 20.

The data indicates that CAF formation in this structure has a dependency on both the material and the voltage. All of the materials were CAF free at 0.15 mm [0.006"] and 0.178 mm [0.007"] up to and including 48 V; at 100 V two materials were failing even at 0.15 and 0.178 mm. Once the clearance size was reduced to 0.10 mm most of the materials are capable at low, 10 V, voltage – 50 % are 100 % passing and 50 % are 80 % passing; but once voltage increases to 48 V, only 1 material is still 100 % passing, two are approaching only 60 % pass rate, and one is down to almost 40 %. But even at only 0.076 mm clearance if the voltage is held to 48 V, most of the materials fair pretty well, although 1 material is clearly in trouble. Increasing the voltage to 100 V while keeping the clearance constant at 0.076 mm drops all but two materials to 50 % or less.

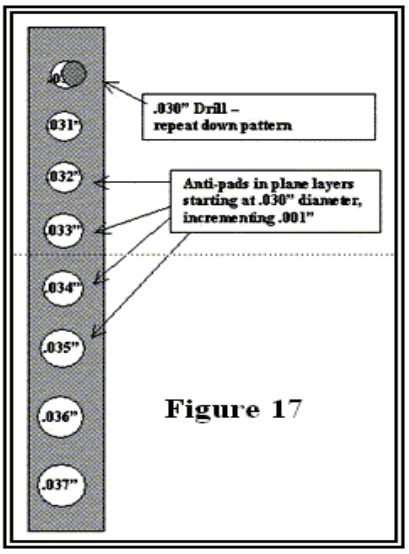

Figure 17 - A Depiction of the PTH-Wall-to-Copper Plane CAF Coupon

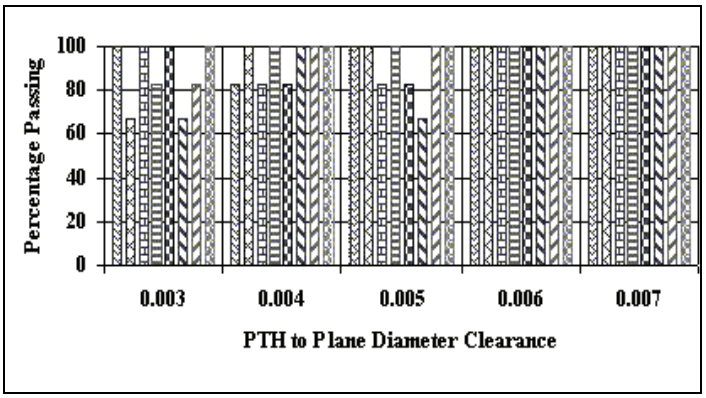

Figure 18 – CAF Results at 10V

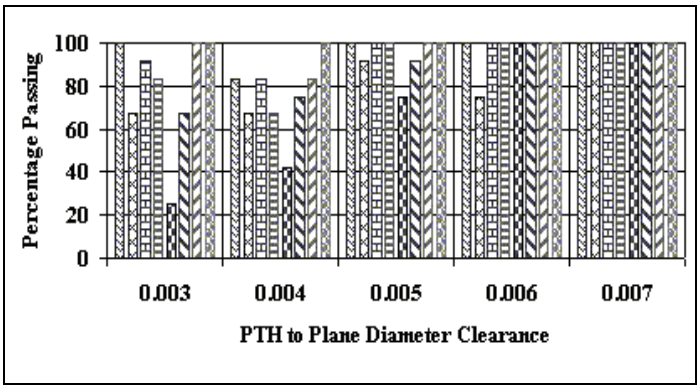

Figure 19 – CAF Results at 48V

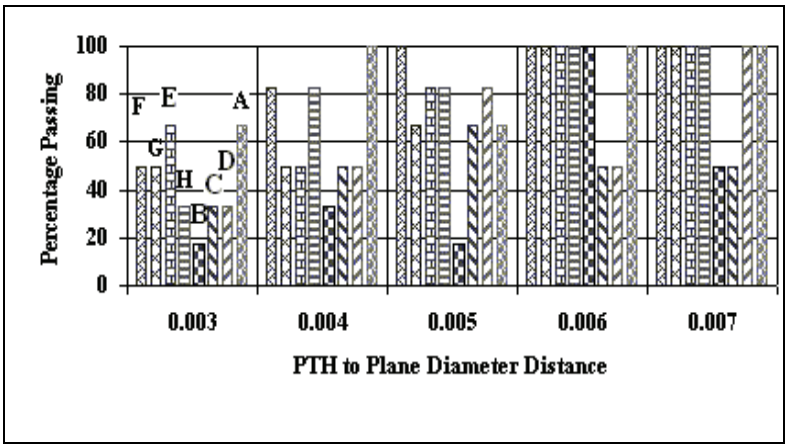

Figure 20 – CAF Results at 100V

PTH-to-PTH CAF – For PTH-hole-wall to PTH-hole-wall CAF we placed identical coupons parallel to the length of the panel and an equal number perpendicular to the length of the panel. Within the coupon area were a series of daisy-chained vias; the drill size was 0.89 mm [0.035"], finishing at 0.76 mm [0.030"], in a 1.02 mm [0.040"] diameter pad. The hole wall-to-wall spacing varied from 0.30 mm [0.012"] to 0.635 mm [0.025"]. Each chain had 20 PTHs; there were 64 chains per material, for a total of 1,280 spacings tested per material. A response by decreasing space and by increasing voltage was expected, and the data does show susceptibility to CAF based on space and voltage. Also, for at least one material, a strong response was seen between orientation of the daisy chain to the panel and CAF fails.

For CAF testing the first step in the procedure is to precondition the boards by soaking at temperature and humidity prior to the application of voltage. Immediately after the soak and prior to the initiation of the test voltage, the resistance of each daisy chain is taken at 100 V and logged as the "starting" resistance.

In the setup a 10^6 ohm current limiting resistor is wired in series with each current path (if not otherwise built into the test system). When a "net" reads 10^6 ohms that is actually a reading of the resistor and not the net. Once a net reads 10^6 it is considered "failed". If the first reading of the net after preconditioning and prior to steady state application of voltage is 10^6, that net is "excluded" from the test population.

We found a very high percent of nets "excluded" from the population which went on to test at voltage; that is to say, that a very high percent of nets were already "bad" as soon as current was applied. These "Excluded" nets tended to increase with increasing difficulty of the structure, which is to say, as spacing decreased. Some materials had more Excluded nets than the others.

Another observation was the large number of nets that failed within 100 hours of the application of voltage; these mostly occurred at the smaller spacings; and, some materials were more prone to these "Early Fails" than others.

A third observation is the influence of orientation of the nets to the panel: nets parallel to the vertical grain of the panel as opposed to identical nets perpendicular to the vertical grain of the panel. "Orientation" (where "vertical" is parallel to the grain and "horizontal" is perpendicular to the grain) impacted not only Passing nets, but also Excluded and Early Fails. Where Orientation seemed to be most pronounced, it was an effect for of all the laminates in a Manufacturer's line up.

These results occasioned a lot of discussion with Laminators, and there are theories and there is work in progress to mitigate or eliminate these effects; but at the time of this writing, these data still stand and the root cause(s) and corrective actions have not yet been validated. Review Figure 21: the upper right hand graph is all Nets passing in the Horizontal Orientation. Note that there is 100 % passing for 0.635 mm [0.025"], 0.56 mm [.022"], 0.51 mm [.020"] spaces; at 0.46 mm [.018"] spacing and below the percentage passing falls off, until only one material passes only 66 % at 0.25 mm [.010"] spacing. (Note: given that the population of nets was different for each segment, the data were calculated as percentages of the total of nets in that segment).

Next look at the upper left hand chart, Nets Passing in the Vertical Orientation: there are far fewer passing nets, instead those nets can be found some in the Failing group, but an equally large number in the Excluded group. The Excluded group in the Vertical Orientation is a far greater proportion of the population than the Excluded group in the Horizontal Orientation.

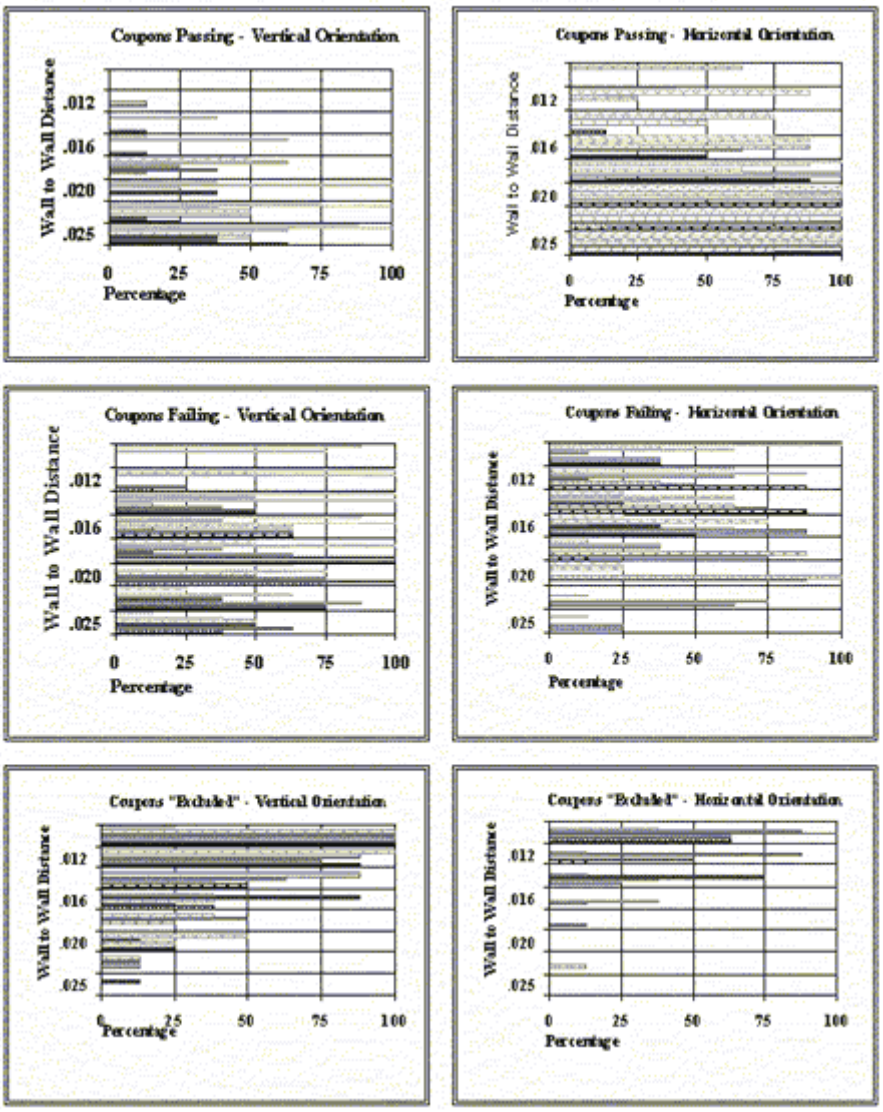

Figure 21 – Nets Passing in Vertical/Horizontal Orientation, Nets Failing in Vertical/Horizontal Orientation, Nets Excluded in Vertical/Horizontal Orientation

These results were further exploded by separating materials into spaces and orientation, as shown in representative graphs in Figure 22. This is the same material at the same voltage at the same spacing with Orientation as the only variable. This pattern was repeated over and over for all spaces. As spaces got below 0.46mm [.018"], orientation alone was no longer the dominant effect. All materials show at least some orientation effect, the difference being that this material, shown, was nearly perfect in one axis – an overwhelming majority of the fails were in the Vertical orientation. For some of the other materials, the Vertical was worse than the Horizontal but not to such a extreme.

One material was notable in that both Vertical *and* Horizontal nets (Figure 23) Passed down to 0.51 mm [.020"] spacing.

Figure 24 is an example of the typical response for PTH-to-PTH CAF seen in this experiment. Note the large number of Early Fails after less than 100 hours at voltage.

(Note: Resistance measurements are not continuous; the coupons are pulled from the chamber and tested at 100 V, regardless of test input voltage, approximately every 100 hours; therefore, a failure showing at between 264-288 hours could have occurred any time after the 144-168 hours' check; that the hours at which the resistance was checked ranges between 2 times is not significant - it is an artifice of when the technician was able to take the readings at or close to every 100 hours.)

Figure 25 is a material with a large number of Excluded (circled at 96 hours), a large number of Early Fails (circled at 144-168 hours), and then some fails as time progressed; by the end of 500 hours at voltage there are very few nets that have passed (circled at 596 to 600 hours). The last example is Figure 26 which shows a material with a few Excluded nets, very

few Early Fails, and a large number of Passing nets. So, clearly there are major differences in susceptibility to CAF between the materials, at least as recorded in this experiment. Since one material did very well, it was possible to do well in this test.

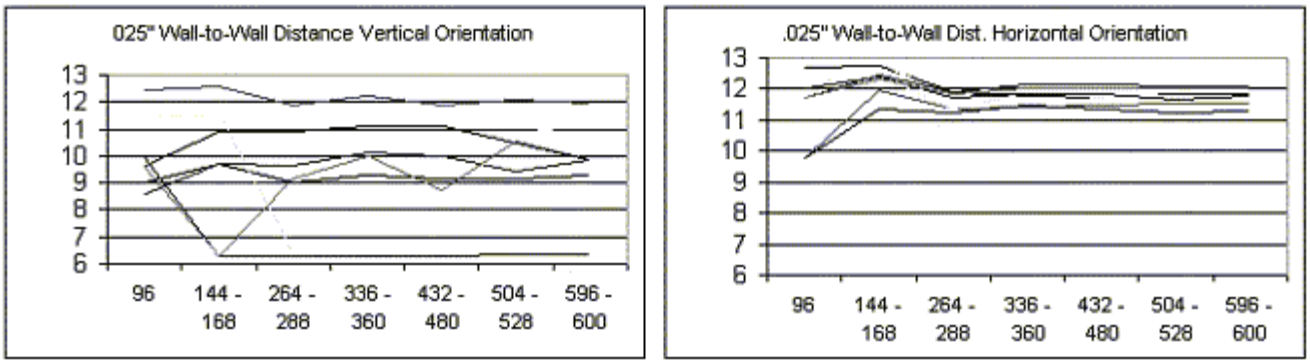

Figure 22 - Separating Materials into Spaces and Orientation

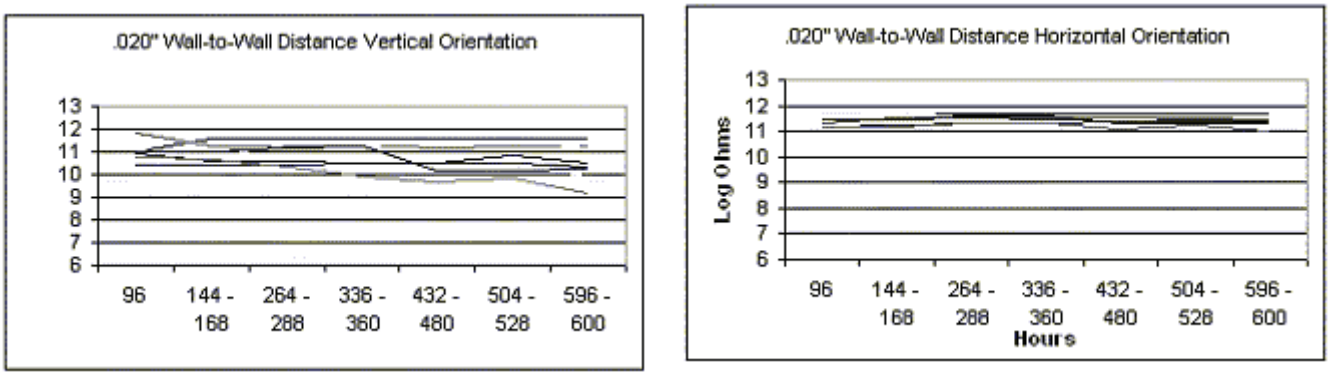

Figure 23 – Both Vertical *and* Horizontal Nets Passed Down to 0.51 mm [.020"] Spacing

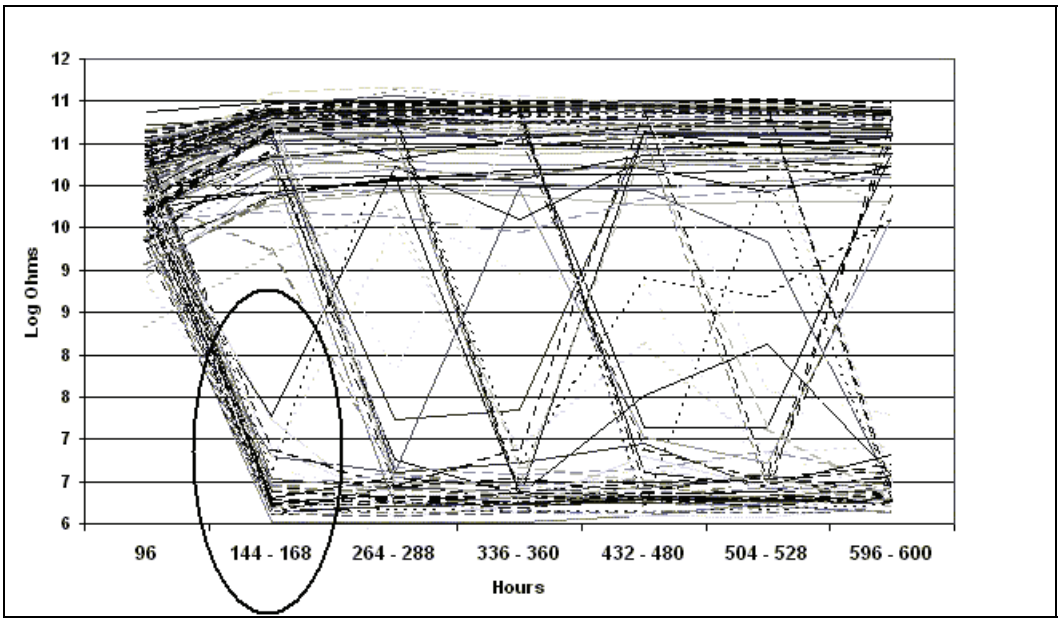

Figure 24 – PTH to PTH CAF (Without Excluded Vias)

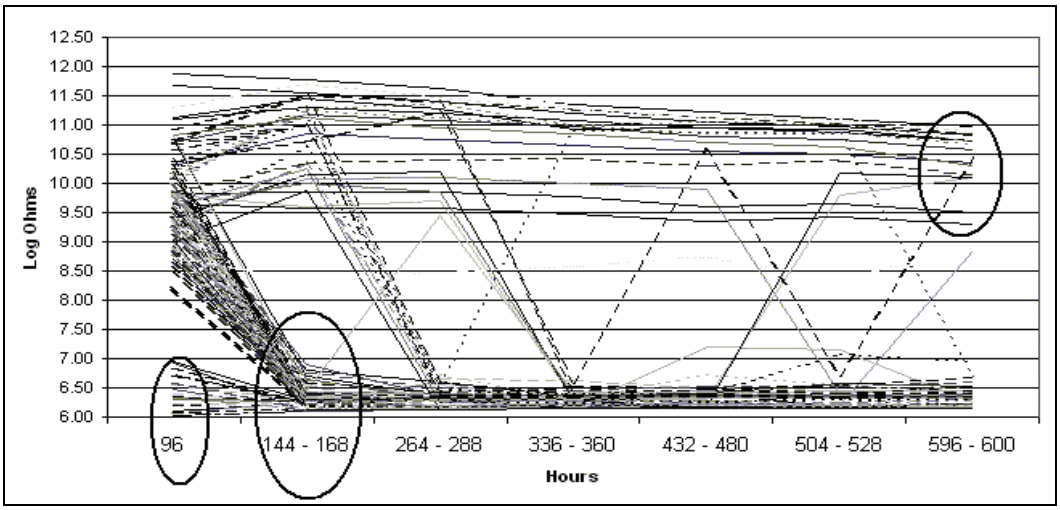

Figure 25 – Material with a Large Number of Excluded (Circled at 96 hours), a Large Number of Early Fails (Circled at 144-168 hours), and Then Some Fails as Time Progressed

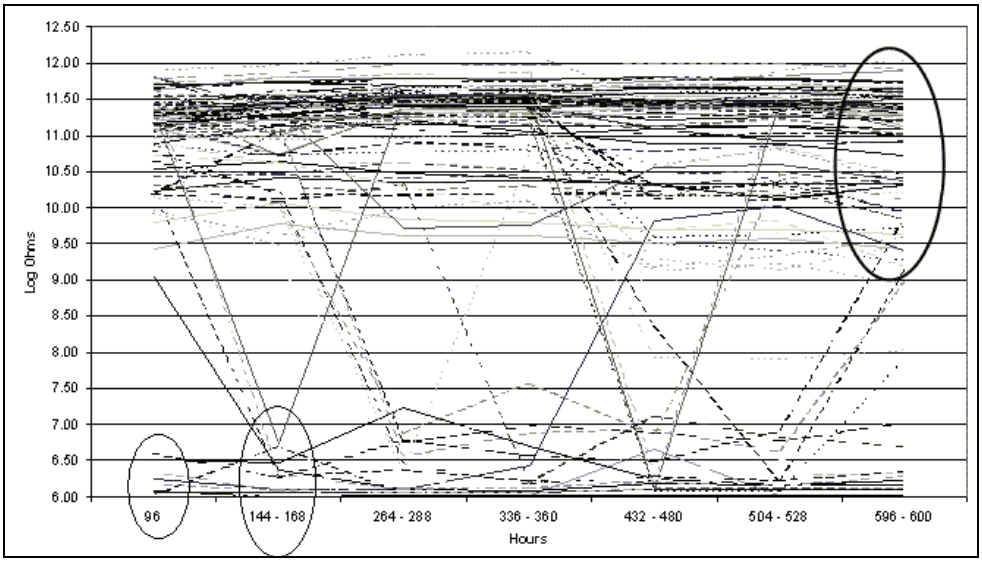

Figure 26 - Material with a few Excluded Nets, Very few Early Fails, and a Large Number of Passing Nets

The last progression of charts, Figure 27, is the evaluation of the effect of voltage; some examples are selected.

From left to right, top to bottom, are the data for nets tested at 10 volts, similar nets tested at 48 volts, and similar nets tested at 100 volts, for 3 selected laminates. As a reminder, 50 % of the available coupons were tested at 48 volts, and 25 % were tested at 10 volts and the last 25 % tested at 100V – this means that there are twice as many nets in the population tested at 48 volts – what should be evaluated, then, is not the absolute number of nets that went to 500 hours, but the percent of the tested population for that segment that went to 500 hours; or, conversely, what percent failed and when.

Laminate "H" faired well at 10 volts; by 48 volts Early Fails increased, as did fails at later points in the testing; but 100 volts doesn't seem to be appreciably different from 48 volts. Laminate "C" is already showing Early Fails even at 10 volts, then some fails as the test progresses; at 48 volts a good half of the test population fails early (or goes the distance); at 100 volts there is some further acceleration of fails, which continue to occur as the test progresses. Laminate "A" had only one net at 10 volts that "bounced": failing and recovering and failing again and recovering again; at 48 volts more nets failed and stayed failed, and nets failed at different lengths of time at that voltage stress; at 100 volts this material is still doing well as compared to the other laminates. You can see the effect of the voltage on the population as a whole, which sees a reduction in resistance levels; but the number of nets as a percent of the total population that fail is still pretty low.

In part the decision to vary voltage was done to determine what is a good test voltage to specify: would 10 volts be too little? Would 100 volts be too much; would too many nets fail on every laminate to not be able to see differences between the laminates? Forty-eight volts is a common voltage bias for our products, so that was the voltage of most interest. From the

results of this test we concluded that 10 volts is not a sufficient stressor, except in the case of some laminates which are prone to CAF even at very low voltages; also, it seems that 100 volts is not necessarily needed to show susceptibility and differentiation. Actually, we were originally going to use 150 volts for the upper test range, but the equipment limited us to 100 – so we cannot say what happens with higher voltages, but there does not seem to be a step effect at 100 volts as compared to 48 volts.

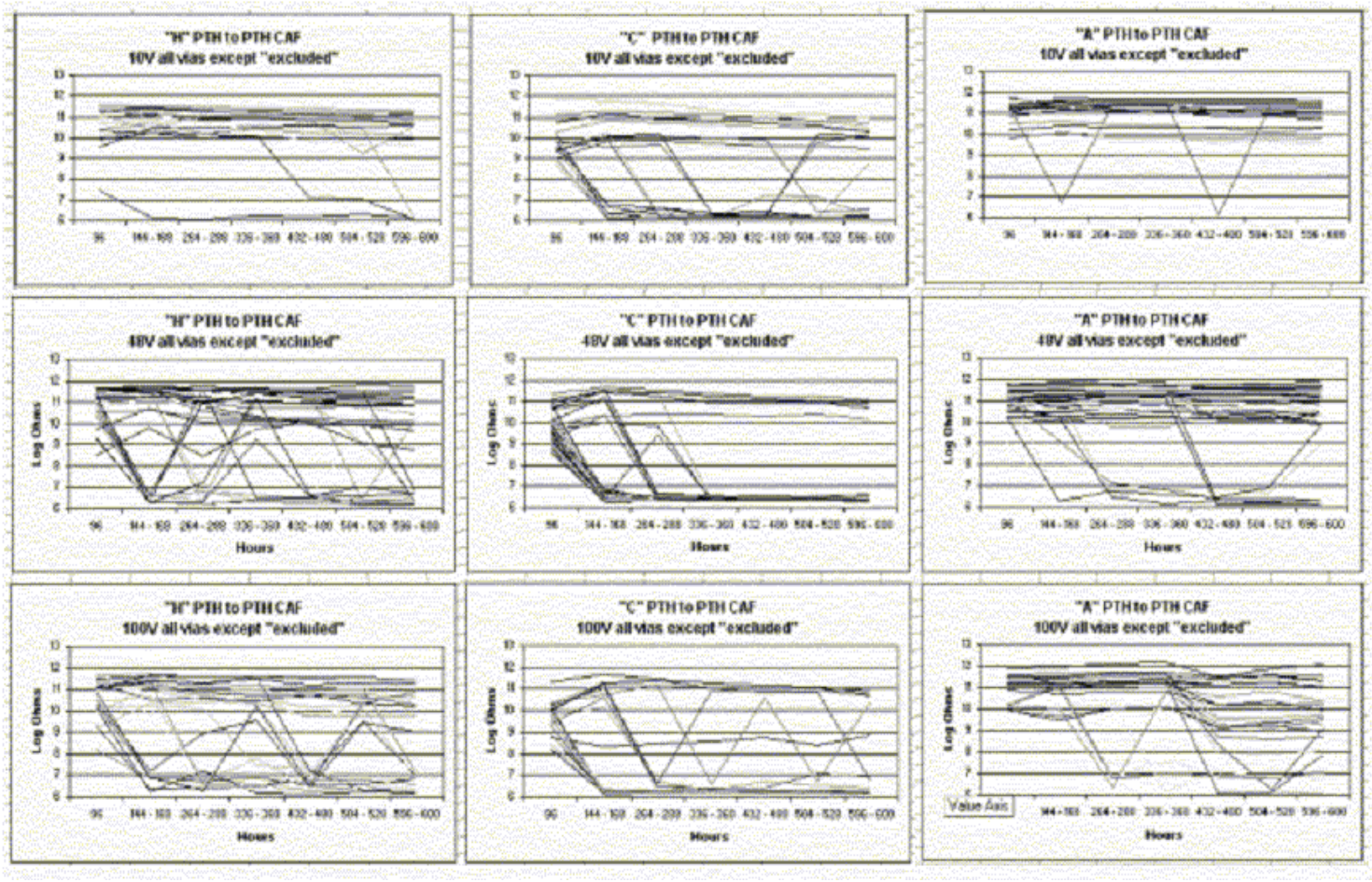

Figure 27 - The Evaluation of the Effect of Voltage

Solder floats and Microsection Evaluations – copper peel strength, solder float and microsection evaluation was conducted on each material. The testing consisted of:

- Peel Strength of Metallic Clad Laminates IPC-TM-650 Method 2.4.8 (Figure 28)
  1. Condition A "As Received": 4 samples
  2. Condition B "After Thermal Stress [288°C]": 4 samples, and
  3. Condition C "After Exposure to Processing Chemicals": 4 samples
- Thermal Stress Plated Through Holes

IPC-TM-650 Method 2.6.8 (Figure 29)

  4. Test Condition A [288 °C]
     x 3 floats: 3 coupons
  5. Test Condition A [288 °C]
     x 6 floats: 3 coupons
  6. Test Condition B [260 °C]

x 3 floats: 3 coupons

  7. Test Condition B [260 °C]

x 6 floats: 3 coupons

- Plated Through Hole Structure Evaluation IPC-TM-650 Method 2.1.3
  8. .0135" Diam. FHS array; 7 mounts
  9. .0350" Diam. FHS array; 7 mounts

Copper thickness readings on all the holes were collected to verify that HATS, IST, and solder float results were representative of PTH barrels with relatively similar plating thickness and all minimum plating requirements had been met.

Material	A	B	C	D	E	F	G	H
Copper	*Avg / 1 σ*	*Avg / 1 σ*	*Avg / 1 σ*	*Avg / 1 σ*	*Avg / 1 σ*	*Avg / 1 σ*	*Avg / 1 σ*	*Avg / 1 σ*
Small vias	1.57 / 0.29	1.35 / 0.10	1.62 / 0.16	1.40 / 0.16	1.45 / 0.14	1.66 / 0.09	1.55 / 0.08	1.79 / 0.09
Large Vias	1.93 / 0.40	1.47 / 0.12	1.73 / 0.10	1.54 / 0.24	1.59 / 0.04	1.55 / 0.13	1.79 / 0.09	1.75 / 0.13

Figure 28 - Copper Peel Strength in Lbs. / Square Inch

Material	As Received	260 °C Solder Float	288 °C Solder Float
B	Pass	Pass	Pass
C	Pass	Pass	Pass
D	Pass	Pass	Pass
F	Pass	Corner Cracks	Pass
G	Pass	Pass	Delamination
E	Pass	Pass	Pass
H	Fail	Fail	Fail
A	Med. Void	Pass	Sm. Void

Figure 29 - Solder Float Evaluation

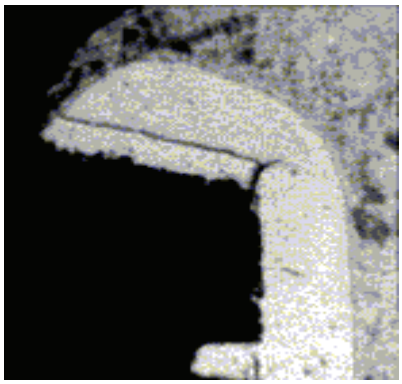

Figure 30 - Corner Crack
Laminate "F"

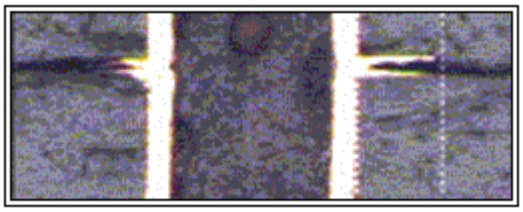

Figure 31 - Delamination/Voiding
Laminate G

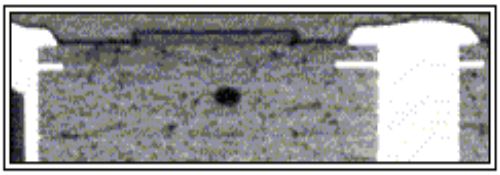

Figure 32 - Small Voidin
Laminate "A

Conclusions

The CAF data in particular was hard to quantify in absolute terms. For CAF we essentially ranked materials by viewing the performance charts side-by-side, then made a subjective classification of the laminates based on those results. A matrix of results (Figure 33) was devised to better assimilate the information on each material. We did not find a "perfect" material; we did find a few that were "very good " but in need of a bit more development work; a handful that were "OK" or even "good", but clearly needed improvements to be useful in a broad range of applications; and of course, a few which would be eliminated from further consideration, at least in the state that they were in. Should newer formulations came along later which resolved the key issue(s), we might re-evaluate the newer material.

We determined:

- "B" is close, but needs further improvements in thermal stability, which might also increase it's reliability as measured by the HATS test.
- "C" is not suitable; it's low thermal stability values in conjunction with low t poor results in IST, HATS and CAF, make it too risky to use for LFA use
- "D" is close, but needs especially to resolve it's CAF susceptibility
- "F" is not suitable; it's low Tg combined with low to poor IST, HATS and CAF make it too risky for LFA use
- "G" is close, but it will not be used until the peel strength is improved
- "E" same as "C"
- "H" is close, but the delamination and voids seen at solder float must be resolved before it could be used for LFA, and
- "A" Passed; ready to use for LFA.

From 12 laminates we found 1 ready to go; 3 to be close if they can resolve a specific issue; a few that will need to go back to formulation; and there are a few still in the build-and-test pipeline.

SUMMARY	Thermal Stability	Peel Strength	Solder Float	Elec	IST	HATS	CAF
B	Low T288	Good	Good	Good	OK	Good	OK
C	Low T288	Good	Good	Good	Low	Low	Poor
D	Low T288	Good	Good	Good	V. Good	V. Good	V. Poor
F	Low Tg	Good	Good	Hi Df/Dk	Poor	Low	Poor
G	OK	Low Peel	OK	Good	Low	OK	Good
E	Low T288	[no data]	Good	Good	Low	Low	OK
H	Good	Ok	Fail	Good	V. Good	V. Good	Good
A	Good	Good	OK	OK	V. Good	V. Good	Best

Figure 33 - Matrix of Results

Discussion

Several test issues were continually problematic, and remain so (or at least that is our current thinking). Even standard tests are not being conducted in the standardized way, and/or the interpretation of the results has a lot of latitude. Other tests leave a fair number of variables to the tester, and so the consumer of those data needs to be absolutely clear on what was tested and how it was tested. In general, testing done by the lamination industry is not aggressive enough; test structures which are

closer to the real and challenging applications which are routinely designed need to be taken into account when developing test vehicles. Last, there does not yet appear to be one clear "property" test and value, or functional test, which aligns to a high confidence for LFA processability.

There are some obvious and promising avenues for laminators to investigate in their pursuit of improvements in their end product, chiefly the glass products that are the foundation of the cores and prepregs. Why are some glass styles more prone to CAF than others? Why is one orientation more prone to CAF than the other?

A good percentage of these materials, even thought they were "production ready" at the outset of the project, were being "tweaked" as this project progressed and as new data came in; some have had or are about to have significant reformulations. Relatively speaking, this is still early in the life cycle of a new laminate. Until many many different types of boards by different fabricators using different processes at different times of the year in different regions are manufactured and assembled there is no doubt that these new laminates and their components will continue to be tweaked and refined to produce ever better results. Fabricators and OEMs should stay in close communication with their laminate suppliers to make sure they have the most current processing and performance information.

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References
1. IPC-TM-650, TEST METHODS MANUAL.
2. S. Mirshafiei, "The Next Generation high-Tg products for Telecom and Broadband Applications", November 2004.
3. Bob Neves, et al, "Highly Accelerated Thermal Shock (HATS) Reliability Testing", Proceedings, IPC Printed Circuit Expo, March 2003.
4. Gerard Gavrel, "Understanding IST Technology", http://www.pwbcorp.com/.
5. IPC-TM-650 Number 2.6.25, "Conductive Anodic Filament (CAF) Resistance Test: X-Y Axis".
6. CAF coupon design by Alcatel.

Appendix