Lead Free Assembly Qualification of Stacked MicroVia Boards

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Abstract
Beginning July 2006, the electronic industry will enter the age of lead –free assembly and products in Europe. The removal of lead from electronics brings massive changes for all companies in the supply chain, OEMs and contract manufacturers.

Lead Free SMT assembly poses many challenges for soldering and reflow processes. It requires significant process optimization efforts to perform high volume manufacturing successfully and get good, reliable solder joints. Migration to lead free assembly requires careful balancing of bill of materials with reflow profile. Double sided reflow requires careful balancing of delta T from Side A to Side B reflow.

Cellphone assembly requires the use of thin form factor PWBs to meet the drive for miniaturization and thin, light products. This is accomplished by using HDI- high density interconnect boards or build up technology boards. [1]. These PWBs have stacked microvias, which are laser drilled and plated. The switch to lead free assembly requires the use of higher reflow temperatures, so evaluation of the microvia connections after reflow is critical after assembly.

Solder joint reliability evaluations have to focus on Ball Grid array solder joint integrity, SMT packages, passive components and connector solder joints. Rework processes are an essential part of the reliability evaluations as higher peak temperatures for rework may affect PWB laminate, near neighbor components and package integrity.

This paper presents the results of lead free solderability qualification conducted at Kyocera-Wireless Corporation. The report summarizes the results of X-sectional analysis, shear testing, thermal shock and temperature humidity testing of lead free assemblies using a HDI board.

The paper summarizes the surface mount assembly evaluation conducted to ensure the stability of the laminate and microvias through the double-sided reflow process and rework. This was evaluated as a part of the phone product qualification build.

Key words: PWB, HDI, OEM

Introduction
Fine pitch packages with high pin count and PWB applications requirements are driving the need for high-density interconnect design capabilities using microvias.

HDI and lead free assembly technology is emerging in handset industry; however, production level reliability data for double-sided surface mount assembly is not readily available. This requires users to establish their own reliability data thru reflow and rework processes. Dynamic testing data is also needed to assess reliability of handset applications.

This paper presents the assembly qualification of the HDI technology through 2 pass reflow and 1 pass rework. Results of solder joint reliability testing, shear test and X-sectional analysis are presented.

PWB Design and Fabrication
The PWB was designed as an 8-layer thin board 0.8 mm thick. The PWB had an HDI configuration with copper plated microvias in the outer 2 layers. The PWB laminate was high glass transition temperature (Tg) FR-4. The surface finish on the PWB was electroless nickel/immersion gold. Figure 1 shows the X-section of a HDI PWB with stacked microvias.

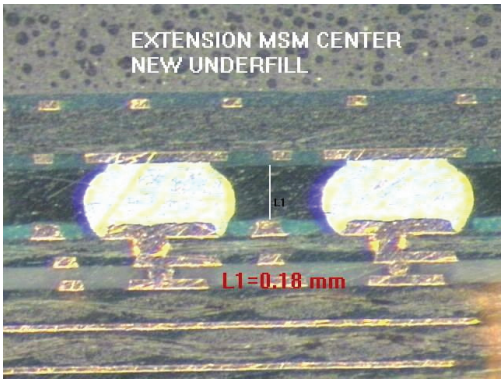

Figure 1 - HDI (High Density interconnect PWB

Wetting Balance Test
Wetting balance test was conducted on several solder paste materials of which one was selected. The selected paste had wetting properties that were better than the leaded paste for both wetting time and wetting force. The wetting force and time is summarized in Table 1.

Table 1 - Wetting Balance Test Results

	Pb Free Paste	Pb Paste
Wetting Time (sec.)	0.3-0.5	0.8-1.3
Wetting Force (mN)	10-14	6-13

Board Assembly:
Board assembly process was a double-sided surface mount assembly soldering of ball grid array packages, connectors, chip resistors, capacitors, diodes, and several other fine pitch SMT (surface mount) packages.etc. The assembly was reflowed in convection air at a peak temperature of 245C. The solder paste used for assembly SAC 305 (Tin96.5/silver 3/copper 0.5)– No Clean version. The product required a double-sided assembly. Lead based assembly was conducted using (tin/lead /silver 2%) paste as a control to compare results with lead free.

Shear Testing:
Mask defined as well as etch defined pads were used for soldering BGAs. Shear testing was conducted to compare the differences between two pastes. Shear values were also compared to existing etch defined pads used in HDI boards. Table 2 shows Shear Test Post Reflow (Pounds). Lead free paste assemblies had higher shear value.

Table 2 - Shear Test Post Reflow (Pounds)

BGA Shear Test Data		
	Lead Based	Lead Free
Mean	45 lb	55 lbs
Std. Devn.	8.29	4.9

Post Reflow X-Sections
X-sections were performed on the BGA packages and other components to evaluate the quality of the solder joints and ensure compliance to IPC 610 – Rev D for lead free packages and IPC 7095 for BGA packages. Also microvia integrity was evaluated with X-sectional analysis. X-sections showed acceptable solder joints and no degradation of microvias. [2, 3]. Figure 2 shows the X-sections on an etch defined pad and Figure 3 shows the X- section of a mask defined pad. The standoff height of the joint is higher for a mask-defined pad. For PWB assembly process, lot/lot consistency is essential. The

tolerances of the etching processes are preferred as compared to the solder mask apply process, so the etch defined pads were used.

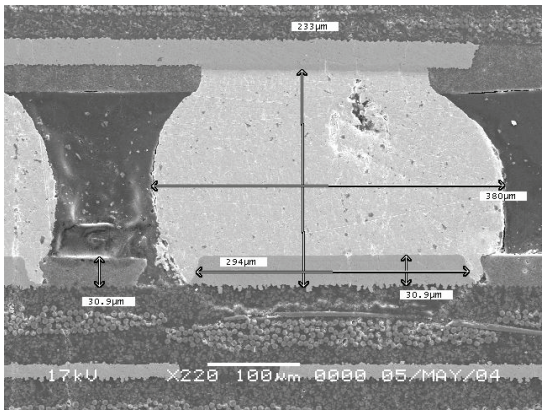

Figure 2 - BGA Solder Joint- Etch Defined Pads

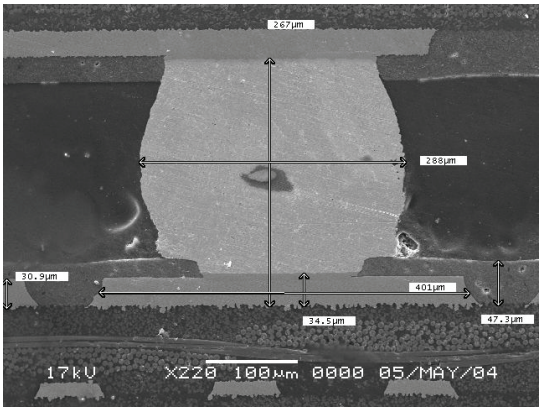

Figure 3 - BGA Solder Joint – Mask Defined Pads

Intermetallic Thickness Measurement

The ball to pad interface is critical for solder joint reliability. The interface area is where the Tin/Nickel /Tin/Copper intermetallics are formed. The interface for the leaded paste and the lead free paste are shown in Figure 4 and Figure 5.

Intermetallic thickness was measured on both leaded and lead free samples. On an average Intermetallic thickness ranged from 60 microinches for lead free samples, post reflow and 80 microinches average after thermal shock test. The intermetallic thickness data is summarized in Table 3.

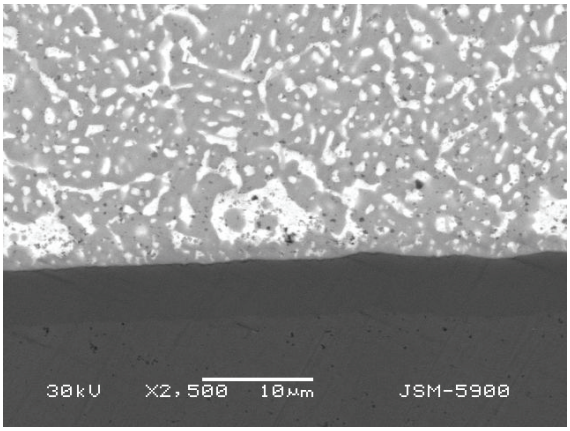

Figure 4 - Ball/Pad Interface – Leaded Paste

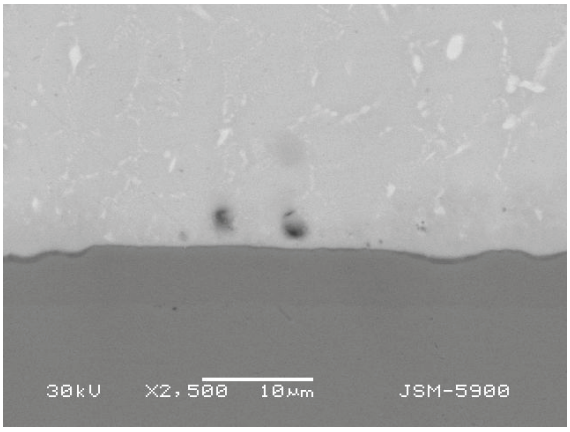

Figure 5 - Ball/Pad Interface – Lead Free Paste

Table 3 - Intermetallic Thickness Measurement Data

Intermetallic Thickness Post Reflow (Microns)							
Leaded	1.46	4.14					
Lead Free	0.48	2.44					
Intermetallic Thickness Post Thermal Shock (Microns)							
Leaded	*1.8*	*4.4*					
Lead Free	*0.58*	*3.28*					

Rework Evaluation:
Rework of SMT packages is performed using hot air soldering tools and application of heat using controlled ramp/soak profile. Board pre-heat was used during rework. The concern was damage to microvia connections and PWBs pads during component removal and reattach. Component rework was performed 2X on the leaded packages and 1X on the Ball-Grid Array packages. All packages survived rework. There were some lifted pads, but no major damage to PWB pads, or blistering of solder mask during rework. No damage was seen on microvia connections. Figure 6 and Figure 7 show PCB surface after package removal showing no lifted pads.

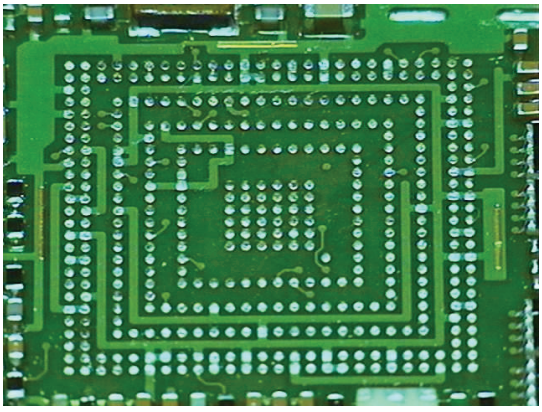

Figure 6 - BGA Pads 0.3 mm after package removal

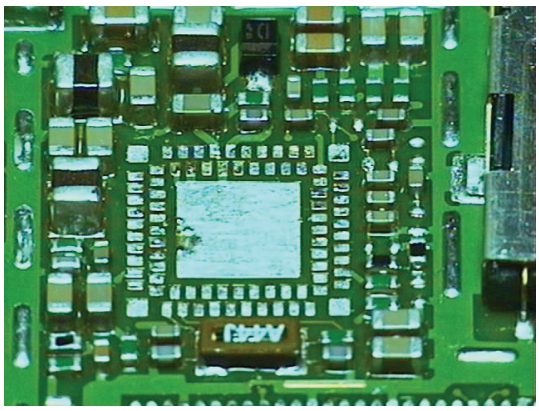

Figure 7 - BCC Pads after Package Removal

Solder Joint Reliability Test: Thermal Shock

Solder joint reliability testing was performed for assembly qualification per IPC 7091. Assemblies were thermal shock tested from –25C to +125C for 500 cycles and extended to 800 cycles. [3,4] Temperature humidity testing was performed at 85C/85% Relative Humidity for 1000 hours. Samples were X-sectioned post-test to evaluate the joint quality. The joints appeared slightly grainy after thermal shock test and oxidized after temperature humidity testing, but no cracks were seen in the joints. No separation was seen where the microvia connected to the capture pad. Figure 8 shows X-sections after thermal shock test.

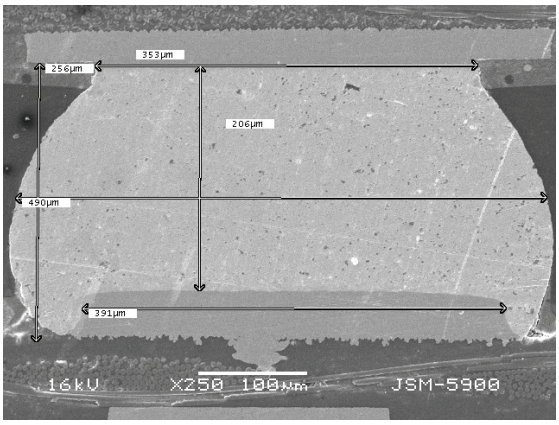

Figure 8 - BGA Package – Post Thermal Shock

Visual examination was done after thermal shock test. Some ceramic packages had cracked due to CTE mismatch

All plastic packages and BGA packages were intact after thermal shock test.

Samples were tested at 500 cycles and 800 cycles for open joint via probe test. Leaded paste samples showed earlier and more failures than the lead free paste samples. Table 4 summarizes the results of open joint evaluation.

Table 4 - Open Joint Analysis Data

Thermal Shock Testing				
	500 Cycles	800 Cycles		
Leaded	1/8 fail	8/8 fail		
Lead Free	All Pass	All Pass		
Package Tested - 208 Pin BGA				
Requirement is -25C - +125C, 500 cycles; Fail if resistance increase >10%				

Temperature Humidity Test
The PWBs showed some discoloration and some component solder joints were oxidized after temp. Humidity test. No bubbles, blisters etc. was seen in the PWB or solder mask. All PWBs passed board level electrical test. No lifted pads, traces or via separation was observed in X-sections. Figure 9 shows X-sections Post Temp. Humidity.

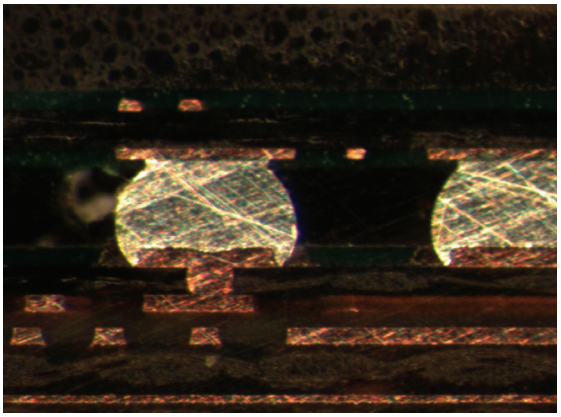

Figure 9 - X-section Post Temp. Humidity

Phone Level Drop Test
Phone level drop tests were performed at 1.5 meters on a hard vinyl surface. Assemblies were X-sectioned post drops to evaluate solder joints and microvia connections. The intent was to study the mechanical integrity of the boards and joints during phone level drop test. No via cracking or pin cracking was observed.

No solder joint failures or microvia cracks were seen after drop test.

Conclusion
Lead free assemblies with HDI boards have demonstrated reliability through 2X reflow and rework operations. The assemblies have survived thermal shock and temperature humidity test and drop shock testing.

Since no failures or cracks were seen in the joints or microvias, the assembly passed solder joint reliability qualification testing.

References
[1] John H. Lau, S. W. Ricky Lee, Microvias for low cost, high density interconnect

[2] IPC A-610 Rev D, Acceptability of Electronic Assemblies

[3] IPC 7095, Design and Assembly Process Implementation for BGAs

[4] IPC 7091 Guidelines for Accelerated Reliability Testing.