Visual and Reliability Testing Results of Circuit Boards Assembled with Lead Free Components, Soldering Materials and Processes in a Simulated Production Environment

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Abstract
The New England Lead-free Electronics Consortium is a collaborative effort of New England companies spanning the electronics supply chain, sponsored by the Toxics Use Reduction Institute, the U.S. EPA, and the University of Massachusetts Lowell. The consortium has completed and published the results of two phases of manufacturing and testing of lead-free Printed Wiring Boards (PWBs) with the goal of achieving zero-defect lead-free soldering processes with comparable reliability to that of leaded solder processes. Phase I examined various solder alloy combinations and reflow profiles, while Phase II focused more broadly on processing parameters, utilizing a mix of component types and finishes in combination with five different PWB finishes, two reflow atmospheres (air and nitrogen) and three solder paste compositions based on the same Sn3.8Ag0.7Cu alloy.

Phase III efforts began in August 2004 and will be completed by November 2005. The objective for Phase III testing is to focus on implementation issues by simulating an actual production board for parameters such as board layers, board size, and component density. The Phase III PWB is a twenty layer board with components on both sides, and populated with 1,750 components. Thirty-six PWBs were built and inspected to IPC 610 D standards by Benchmark Electronics in April 2005. The PWBs underwent thermal cycling at Raytheon Reliability Labs test facilities and Highly Accelerated Life Testing (HALT) at Teradyne test facilities. Pull testing was conducted at the University of Massachusetts Lowell. In this paper, the authors will present the results of Phase III efforts, including the PWB interconnect stress test, test coupon failure mode analysis, visual inspection, thermal cycling, HALT, and pull tests.

Key words: Lead Free, Visual testing, Reliability testing, Thermal Cycling, Design of Experiments.

Introduction

In January 2003, The European Union (EU) published Directives 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE) and 2002/95/EC on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment (RoHS). These emerging directives have been the primary drivers for a global movement toward lead-free electronics. The RoHS directive prohibits products that contain lead to be sold in the EU after July 2006, unless the use is specifically exempted.

New England Lead-Free Consortium

Two organizations, the Toxics Use Reduction Institute (TURI) and the University of Massachusetts Lowell (UML) were the primary initiators of the lead-free consortium. These organizations were engaged to provide training and information, and conduct research in innovative technologies to support toxics use reduction. In 1999, as the movement toward lead-free emerged, TURI began supporting research at UML to investigate the alternative lead-free solders.

The Massachusetts Lead-Free Electronics Consortium was formed in 2000, consisting of TURI, UML, and at least one representative from each part of the electronics supply chain. Members contributed time, materials, facilities, funding and expertise as they jointly developed and implemented testing plans for the Phase I and II efforts. In 2004, many other companies were added from the New England region, and the consortium changed its name for Phase III efforts to the New England Lead-Free Electronics Consortium. Phase III efforts are sponsored by U.S. EPA under work order number 4W-1362-NAEX. The Consortium is a successful working partnership between industry, academia, and government. Key consortium members and their companies are listed as co-authors in this paper.

In addition to supporting the consortium, TURI periodically brings together firms from the electronics supply chain to exchange information, to communicate the latest technical and regulatory developments, and to report on the consortium's research program (for summaries of papers and presentations, see TURI's web site: www.turi.org).

Phase III Testing of Lead-Free Electronics Assembly

Phase III testing efforts focused on examining the manufacturing issues of implementing lead-free electronics assembly for PWBs more closely resembling actual production boards. Whereas previous phases of the project utilized experimental PWBs that were single layer, single sided, small footprint, and sparsely populated with only SMT components; the PWB for Phase III was designed to better simulate actual production boards commonly used in industry. The Phase III board had a variety of component types and finishes, as well as some active circuitry that could be tested for electrical performance. The object of Phase III was to compare the solder joint integrity and circuit performance between lead and lead-free electronics assembly for production scale boards. The primary metrics for this comparison are defects per unit (DPU) as identified during the visual inspection process, and peak pull strength as measured during pull testing.

The Phase III PWB is comprised of twenty layers and has a large footprint of 16 inches by 18inches. The PWB is densely populated with components on both sides. Phase III will include thirty-six PWBs. Each PWB contained 1,713 SMT type components and 53 THT type components, for a total of approximately 62,000 components included in the Phase III experiment. The following eight consortium members supplied these components: Raytheon, Textron, Teradyne, Skyworks Solutions, Benchmark Electronics, American Power Conversion, Texas Instruments, and M/A-COM.

Prior results of consortium testing efforts, as well as other published research was incorporated into the material and process selection for Phase III lead-free testing. New consortium members were added to provide resources and background to volume production application of lead-free electronics assembly. These companies provided valuable knowledge and material contribution of mass market volume applications.

- Factors and levels of the Lead-free experiment:
  The following factors were selected based on results of Phase I and II efforts, as well as the collective experience of the consortium members: 2 lead-free solder suppliers ("A" and "B"), 3 surface finishes and 2 types of laminate materials ("Y" and "Z"), as shown in Table 4. The three surface finishes are electroless nickel immersion gold (ENIG), immersion silver, and organic solderability preservatives (OSP). The lead-free solder from both suppliers will use the SAC 305 alloy and no-clean flux. Other factors such as solder reflow profile (as recommended by the supplier) and atmosphere (air) were fixed based on member consensus. Each PWB will undergo at least two reflows during assembly; one for topside of the PWB, another for bottom side of the PWB. Two PWBs were built for each of the lead-free experiments listed in Table 1, for a total of 24 lead-free PWBs.

Table 1 - Phase III Lead Free Solder Test Plan

Experiment #	Surface Finish	Solder paste	Laminate
1	(1) Imm Ag	LF "A"	"Y"
2	(1) Imm Ag	LF "A"	"Z"
3	(1) Imm Ag	LF "B"	"Y"
4	(1) Imm Ag	LF "B"	"Z"
5	(2) OSP	LF "A"	"Y"
6	(2) OSP	LF "A"	"Z"
7	(2) OSP	LF "B"	"Y"
8	(2) OSP	LF "B"	"Z"
9	(3) ENIG	LF "A"	"Y"
10	(3) ENIG	LF "A"	"Z"
11	(3) ENIG	LF "B"	"Y"
12	(3) ENIG	LF "B"	"Z"

- Baseline leaded solder experiments
  To reduce the number of iterations, only one laminate material was used with three different surface finishes and 2 different leaded solder suppliers providing the lead baseline experiments as shown in Table 2. Two PWBs were built for each of the leaded experiments listed in Table 2, for a total of 12 leaded PWBs.

Table 2 - Leaded Solder Test Plan

Experiment #	Surface Finish	Leaded Solder paste	Laminate
1	(1) Imm Ag	TL "A"	"Z"
2	(1) Imm Ag	TL "B"	"Z"
3	(2) OSP	TL "A"	"Z"
4	(2) OSP	TL "B"	"Z"
5	(3) ENIG	TL "A"	"Z"
6	(3) ENIG	TL "B"	"Z"

- Components
  Surface mount and through hole technology components were used for the Phase III PWB. Component types include ball grid arrays (BGAs), small outline integrated circuit (SOIC), connectors, resistors, capacitors, relays, inductors, and quad flat packs (QFP). A variety of component finishes were included for the Phase III PWB, including the following: nickel/palladium/gold, tin, tin/lead, gold, nickel/gold, tin/nickel, palladium/silver, tin/copper, tin/silver/copper, tin/bismuth, and matte tin. Some components were available in daisy chain configurations for electrical testing.

Phase III Assembly Process

The PWB was designed by Benchmark Electronics, and the raw PWBs were manufactured by Dynamic Details Inc. Two stencils (one for top and one for bottom of the PWB) were manufactured by Stentech and are 6 mils thick stainless steel electropolished laser cut. There was a step-down to 5 mils on both stencils to accommodate the microBGAs.

A ten percent (10%) standard reduction was used for the apertures on the top stencil. The apertures for the bottom stencil included: For leaded devices, there was a 10% expansion in length for both directions, and a 1 to 1 ratio for width. For fine pitch devices, aperture ratio was based on pad size. For discrete components there was a 10% increase in length on the termination side only, and a 1 to 1 ratio for the width. The same stencils were used for both the lead-free and tin/lead PWBs.

The discrete components were divided into four groups (each group containing both resistors and capacitors). Each group has different aperture styles including: radial aperture, home plate, king's crown, or standard aperture.

Assembly of the Phase III PWBs was conducted at Benchmark Electronics. The equipment used for the SMT components included a DEK Horizon 265 screen printer, a Universal 4791 high speed placement machine, and a Vitronics XPM reflow oven with 10 heating zones and three cooling zones. For the THT components, Premier Rework machines were used. The solder pot temperature was 260 degrees Celsius for the tin/lead PWBs and 280 degrees Celsius for the lead-free PWBs. The automatic optical inspection was conducted using an Omron VT-WIN inspection system. Visual inspectors then conducted

100% visual tests on all solder joints for each of the Phase III PWBs. The PWBs were then available for consortium members to conduct further visual inspection and electrical testing of their components.

Upon completion of visual inspection and electrical testing, the PWBs then underwent reliability testing. The Phase III PWBs were divided evenly for the reliability testing. Half of the PWBs underwent thermal cycling, and the other half underwent highly accelerated life testing (HALT) testing. Pull tests will be performed on the four spare PWBs prior to thermal cycling, and after the thermal cycling for eighteen PWBs. The four spare boards are all lead-free PWBs.

After the pull testing has been completed, the PWBs will be available for consortium members to test the circuit performance of the components that they supplied for the Phase III PWB.

Interconnect Stress Test

Initially, all PWBs were tested using a coupon for interconnect stress test (IST) to evaluate the higher temperature effects on the laminate materials. This test measures changes in resistance of plated through hole barrels and internal layer connections as the test coupon is subjected to thermal cycling. Thermal cycling is produced by applying an electrical DC current through the test coupons. Switching the current on and off creates thermal cycles between ambient temperature and the desired maximum temperature.

To simulate a lead-free assembly environment, the IST preconditioning temperature was set at 260 degrees C. To obtain a greater understanding of the effect of multiple heat excursions on the laminate material, half of the test coupons had three heat cycles during preconditioning and the other half of the test coupons had six heat cycles during preconditioning. The preconditioning temperature profile is shown in Figure 1.

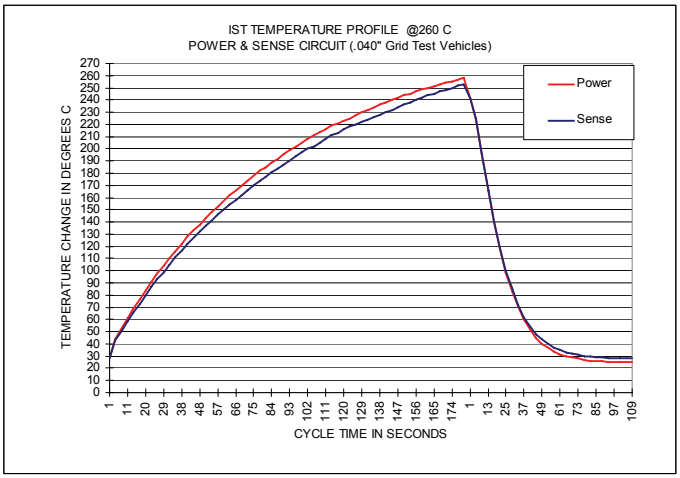

Figure 1 - IST Preconditioning Temperature Profile

Once the test coupons passed the preconditioning, they then underwent IST cycling for up to 500 cycles. Each IST cycle was approximately 85 minutes in duration and the temperature was cycled between ambient and 150 degrees Celsius. The thermal profile for the IST cycling is shown in Figure 2:

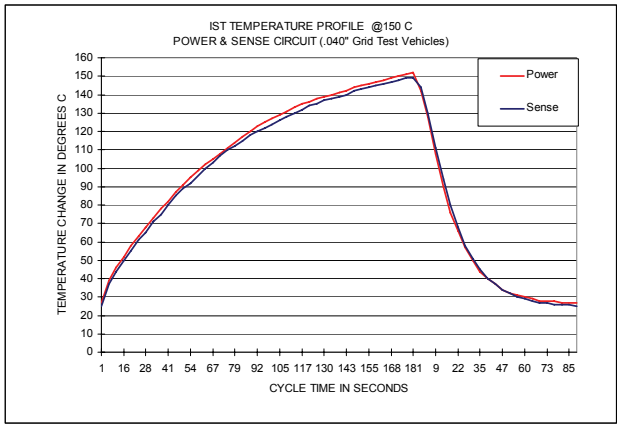

Figure 2 - IST CycleTemperature Profile

The number of cycles to failure was recorded for each test coupon. The results are shown in Table 3. The results revealed a bimodal distribution in that the test coupons either failed early in the thermal cycling, or they made it all the way through the preconditioning and IST cycles without failure. A possible cause for the bimodal data could be that there were defects in the hole for some PWBs, such as the presence of debris or insufficient plating of the high aspect ratio through holes.

Another interesting result is the high number of failures for the test coupons with OSP surface finish, and the low number of failures for test coupons with ENIG and immersion silver surface finishes. Board surface finish is not expected to be a significant factor for IST results. The OSP coating was not applied before the IST testing. Therefore, the IST testing was done on bare copper in an air environment. The OSP failures could have been false failures caused by the formation of copper oxide at higher temperatures.

Table 3 - IST Results

Material	Finish	Precondition Cycles	P/F	Cycle Failure Occurred	No. Of IST Cycles
A	ENIG	3x	P		500
A	OSP	3x	F	Cycle 3	
A	Ag	3x	P		500
A	ENIG	6x	F	Cycle 5	
A	OSP	6x	F	Cycle 5	
A	Ag	6x	P		500
B	ENIG	3x	P		500
B	OSP	3x	P		29
B	Ag	3x	P		500
B	ENIG	6x	P		500
B	OSP	6x	F	Cycle 1	
B	Ag	6x	P		500

In general, it was believed that the laminate materials performed well during the IST testing, and that the board finish is not considered to be a factor for IST failures. Failure analysis will be conducted on the test coupons that failed during either preconditioning or IST cycling. This analysis will be essential to determine the root cause of the test coupon failures.

Visual Inspection Results

After the Phase III PWBs were assembled, they were visually inspected at Benchmark Electronics. Seven visual inspectors conducted 100% visual tests on all solder joints based on IPC inspection standard 610D. The results of the Automatic Optical Inspection were reviewed for false/true calls by the visual inspectors. The microscopes were set at 10x magnification, and inspections were conducted in accordance with Class 2 requirements. Each of the thirty-six PWBs was inspected by two different visual inspectors.

Seventy potential defect and process indicator categories were looked for during this visual inspection including non-wetting, pinholes, solder balls, solder bridging, and tombstoning. Table 4 reveals the actual defects and process indicators that were identified during Phase III for both the tin/lead and lead-free PWBs.

Table 4 - Identified Defects and Process Indicators

Description	Tin/Lead PWBs	Lead-free PWBs
209: Bent pin	Y	Y
261: Tombstone	Y	Y
602: Solder bridge	Y	Y
615/616: Non-wetting	Y	Y
626: Disturbed solder	Y	Y
713: Foreign matter	Y	Y
606: Pinholes, blowholes	Y	Y
613: Insufficient solder	Y	Y
672: Solder balls	Y	Y
205: Misregistration	Y	Y
270: Raised part	Y	Y
603: Solder splatter	Y	Y
612: Excess solder	Y	Y
620: Unsoldered lead		Y
701: Delamination		Y
770: Damaged pad	Y	Y

The total amount of defects identified during the visual inspection was 993 defects. This total includes two visual inspections for each of the thirty-six PWBs. Table 5 shows further detail for the defects found.

Table 5 - Defects Identified During Visual Inspection

	Lead-free 24 PWBs (x2 inspections)	Tin/Lead 12 PWBs (x2 inspections)	Totals
SMT	377	349	726
THT	246	21	267
Totals	623	370	993

For the SMT components, the defects per unit (component) rate was 0.005 for the lead-free PWBs, and 0.008 for the tin/lead PWBs. For the THT components, the defects per unit (component) rate was 0.193 for the lead-free PWBs, and 0.033 for the tin/lead PWBs.

The results of the visual inspection will be presented in three steps:

1. Design of Experiment Analysis 1: Lead-free PWB Visual Defects
2. Design of Experiment Analysis 2: Tin/lead PWB Visual Defects
3. Comparison of Lead-free versus Tin/lead PWB Visual Defects

The null hypothesis is that there is no difference between the compared values. The alternative hypothesis is that there is a difference between the compared values. A 95% significance level was used for the visual inspection results. If the calculated probability was less than 0.05, then the null hypothesis was not rejected. If the calculated probability was greater than 0.05, then the null hypothesis was rejected, indicating that there was a difference between compared values.

Design of Experiment Analysis 1: Lead-free PWB Visual Defects
The mean defects per PWB are provided in Figure 2. The mean defects per board for lead-free solder “A” was 10.83, and the mean defects per PWB for lead-free solder “B” was 4.87. With a probability of 0.055, there is borderline significance that there is a difference between the performance of lead-free solders “A” and “B”.

The mean defects per PWB for laminate material “Y” was 10.83, and the mean defects per PWB for laminate material “Z” was 4.87. With a probability of 0.055, there is borderline significance that there is a difference between the performance of laminate materials “Y” and “Z”.

For the three board surface finishes, there was a probability of 0.298. Therefore, there is no statistical difference between the three surface finishes for the lead-free PWB visual defects.

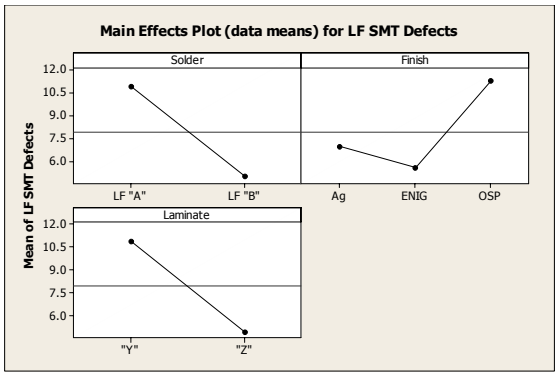

Figure 3 - Mean SMT Defects Per Lead-free PWB

From the interaction analysis, there was only statistical significance for the laminate and solder paste interaction. The interaction of lead-free solder "A" with laminate material "Y" had a mean defects per PWB of 17.17, which was very much higher than for the other three lead-free solder and laminate combinations. The values of all the interactions can be seen in Figure 4.

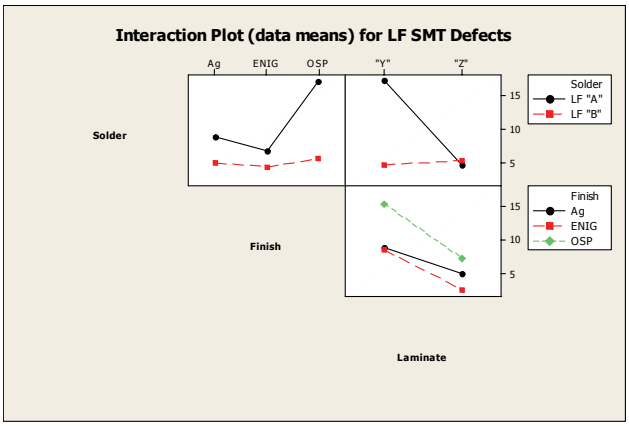

Figure 4 - Lead-free Interaction Effects

For the through hole technology (THT) components on the lead-free PWBs, there was no statistical significance for any of the factors: laminate material, surface finish, or solder paste. There was also no statistical significance for interaction effects for the THT components.

Design of Experiment Analysis 2: Tin/lead PWB Visual Defects
The following figure illustrates the mean defects per PWB for the tin/lead PWBs.

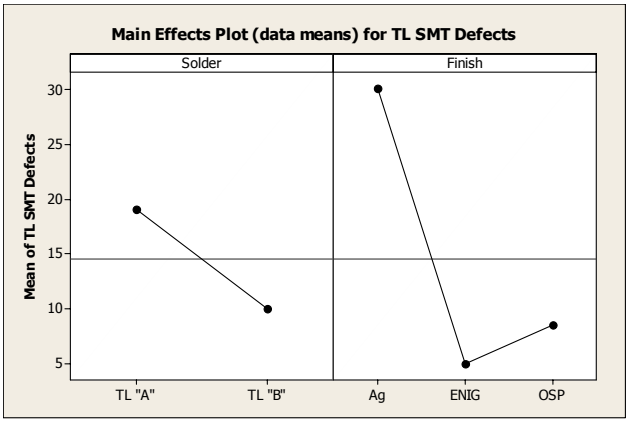

Figure 5 - Mean SMT Defects per Tin/Lead PWB

For the tin/lead PWBs, there was no statistical difference for solder paste, surface finish, or interaction effects for SMT or THT components.

Comparison of Lead-free versus Tin/Lead PWB Visual Defects
The mean for THT visual defects per PWB was 10.2 for lead-free boards, and 1.7 for tin/lead PWBs. Because the probability is less than 0.05, there is a statistical difference between the means for lead-free and tin/lead PWBs. Therefore, the tin/lead process has a lower rate of defects for THT components.

The mean for SMT defects per PWB was 7.9 for lead-free PWBs, and 14.5 for tin/lead PWBs. Because the probability is greater than 0.05, there is no statistical difference between the means for lead-free and tin/lead PWBs. Therefore, the tin/lead and lead-free process have a similar rate of defects for SMT components.

Component Finish Visual Defects
There were ten different SMT component finishes used for the lead-free and tin/lead PWBs. The following table illustrates the solder joint defect rate for each of the component finishes. Because of the small sample sizes for each PWB, no statistical analysis could be performed as to the significance of these results, but the defect rate is given as a relative indication of the performance of each finish.

Table 6 - SMT Defects by Component Finish

Component Finish	Number of SMT Components	Defect Rate (Lead-free solder)	Defect Rate (Lead solder)
Tin/copper	144	0%	0%
Tin/bismuth	432	0.3%	0%
Tin	59,076	0.3%	0.8%
Gold	108	1.4%	0%
Tin/lead	468	2.1%	0%
Nickel/ palladium/gold	612	3.1%	1.0%
Matte tin	324	5.1%	8.3%
Nickel/gold	240	9.1%	18.7%
Tin/silver/copper	168	13.5%	4.2%
Palladium/silver	36	16.7%	0%

There were five different THT component finishes used for the lead-free and tin/lead PWBs. The following table illustrates the solder joint defect rate for each of the component finishes. No statistical significance analysis could be performed because to small sample sizes.

Table 7 - THT Defects by Component Finish

Component Finish	Number of THT Components	Defect Rate (Lead-free solder)	Defect Rate (Lead solder)
Tin	576	15.1%	1.8%
Other lead-free	198	15.5%	2.3%
Tin/copper	54	17.4%	5.6%
Nickel/ palladium/ gold	36	20.8%	0%
Tin/nickel	90	46.7%	15%

Visual Inspection Observations
Several observations were noted by the inspectors during the visual inspection process. In general, the wetting for the lead-free solder joints was as good or better than the wetting of the tin/lead solder joints. The lead-free solder flowed further up the lead than the tin/lead solder. For the component with gull wings, the heel fillet filled more than the toe fillet when using the lead-free solder paste. The lead-free combination with the best solder joints was considered to be PWBs with the following levels: ENIG surface finish, laminate “Z”, and solder paste “B”.

A ten percent standard reduction was used for the apertures on the top stencil. The apertures for the bottom stencil included a 1 to 1 ratio with some exceptions (as noted earlier in this paper). In general, the components on the bottom had better overall solder joints, including much better wetting performance and fewer defects.

Phase III Reliability Testing
To better understand the reliability of the lead-free and tin/lead solder joints, thermal cycling and Highly Accelerated Life Testing (HALT) was conducted on the Phase III PWBs.

The thermal cycling was performed at Raytheon's environmental testing facilities in Massachusetts. A Thermotron F125 chamber was used for the thermal cycling. Thermocouples were used to monitor the air temperature throughout the chamber. The thermal profile used for temperature cycling was selected to meet the requirements of IPC-9701, test condition TC1. These conditions were selected to facilitate direct comparison of our results with those of other investigators. The thermal cycling parameters are outlined below:

- Minimum temperature of 0° C, and maximum temperature of 100° C.
- Ramp rates (up and down) = 10°C/min.
- Dwell times at maximum and minimum temperatures are 10 minutes.
- The number of thermal cycles selected for Phase III was 2,000 cycles.

The thermal cycling parameters are illustrated in Figure 6.

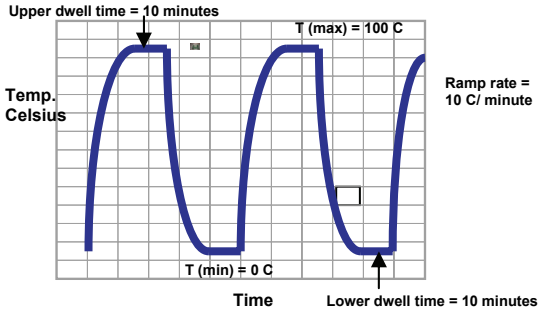

Figure 6 – Thermal Cycling Profile

The HALT testing was conducted at Teradyne's facility in Massachusetts. A Qualmark HALT chamber was used for the testing. The HALT parameters included temperature cycling between –60 degrees C to 160 degrees Celsius, and vibration between static and 80 Grms. A single 206 minute test cycle was conducted for each PWB. Therefore, the PWBs were not cycled to failure. Figure 7 illustrates the HALT profile.

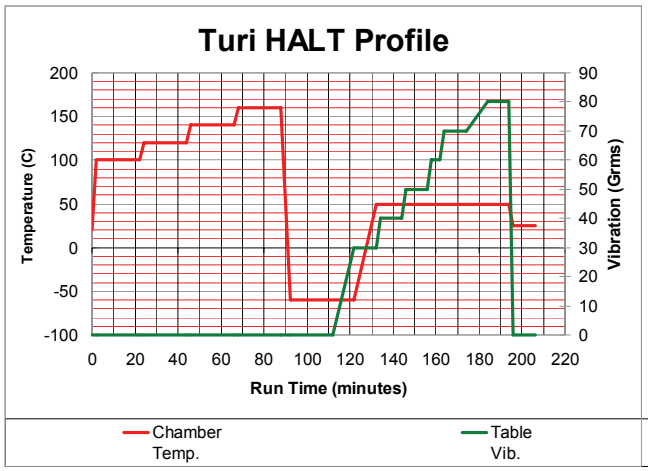

Figure 7 - HALT Profile

In addition, dynamic testing was done for seventeen daisy chained links. Numerous components were included on each daisy chain. Figure 8 shows a Phase III PWB in the HALT chamber with the daisy chain connection.

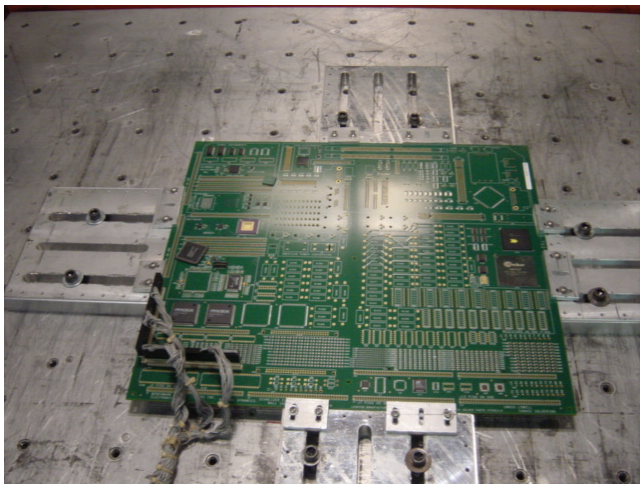

Figure 8 – PWB in HALT Chamber

During the HALT testing, components U1 (plastic leaded chip carrier) and U78 (ball grid array) were considered to be the only component failures due to solder joint failures. Other component failures were due to lead fractures caused by the high mechanical stress. The HALT testing did not reveal any major differences between the reliability of the lead-free and tin/lead PWBs. Visual inspection will be conducted on the HALT PWBs to further assess the validity of these preliminary conclusions.

Phase III Pull Testing

The test methodology consists of using an Instron pull test machine to pull the leads of a component and record the maximum pull force. The following four components will be included in the pull test:

- 2 SOIC components with a tin finish
- 2 SOIC components with a tin/bismuth finish

Four (4) leads will be pulled on each of the SOIC components. The process of pulling the leads will be as follows:

1. The PCB is loaded at a 45 degree angle to the Instron machine and affixed with 6 screws to a specially designed hold down fixture. A 45 degree angle was chosen to measure both vertical and shear stresses.
2. The leads adjacent to the ones that will be pulled will be removed (clipped) to facilitate pulling of target leads.
3. The leads that will be pulled will be tied with a wire loop through the component leads. Fishing line (#24 lb test) will be used for pulling the SOICs.
4. A new loop will be made for each component pulled.
5. The pull rate will be 0.1 inch per minute, and recording the peak pull force.
6. The fractures will be inspected and failure mode for each pull will be noted.

The pull testing will provide information for comparing the levels of solder joint strength between lead-free and tin/lead PWBs, as well as comparing the solder joint strength before and after thermal cycling. Four spare PWBs will be pulled prior to thermal cycling, and 18 PWBs will be pulled post thermal cycling.

Phase III Overall Results and Conclusions

Based on the visual inspection results, the solder joint integrity for SMT components on the lead-free PWBs was comparable to the tin/lead PWBs for the selected solder paste suppliers, laminate suppliers, and board surface finishes. Therefore, attaining acceptable solder joint integrity with lead-free assembly is possible using existing equipment and with careful selection of materials. Conclusions regarding the reliability of the solder joints will be published upon completion of the analysis of the HALT PWBs, and the pull testing of the PWBs that underwent thermal cycling.

The rate of solder joint defects for THT components was higher for lead-free PWBs than for tin/lead PWBs. Therefore, the consortium may undertake further process optimization for THT components.

Efforts were underway at the time of submission for this paper in the following areas: post-HALT visual inspection, failure analysis of interconnect stress test coupons, and pull testing.

The results from the post-HALT visual inspection, failure analysis of interconnect stress test coupons, and pull testing will be presented during the IPC Printed Circuit Expo, APEX, and Designer Summit 2006 in Anaheim, California.

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- Niton LLC for providing a portable XRF analyzer for verification and non-destructive analysis of lead content in the various materials included in the experiment.
- Teradyne for providing HALT test facilities and testing expertise for Phase III.
- Raytheon Company Reliability group for providing their testing expertise and the equipment for thermal cycling of the PWB's.

References, Consortium Publications and Presentations

[1] Lead Free Electronics Workshop, hosted by Lucent Technologies, Merrimack Valley Works, North Andover. MA, Tuesday April 13, 2000. Lecture by Dr. Sammy Shina, UMass Lowell Faculty

[2] TURI Continuing Education Conference, "TURI in Massachusetts: The Next Generation" on Tuesday April 25th 2000, Session, C2, the Lead Free electronics, at the Best Western Royal Plaza and Trade Center, Marlborough, MA, by Dr. Sammy Shina, UMASS Lowell Faculty.

[3] State of Massachusetts Legislative committee on education policy, UMASS President Bulger's Office, May 4th, 2000, presented by Karen Walters of BTU, a member of the Massachusetts Lead Free Electronics Consortium.

[4] IMPAS New England, 27th annual symposium and exhibition, Tuesday May 9th 2000, Holiday Inn Conference Center, Boxborough, MA, session F, Surface Mount Technology, presented by Hemant Belbase, UMass Lowell Graduate Student.

[5] CEAM/TURI Conference on University Research in Sustainable Technologies Program (URST) at UMass Lowell, June 2nd 2000, presented by Hemant Belbase, UMass Lowell Graduate Student.

[6] 2nd Workshop on Lead-Free Electronics, Technical Issues and Challenges in the Transition To Lead-Free Technologies, Thursday, June 29, 2000, at BTU International North Billerica, Massachusetts, presented by Karen Walters of BTU.

[7] Consortium authors, "Design Of Experiments For Lead-Free Materials, Surface Finishes And Manufacturing Processes Of Printed Wiring Boards", published by the SMTA International Conference at Rosemount Trade Center, Chicago, IL, September 2000, presented by Karen Walters of BTU.

[8] Consortium authors, "Design Of Experiments For Lead-Free Materials, Surface Finishes And Manufacturing Processes Of Printed Wiring Boards", published by the Chinese Electronics Association Journal, in Chinese

[9] Consortium authors, "Selecting Material and Process Parameters for Lead-Free SMT Soldering Using Design of Experiments Techniques", APEX Conference, January 2001, San Diego, CA, presented by Karen Walters of BTU and David Pinsky of Raytheon, members of the UMass Lowell Lead-Free Consortium

[10] "Lead-Free at UMass Lowell", Workshop on Modeling and Data Needs for Lead-Free Solders, sponsored NEMI, NIST, NSF, and TMS, Thursday, February, 2001, New Orleans, LA, short summary by Dr. Shina

[11] Consortium authors, "Reliability Testing Techniques for Lead-Free Soldering of SMT Technology", ETRONIX Conference, Anaheim, CA, March 2001, presented by Don Abbott of TI and David Pinsky .of Raytheon Material Engineering.

[12] Above paper translated into Japanese Journal ANBE, SMT, Kanagawa, Japan, July 2001

[13] Presentation by Karen Walters on the project research to the SMTA Georgia Chapter in Atlanta, Georgia, April 19, 2001

[14] Presentation by Karen Walters on the project research to the IMAPS Boston Chapter in Marlboro, MA May 8th, 2001

[15] Consortium authors, “Process and Material Selection for Zero Defects and Superior Adhesion Lead-Free SMT Soldering”, the SMTA International Conference, Chicago, IL. September 2001.

[16] Consortium authors, “Lead-Free UMass Consortium”, conference sponsored by the Strategic Envirotechnology Partnership (STEP), Boston MA, November 2nd, 2001, presented by Sammy Shina.

[17] Book Chapter on Design of Experiments for Lead-free soldering, ““Environment Friendly Electronics: Lead-Free Technology,” J. Wang editor, published by Electrochemical Publications Ltd in November 2001

[18] Mass Lead-free Consortium Status Update; Annual New England IMAPS Symposium; IMAPS Chapter Symposium, May 2003; Boxborough, MA, Presented by Dick Anderson of MA/Com.

[19] Consortium authors; “Materials and Processes for Surface Mount Lead-Free Soldering”, proceedings of the APEX Conference, Anaheim, CA, March 2003, pp. 20-2-1/9, presented by George Wilkish and Helena Pasquito of MA/Com

[20] Consortium authors, “Testing Results for Lead-Free PWB’s by the Massachusetts Lead-Free Electronics Research Consortium”; 2003 IEEE International; Symposium on Electronics and the Environment (ISEE); Boston, MA, May 2003. Presentation By R. Anderson of MA/Com.

[21] Shina et al; Consortium authors. “A Comparative Analysis of Lead-Free Materials and Processes Using Design of Experiments Techniques”, SMTI International, Chicago, IL, September 2003

[22] Shina et al; Consortium authors. “Lead-Free Conversion Analysis for Multiple PWB/Component Materials and Finishes using Quality and Reliability Testing”, APEX conference, Anaheim, CA, February 2004.

[23] Shina S. And MacFadden T., “Lead-Free Conversion issues in Component and PWB Surface Finishes”, SMT Journal, May 2004, p73.

[24] Previous paper translated to Korean for Chomdan Publishing Company in Korea.

[25] Shina S. and Morose, G., “Analysis of Testing Results of Surface Mounted Lead-free Soldering Materials and Processes, Pan-Pacific Microelectronics Conference, January 2005.

[26] Shina S. and Morose, G., “Reliability Testing Results of Surface Mounted Lead-free Soldering Materials and Processes”, APEX conference, Anaheim, CA, February 2005.