Reliability of Partially Filled SAC305 Through-Hole Joints

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Abstract
Consistently achieving acceptable wave solder through-hole fill on thick boards is a well-known process challenge, but the introduction of lead free solders has created additional difficulties. There are many reasons why one might achieve lower fill with lead free solders and there is much room for improvement in flux materials and process development, but unnecessary scrap and rework may be avoided by allowing lower barrel fill in some cases.

Most OEMs have a waiver process to allow lower barrel fill than required by IPC-A-610D Acceptability of Electronic Assemblies for individual holes, but it seemed critical to gather more information for lead free solders in order to support the possibility of lowering the fill requirements for more boards and components by class. This study updated the previous work that had been done on through-hole reliability by considering joints made with Sn-3.0Ag-0.5Cu (SAC305) solder and a range of fill percents, including lower fill percents than are required by IPC-A-610D.

SAC305 through-hole joints (with components loaded) were soldered on 0.062", 0.097", and 0.130" thick boards, with fill percents between 10% and 100%. These boards were subjected to thermal cycling, shock or vibration. After the stress exposure, the pull strengths of the joints were measured.

The data showed that pin wetted length correlates well with the pull strengths of through-hole joints for different PCB thicknesses. Shock and vibration were the most detrimental stressors in the range tested. Minimum fill requirements were determined, based on board thicknesses and load per pin. This work has shown that lower fill levels than are sometimes required by IPC-A-610D will produce reliable SAC solder joints.

Introduction
Consistently achieving acceptable through-hole fill on thick boards has been a process challenge for decades, even with Sn-Pb solders. The introduction of lead free solders has created additional difficulties for many reasons, including:
Surface tensions of the replacement solders inhibit the wicking of the proper amount of solder volume into plated through-holes (PTHs),

Currently available fluxes are not able to compensate for the wetting performance of the alloys without being unduly aggressive,

In the case of selective soldering, higher temperatures required for replacement alloys make the shielding of SMT components near PTH components more critical and reduces the thermal contact of board to pre-heaters or to the wave itself, such that pins close to pallet openings are harder to fill, and

Familiar problems with soldering power and ground plane connected pins on thick boards have been exacerbated by the new alloys and the process temperatures that they require.

Although there is much room for improvement in flux materials and process development, considering the vastly superior mechanical strength of through-hole joints over surface mount joints (whether leaded or lead free), it may be reasonable to avoid unnecessary scrap and rework by allowing lower barrel fill in some cases.

The through-hole fill requirements in IPC-A-610D Acceptability of Electronic Assemblies have not changed with the introduction of lead free solders. Class 2 and 3 products require vertical fill of 75% for most holes and allow 50% fill for plated through-holes (PTHs) connected to power or ground planes. These planes act as heat sinks during the soldering process drawing heat away from the intended bonding site. This retards flux activation and barrel fill. Manufacturers will often struggle with hand soldering or solder fountains to correct under-filled through-hole solder joints, which can result in decreased assembly reliability due to:
Additional thermal exposure of laminates and components[1]

Thicker intermetallic layers (brittle bond lines)

Trace, ring and barrel thinning from copper dissolution during exposure to solder fountain

Mechanical damage from the additional handling for rework processes

Pooled, un-activated flux deposits from rework that reduce service life with corrosion or electrochemical migration failures

In addition, there is the obvious expense of rework and scrap that should be avoided as long at the product meets targeted reliability goals.

For 0.062" and thinner boards, the 75% requirement not only ensures mechanical strength but also avoids masking process deficiencies. However, for thicker boards or for high pin count/low load per pin components, like DIMM sockets, these requirements may be unnecessarily high, which if reworked may potentially decrease the overall reliability. Complete fill is still the desired goal, but due to the practical difficulty of filling through-holes with the flux materials currently available and the risks and expenses of reworking through-hole joints, there is a need to consider lowering the fill requirements for more boards and components by class and also to provide guidance on how to disposition material in the cases of widespread deficiencies in PTH barrel fill.

Background

Wild (IBM) did seminal work on through-hole fill examining the reliability of filled and unfilled PTHs. As early as the 1970s, IBM was having trouble achieving 75% fill with Sn-Pb wave soldering on thick boards, and investigated whether a fill lower than 75% could still meet reliability requirements.[2, 3]

A later experiment looked at thermal fatigue for 0%, 15%, 25%, 50%, 75%, 100% fill on 0.118", 0.140" and 0.200" thick boards when cycled from -55 to +105C. No failures were observed to 535 cycles as long as PTHs had at least 25% PTH fill.[4] Although cracks were seen, there were no PTH solder joint failures when pins had at least 15% solder penetration (0.030" wetted length).

High reliability products with challenging through-hole soldering situations spurred periodic engineering efforts to understand whether PTHs with vertical fills below the levels required by IPC-A-610 would meet the reliability need of the users. This work usually lead to localized waivers based on case-by-case evaluations, often after significant quantities of high-value boards had been built with lower than required barrel fill.

For example, low PTH barrel fill at a contract manufacturer sparked a crisis in the AlphaServer Division of Compaq in 2001, when hundreds of high value, high reliability boards were found to have lower barrel fill than required by IPC-A-610. Extensive computer modeling and validation testing were completed to determine if the fill levels on those particular components (DIMM sockets, PGA, and PCI connectors) in the expected loading and environment would meet the needs of the user. The finite element analysis, accelerated thermal cycling, and pull tests revealed that the 75% fill requirement was very conservative for the components in question, and it was demonstrated that a minimum of 25% barrel fill (~0.015in pin wetted length) with a 180deg circumferential solder joint of well-wetted solder was enough to meet or exceed the product service life requirements.[5]

Evidently there was ample evidence with Sn-Pb that fill requirements could be lowered without negatively impacting product reliability; especially considering that though-hole joint failures are relatively rare.[6] There was an urgent need, however, to understand the impacts of lower fill for lead free solders, given the observed difficulties in achieving complete fill. A set of experiments was devised and completed to determine the equivalent minimum fill guidance for SAC305 through-hole solder joints.

Experiment

Sn-3.0Ag-0.5Cu (SAC305) and Sn-37Pb through-hole joints were soldered on 0.062", 0.097", and 0.130" thick OSP boards, generating vertical fill percents between 10% and 100%. Figure 1 shows a loaded test vehicle. The test component for the measurements was a 278 pin DIMM connector, with Sn over Ni plating on rectangular 0.165" long pins. Finished hole size was 0.031".

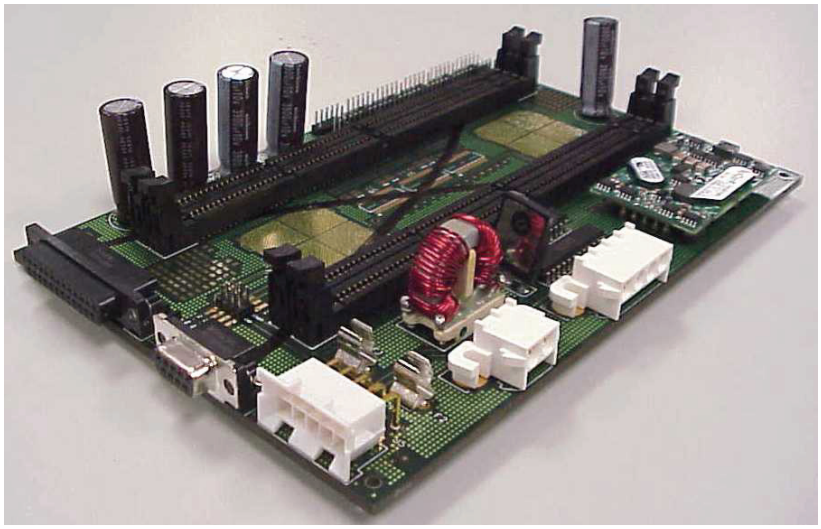


Figure 1: Test vehicle

Table 1: Preconditioning Prior to Pull Strength Measurements

	Current Study	
Random vibration	1, 4, and 9g-rms 1hour per axis	0.0016 to 0.017 lbs per pin
Shock	200g, 400g 1 shock per axis	0.35 to 0.70 lbs per pin
Thermal cycling	+25 to +100C 500, 1000, 1500, and 2000 cycles	

Test boards were subjected to thermal cycling, shock or vibration according to the conditions in Table 2. After the stress exposure, the pull strengths of the DIMM connector through-hole joints were measured and the vertical fill was recorded or estimated.

The pull strength of each joint was measured on an Instron Model 5544, with fixturing that allowed independent pin selection. The strain rate was 1mm/min. Vise grips with modified tips were used to facilitate pin access, as shown in Figure 2. Over 3500 pins were measured during the testing phase.

Figure 2: Tester with modified vise grip and fixture

The vertical hole fill was calculated by first measuring the length (from the tip of the pin) of the mark that the solder left on the pin during the soldering/wetting process (Figure 3). This was done for each pin after extraction. Red dye was applied before the extraction to help in the identification of the wetting mark.

Figure 3: Pin extracted showing solder wetting mark

The pin protrusion (extension of the pin out of the board) was then subtracted from this measurement, naming this new converted measurement as Pin Wetted Length (PWL). Finally, the PWL was divided by the board thickness. To summarize, the following equation (1) was used to calculate the vertical fill:

$$\text{Vertical hole fill} = \frac{\text{Wetting mark} - \text{pin protrusion}}{\text{PCB thickness}} = \frac{\text{Pin wetted length (PWL)}}{\text{PCB thickness}} \quad (1)$$

Equation (1) assumes nominal dimensions and that no PCB-component separation occurs. Since the pin geometry was rectangular, two length measurements were taken on opposite sides for each pin. During the test, non-uniformity in vertical fill was observed on the same pin. This was measured by the difference (delta) in length values from both sides of the pin. A pictorial representation of this effect appears on the left pin on Figure 4.

This condition is frequently observed in through-hole joints produced by wave soldering. Empirical data for non-uniform fill appears to support the theory that the larger this delta, the higher the pull force required to separate the pin from the PCB. It was also understood that the pull force obtained from a non-uniform fill joint was comparable to the force due to a uniform fill at the middle of the delta. Therefore, the PWL was calculated by measuring the total length after extraction of the pin wetted by the solder on opposite sides and averaging the two values.

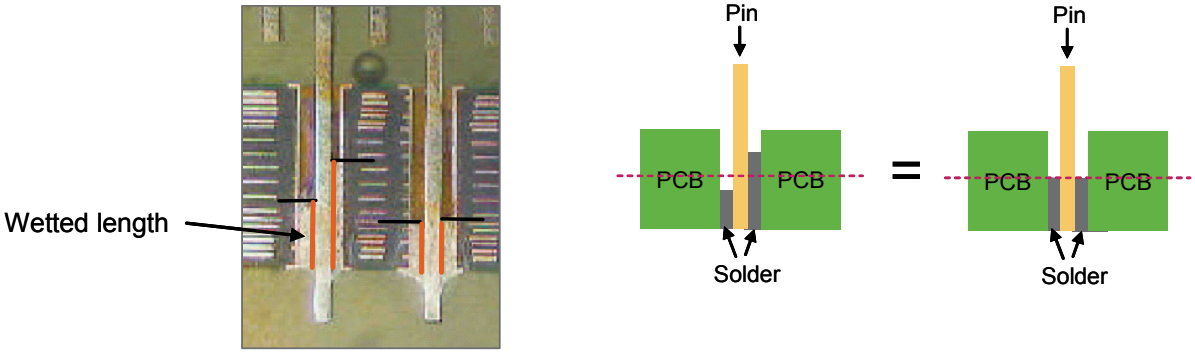


Figure 4: Non-Uniformity in Vertical Fill

Pin Wetted Length (PWL) was used as the metric rather than the vertical fill percent as defined in IPC-A-610D because PWL does not depend on board thickness, as seen in the Formula (1). Figure 5 shows equivalent PWL corresponding to different vertical fill percent depending on board thickness.

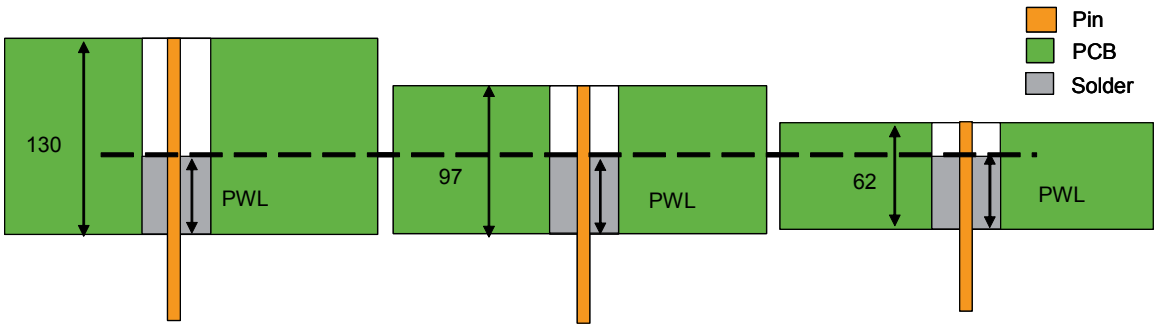


Figure 5 - Equal pin Wetted lengths (PWLs) Correspond to Different vertical Fill Percents Depending on Board Thickness

Results

SnPb vs. SAC 305

In this study pins were pulled with SnPb and SAC305 solder alloys in printed circuit boards with 0.130" thickness. The initial comparison used boards with no pre-stress condition. Figure 6 presents a scatter diagram for the pull force as a function of pin wetted length (PWL). The wetted length obtained for SnPb alloy appears to be higher in general; this is consistent with manufacturers experience when introducing SAC solder alloys with similar process conditions used for SnPb. For the same PWL, pins soldered with SAC305 provide higher pull force. This can be confirmed by considering the linear regression model obtained for the data shown. The ordinarily least squares (OLS) model is:

$$\text{Force (lbf)} = 7.79 + 0.154\ \text{Pin Wetted Length (mils)} - 1.12\ \text{SnPb} \qquad (2)$$

In this model the coefficient for variable SnPb is interpreted as the displacement in the intercept due to the pins soldered with SnPb as compared with SAC305 pulled pins. The negative coefficient in (2) indicates that the pull force obtained from SnPb pins for the same minimum length is lower than the SAC305 pins by 1.12 lbf. on average.

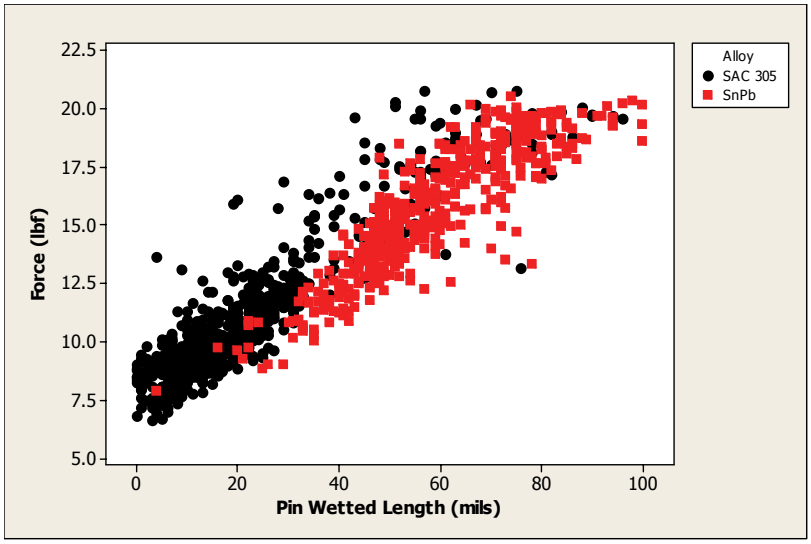


Figure 6: Pull Force as a Function of PWL for SnPb and SAC305 Solder Alloys

Before Stress
The use of PWL was studied by plotting the force versus PWL for the three board thicknesses, 0.062", 0.097" and 0.130", soldered with SAC 305, and verifying that the data was not statistically different, as seen in Figure 7.

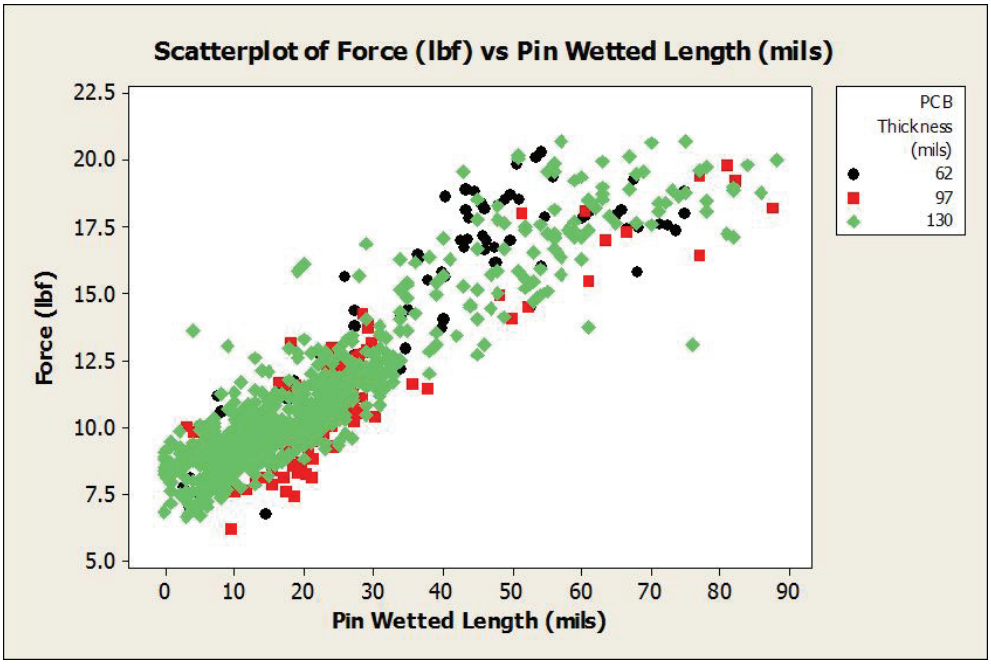


Figure 7: PWL correlates to joint strength regardless of board thickness for both alloys

No appreciable difference among PCB thicknesses can be seen in this graph, indicating that PWL controls the through hole joint strength instead of the current criteria of hole fill percentage. Therefore PWL was used, rather than vertical fill percentage, for the analysis and presentation of the results.

After Stress
Pull forces for the various stress conditions are shown in Figure 8 for SAC305.

For a given PWL the analysis in the previous section demonstrated that on average both solder alloys provide almost the same pull force with a minimum advantage for the lead free alloy. The analysis that follows includes stresses to lead free solder joints. Loaded printed circuit boards were subjected to three different stresses: vibration, shock, and thermal cycling. Once more the 0.130" board thickness was considered. Stress conditions included 1000, 1500 and 2000 cycles (25°C to 100°C) for thermal stress (ATC), 200g for shock and 1g-rms, 4g-rms and 9g-rms for vibration. Baseline refers to non-stressed joints. Figure 8 presents scatter diagrams for all these stress conditions. When compared to the baseline (no stress condition) certain degradation in the pull force is observed for shock and vibration stresses, while thermal cycling does not appear to have a detrimental effect on the pull force.

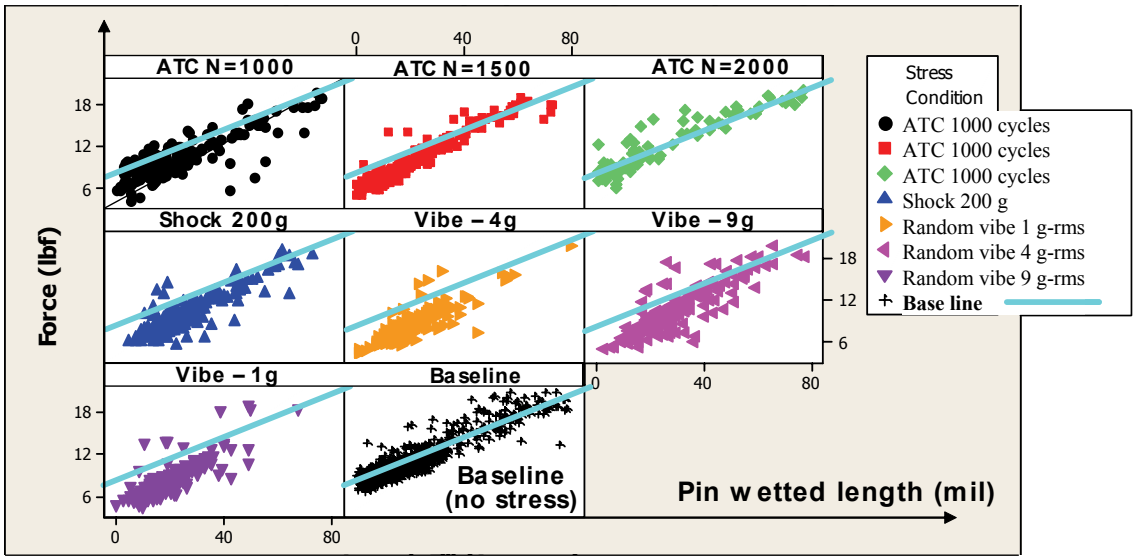
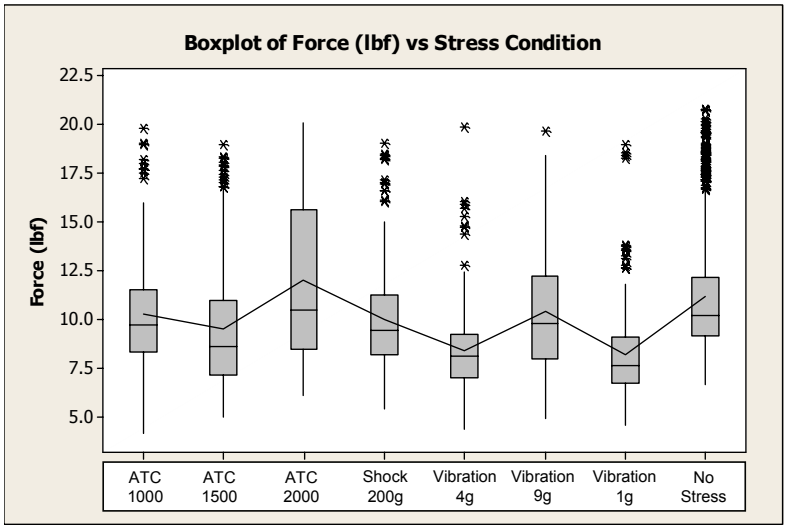


Figure 8: Joint Strength vs. Pin wetted Length for each Stress Condition for SAC305

Figure 10 shows a summary of the effects of stress conditions on joint strength for SAC305. This data was generated after linear regression was performed on all the data sets and after it was observed that there was very little influence of the stress level on the residual strength in the range studied. In the case of thermal cycling, it is speculated from previous work that cracking develops, but does not propagate far in the barrel. There was some degradation of through-hole joint strength for both alloys due to thermal cycling and shock, but vibration caused the largest drop in joint strength (25% for SAC305) indicating that random vibration causes the most significant degradation for low PWL. For very low PWL with loads corresponding to less 4 lbs, there is some departure from linearity after thermal cycling and it is speculated that cracking may have been significant compared to the PWL.

Figure 9: Box plots of effects of stress conditions on joint strength for SAC305



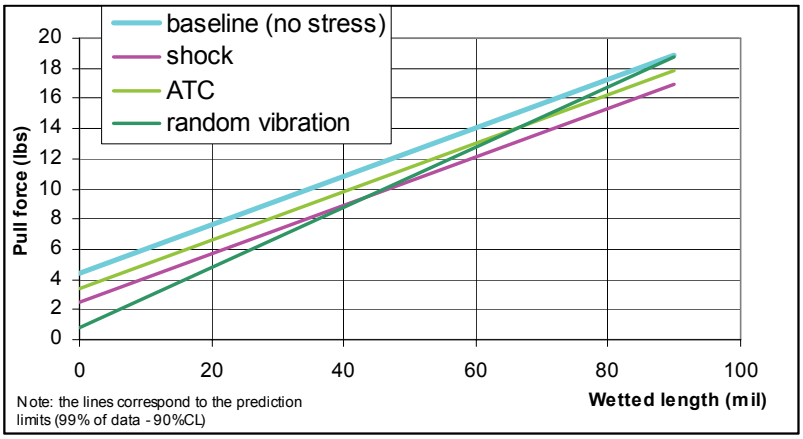


Figure 10: Effects of Stress Conditions on Joint Strength as a Function of PWL for SAC305

Discussion

Even with some degradation, the residual through-hole joint strengths observed in these tests are generally much higher than surface mount joints and could be far above what is needed for service conditions for many applications. Several assumptions and simplifications were made to determine the minimum residual strength needed to provide sufficient reliability in the service environment.

The following stresses were considered:

Static (for example, the insertion of a DIMM card into the corresponding DIMM socket),

Thermal (fatigue induced by temperature fluctuations and mismatch of thermal expansion coefficients), and Shock and vibration (induced during transportation or normal use).

In the particular case of DIMMs, static loads were estimated from previous mechanical testing simulating DIMM card insertion. For thermal loading, the temperature cycling carried out up to 2000 cycles between 25C and 100C is more severe than the effect of temperature excursions anticipated in the field for most HP products. Finally, for shock and vibration, the stresses seen by solder joints in the field or during transportation were estimated using the component mass per pin and the maximum acceleration levels anticipated in the field.

For low mass-per-pin components, including small capacitors and DIMM sockets, the upper bound of the loads the joints see in the field was estimated at 5 lbs, which is driven by shock requirements. This provides a simple criterion; the barrel fill and PWL should be such that the residual pull strength is greater than 5 lbs. This can easily be determined from the graph showing the residual pull strength as a function of the PWL. For higher mass-per-pin components, the same methodology can be used to estimate the upper bound of the load per joint seen in the field. However, in this study, the stress level to which the joints were subjected during the shock and vibration tests was too small to draw any rigorous conclusion. It is recommended to generate additional data either at higher acceleration levels on DIMM joints or, more simply, with parts having a higher mass per pin. The only qualitative information collected regarding heavy components was that the large capacitors seen on the test vehicle in Figure 1 did not fall off the boards after the shock and vibration test, but no residual strength data was gathered.

To compare the pull strength as a function of the PWL to the previously described criterion, the data was first condensed into a single line since there was significant scatter. The 90% prediction line was chosen to increase the weight given to the weakest joints. Designers are generally more interested in the tail of the distribution than the average, since the tail will indicate possible early failures.

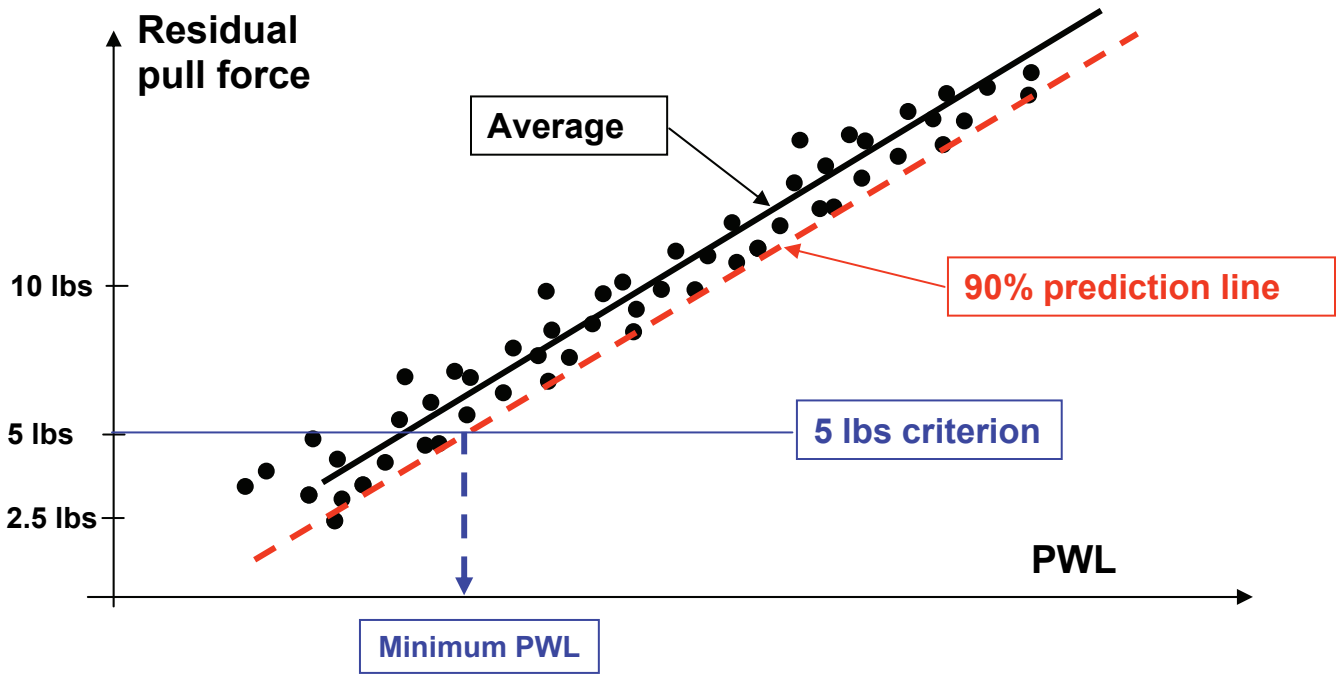


Figure 11: Determining minimum PWL based on test results
It is important to note that there are no safety factors in the minimum PWL values determined from the raw data with this approach. For low-load-per-pin parts on thick boards, the corresponding vertical fill percents can be quite low, although consistent with Wild's findings for SnPb that found no failures with vertical fills as low as 15%.

Figure 12 shows the minimum vertical barrel fill percent for SAC305 as calculated from the minimum PWL values with no safety factors for cumulative damage or measurement errors. As a reference value, the minimum PWL corresponding to joints that have not seen any stresses is also included in Figure 12.

PCB Thickness	Low mass pin		High mass pin	
0.130"	No stress	Vibration	No stress	Vibration
	5%	**16%**	**28%**	**35%**

PCB Thickness	Low mass pin		High mass pin	
0.097"	No stress	Vibration	No stress	Vibration
	6%	**22%**	**38%**	**47%**

PCB Thickness	Low mass pin		High mass pin	
0.062"	No stress	Vibration	NC	Vibration
	10%	**35%**	**60%**	**75%**

Figure 12: Theoretical Minimum Vertical Hole Fill for SAC305 for Surviving Random Vibration

Although it is useful to have guidance on individual hole fill as described above, of more interest is the generic case of board level recommendations. Assuming that the load per pin is unknown across an assembly, the worst case assumes that there are high-load-per-pin components, and we can set the minimum acceptable vertical fill according to the higher levels, as shown in Table 2.

Table 2: Alternate acceptability Criteria for Thicker Boards

		IPC Product Classes		
		Class 1	Class2	Class3
Current IPC-610D Criteria	Minimum barrel fill percentage of solder	Not specified	75% (signal) 50% (ground)	75% (all)
	Minimum Pin Wetted Length (PWL) on a 62 mils board (based on criteria above)	Not specified	46.5 (signal) 31 (ground)	46.5 (all)
Alternate Criteria	* Minimum barrel fill percentage of solder for a 130 mils PCB thickness	Not specified	36% (all)	36% (all)
	* Minimum barrel fill percentage of solder for a 97 mils PCB thickness	Not specified	48% (all)	48% (all)
	* Minimum barrel fill percentage of solder for a 62 mils PCB thickness	Not specified	75% (all)	75% (all)

Recommendations

It is critical that process engineers continue to improve wave solder processes and materials to try to reach the 100% vertical fill target. The work described in this paper is not meant to undermine progress in these important areas. However, when process and material options have been exhausted and 75% vertical fill is still not possible with SAC305, engineering judgment can be used, as it has with SnPb in the past, to allow lower vertical hole fill in some cases. The results presented in this paper may be used to expand the lower fill requirements beyond the narrow exceptions listed in IPC-A-610D.

However, it is notable that the acceptability criteria for HP products have not changed, and for most cases rely on the current IPC-A-610D requirements. These proposed alternate criteria are only invoked in certain cases, such as thick boards with low-load-per-pin components like DIMM connectors, and with the help of engineers to determine the appropriate applications. For example, if DIMM connectors on 0.130" thick boards have a few pins with less than 75% vertical fill, these alternate criteria could be used by engineers to waive rework. Conversely, 0.062" thick boards should all meet the 75% fill requirement not only to create joints with adequate physical strength, but also to avoid masking a poor process or degrading an assembly through multiple rework attempts to achieve better barrel fill.

Future Work

More sophisticated sorting of component types and pin geometries will be completed to provide specific help to engineers faced with these decisions, and data will be collected on heavier components. Also, there is some interest in considering cumulative damage, such as thermal cycling after shock or vibration, since that combination of stresses would more closely match the environment in which these connectors would be utilized. Additional levels of shock and vibe using loads on the connectors or using heavier components to simulate heavy backplanes are under consideration for a more detailed view of the field behavior of these connector systems.

Another area for future work may be around barrel cracking in partially filled holes because laminates exposed to lead free process temperatures are already struggling to meet PTH reliability requirements in many cases, and it may be important to understand if lower fill levels reduce PTH reliability. The effect of lower fill level on electrical or RF response may also be important information for the newer high speed connector systems.

Given that one of the central motivations for this work was to avoid unnecessary through hole rework, a comparison study of reworked versus non-reworked barrels would likely be useful in understanding when to use the adjusted fill requirements.

Acknowledgements

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