Prediction of Digital Circuit Board Reliability Using Computational Reliability Modeling

Loren Nasser, Robert Tryon
VEXTEC Corporation
Brentwood, TN 37027

Abstract
A process called computational reliability modeling is described herein as well as how the reliability predictions from this modeling approach match experimental data (both lead and lead-free solder). It is described that material simulation is rolled up to the overall board or system level to predict overall electronics reliability.

Introduction
The cost of physical tests is rising. The cost of computer cycles is plummeting. It seems only common sense to replace the former with the later. The practicality of replacing the old "test it" paradigm with a "compute it" paradigm will be described by this paper. The reliability of the digital circuit board is a function of the reliability of all of the parts, including interconnections. If component and interconnection reliability is sufficiently understood, it becomes possible to mathematically model the contributions to overall system reliability. This is accomplished using well understood and accepted simulation techniques. Furthermore, it is possible to apportion a top down 'reliability budget' on system component parts based on a needed overall system level reliability. This top down technique allows engineers to robustly explore 'what if' options by analytically gauging the trade-off of reliability improvements in specific components against the costs of making those improvements. Disregarding operator error, products fail because of a material failure in a component or interconnect. As an example, materials fail because repetitive stress applied over time causes internal micro-structures (e.g. grain domains) to move or distort sufficiently to nucleate a discontinuity which leads to the propagation of a small crack, leading to a larger one, and finally to outright material separation and failure. With inputs from all load and geometric conditions, plus parameters inherent to the material itself, this process is physically deterministic at some fundamental microstructural level. At the lowest scale, computational reliability modeling considers the randomness of grain properties that gives rise to the failure mechanisms observed in real physical systems—macroscopically identical parts subjected to the same stress profile will fail differently, with a probability distribution governed by the specifics of the grain structure and part geometry. In order to predict overall board reliability, the modeling process rolls up material failure to the overall system level.

Electronics, are reliant on the integrity of interconnects or solder bonds. The reliability of interconnects is a concern because it is widely expressed that fracture failures in solder joints accounts for up to 70% of failures in electronic components. Conventionally the reliability of electronic devices is assessed using empirically based models. Design of experiments is a commonly used tool in which the experimental conditions are systematically varied and a mathematical relationship is "fit" to the data that represents the influence of the conditions to the time or cycles to failure. However, one problem is the fact that there is so much variation in the time or cycles to failure that device life can only be conveyed in the form of a statistical average, such as mean time to failure (MTTF) or the mean time between failure (MTBF). Although these statistical averages provide a general sense above average overall failure, and they are a hold over from a time when computer processing power was expensive. They only provide information on a single point number and with no insight about real world probabilistic variation, true failure mechanisms or the impact those mechanisms have on how a specific design will react to actual field conditions.

None of the electronics industries traditionally used fatigue models account for the large scatter in the solder weld properties. The nature of the packaged components and variability within the assembly process creates large variations in the solder welds for even the strictest manufacturing tolerances. The very small size of the welds causes variation of the weld footprint from weld to weld. In addition, the microstructural development of the weld is greatly controlled by rate of cooling from the melt stage. Conventionally used electronic device reliability prediction, largely empirically derived, do not account for this real world variability.

Interconnect Fatigue Simulation
A machine can fail even though the stresses on its parts are well below a constant load failure level. This is classic fatigue, and is caused from fluctuating loads applied numerous times. It is estimated that perhaps 90% of all machine failures are caused by fatigue. Although less obvious, this same mode of failure applies to static structures as well. Static structural components are subject to vibrations and movements created from thermal expansion and contraction. Though the movements may be slight, large cyclic forces can result. Electronic systems are static structures that are subject to these same

types of phenomenon. Solder joints are particularly vulnerable to fatigue failure. As systems are powered up and down, these interconnect elements are subject to thermal gradient cycling, which, working in combination with vibration, impact, and shock loadings, creates dynamic conditions conducive to fatigue. The typical electronics printed circuit board (PCB) manufacturing processes, in which solder is melted and then cooled, creates joints with complex internal grain structures. These grain structures are under stress from the cooling process, and undergo continuous movement in response to these stresses. This movement, which is on going even as the system is sitting under nonoperating conditions in a warehouse, is in itself sufficient to contribute to fatigue vulnerability

In short, fatigue must be considered a primary mechanism behind electronics failure, and applying the types of modeling techniques advocated in this white paper can lead to major improvements in the understanding of electronic system reliability.

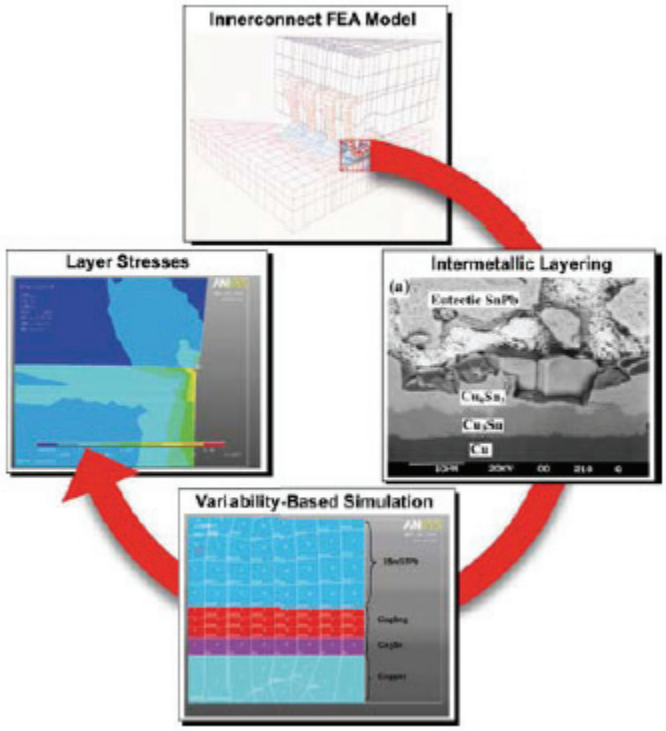

Figure 1 - Global Stress Translated to Local Microstructure Through Simulation of Intermetallic Layers in Solder

We base our methods for predicting fatigue failure on a proprietary virtual prototyping approach (VPS-MICRO™) that allows the simulation of real material behavior. The major inputs to this simulation are details on the grain structure properties of the material being simulated, and the external conditions the material experiences. Because grain structure orientation is randomly distributed through any macro sized structure, a Monte Carlo simulation is used to give a probabilistic distribution of fatigue failure outcomes over the operating life of the structure. In the case of solder joint interconnects, this process can be applied to all joints in the system, with each joint being appropriately loaded and heated depending on its position in the system.

Fatigue failure is a localized, material-driven process. An extensive amount of research has been conducted as to how and why cracks initiate and grow within solder connections. This knowledge was adopted within the developed local simulation modeling approach. High stresses are translated from global loadings to the local material. In particular these stresses exist at the interface between the copper lead and the solder. These localities are of compounded significance due to the existence of a complex microstructure of intermetallic layers between the copper and the solder. When molten Sn-Pb solder contacts the lead, intermetallic compounds (IMC) are formed between the solder and the lead. T o model the complex stress state of the microstructure at the copper/solder interface, finite element models were created by us for the copper/intermetallic/solder region (Figure 1). Because the thickness of the intermetallic layers change with time, a series of finite element models must be incorporated within the modeling approach.

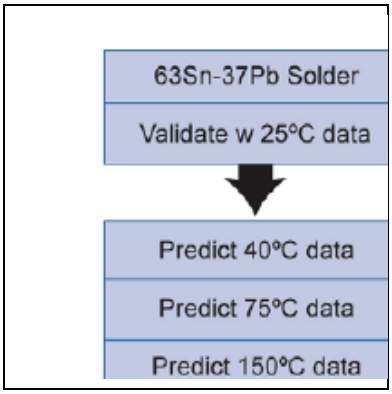

Figure 2 - Process Used for Predicting Lead and Lead- Free Solder Fatigue

Interconnect Fatigue Simulation Results

This documents our success in predicting lead solder fatigue response at high temperature based on model development with room temperature data. Thereafter, as indicated in Figure 2, it was assumed that the same failure mechanisms driving lead solder response were active in lead-free response and fatigue predictions were made for lead-free solder material. Prior to this effort research, we had only used our software model to simulate fatigue for aerospace materials and structures (i.e.: nickel, titanium, steel, etc.); therefore the first step was to develop an input library for solder alloys. Needed were the appropriate input parameters for simulation of damage mechanisms at the microstructural scale.

Table 1 - Input Parameters Required for Simulation of Lead Solder Fatigue

Parameter	Reference
Bulk shear modulus	Siewert et. al.[1]
Poisson's ratio	Siewert et. al. [2]
Grain size and phases	Liu et. al. [3]
Small crack growth coefficient	Unknown
Long crack growth coefficients	Zhao et. al. [4]
Frictional strength (Yield strength of the grain)	Siewert et. al. [1]
Grain boundary SIF	Zhao et. al. [4]
Orientation factor	Assumed
Specific fracture energy	Unknown

This simulation procedure must account for variations in material parameters like grain size, grain orientation, crack growth coefficients and inherent strength of the grains. Since 63Sn-37Pb eutectic solder alloy has been extensively studied by the electronics industry, this material seemed to be a logical starting point. Material performance data on this alloy are widely available at various temperatures and frequencies. Table 1 presents a listing of the model input parameters used for 63 Sn-37Pb simulations along with the references from which these data came. As indicated in the table, values for some parameters could not be found in the literature available to Vus. Therefore, engineering judgment was used to estimate these parameter values and fatigue was predicted for a strain range of 2%. These predictions were compared to experimental data in *Low cycle fatigue models for lead-free solders5*. Thereafter these few parameters were further tweaked until the model successfully replicated these limited experimental data at 25C. Upon achieving satisfactory results at 2% strain range, the complete 25C S-N (strain range – number of cycles to failure) curve was predicted for lower strain ranges (Figure 3). Unfortunately we had no experimental data available to compare with these predictions. As shown in Figure 3, the model predicts the expected scatter in fatigue life. The art and science of modern day fatigue analysis can now account for the real world microstructural variability that exists in solder materials.

This model, developed based on 25C data, was then used to make higher temperature predictions for the same SnPb solder alloy. This was accomplished by first studying the effect of temperature on the material properties of the SnPb solder and making appropriate modifications to model input parameters. Figure 4 shows the comparison of the predictions at 25C and 150C. Through the open literature, we were able to access a single 150C fatigue test data point for this material. As shown in the figure, this data point falls within the expected scatter at approximately 0.7% strain range. This suggests that the model can successfully simulate solder temperature effects. As expected, the 150C fatigue lives are lower than those at 25C. It is interesting to note that the model predicts that the effect of temperature is more pronounced at lower strain ranges than at higher ones.

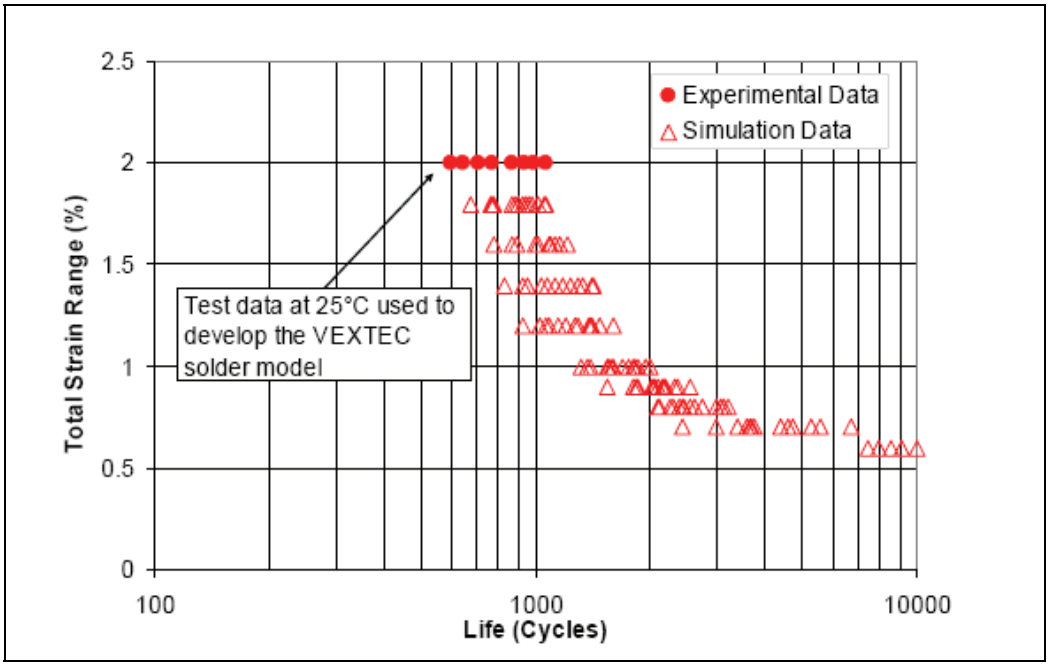

Figure 3 - Fatigue Simulation for 63Sn37Pb at 25C, 1Hz

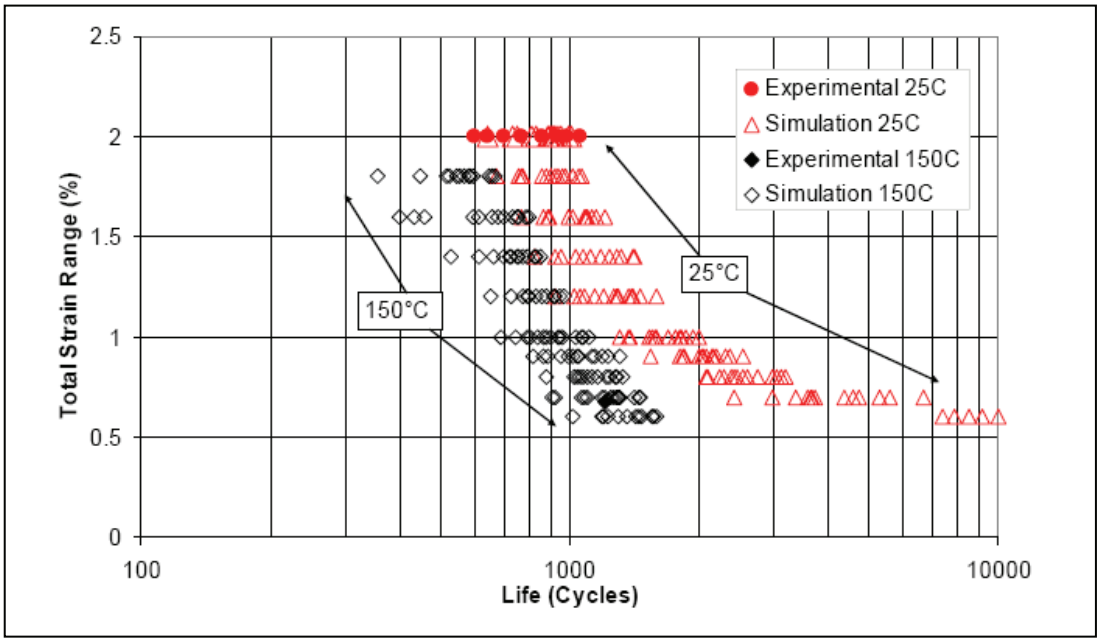

Figure 4 - Comparison of 63Sn37Pb fatigue predictions at 25C, 1Hz and 150C, 1 Hz

Simulations were also made at 40C, 1Hz and 75C, 1Hz since we were able to obtain a single test data point for each of these temperatures. A gain the actual fatigue test point was within the predicted scatter for the appropriate strain range; therefore, the model appears to be successfully predicting temperature effects on solder fatigue life. Figure 5 presents a comparison of the mean predicted life with experimental data at the appropriate strain range.

Prediction of Lead-Free Solder

As stated previously, it was assumed that the same failure mechanisms driving lead solder response were active in lead-free response. Therefore the VPS-MICROTM inputs were only modified to account for collected information about microstructural properties (i.e.: grain size) and bulk material properties. Thereafter our model was used to make fatigue

predictions for lead-free solder material. Since the national electronics manufacturing initiative (NEMI) has suggested that 95.5Ag-3.5Sn-1.0Cu solder has promising characteristics for wide spread electronic industry use, that material was selected for evaluation. The input parameters used in the model are listed in *Electronic material, variability-based, total life fatigue prediction approach*[6].

The model was used to make 25C, 1Hz fatigue predictions and compared with limited experimental data available in Pang et. al. As shown in Figure 6 predictions accurately capture the two experimental data points presented in the referenced paper. Along with the lead-free predictions, the earlier presented lead solder predictions at 25C are shown in Figure 6. The simulations show a very interesting feature, the lead and lead-free fatigue lives cross over. This suggests that lead solder actually performs better than lead-free solder at lower strain ranges. One possible reason for this could be the strain hardening effect that occurs when the lead-free solder material is at room temperature. This strain hardening nature was observed in one hysteresis loop assumed to be the cycle at half-life. Further data on cyclic hardening is needed to verify the strain hardening phenomenon. Further it must be noted that the results shown here are for a laboratory material specimen and not for an actual solder joint geometry. For an actual solder joint, other issues such as thermal residual stresses and intermetallics play a role influencing fatigue life.

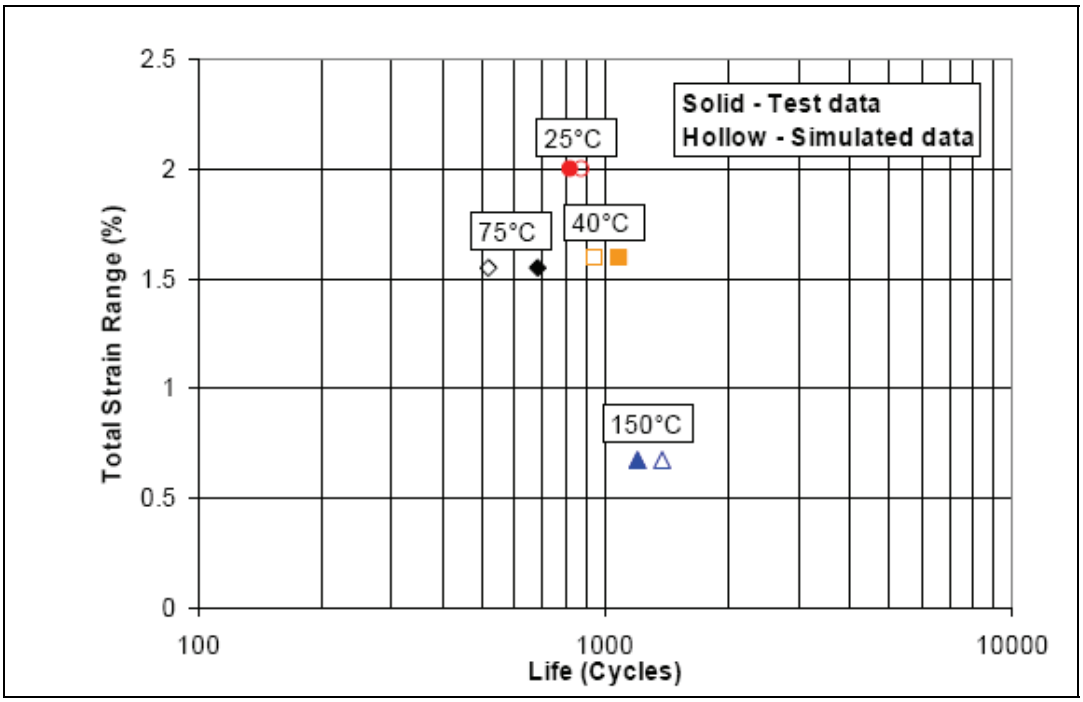

Figure 5 - Comparison of Mean Simulation Values with Test Data at Various Temperatures

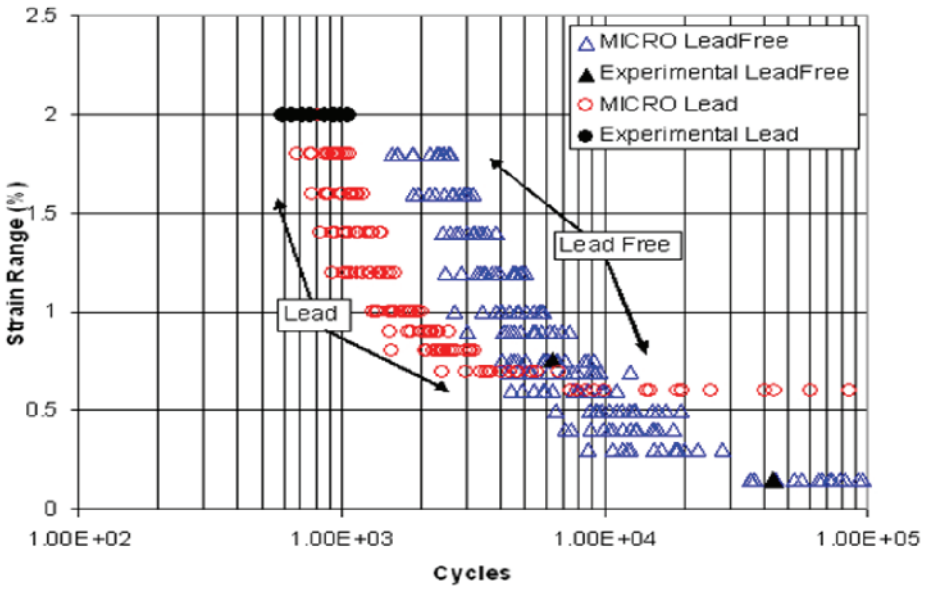

Figure 6 - Comparison of lead and lead-free solder predictions at 25C, 1Hz

The final step in this process was to verify that the model could successful predict the temperature effects on lead-free solder fatigue. Fatigue predictions at 125C, 0.001 Hz lead-free solder are presented in Figure 7. Within the modelt, only the material properties were modified to account for the temperature and frequency change effects. As shown these predictions compare well with single experimental result obtained from *Low cycle fatigue models for lead-free solders*[5].

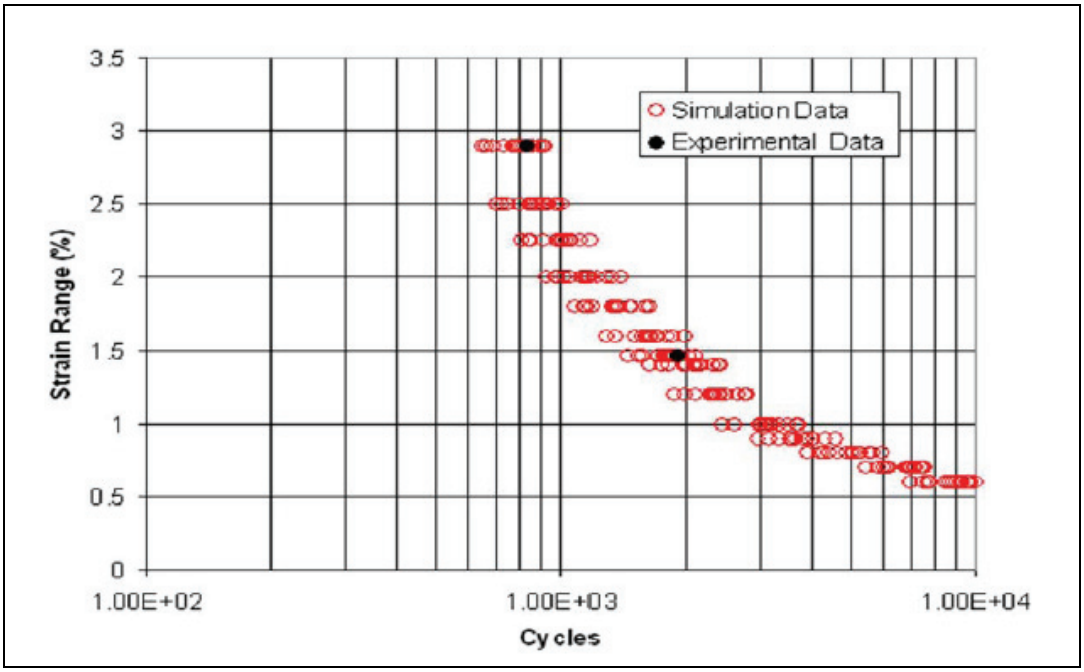

Figure 7 - Lead-Free Solder Predictions at 125C, 0.001Hz.

Reliability Roll-up

Our integrated vehicle test simulation software for prediction of overall vehicle and fleet reliability has been in use at DaimlerChrysler for 3 years. Given that the prediction results correlate well with field warranty data and integrated vehicle test data, integration of this approach with the previously described fatigue simulation is a logical next step. The system-level reliability "roll-up" methodology uses existing failure data, test data or reliability estimates for the various elements that make up the system. The simulation virtually "cycles" or tests the specified number of systems. If, as in the case of the automotive world, systems are repaired or replaced as failures occur – the simulation allows for that.

Overall vehicle electronics are a system of individual modules. The vehicle OEM has historic warranty records, test results, or engineering reliability estimates. Taking advantage of these data, the new CRM paradigm will serve to identify those modules that most critically define overall vehicle reliability and so that reliability specification goals can be established for Tier I contracts.

Tier I electronic modules are made up of any variety of printed wiring boards (PCB), devices (i.e.: monitors, controllers, etc) and connections. When an individual board is found to be compromising overall vehicle (fleet) reliability, corrective action could be to re-engineer the board or to procure a similar board from an alternative supplier. At the PCB supplier level, interconnect reliability is a primary cause of overall board failure. Interconnects are made of various materials (i.e.: lead, lead-free, etc) and material suppliers provide sources of variability that impact interconnect reliability (i.e.: variation in grain size, defect populations, etc). Predictions from EDA and/or FEA software already used within the electronics design space establish "global" stresses. As shown in Figure 8, global stress can be translated to the material level and material specific failure physics algorithms can be used to predict interconnect life or reliability. Given this the when designer changes a chip scale package (CSP) within the board layout, then the stresses imposed on the CSP will change as well as the associated life prediction. Interconnect design immediately rolls up to establish PCB reliability which rolls up to establish module reliability which establishes overall vehicle electronics reliability.

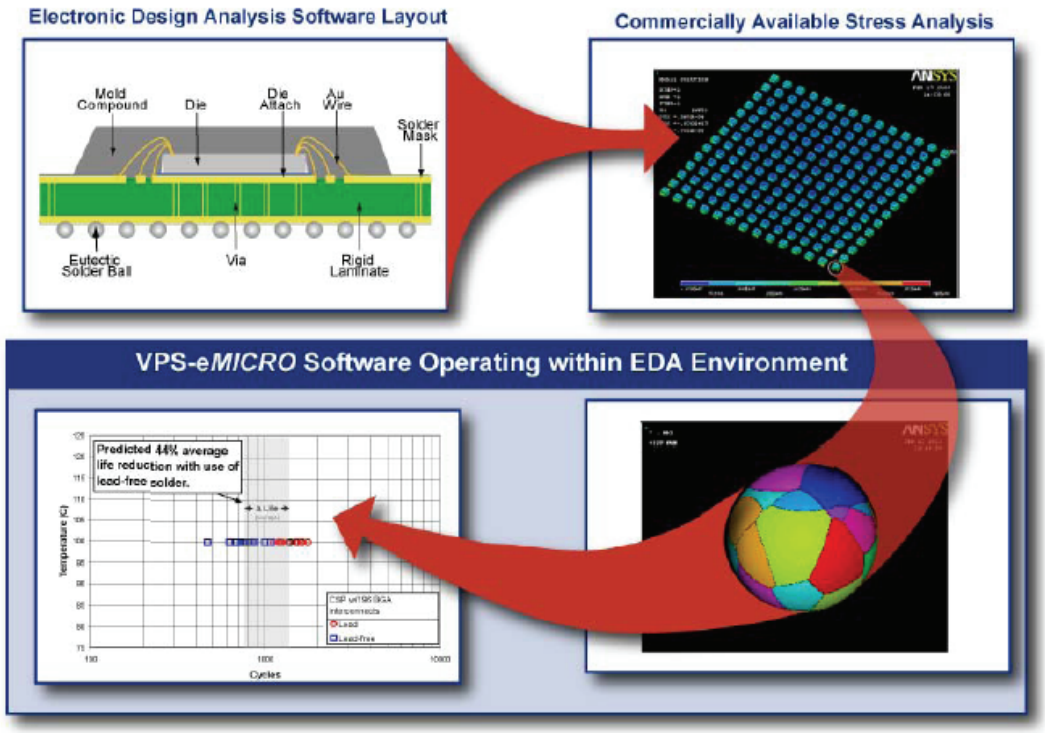

Figure 8 - Physics of Failure Simulation within EDA Framework

Summary

The old "MTBF view" of reliability is a hold over from the days where computing power was expensive. The mechanisms here described for computational modeling may have been understood by some specialists as conceptually desirable, but implementing them was completely beyond the tools of the time. Such ideas could not make their way into common practice, because there was no practical way for engineers to take advantage of them. But that was then. Today, engineers use powerful computational tools for almost everything they do. Design automation software is pervasive. Engineers bring finite element stress modeling and computational thermal analysis into the engineering design process. CRM will build on that existing base of software and expertise. To achieve the type of computational reliability analysis this paper advocates the adding of extensions to the engineer's existing software toolkit that allows the explicit analysis of variability at all levels of a product's construction, along with a module for modeling the physics of grain structure response to stress. The basic kernel technology for doing this is already in place and well proven. To transform these kernels, developed under research grants

from the military over the past five years, into software tools practical for everyday engineering use will take a significant commercialization effort. But such an effort is now under way, and a practical product is well within reach.

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Biography:

Loren Nasser is COO responsible for day-to-day operations at VEXTEC Corporation. He has been actively involved in the development of reliability prediction software within the aerospace, electronic and automotive marketplace. He has a M.S. in engineering science from the University of Tennessee and B.S. in mechanical engineering from Rose-Hulman Institute of Technology. Robert Tryon is co-founder and CTO at VEXTEC Corporation. He has lead the development of the patent-pending "VPS-MICRO" software. He served as principal investigator on VEXTEC's DARPA and NAVAIR prognosis technology development projects and has served in a similar role on numerous other projects. He received a Ph.D. in structural engineering from Vanderbilt University and a M.S. and B.S. in mechanical engineering from Rose Hulman Institute of Technology.