Building Reliability into the PWB: Optimization of the Desmear and Metalization Processes for Use on High Frequency and Lead Free Laminate Materials

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Abstract
High Frequency and Lead-Free laminate materials are finding increased use in the PWB fabrication industry driven by end user requirements for high-speed signal transmission and lead-free soldering temperatures. Along with these newer materials has been the need for improved reliability. End users are continually pushing for thermal performance to exceed five solder floats and exceed 300 cycles to failure on IST testing. The PWB industry, faced with ever increasing reliability requirements compounded by the fact that these new resin materials are more difficult to desmear and metalize, have become more concerned with plating adhesion to the copper interconnect and resin material. Concerns over interconnect defects and resin adhesion of the copper are causing fabricators to reinvestigate their metallization technologies. The purpose of this paper is to provide information on how to improve the adhesion of the copper deposit through a closer study of the critical success factors influencing the metal adhesion to both the interconnect and hole wall. The research showed that the electroless copper grain structure, plating rates and desmear parameters have a significant influence on PTH reliability. Specially designed high layer count test vehicles were employed to quantify the adhesion and overall PTH reliability. The results were verified with micro section evaluation after multiple solder float excursions and Interconnection Stress Testing (IST). This work validates the necessity of the metallization process to improve the robustness of the PTH under high temperature conditions.

Introduction
Printed wiring board fabricators and end users must manage ever-increasing complexities in PWB design, technology requirements and long-term reliability. It is extremely critical that key processes such as desmear and electroless copper provide optimum reliability through a defined process window. This is important because the designer selects the interconnect technology and feature sizes required for the intended application. These various selections including the resin material chosen, impact the printed wiring board reliability. While the designer must work within the parameters of form factor, weight and overall thickness, significant discretion with respect to wiring density, layer counts, hole size diameters, copper thicknesses and material properties is often exercised.

The material, hole sizes, copper layer thicknesses and electrical requirements can significantly impact the manufacturability, reliability and performance of the printed wiring board. In addition, end users are pushing the envelope on reliability by requiring multiple thermal excursions in the form of higher temperatures and longer dwell times at temperature. The higher temperature values are in response to lead-free soldering. In order to insure that greater reliability requirements are met, fabricators are being forced to re-qualify through the manufacture of more complex test vehicles. These test vehicles are most often designed to introduce more stressful conditions through the interconnect and barrel of the via. Adhesion of the electroless copper to the innerlayer copper foil interconnects as well as the surface foil is severely tested under these conditions. Dielectric thicknesses between the layers and copper foil thicknesses (1/2 ounce versus 1 ounce) have an effect on reliability.

In addition to concerns about foil and dielectric thickness, the type of resin material may have an influence on the through hole and interconnect reliability. Failure of the copper to adhere to the resin material is exacerbated due to several factors including poor overall adhesion of the copper to the resin, stress of the electroless copper deposit as well as grain size of the copper. Process parameters, deposition rates, resin topography, palladium catalyst interaction with the resin, and copper deposit characteristics all have an impact on PTH reliability.

Finally, achieving PTH reliability in view of the introduction of materials designed for high frequency and lead-free applications further complicates the concern over reliability. First and foremost, differences in peak assembly temperatures for lead-free (250-260 C) versus lead based soldering (230-235 C) are significant both for the laminate material as well as the copper adhesion. In addition, increased complexity of interconnect designs with flip chip, die attach, and wire bonding increases the number of thermal stresses for the bare PWB. (1)

Critical success factors
The challenge for fabricators is to be able to build printed wiring boards that are thermally robust. In other words, the circuit board must be able to achieve ever-increasing levels of reliability (often measured by IST and thermal shock testing) while undergoing significant thermal excursions. Many of the newer laminate materials developed to meet higher temperature requirements and increased technological performance attributes provide challenges of their own. Fabricators must

understand the differences between Tg (glass transition) and Td (temperature of decomposition). Materials with a high Tg rating do not necessarily reflect thermal robustness (2). On the contrary, materials with lower temperatures of decomposition lead to cracked vias and less reliable interconnects. Regardless, the metalization system (desmear and electroless copper) must be designed to mitigate the effects that the newer materials have on process ability. Those concerns are:

- Less than optimum topography of the resin after desmear
- Drill debris due to pulverization of resin materials
- Providing a continuous void free copper deposit in small blind and through hole vias without the necessity of multiple plating cycles
- Improving adhesion of the copper to the interconnect and increasing mean time before failure

Methodology

A base line study of several board fabricators was undertaken to determine the level of robustness with current metalization processes. Interconnection Stress Testing and Solder Shock testing were utilized in order to gain a baseline understanding of thermal robustness. Critical attributes of both the desmear and the metalization process were measured as to their effect on PTH reliability. Then, an alternative process was developed and tested for PTH reliability.

Desmear of High Tg, High Td materials

With the introduction of higher temperature resistant laminate materials, including those deemed RoHS compliant, the concern centered on the issues of hole wall topography after desmear, and the overall effect of the topography on the quality of the electroless copper deposit. Figure 1 shows the condition of the hole-wall after drilling. The material in question is a high Tg, FR-4 material. These material types tend to show a high amount of debris in holes after drill. This is most evident in small holes, which is most likely due to thermal decomposition from higher drill temperature. As a consequence, fabricators attempt to affect a very high surface topography by implementing a very aggressive alkaline permanganate process (Figure 2). One such consequence of this action is overall solvent penetration and solvent retention (Figure 3).

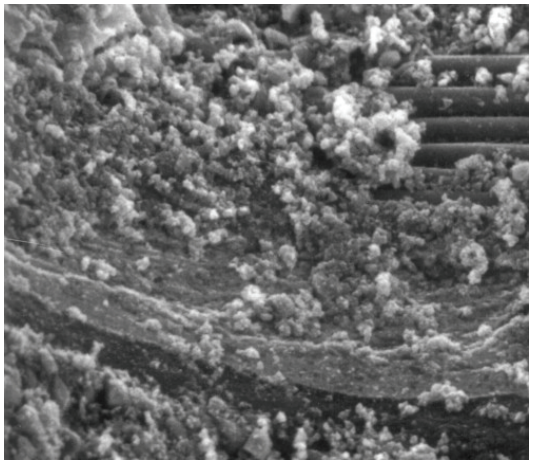


Figure 1 - High Tg FR-4 Material After drill. Note Debris on Hole Wall from Drilling

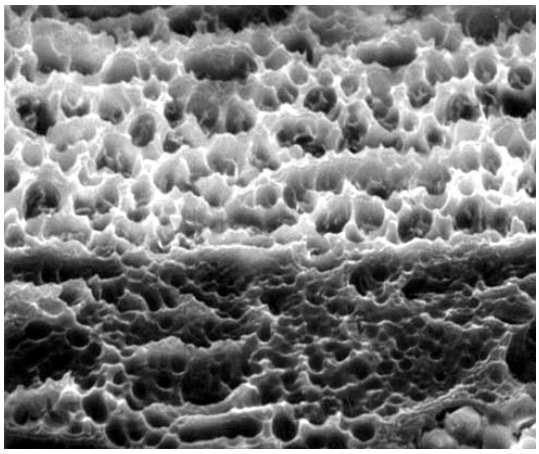


Figure 2 - High Tg Material after Alkaline Permanganate Desmear.

While the topography of the resin appears to be ideal for electroless copper seeding and eventual copper metalization, the issue is that an overly aggressive permanganate treatment will very likely lead to solvent retention. The effect of solvent retention is shown in Figure 3. As the solvent time is extended for a constant permanganate time the amount of solvent absorption increases and the net weight loss after permanganate decreases.

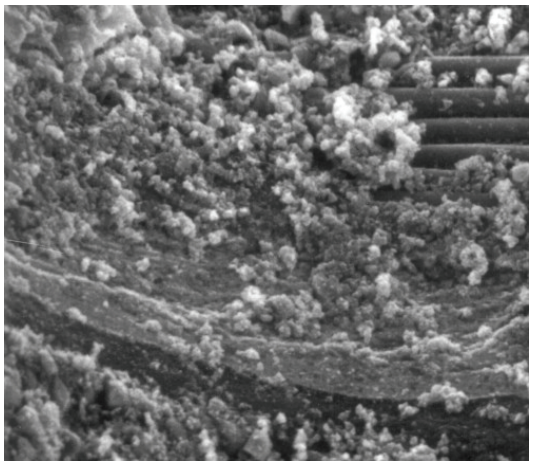


Figure 3-Solvent Adsorption Versus Resin Weight Loss as a Function of Time.

Solvent retention is known to cause other defects including wedge voids and wicking. On the contrary, the risk of solvent over penetration and retention may cause significant defects such as resin voiding (Figure 4a) and electroless voiding (Figure 4 b).

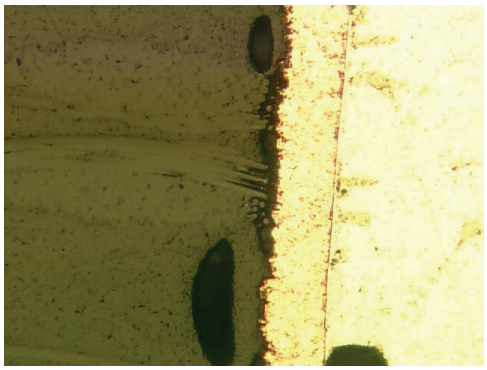


Figure 4a - Resin Voiding from Solvent Retention.

Thus, the honeycombed topography engineers have become accustomed to with 140 Tg materials should no longer be considered an option. It is quite evident that one cannot rely on micro-roughened resin to promote metal adhesion or plating continuity. Concerns of catalyst adsorption due to the lack of topography raised the bar for the plating process as well.

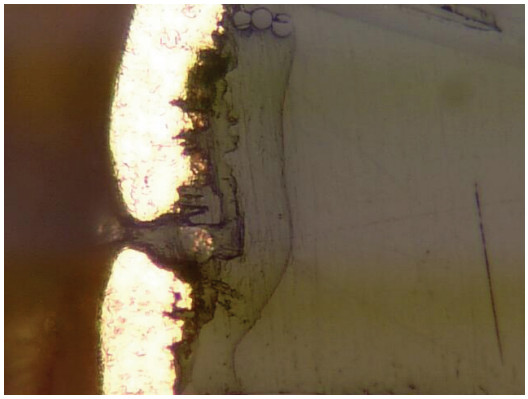


Figure 4b - Example of Electroless Copper Voiding Due to Solvent Retention.

With the less than optimum topography a grave concern, the process design required an improved mechanism for promoting catalyst adsorption to the resin and glass. In addition, it was deemed important to understand deposition rates of the copper and determine whether or not this had an influence on PTH reliability. In addition, previous studies indicated that the grain structure of the electroless copper deposit itself may play a role in PTH reliability. The research team believed that deposition rates and copper deposit grain size have an effect on PTH reliability. In order to test this hypothesis, the team studied several commercially available electroless copper processes. Reliability data based on IST and Solder float were gathered through the use of appropriate test vehicles. Deposition rates for each process were noted. In addition, grain structure of the electroless copper deposit generated from these processes was recorded with a scanning electron microscope. Finally, a new electroless copper formulation designed to produce a large and tight grain structure was tested. The process under study provided a deposit thickness of 50-70 microinches in 30 minutes. This was contrary to the commercially available processes in this study that deposited 90-120 microinches in 30 minutes.

Baseline IST and Thermal Stress Studies

Interconnect Stress Test (IST) Technology has emerged as a standard test methodology for the assessment of Printing Wiring Board (PWB) interconnect. IST has the capability of effectively and rapidly quantifying the integrity of the Plated Through Hole (PTH) and the unique ability to identify the presence & levels of post separations within the multilayer board (MLB). IST both complements and/or dramatically reduces the levels of microsection analysis required for PWB interconnect quality assessment.

IST engineers have designed vehicles to measure extremely small levels (and sometimes not so small levels) of change that occur at (and adjacent to) the interface of the inter-plane connection. If this interface is created with a perfect chemical bond, in theory we should measure minimal (if any) resistance change during accelerated stress testing. The chemical bond should in fact be stronger than the integrity of the laminate's copper foil. Additionally, the rotational strains that are applied to the innerlayers create a bending moment that occurs approximately the thickness of the copper foil "behind" the hole wall. If the interface is chemically bonded we should expect to see microcracks coalescing in the copper foil at approximately .0005" to .0013", measured from the edge of the PTH barrel (Figure 5).

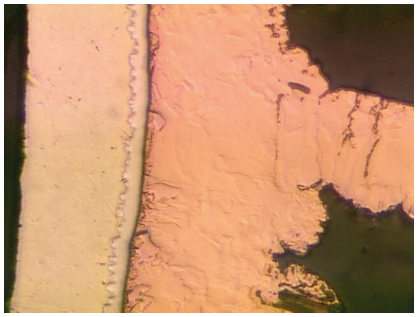


Figure 5 - Microcracks Present after IST Cycling

The various degrees of fatigue are primarily related (but not limited) to the following:

1) The failure hierarchy of the interconnect (See below)
2) Hole diameter
3) Material Tg/CTE

4) Foil thickness/Foil quality
5) Damage accumulation from PWB processing and assembly environments
6) Position of the innerlayers relative to the surface of the substrate

It has been determined that the failure hierarchy of the interconnect plays an important role in establishing whether the foil (or post interconnect) becomes a dominant or latent failure mechanism. The basis for the hierarchy is determined by the reliability of the PTH barrel, traditionally we should expect that the PTH barrel would precipitate as the "only" reliability concern, although in recent years an increasing number of electronics companies are becoming fully aware of issues with "internal opens", that are often not diagnosed to their root cause.

The bottom line regarding failure hierarchy is as follows;

a.) If the PTH barrel is robust (or the post interconnect quality is very poor), the inter-plane connection will receive increased/extended levels of strain (equally distributed between the PTH barrel and innerlayer copper foil interface), the extended strain and/or poor quality at the interface could precipitate as inter-plane separations.

B.) If the PTH barrel is not robust, the failure mode of barrel cracking will totally dominate the interconnect performance, thus the stresses are not given the opportunity to distribute to the innerlayer copper foil interface in order to precipitate microcracks.

The consequence of the stronger PTH barrel has simply permitted the inherent hydrostatic stresses to "re-distribute" themselves (for a longer period) to the next weakest link in the chain. The inter-plane connections are now expected to withstand higher levels of stresses, especially in the assembly and rework environments. At the same time the laminate manufacturing industry (in order to reduce their costs) have progressively reduced the thickness of copper foils, traditionally we expected 1/2oz copper foils to measure 0.0007", today it regularly measures between 0.0005" & 0.0006". The combination of increased levels of strain and thinner copper foils has resulted in a growing number of interconnect reliability issues. The stresses and strain are exacerbated by the lead-free soldering cycles and anything that compromises adhesion of the copper deposit to either resin or the copper interconnect (3).

In order to gain a perspective on PTH reliability with the current desmear and electroless copper processes, the researchers worked with several fabricators to obtain baseline reliability data. Since OEMs desire to have IST data, the research team sought IST data generated on special test coupons fabricated from several material types. In addition, a specially designed test vehicle was manufactured in order to gain an empirical understanding of interconnect integrity. For this study, the test vehicles were subjected to multiple floats on molten solder.

Test vehicles for both solder float testing and IST (Interconnection Stress Test) were fabricated. The vehicles were processed through desmear and electroless copper metalization. After imaging, the panels were plated with copper to a nominal thickness of 25 microns, followed by an etch resist. Following resist strip, the panels were etched and metal etch resist removed. Test coupons were routed out and subjected to solder shock and IST. The results of the testing are shown in Figure 6 and Figure 7. The IST coupon test vehicle utilized a twelve-layer PWB fabricated with 140 Tg material. (140 Tg material was used to provide more z-axis expansion, thus increasing the likelihood of interconnect and PTH failures). The Figures below show the IST cycles to failure from test vehicles submitted from a sample of selected PWB fabricators. The data supports the theory that achieving robust PTH reliability is a difficult task.

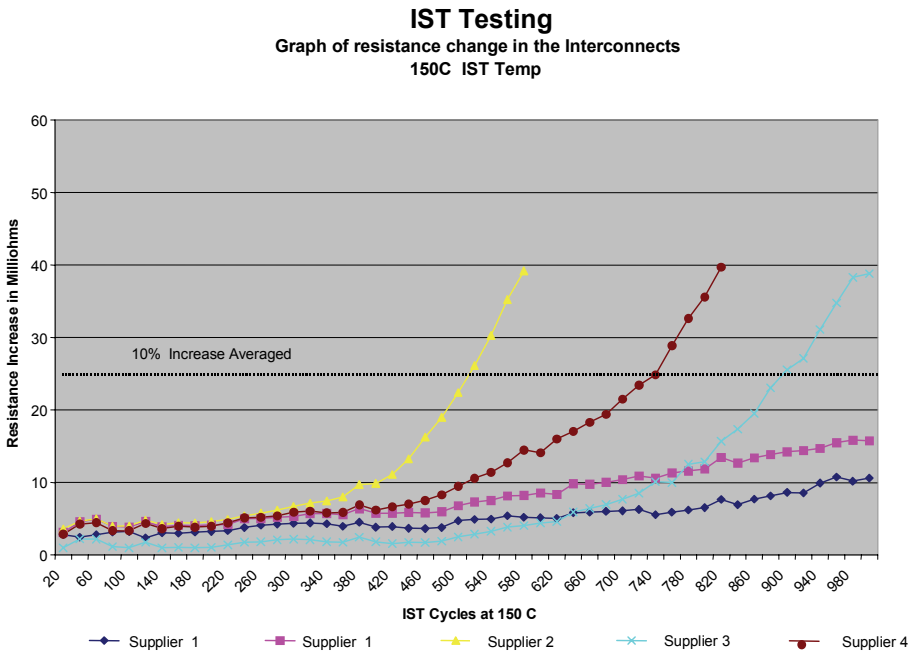


Figure 6 - IST Results From Four Commercially Available Electroless Copper Processes.

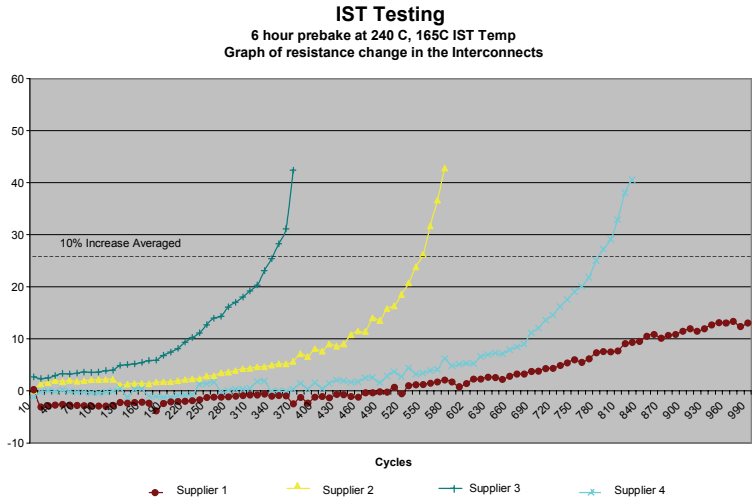


Figure 7 - IST Results from Four Commercially Available Electroless Copper Processes. Results obtained after preconditioning the test coupons for six hours at 240 C.

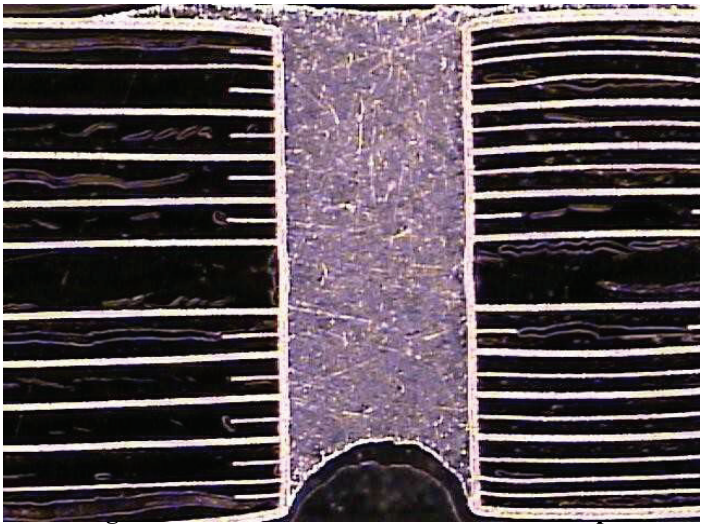
The results show that there is a cross section of fabricators that supply finished printed wiring boards that are borderline with respect to plated through-hole integrity. Indeed, as the results in Figure 6 show, subjecting the test vehicles to pre-conditioning temperatures in order to simulate lead-free assembly leads to further degradation. It has been reported that lead-free assembly cycles will reduce the fatigue life of the plated through hole by 50-80% (1). Copper separating from the post is a common failure mode. This failure mode is exacerbated by excessive Z-axis expansion brought about by higher resin content required by certain board constructions (3).

In addition, solder shock testing was employed on the test coupons. The coupons were subjected to 6 X solder floats at 288 C for 10 seconds.

Test Vehicle Description for Solder shock testing
Figure 8 shows the test vehicle used for solder shock testing. This vehicle was designed as follows:

- Panels are FR-406 laminate, 0.100” thick, 0.010” and 0.042”holes.
- Solder Shock test vehicle is a 22 layer with the n-1 layers 0.003” from the outer foil. Half and one oz. foils are used with the n-1, 2 and 3 layers as ½ ounce.

There are 84 interconnects per coupon. The data shown in Figure 9 indicates a high failure rate after 6X solder floats at 288 °C.



Failure analysis indicates that the primary failure occurs at the interconnect mainly due to CTE mismatch between the resin material and the copper. In addition, any weakness in the crystal structure of the electroless copper deposit on the internal copper foil is a potential breaking point as well. It was postulated that grain size of the deposited copper and inherent stress levels in that deposit cause the deposit to separate from the copper interconnect. And, according to **Kobayashi et al,** the greater the deposition rate of the copper, the lower the adhesion strength of the copper to resin (4). It is possible that conditioner type, catalyst influence and condition of the resin after desmear influences adhesion.

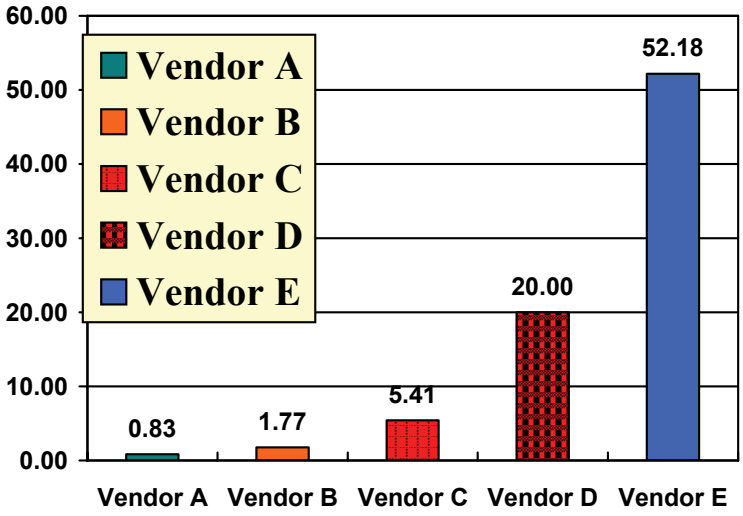


Figure 9 - Y-Axis Denotes the Percentage of Interconnects that Display at the Least a Hairline Fracture after 6X Solder Floats.

The results of thermal shock testing indicate there are significant issues with respect to reliability from one electroless copper process to another.

Process Modifications

In order to develop a robust PTH metallization system, an integrated approach was required. First and foremost it was established that improved adhesion of the copper deposit to the resin and copper interconnect are desirable attributes to enhance reliability. At the same time, the goal was to slow down the deposition rate of the copper especially in the beginning stages of initiation. In addition, the influence of the cleaner/conditioner on catalyst adsorption and catalytic activity is well documented (5). The goal here was to optimize catalyst adsorption to the resin to insure a void free deposit without negatively influencing adhesion. Testing of cleaners included evaluation of electroless coverage, HWPA and initiation time of the electroless copper bath. Based upon this work a new cleaner was developed.

A second important modification was the development of an organic stabilizer that served a two-fold purpose. This stabilizer is instrumental in slowing down the deposition rate of the copper. This is believed to aid in modifying the grain boundaries of the copper as the metal nucleates over the palladium catalyst during autocatalytic deposition..

Finally, no discussion about process development is complete without studying the effects of the non-proprietary process chemistry. Recognizing that the desmear topography is less than optimum and cleaner conditioner formulations effect catalyst adsorption, the research focused on interconnect integrity as influenced by caustic content and formaldehyde concentration.

The results of the experimental designs are shown in Figures 10 -11.

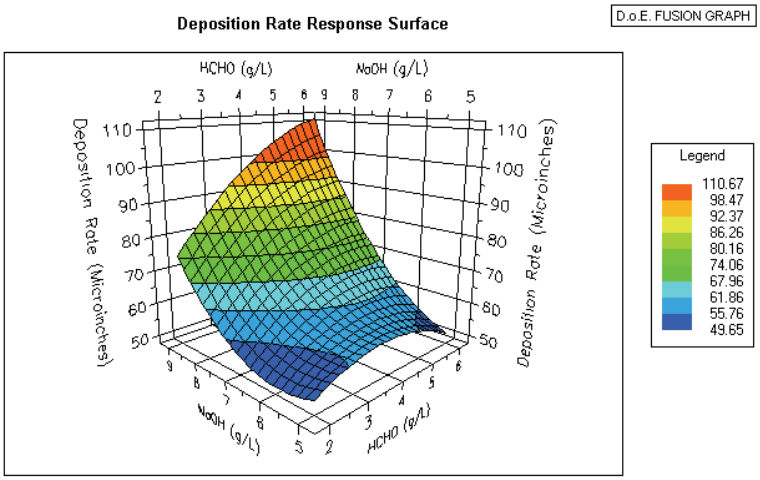


Figure 10 - Deposition Rate of Electroless Copper as Influenced by Sodium Hydroxide Content and Formaldehyde Concentration.

The experimental results show that increasing concentration of hydroxide increases the deposition rate, as does formaldehyde. However, sodium hydroxide appears to have a greater influence than formaldehyde.

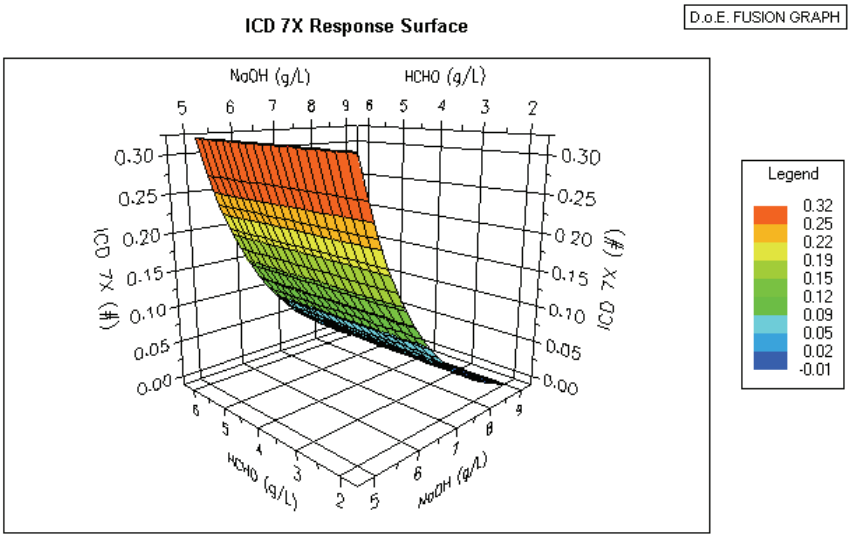


Figure 11 - ICD Response Based on Interaction of Formaldehyde and Sodium Hydroxide Concentrations. ICD's Determined After 7 X solder Floats. ICD Test Vehicle as Described in Figure 7.

The experimental results show that increasing the concentration of both sodium hydroxide and formaldehyde decreases the number of ICDs.

Grain structure study

The literature reviews and the research team's own testing provided evidence that the grain structure of the copper deposit influences the deposit's adhesion to the copper interconnect. Microsections taken from test boards processed in the reformulated electroless copper process showed deposit grain structures similar to that shown in Figure 12. Interestingly, this structure had a high correlation to good interconnect reliability as determined by IST and thermal shock results. Test coupons that gave early cycle failures both in IST and thermal shock testing most often displayed a loose grain structure as shown below (Figure 13).

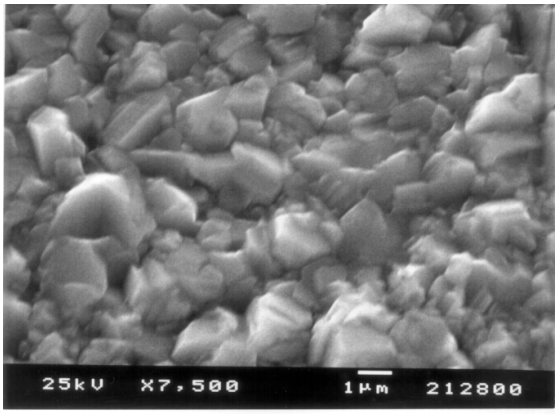


Figure 12 - Tight Grained and Angular Deposit of Copper on the Interconnect.

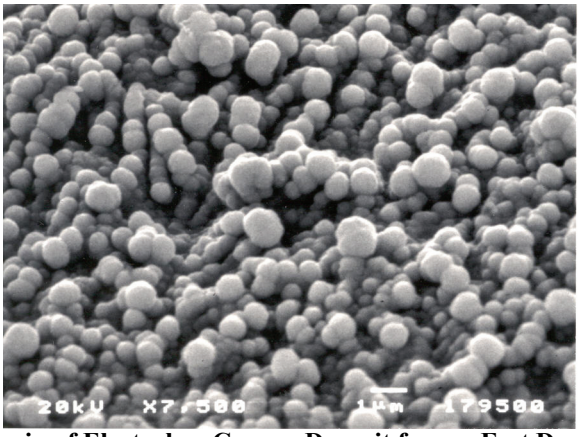


Figure 13 - Large and Loose Grain of Electroless Copper Deposit from a Fast Deposition rate Electroless Copper Process.

Summary and Conclusions

When considering applications for high Tg resins and for lead-free soldering applications it is important to consider many factors with respect to desmear and metalization of the PWB. Both IST and solder float testing are useful tools in process optimization. Optimization of the desmear process involves effective removal of the resin without creating problems due to solvent retention. For the electroless copper process cleaner conditioner type and process parameters must be matched with the electroless copper bath being used to provide acceptable reliability in terms of HWPA, voiding and resistance to thermal excursions experienced during assembly and end use. Key factors for the electroless copper bath include proper selection of the stabilizers used and control of formaldehyde and sodium hydroxide concentrations. Optimization of these and other bath parameters will result in a consistent grain structure of the electroless copper deposit that makes it well suited for maintaining excellent reliability for high frequency and lead-free laminate materials.

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