Concurrent Testing: Increasing Test Coverage without Affecting Cycle Time

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Abstract
Volume electronic manufacturing environments are constantly seeking solutions to bottlenecks at end-of-line test. Bottlenecks are being seen increasingly on high volume automotive, telecomm & consumer electronic product lines where assembly beat rates are much faster than that of the test processes. Manufacturing engineering teams have few available solutions that can maintain test coverage and not increase the unit cost of test. Until recently the only viable solution required replicating the test platforms to gain more capacity to deal with the higher volume demand. This solution consumed more floor space, capital budget, operators & maintenance time. New solutions using concurrent test techniques promise to un-block the test bottleneck by maximizing the test platform asset utilization across multiple units under test simultaneously.

Electronics evolutions and revolutions – whether in component technology or in the products in which they are used – continue across the globe. While the world awaits the next electronic must-have marvel like the PC or the cell phone, the evolution and continual re-engineering of existing consumer, commercial and aerospace products is as fast-paced as ever. Electronics manufacturers continue their quest for products that provide greater functionality and consume less power, typically in packaging that gets smaller and smaller.

As a result of this continual evolution, new technologies and trends in the production of printed circuit boards are required, presenting new challenges for how PCBs are built and tested.

The current design trend continues toward a higher integration of ball grid arrays (BGAs), Gate arrays and FPGA's. New designs also include more programmable components and more serial busses. As constant as the evolution toward more advanced designs is the challenge of how the new designs will be tested in production. Almost universally, new designs will result in a higher complexity and less nets per board for testing. Another trend toward miniaturization has a dual benefit – components pack more capability into smaller packages, resulting in final products that are smaller than their previous-generation predecessors (again, PCs and cell phones are a good example). However, what is a benefit to the end user is a detriment to those tasked with production testing. Miniaturization results in less available space for testing, with board sizes getting smaller and smaller and components mounted on both sides. These trends are responsible for an increasing number of multiple panels being used in today's electronic products.

In high volume products like automotive or consumer applications, the transition from single boards to multiple panels is especially high. By using multiple panel designs on today's better production machines, handling times are reduced and cycle times are faster. Unfortunately, a faster cycle time is counter productive to the goal of performing comprehensive testing. Compounding the test time problem is the increased inclusion of steps such as memory test, component-programming, serial protocols and boundary scan on these more complex and more highly integrated boards, as seen in Figure 1. As has always been the case, if the test time is not longer than the cycle time, test is not a problem; but if the test time is higher, testing is now a bottleneck that requires additional focus to remedy the situation (see Figure 2.)

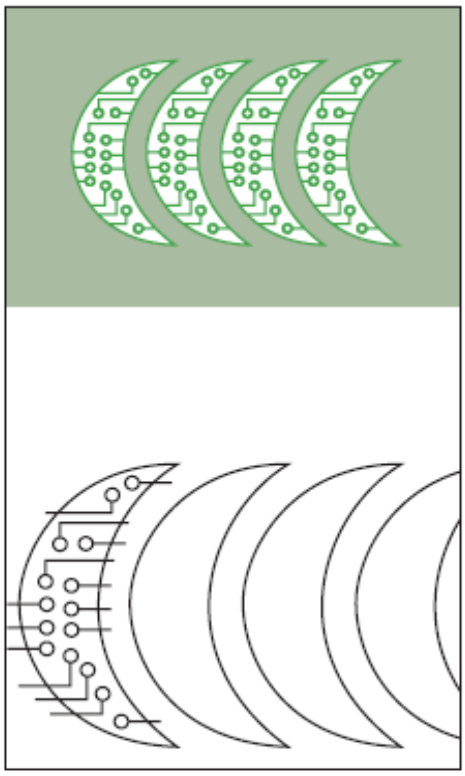

Figure 1. Steering-column sensors, having shapes similar to that of a crescent moon, would present significant handling problems, but multiple images can be assembled in a single rectangular board.

How, then, do you develop a test that can handle higher line production rates, multiple image boards, and increased product functionality-without creating a major end-of-line bottleneck? As Eliyahu M. Goldratt has pointed out in several books (Ref. 1, for example), normal test asset costs range from 10% to 25% of the capital cost of the complete assembly line. If traditional thinking is applied to solve the test bottleneck by deploying multiple replicas of the existing test setup, then test costs will rise as a percentage of total line costs-an obviously undesirable situation.

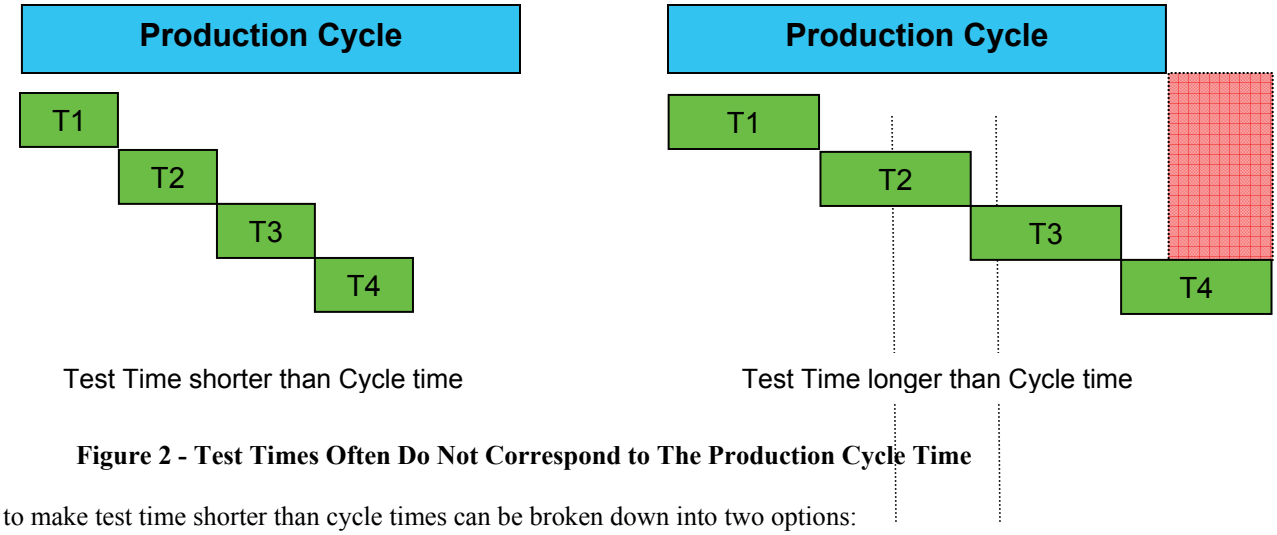

Figure 2 - Test Times Often Do Not Correspond to The Production Cycle Time

The solutions to make test time shorter than cycle times can be broken down into two options:

- **More testers & handlers i.e. more investment, more footprint**
- **Concurrent testing**

Adding more testers and handlers seems to be an easy solution. Assuming that money and footprint are not factors (extremely unlikely), the issue then becomes how to integrate additional test systems into the production process. Complex mechanical solutions are necessary to integrate such solutions. Fixture costs and handler costs are additional expenses to the complete multiplication of the tester hardware.

The second option, the incorporation of concurrent testing, is a beneficial solution in many cases. The advantages of concurrent testing are better utilization of tester resources and parallel testing of multiple boards. By using multiple test heads that are synchronized together and integrated in the same tester frame and utilizing the same handler, the footprint will not increase and the cost for the test equipment will never be n times the single tester price.

Concurrent testing allows the user to perform all the tests that are necessary to ensure product quality without increasing the cycle time, as illustrated in Figure 3. The time needed for programming of flash memories will not be multiplied by the number of boards under test because testing and programming of the individual boards will be done simultaneously.

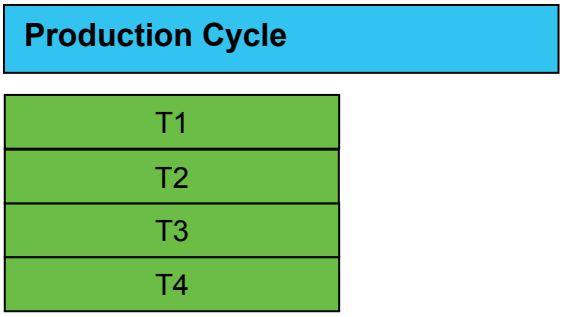

Figure 3 - Concurrent Test Time Allows Longer Test Times Without Affecting the Cycle time

By developing a test head that will provide reasonable pin count (up to 512 test pins) and can be configured with all the functional test modules available for the MTS tester family Digitaltest offers a proven methodology that is designed for concurrent testing, as illustrated in Figure 4.

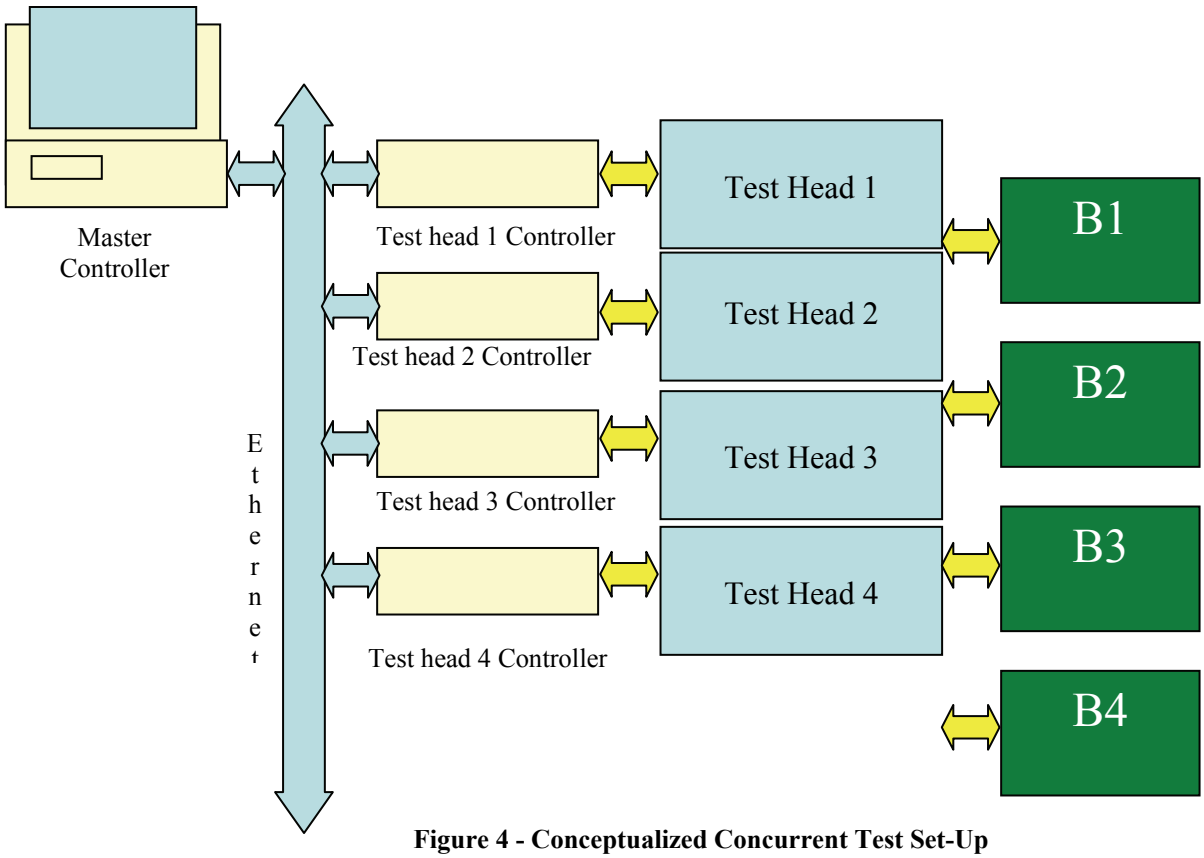

Figure 4 - Conceptualized Concurrent Test Set-Up

Other test resources such as power supplies, VXI/IEEE instruments can be multiplied or shared between the different boards. A major strength of the concept is that it also allows the mix between parallel testing and sharing of test resources such as expensive VXI or IEEE measuring modules by performing the measurements sequentially, as illustrated in Figure 5.

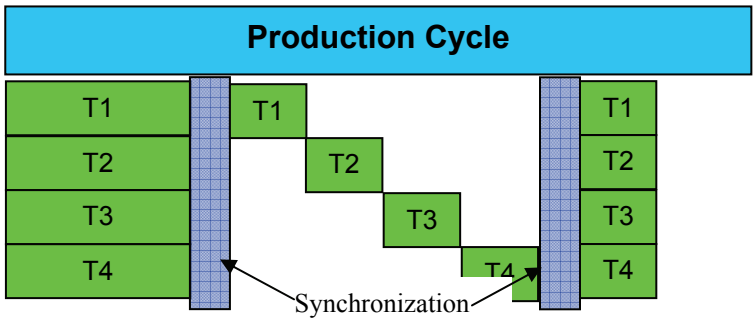

Figure 5 - Concurrent Test allows Parallel Test as Well as Sharing of Test Resources

CITE the system software generates the test program for one board so that one test program can be developed, debugged, modified and at the end compiled. The concept however will allow local modifications for each board under test. CITE generates a control program skeleton that can be modified/enhanced by the user if required. The skeleton program will be loaded in the Master controller, identify the board under test load the proper test program for the various test head controllers and handle the test synchronization points. Test start and monitoring test end are also handled by the master controller.

The use of Microsoft Visual Basic a programming language for the MTS tester family provides powerful programming, communication and the handling of data between the test heads. The software provides simple synchronization commands that will facilitate the work of the programmer. The communication between the test heads controller and the master controller are handled by the system software.

While data collection of the various boards is handled by the test head controller at test end the master controller will collect the test data of different boards and generate one datalog file for the complete panel for paperless repair and the Quality management system.

Truly synchronized parallel testing is becoming a necessity to provide comprehensive testing without impacting production cycle times. True concurrent testing includes real parallel test with small, affordable test heads; a powerful and flexible software environment; and, complete integration into an automatic board handler. The convergence of these elements demonstrates once again that a multi-dimensional test strategy can meet the evolving needs of technologies and methodologies in a high-volume electronics manufacturing environment, ensuring the delivery of top quality products to the market.

The concept of concurrent testing maximizes the depth of test and test coverage, the utilization of the tester hardware while minimizing the floor space impact and the costs of test hardware and handling systems.

Reference

1. Goldratt, Eliyahu M., Critical Chain, North River Press, Great Barrington, MA, 1977

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