Predicting Plated Through Hole Life at Assembly and in the Field from Thermal Stress Data

Michael Freda
Sun Microsystems, Inc.
Menlo Park, CA

Dr. Donald Barker
University of Maryland
College Park, MD

Abstract:
Over the past ten years, two new test methods: Interconnect Stress Test [1] and Highly Accelerated Thermal Shock [2] have been developed to perform thermal cycling testing and in particular, to measure plated through hole reliability. Both of these test methods have proved useful in their ability to quantify plated through hole reliability and have gained a wide level of acceptance and creditability within the industry. Along with more tradition air-to-air and liquid-to-liquid thermal cycle methods, these two new test methods expand the test methods available to the interconnect industry. While the number of testing options for plated through hole thermal cycling has increased, there has been little work performed within the industry on developing methods to analyze and use the data coming from these new test methods.

This paper covers use of IST testing to obtain plated through hole cycle to failure data followed by methods to analyze and plot the data over a wide range of temperatures. In particular, the paper will focus on the use of material properties like the modulus as a function of temperature and the coefficient of thermal expansion as a function of temperature to calculate the stress on a plated through hole versus temperature. In this paper we will also explore the use of the Inverse Power Law (IPL) to analyze the plated through hole stress versus cycle to failure relationship. Once we have used IPL to established the cycle to failure relationship to stress for a given laminate and PCB design, it is then possible to estimate the number of cycles to failure in the field as a function of the number of cycles of assembly stress, the peak assembly temperature, and the maximum temperature in the field.

Keywords
IST, HATS, Lead-Free, CTF, Cycles to Failure, Via Reliability, PTH Reliability

Introduction
Sun Microsystems, Inc. has utilized IST for the past seven years. Early in that usage of IST Sun performed testing using multiple precondition steps from ambient to 230°C to simulate eutectic tin/lead assembly and rework followed by test from ambient to 150°C. IST test equipment has a minimum temperature of ambient so, all further references will list only the peak temperature and ambient is 22°C. Typical preconditioning levels used were 0x, 3x, and 6x at 230°C and test results clearly show the negative impact of thermal cycling at assembly peak temperatures. As the high-end server product that initially utilized IST for plated through hole reliability confirmation moved into full production, Sun standardized our IST test protocol at 6x preconditioning at 230°C followed by thermal cycling to 150°C. The typical IST cycle is a linear ramp from ambient to peak in three minutes followed by a two-minute cool down back to ambient. In-situ electrical resistance heating circuits heat the IST coupon to peak temperature. Blowers using ambient air cool the IST coupon down. During Sun's initial three-four years of using IST and as pcb fabricator processes improved, IST testing at 6x at 230°C followed by thermal cycling at 150°C often led to long test times, due in part to Sun's requirement for test to failure.

About three years ago, Sun started to introduce thermally resistant, phenolic cured laminate materials into production to gain experience for the upcoming industry wide shift to lead-free assembly. Using phenolic laminate materials, the cycles to failure increased dramatically making IST test times burdensome, especially when preconditioning was performed at 230°C for eutectic solder assembly. Additionally, Sun began test of lead-free laminate materials during this period, but the actual peak temperatures that would be required for lead-free assembly remained a bit of an unknown. For all the reasons discussed above, Sun started to use cycle to failure testing at temperatures above laminate material Tg. Figure 1 shows a comparison of HATS and IST test temperature range. You can see that the test temperature range of IST is well suited for testing above laminate material Tg. IST testing above laminate material Tg is quick and cost effective due to low cycles to failure. With appropriate reliability software, it is possible to use this data to predict cycles to failure at any potential lead-free assembly temperature.

Sun has previously reported on IST testing performed on thick, high aspect ratio pcb fabs using test to failure at multiple temperatures [3, 4]. This work showed promise in our effort to develop a new test and data analysis method, but since that work had many design of experiment (DoE) factors relating to board design, a couple of pcb fabrication variables, plus DoE factors in the testing and analysis the result was a small sample size per cell. Therefore, the testing that is reported in this paper is focused entirely on the development of improved test and data analysis methods. The IST coupons used are from a high volume, high-end server CPU card. By using a mature pcb fab design with no design or pcb fabrication variables, we are able to focus on the test and data analysis variables and use a larger sample size per cell.

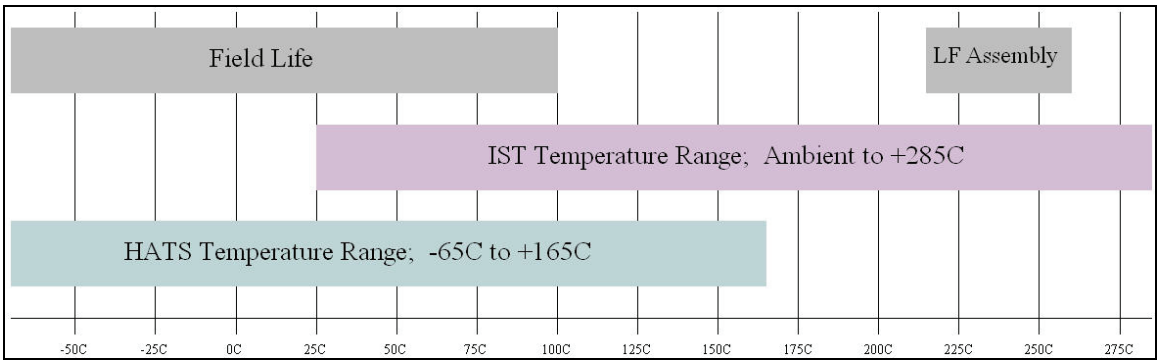


Figure 1 – Comparison of HATS and IST test temperature ranges to Field Life and Lead-Free Assembly temperatures.

Test and Analysis DoE Description

The product selected for test in this paper is the CPU Uniboard that is used in a number of Sun's high-end servers. The current version of the Uniboard has four dual core processors per card, and 32 DIMM sockets that accommodate up to 64 Gb of on-board random access memory. There are also eight level 2 cache memory cards with 512 Mb of SRAM memory each. The largest system manufactured that utilizes the Uniboard CPU card has a maximum configuration of 144 CPU cores per system. The CPU board and IST coupons which are fabricated on the same panel are 26 layers, 2.8mm thick (110 mil), high resin percent, 0.35mm (13.8 mil) minimum drill diameter, uses a phenolic cured FR-4 laminate material, and has both Cu/HASL plating and selective Cu/Ni/Au plating. For this paper, only the Cu/HASL IST coupons were tested.

Figure 1 – Pictures of Sun high-end servers. The two largest systems on the left use the Uniboard CPU card shown on the right.

The IST coupon fabricated on the Uniboard panel has the following design features:

- 27.9 x 76.2 x 2.8mm (1.1 x 3.0 x .110 inch)

- 1.5mm hole pitch (.060 inch)
- 144 PTH interconnect holes drilled at .35mm (.0138 inch) diameter; a 8:1 aspect ratio
- PTH interconnect daisy chain runs from layer 1 to 26 to 1 to 26…
- 144 POST interconnect holes drilled at .85mm (.0335 inch) diameter; a 3.3:1 aspect ratio
- POST interconnect daisy chain runs from layer 2 to 3 to 2 to 3… and from layer 25 to 24 to 25 to 24…
- The PTH interconnect holes are orientated interstitial to the POST interconnect holes

IST Testing and Data Analysis Above Tg

Initial IST testing was performed above Tg as shown in Table 1. Testing was performed at four temperatures above Tg: 215°C, 235°C, 255°C, and 275°C. Shown is the sample size for both the initial DoE plan and the actual DoE. Graph 1 shows the Lognormal plot of cycles to failure versus cumulative failure percent for the IST testing above Tg. The data follows expected trends, i.e., the higher the test temperature, the shorter plated through hole life. For this reason, a sample size of 12 coupons per cell was deemed sufficient.

Table 1 – Planned and actual DoE sample size per cell.

DoE Plan

CTF above Tg

Temp	Sample Size
215C	18
235C	18
255C	18
275C	18

CTF below Tg

	IST temp after Precondition		
Precondition	120C	135C	150C
2x at 245C	18	18	18
6x at 245C	18	18	18
10x at 245C	18	18	18

Total IST coupons plan = 234

DoE Actual

CTF above Tg

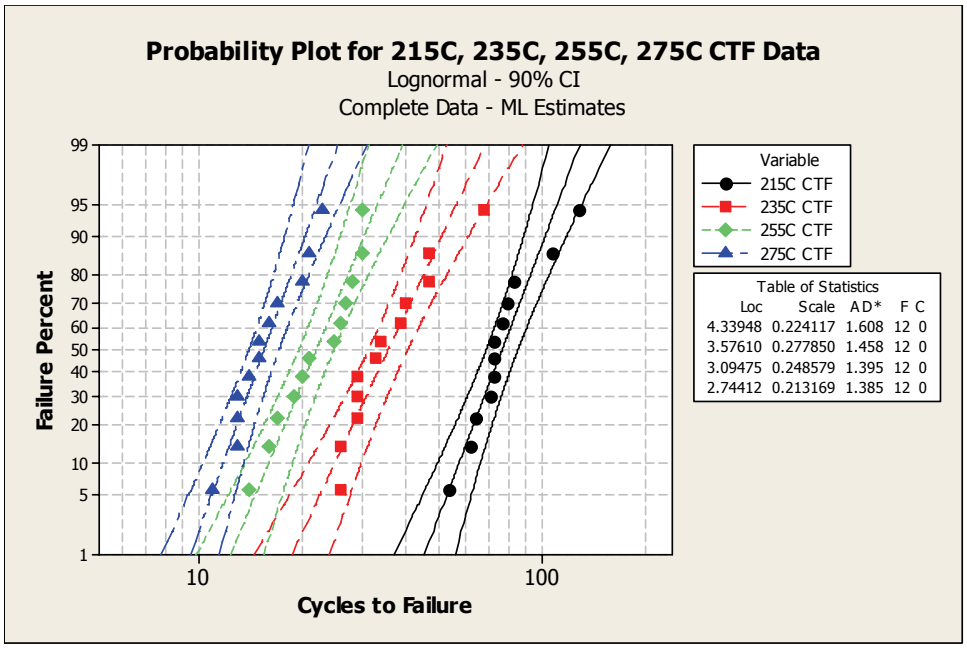
Temp	Sample Size
215C	12
235C	12
255C	12
275C	12

CTF below Tg

	IST temp after Precondition		
Precondition	120C	135C	150C
2x at 245C	0	0	18
6x at 245C	0	12	18
10x at 245C	6	12	18
18x at 245C	18	18	18

Total IST coupons actual = 186

Graph 2 uses the same raw data as Graph 1. The difference is the analysis method used where instead of performing an independent Lognormal analysis on the cycle to failure data for each test temperature; the analysis uses all data from the multiple test temperatures to obtain a best fit to both a Lognormal distribution and an Inverse Power Law (IPL) relationship. Sun typically uses a Lognormal distribution since our experience shows that it is a better fit than a two-parameter Weibull distribution in the majority of cases (Lognormal goodness of fit parameter is better than Weibull in >50% of the cases). An added benefit is the Lognormal distribution usually has a better fit to early life failures that is Sun's primary concern. Nonetheless, use of a Weibull distribution should yield similar results to those in this paper. Sun uses the 1% cumulative failure rate to rank laminate materials and the pcb fabricators plated through hole formation processes; it is hard to separate the effect of these two from each other. Mathematical descriptions in terms like Scale Factor, Location, MTTF, Characteristic Life, Eta, Beta, etc. are difficult for many people to relate to. It is easy to explain T1%, it is the number of cycles where one would expect a 1% cumulative failure or when you would expect the first failure if testing 100 parts. Additionally, T1% is sensitive to both the location (indicative of process used) and slope (indicative of process variation) of the Lognormal distribution making it a useful "**single**" parameter to summarize results from multiple parameter distributions.



Graph 1 – IST results from testing above Tg at four temperatures.

We used the Inverse Power Law relationship since it is widely recognized that non-ferrous metals like copper usually follow the IPL relationship [5, 6]. Models like Arrhenius or Eyring are not appropriate since they deal with failure modes that are thermally induced. At first glance, this may also appear to be the case with the fatigue failure of plated through holes during thermal cycle testing. Nonetheless, in the temperature range that we study in this paper, metallic copper is not going through any physical change. Since it is a pure metal and there are no chemical reactions to occur, an activation energy based model like Arrhenius is not appropriate. What is happening is that there is stress applied due to the high Z-axis coefficient of thermal expansion of the epoxy/glass laminate material which surrounds the copper plated through hole structure and creates tensile stress on the copper. This makes the IPL relationship the appropriated model to follow. Latter in this paper we will discuss converting data from temperature versus cycles to failure to the more correct stress versus cycles to failure relationship.

The equation for the IPL relationship follows. As shown in equation 2, it is easy to perform a Logarithmic transformation on the IPL relationship followed by rearrangement so it follows a conventional linear slope/intercept model of f(x) = m*x + c. In the graphs that follow it is common to see a Log/Log scale in use.

$$L(V) = 1/KV^n \qquad \text{eq. 1}$$

$$\text{Log}_{10}\, L(V) = - n\text{Log}_{10}V - \text{Log}_{10}K \qquad \text{eq. 2}$$

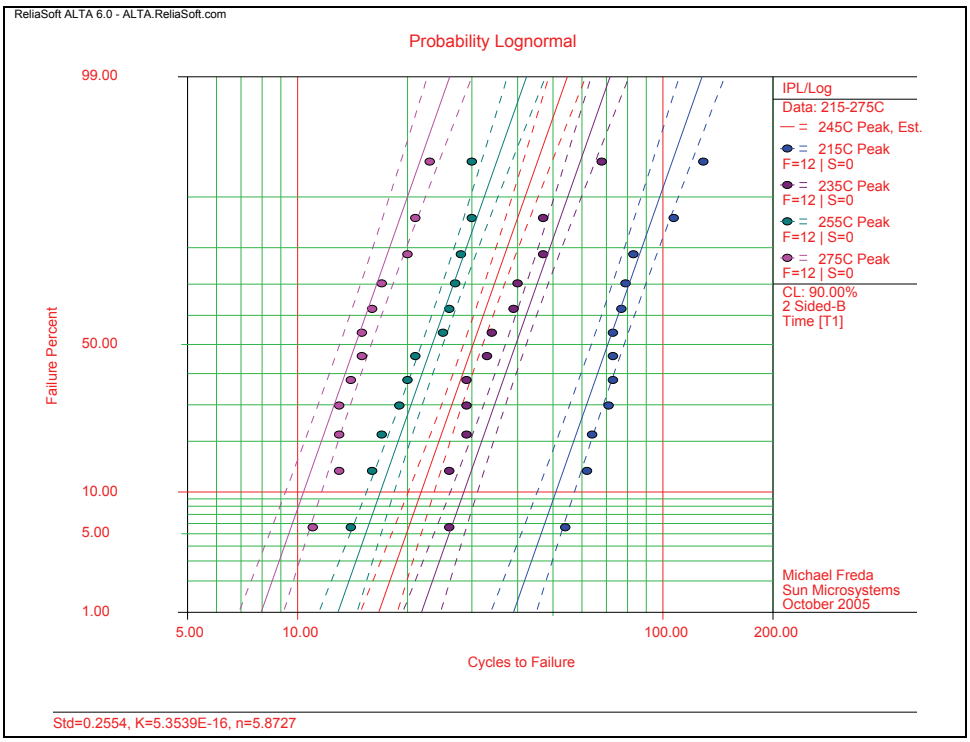
Where,

L represents a quantifiable life measure; for this paper both Mean life and T1% life are used
V represents the stress level
K is one of the model parameters to be determined, (K>0)
N is another model parameter to be determined

During our testing above Tg, we decided to IST test at four temperatures for a number of reasons:

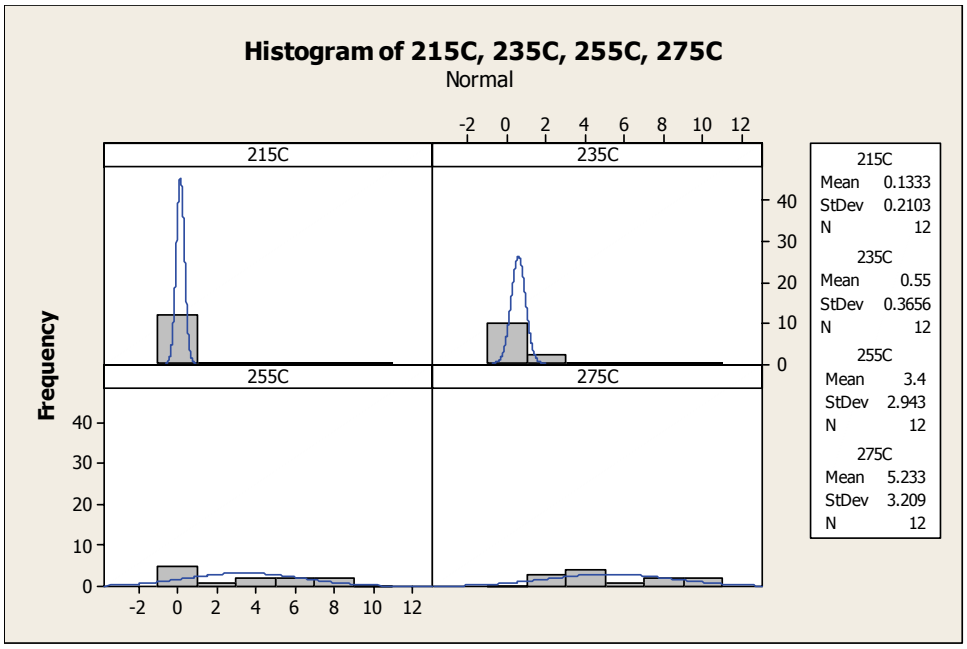
1. To allow making an estimate of cycles to failure over the full range of assembly temperatures
2. By graph cycles to failure versus test temperature we gain insight into the shape of the failure curve
3. To see if testing at high temperatures introduces new failure modes
4. To better understand the safety margins of the laminate materials

In selecting four temperatures above Tg, 215°C is about the lowest you can go and still be far enough above the Tg transition zone where there are significant changes in laminate material properties. The rational for using 275°C is to see if there are changes in via failure modes at temperatures above the expected maximum Sn/Ag/Cu lead-free soldering temperature zone.



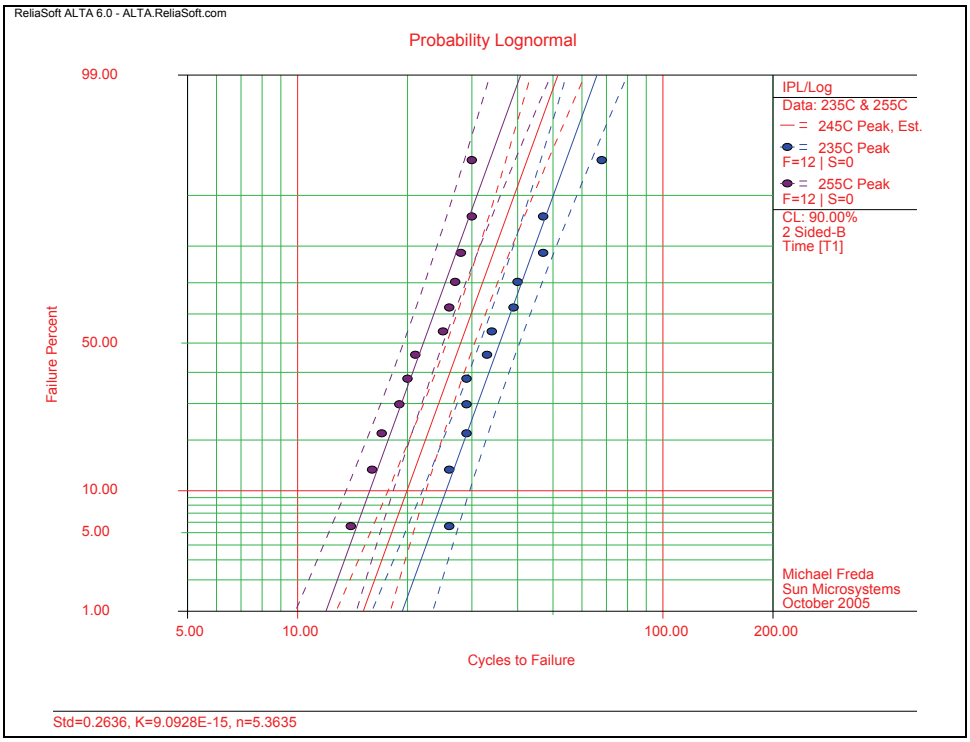
Graph 2 – IST test results from >Tg at four temperatures. Inverse Power Law relationship used to establish the best fit to the data at multiple temperatures. The RED lines show estimated CTF at 245°C.

Neither Graph 1 nor Graph 2 display an obvious failure mode shift as the test temperature is increased. Nonetheless, IST test at 275°C did result in two POST interconnect failures out of 12 IST coupons. To check if a failure mode shift was occurring, we looked at the resistance shift on the POST interconnect daisy chain in the IST coupon versus temperature. A typical IST coupon design has two daisy chains referred to as a PTH and POST daisy chain. The PTH daisy chain is for test of small via diameters, runs from layer 1 to 26 to 1 to 26…, and is sensitive to fatigue in the center of the via. The POST daisy chain is for test of large via diameters, runs from layer 2 to 3 to 2 to 3… and from layer 24 to 25 to 24 to 25…, and is sensitive to interconnect separation between the plating in the hole to the inner layer connection pad.



Graph 3 – POST interconnect resistance increase (0-10%) versus IST test temperature.

In large, thick, high-end server pcb fabs with small pitch BGA components, the normal failure mode is fatigue of the small diameter plated through holes. The failure criteria used by Sun is a 10% resistance increase over the initial resistance of either daisy chain, which ever fails first. With the exception of the two IST coupons that failed for POST interconnect separation at 275°C; the remaining 46 coupons from test above Tg were all PTH failures. Graph 3 is important, it clearly shows the increase in resistance on the POST interconnect daisy chain as the IST test temperature is increased. So, even though only 2 of 48 IST coupons failed due to POST interconnect failure, Graph 3 shows there is a definite shift from small plated through hole interconnect failure to large plated through hole POST interconnect separation failure as the assembly peak temperature increased. Due to this failure mode shift on the 275°C IST data and concern that the cycle to failure data at 215°C is too close to the Tg transition zone, data from 235°C and 255°C is used to make the IPL/Lognormal estimate of cycles to failure at a Sn/Ag/Cu assembly temperature of 245°C. We will use 245°C as our lead-free assembly temperature for the remainder of this paper. From the data obtained from cycle to failure test of laminate material above Tg and data analysis method we utilized, it is easy to estimate cycles to failure at other temperatures within the range of 215°C to 275°C. Graph 4 shows the IPL/Lognormal plot and Table 2 summarizes the analysis from the three temperature combinations investigated.



Graph 4 – IST test results >Tg at two temperatures, 235°C and 255°C. The RED lines show estimated CTF at 245°C.

Table 2 – Cycle to failure estimates versus failure rate.

	CTF at 245C from IPL/Log Normal Model			
	T1%			T50%
Temperatures Used for Model	LCI	Nominal	UCI	
215, 235, 255, and 275C	15.35	17.70	19.27	31.23
215, 235,and 255C	13.58	16.45	18.30	29.35
235 and 255C	12.34	15.94	17.92	28.93

IST Testing and Data Analysis Below Tg

After completion of IST testing and data analysis above Tg, the team at Sun selected the preconditioning temperature to use (245°C) and the number of preconditioning cycles to use (2x, 6x, and 10x). Since IST test equipment is small and modular with each test machine holding six coupons, we started testing with preconditioning and then cycle to failure at the higher temperature of 150°C. At no time did we attempt to test more than six coupons of any single test condition at a time. In hindsight, this was fortunate since the cycles to failure for IST coupons with low preconditioning cycles and coupons tested at 120°C took much longer to cycle to failure than our original estimates. In the end, we decided to add a fourth level of preconditioning of 18x at 245°C and forego testing in three cells with either a low number of preconditioning cycles, a low peak temperature below Tg, or both since they would have taken too long to cycle to failure. See Table 1 for the original DoE plan and the actual DoE we ended up using.

From the perspective of data analysis, combining data from test above Tg, and from test below Tg where different levels of preconditioning were used is a challenge. As previous mentioned, while the IPL relationship is valid for non-ferrous metals, we need to understand the stress versus temperature to enable plotting of cycles to failure versus stress. This is due to the large change in laminate material properties below and above Tg. In past work Sun has tested Miner's Rule (also called the Palmgren-Miner cycle-ratio summary theory) [8], but the amount of data was not statistically significant. Miner's Rule does not deal with temperature versus stress issue already discussed, and over the wide temperature range in which we are interested, changes in failure modes can invalidate predictions made at low temperature. This paper will now look at a number of data analysis techniques, including Miner's Rule, to address these problems.

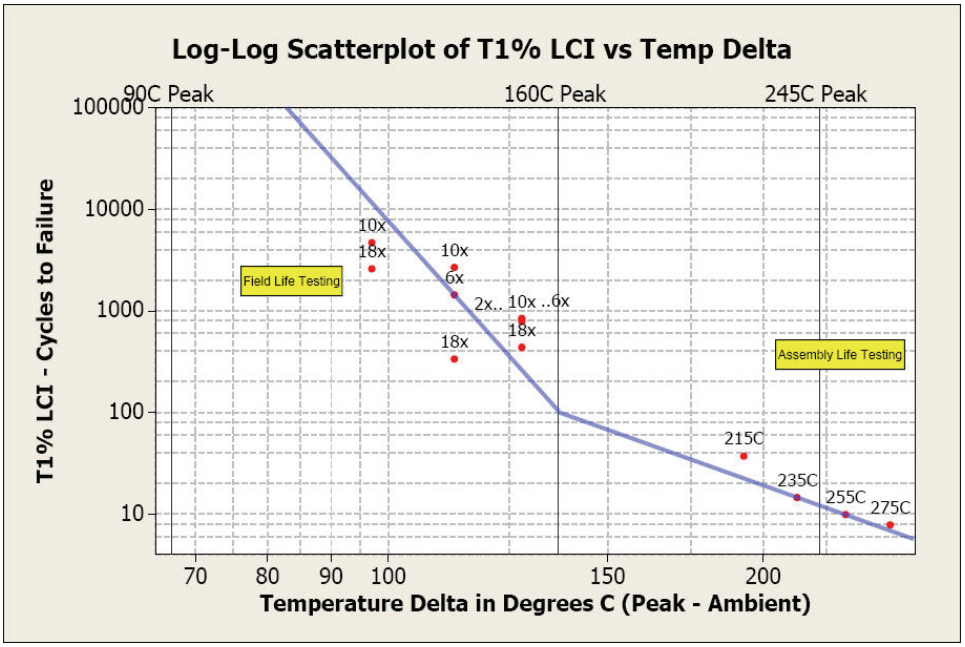
Table 3 – All data from the IST testing discussed in this paper listed below. The method used to derive the stress levels discussed later.

Raw Data - Cycles to Failure

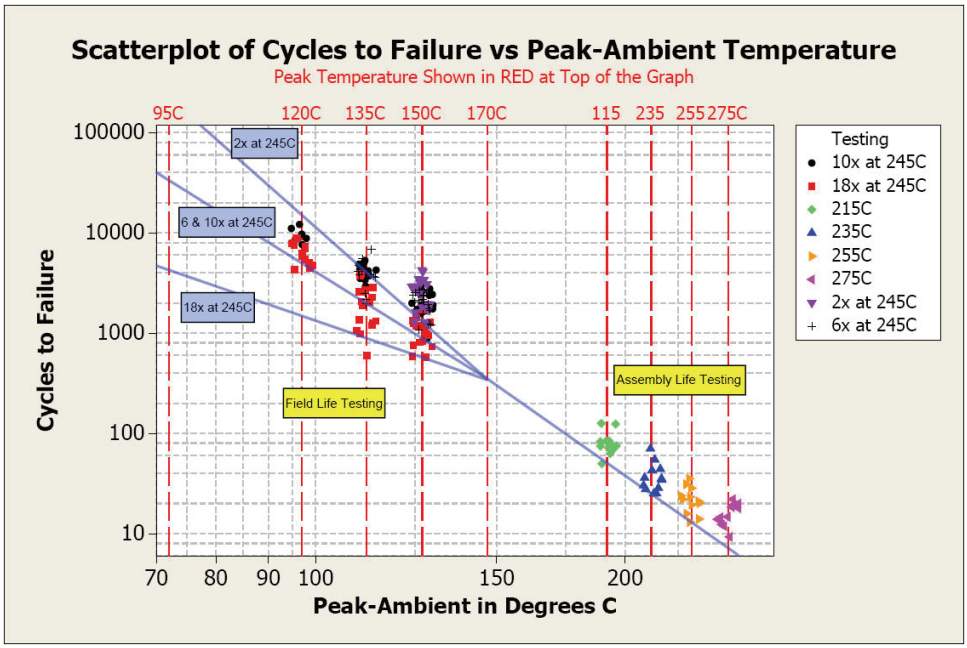
Temperature Stress Levels												
CTF at 215C	CTF at 235C	CTF at 255C	CTF at 275C	2x245C then CTF at 150C	6x245C then CTF at 150C	10x245C then CTF at 150C	18x245C then CTF at 150C	6x245C then CTF at 135C	10x245C then CTF at 135C	18x245C then CTF at 135C	10x245C then CTF at 120C	18x230C then CTF at 120C
Stress Levels (Mpa)												
CTH at 102.4 Mpa	CTF at 108.7 MPa	CTF at 114.4 MPa	CTF at 119.5 MPa	2x111.6 MPa then CTF at 61.9 MPa	6x111.6 MPa then CTF at 61.9 MPa	10x111.6 MPa then CTF at 61.9 MPa	18x111.6 MPa then CTF at 61.9 MPa	6x111.6 MPa then CTF at 52.3 MPa	10x111.6 MPa then CTF at 52.3 MPa	18x111.6 MPa then CTF at 52.3 MPa	10x111.6 MPa then CTF at 44.0 MPa	18x111.6 MPa then CTF at 44.0 MPa
73	29	20	11	**4000**	1806	2209	1343	3718	4286	11	8058	7651
83	68	30	15	3645	2390	1931	631	4010	4278	1209	**12000**	4032
129	29	26	13	3492	2252	1531	1359	5965	4213	2271	10088	4784
77	26	19	13	3348	1088	1460	312	4026	4899	**4000**	8096	6601
73	33	14	13	3359	2103	1711	1024	5319	3657	1483	10627	11
107	47	28	20	**4000**	1087	1777	856	2372	4899	1028	7877	17
73	26	30	16	2915	2566	1970	754	3164	4005	2908		6000
71	47	27	17	2512	2188	2276	1066	2182	3969	2355		4983
62	29	16	23	2804	2291	1966	1419	3825	3410	2895		5485
64	39	21	15	2405	2236	997	821	4966	4008	2417		9
79	40	17	14	2441	1842	1865	1331	2870	3370	**4000**		4034
54	34	25	21	1854	2572	1549	1136	4194	3402	2200		6013
				1710	2025	2476	1129			1023		**8000**
				1334	1695	3030	694			1891		6761
				2029	1751	1435	834			2311		**8000**
				1691	1598	3050	820			577		**8000**
				1836	1242	1945	1038			1357		5473
				1522	2011	1549	1712			1005		6784

Cells in BLUE failed due to POST Interconnect separation, all other failures were for PTH fatigue.
Cells in **BOLD** did not fail. Testing suspended at the number of cycles in bold.
Cells in RED are outliers. These all failed early due to the excessive preconditioning of 18x at 245C.

Graph 5 uses a graphical method plotting the T1%, 90% lower two sided confidence interval and using 6x thermal cycles at 245°C to estimate cycles to failure at a 95°C peak field usage condition. From this we estimate 550,000 cycles to failure in the field. At 365 thermal cycles per year (considered worst case for high-end servers), this is equivalent to over 1,500 years of field life! In Graph 6 we plotted all the raw data to give a feel for the variation. Instead of using the T1% value, we try to stay below the worse case data point. On both Graph 5 and Graph 6 we assume there is an inflection point (or discontinuity) in the laminate Tg transition zone with data below Tg and data above Tg following a different trend line. While this is a good assumption, where to place this inflection point is a matter of judgment that can have a significant effect on the cycle to failure estimates at a 95°C field life temperature. It also should be noted that on both graphs, the data for 6x and 10x preconditioning seems to be reversed with 10x having life close to 6x or if anything a bit longer. We have no good explanation for this other than a combination of a relatively small sample size and random chance.



Graph 5 – Log-log plot of T1% lower 90% two-sided confidence interval versus temperature.



Graph 6 – Log-log plot of all cycle to failure data versus temperature.

In earlier work of this type performed at Sun [3, 4], we noticed a discontinuity in the IPL/Lognormal distribution in data below Tg versus data above Tg. In that earlier analysis, the data to the left (below Tg) had a steeper slope than the data to the right (above Tg). This data does not appear to follow the same trend. At this point we do not know if this is due differences in the laminate material used or due differences in the pcb fab design, e.g., a much thinner pcb fab.

Regression Analysis using Miner's Rule

One common method to analyze paired data is the use of multiple regression. In this analysis example, we decided to use Miner's Rule that has the form of:

$$n_1/N_1 + n_2/N_2 + \ + n_i/N_i = C \qquad \text{eq. 3}$$

Where

$n_{1, 2, \ldots i}$ is the number of thermal cycles applied to the IST coupon at a specific temperature or stress level
$N_{1, 2, \ldots i}$ is the know number of cycles to failure, i.e., the life at a specific temperature or stress level
C is a constant determined by experimentation and is usually found in the range of $0.7 \leq C \leq 2.2$
If C=1 then Miner's Rule becomes a simple equation of what proportion of life is used at each temperature

Since we performed all testing below Tg with preconditioning, we do not know the values for N_{120C}, N_{135C}, or N_{150C}. From testing above Tg, we do know the value of N_{245C}. From testing below Tg, we know the number of preconditioning cycles used, the number of cycles to failure after preconditioning at three temperatures, and have a large set of data to utilize. We have 138 data points to use to predict the four unknowns: N_{120C}, N_{135C}, N_{150C}, and C. At first glance, equation 3 does not seem to follow the format for multiple regression. Therefore, our first step is to transform the general equation 3, customize it for our data, and then transform it to fit a multiple regression format.

$$n_{120C}/N_{120C} + n_{135C}/N_{135C} + n_{150C}/N_{150C} + n_{245C}/N_{245C} = C \qquad \text{eq. 4}$$

Next, define $INVNx = 1/N_x$ and then substitute it into eq. 4 to get eq. 6 eq. 5

$$n_{120C}*INVN_{120C} + n_{135C}*INVN_{135C} + n_{150C}*INVN_{150C} + n_{245C}*INVN_{245C} = C \qquad \text{eq. 6}$$

Since $n_{245C}*INVN_{245C}$ is know, we can further rearrange this to

$$- n_{245C}*INVN_{245C} = n_{120C}*INVN_{120C} + n_{135C}*INVN_{135C} + n_{150C}*INVN_{150C} - C \qquad \text{eq. 7}$$

This equation now has the form of

$$f(x, y, z) = a*x + b*y + c*z + d \qquad \text{eq. 8}$$

and we will solve it for $INVN_{120C}$, $INVN_{135C}$, $INVN_{150C}$, and C (a, b, c, and d)

We performed regression analysis using Minitab Release 14. The regression equation obtained is:

$$- n_{245C}*INVN_{245C} = n_{120C}*.00002103 + n_{135C}*.00008322 + n_{150C}*.00019318 - .67899 \qquad \text{eq. 9}$$

$$.67899 = n_{120C}*.00002103 + n_{135C}*.00008322 + n_{150C}*.00019318 + n_{245C}*INVN_{245C} \qquad \text{eq. 10}$$

$$.67899 = n_{120C}/47{,}551 + n_{135C}/12{,}016 + n_{150C}/5{,}177 + n_{245C}*INVN_{245C} \qquad \text{eq. 11}$$

Table 4 – Regression output from Miner's Rule analysis with Minitab Release 14.

The regression equation is

$$-(n245 \times INVN245) = -0.67899 + (0.00002103 * n120) + (0.00008322 * n135) + (0.00019318 * n150)$$

The regression equation is

$$0.67899 = \frac{n120}{47{,}551} + \frac{n135}{12{,}016} + \frac{n150}{5{,}177} + \frac{}{N245}$$

Predictor	Coef	SE Coef	T	P
Constant	-0.67899	0.03238	-20.97	0.000
n120	0.00002103	0.00000590	3.56	0.001
n135	0.00008322	0.00001082	7.69	0.000
n150	0.00019318	0.00001673	11.55	0.000

S = 0.140212 R-Sq = 54.4% R-Sq(adj) = 53.4%

Analysis of Variance

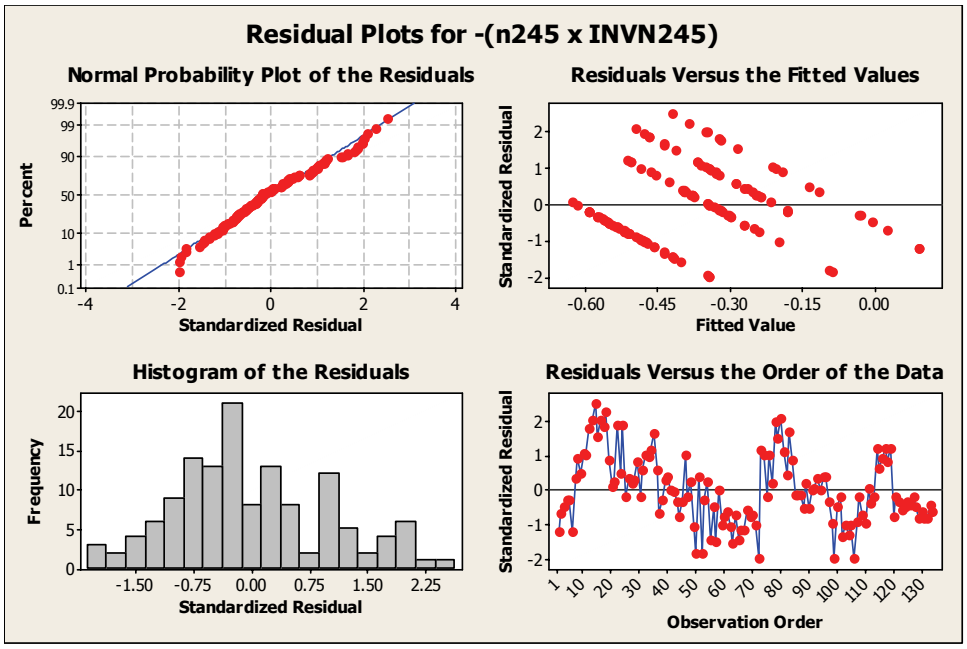
Source	DF	SS	MS	F	P
Regression	3	3.0527	1.0176	51.76	0.000
Residual Error	130	2.5557	0.0197		
Total	133	5.6085			

Source	DF	Seq SS
n120	1	0.4220
n135	1	0.0082
n150	1	2.6225

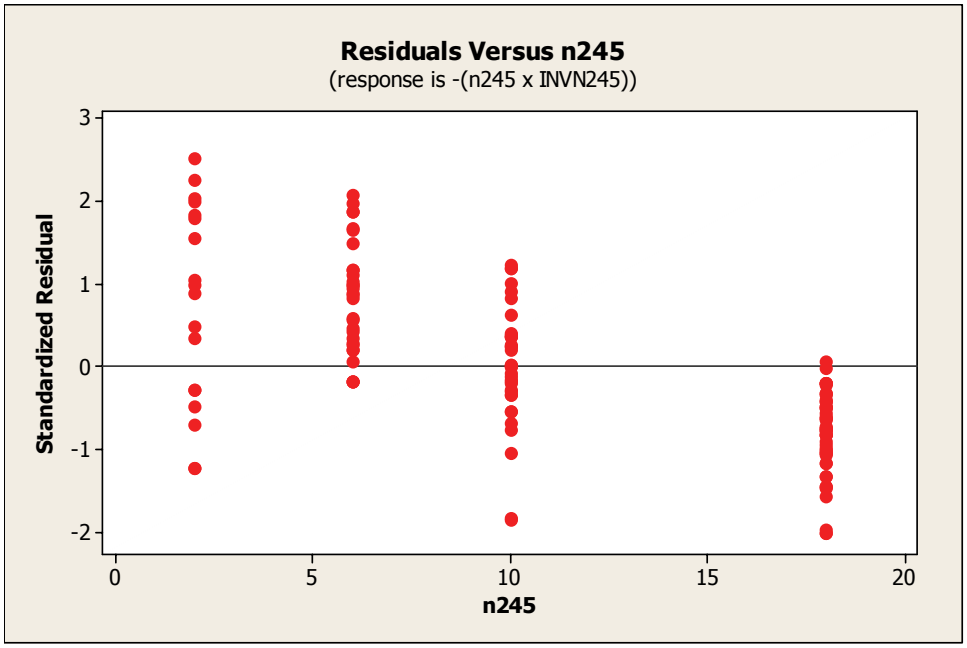
We can make a number of observations from the regression analysis results. Review of the R-Sq value of 54.4% and R-Sq(adj) value of 53.4% in Table 4 that are indicators of the goodness of fit of the model shows they are not the highest numbers, but they are reasonable. Considering that the cycle to failure data for each precondition level and subsequent thermal cycling below Tg had a minimum range of 2:1 from high to low, than with this amount of variation in the raw data used to construct the model, you will not get a high R-Sq value. If you look at the Analysis of Variance section in Table 4, the largest portion of sum of squares (SS) error is due the regression factors with n120 and n150 being the largest two contributors to the SS variation.

Graphs 7 through 9 are various residual plots from the regression analysis. Although we looked hard at the residual plots, no specific cause for the residuals was determined. We thought that the manufacturing date/lot code of the IST coupon might be a factor. To test this we rated each combination of preconditioning level and subsequent thermal cycling below Tg. IST coupons in the upper quartile of cycles to failure in each combination were assigned a value of +1, coupons in the lower quartile were assigned a value of -1, and those in between were assigned a value of zero. Then we totaled each date/lot code score and divided the total by the number of coupons in each date/lot code. We then used the resulting score to order the date/lot codes from one (the best with highest positive score) to seven (the worst with lowest negative score). We than ran the multiple regression analysis again, but this time we included a term for the rating of the date/lot code. The R-Sq values from this analysis did not support adding another term and the residual plot (Graph 9) did not show any strong date/lot code relationship.

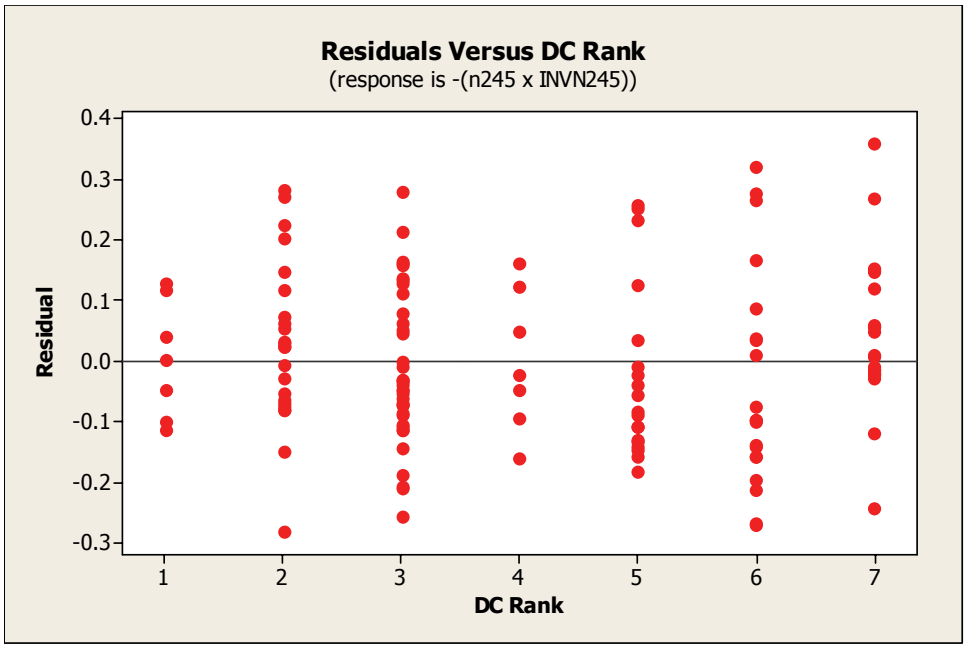
Graph 8 shows the residuals versus the number of preconditioning cycles at 245°C. This graph does show a trend, but we were unable to identify the cause at the time of writing this paper. One suspect is the 18x preconditioning since the cells with this high level of preconditioning also had the most outliers. Also, all but one of the 18x residuals was less than zero.



Graph 7 – Analysis results for regression analysis using Miner's rule..



Graph 8 – Standardized residual versus the number of preconditioning cycles shows a dip in cycles to failure with more preconditioning.

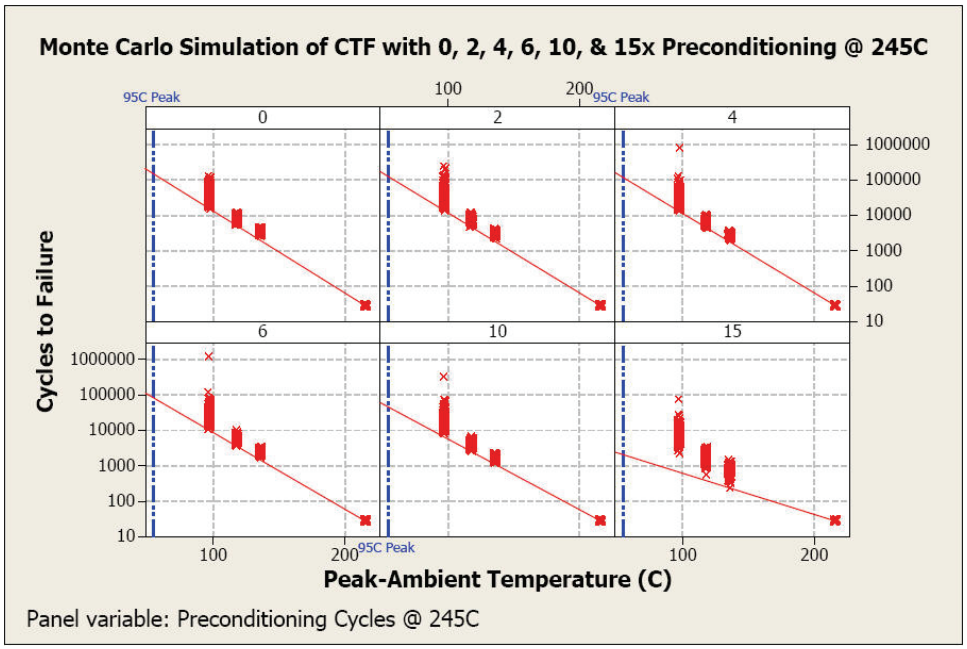


Graph 9 – Standardized residual plot versus the DC (date code) rank. There does not seem to be a trend between date codes. Therefore, the final regression model does not include a term for the data code.

One final observation is that the size of the coefficients from the multiple regression study, i.e., the predicted N_x values, are a good indicator of both the cycles to failure and the acceleration factors (AF) one would expect for thermal cycling without preconditioning.

N_{120} = 47,551 cycles to failure, obtained from multiple regression	$AF_{245\text{-}120}$ = 1,644
N_{135} = 12,016 cycles to failure, obtained from multiple regression	$AF_{245\text{-}135}$ = 415.3
N_{150} = 5,177 cycles to failure, obtained from multiple regression	$AF_{245\text{-}150}$ = 178.9
N_{245} = 28.93 cycles to failure, obtained from Lognormal distribution	$AF_{245\text{-}245}$ = 1

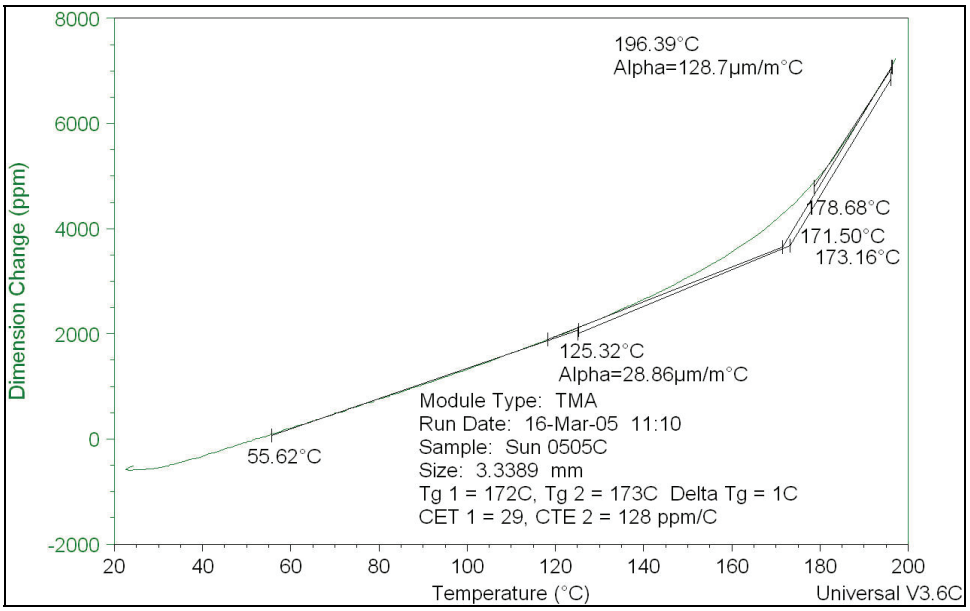
After completion of the Miner's Rule regression analysis, there remain two major issues with the analysis: 1) it returns averaged numbers for estimates of cycles to failure at temperature hiding the inherent variability of the raw data and 2) it does not address the large change in laminate material properties below and above Tg. Graph 10 shows one answer to the first issue, a Monte Carlo simulation that uses the coefficients from the Miner's Rules regression model and the coefficients for the standard error to predict cycles to failure with variation. Once the Monte Carlo model is developed, it is very easy to vary the number of preconditioning cycles at 245°C to gage the effect on field life with a 95°C peak temperature. The second issue, addressing the large change in laminate material properties below and above Tg requires a new analysis approach. We discuss this in the next section.



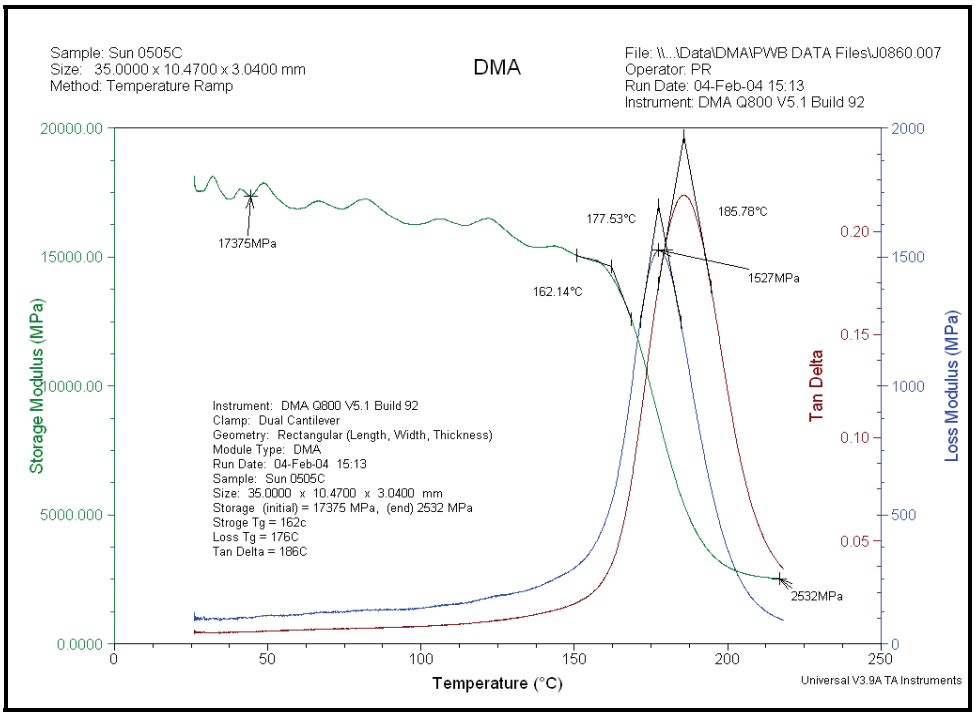
Graph 10 – Shows CTF versus Peak-Ambient temperature as assembly preconditioning at 245°C is varied from 2 cycles to 15 cycles. Each of the four temperatures per graph contains 1000 simulated data points.

Using TMA and DMA Data to Derive the Temperature versus Stress Relationship

Graphs 11 and 12 both show the large change in laminate material properties below and above Tg. Each graph shows the results from laminate material testing on one of the five date/lot codes tested (lot 0505C). Graph 11 shows an increase in the coefficient of thermal expansion (CTE) tested using thermal mechanical analysis (TMA) from 28.9 PPM/°C below Tg to 128.7 PPM/°C above Tg; a 4.45 times increase. Graph 12 shows a decrease in the tested storage modulus using dynamic mechanical analysis (DMA) from 18,000 MPa below Tg to 2500 MPa above Tg; a 7.2 times decrease. Tables 4 and 5 summarize the laminate material test data for five date/lot codes.



Graph 11 – TMA plot of expansion versus temperature for board date code 0505C.



Graph 12 – DMA plot of modulus versus temperature for board date code 0505C.

Table 4 – Expansion rate and Tg data from TMA testing.

TMA Results Using IPC TM-650 2.4.24						
Date Code	T 260 (Minutes)	CTE <Tg (ppm/C)	CTE >Tg (ppm/C)	Tg, 2nd Scan	Tg, 3rd Scan	Delta Tg
0505C	69	29	128	172	173	1
0805B	62	30	113	177	179	2
0805C	56	25	121	178	179	1
0805D	63	25	148	171	172	1
0805E	69	33	129	159	157	-2
Avg	63.8	28.4	127.8	171.4	172.0	0.6
StDev	5.45	3.44	12.99	7.57	9.00	1.52

Table 5 – Modulus and Tg data from DMA testing.

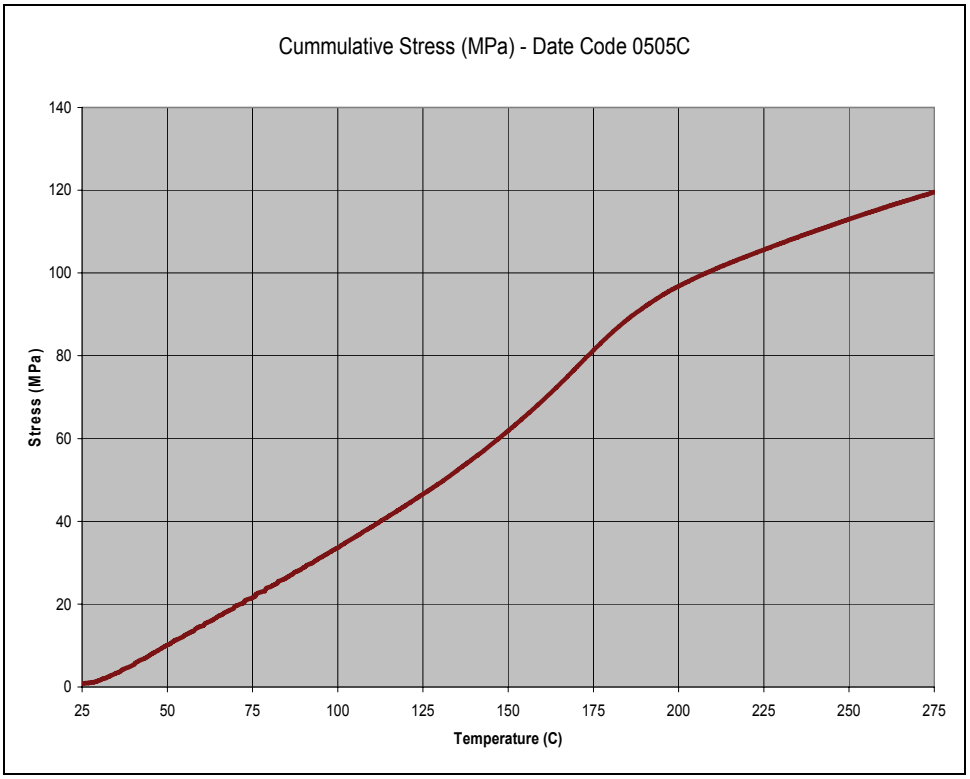
DMA Results Using IPC TM-650 2.4.24.4					
Date Code	Initial Storage Modulus (Mpa)	Final Storage Modulus (Mpa)	Tg from Storage Modulus (°C)	Tg from Loss Modulus (°C)	Tg from Tan Delta (°C)
0505C	17375	2532	162	176	186
0805B	15682	2672	169	181	188
0805C	16522	2858	164	182	188
0805D	16893	2854	167	183	189
0805E	16937	2750	163	182	189
Avg	16681.8	2733.2	165	180.8	188
StDev	635.49	136.64	2.92	2.77	1.22

Thickness: 3.02 to 3.10mm (.119 to .122 inch)

We used a simple 1st order approximation to derive the temperature versus stress relationship:

1. Use the expansion rate data from TMA in small increments and use it to calculate the strain for each small temperature increment (typically <1°C)
    a. Where Strain = $(L_{higher\ temp} - L_{original\ temp})/L_{original\ temp}$ where L is the length
2. Look-up the Modulus at temperature for each expansion increment
3. Calculate the incremental stress (Stress = Strain × Storage Modulus) for each temperature increment
4. Calculate the cumulative stress by adding each increment of stress as temperature rises from ambient to 275°C peak

Graph 13 shows the Temperature versus Stress relationship obtained using this method for one of the laminate material date/lot codes tested. Table 6 is a convenient cross reference of temperature versus stress on the copper PTH for the temperatures used in this paper. Knowing this relationship allows us to quantify the stress on the copper PTH from some of the temperature differences. For example, the lead-free assembly stress for Sn/Ag/Cu solder at 245°C is 111.6 MPa; this is 9% higher than the comparable eutectic solder assembly stress of 102.4 MPa at 215°C.



Graph 13 – Plot of stress on copper PTH vs temperature derived from TMA and DMA.

Table 6 – Cross-reference table from temperature to stress on the copper PTH.

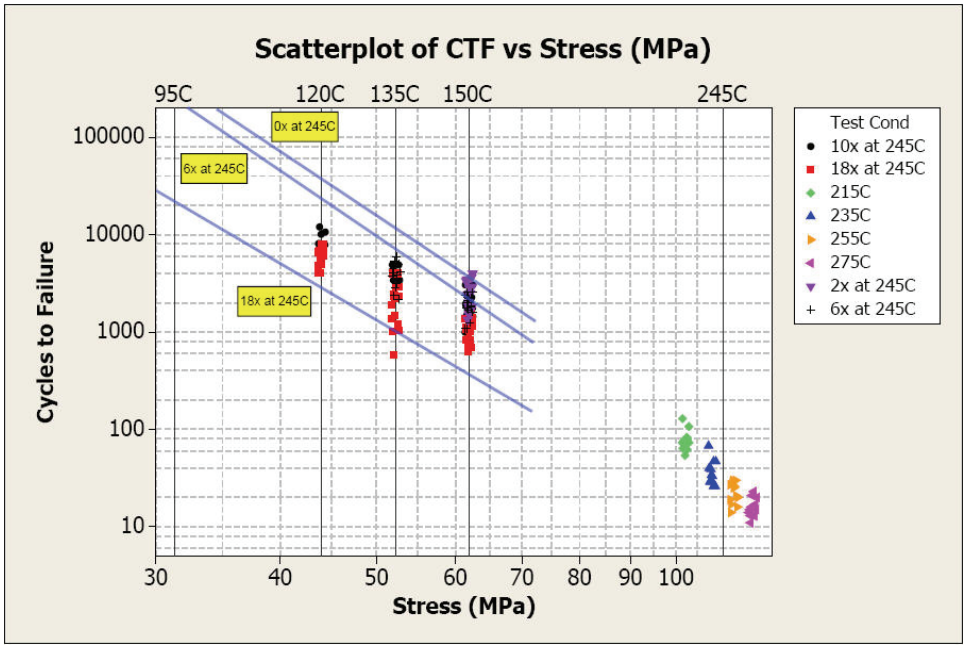
Peak Temperature, Degrees C	Peak - Ambient Temperature, Degrees C	Stress (Mpa)	Stress (PSI)
95	73	31.3	4,540
120	98	44.0	6,382
135	113	52.3	7,585
150	128	61.9	8,978
215	193	102.4	14,852
235	213	108.7	15,766
245	223	111.6	16,186
255	233	114.4	16,592
275	253	119.5	17,332

Analysis of Cycle to Failure Data versus Stress

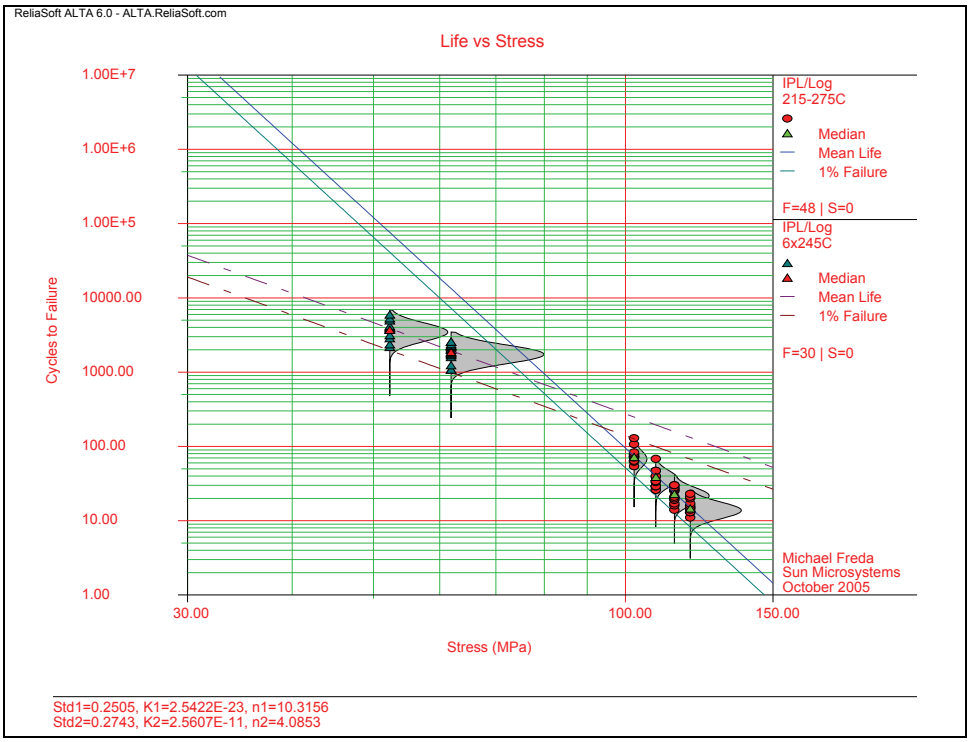
Now that we understand the stress on the copper PTH versus temperature relationship, we will use that information to make additional plots of cycles to failure versus stress. Graph 14 is a log-log scatter plot of all the raw data. The lines projecting to

95°C use Miner's Rule. In fact, switching from cycle to failure versus temperature to cycle to failure versus stress has no effect on the Miner's Rule relationship. Classic Miner's Rule plots are S-N plots so Graph 14 should be closer to Palmgren and Miner's original intend, but in the Table 7 comparison of results, Graph 14 shows the highest cycles to failure estimates of any of the analysis methods.

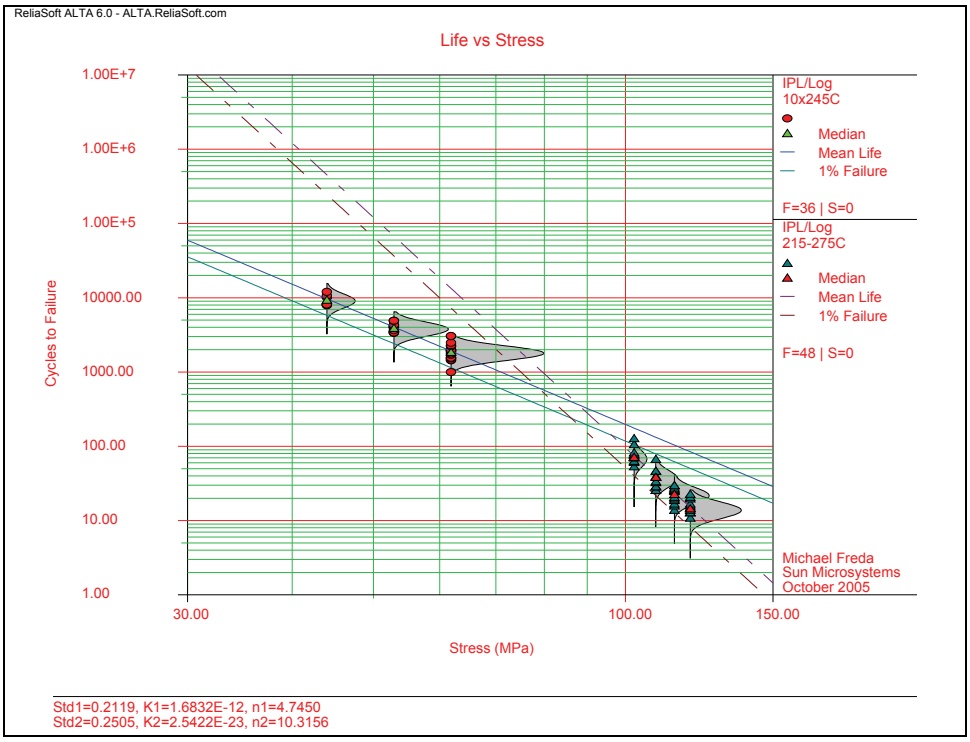
Graphs 15 through 17 use the IPL/Lognormal curve fitting capability of Reliasoft ALTA Version 6. The difference between the three graphs is the preconditioning at 245°C ranging from 6x, 10x, and 18x. In addition, we established a separate IPL/Lognormal relationship for data below and above Tg. Nonetheless, it does look like the data from 215°C (102.4 MPa) falls close to the relationship established from data below Tg. It is possible that 215°C was at a low enough temperature that it did not exhibit any hint of the failure mode shift from PTH to POST interconnect failure. Table 7 shows four estimates using this analysis method including 18x with four outliers removed (graph not included) and 18x with all data including four obvious outliers. As noted earlier, we added 18x preconditioning to the original DoE plan after testing had started. 18x was added due to very long cycles to failure at lower preconditioning cycles and lower thermal cycle temperatures. In hindsight, may be 15x preconditioning would have been a better choice, 18x does appear to be a bit excessive. Graph 17 clearly shows the effect of including the four outliers, it leads to a large drop in the cycles to failure and a skewed distribution. Once again, the cause is excessive preconditioning, if we had looked more carefully at the data analysis from testing above Tg, we would have selected a lower number of preconditioning cycles at 245°C.



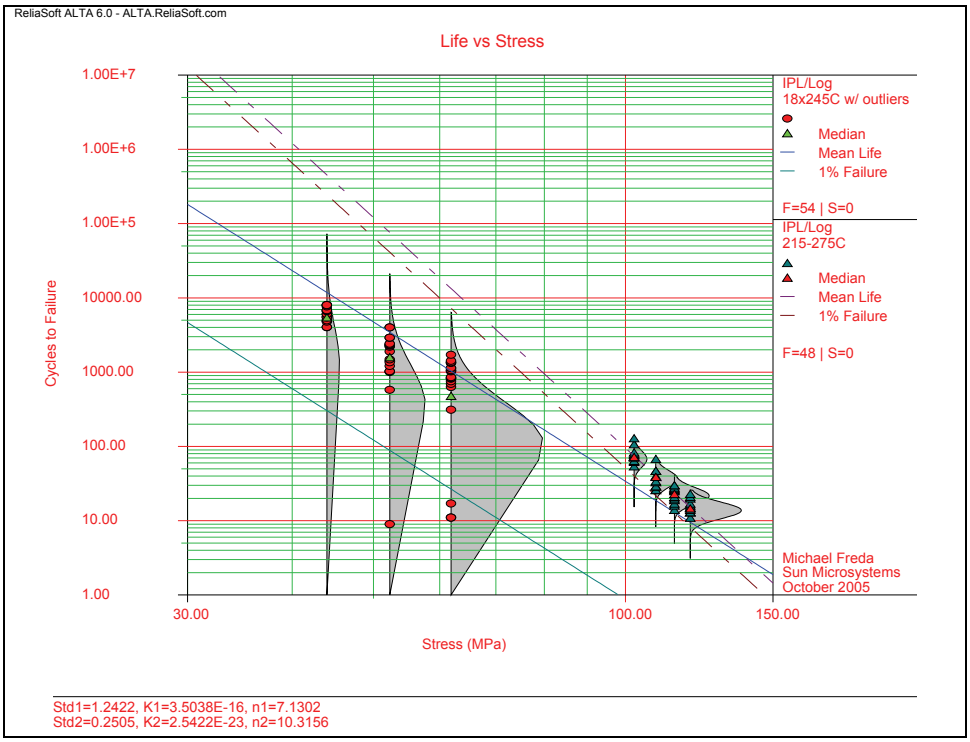
Graph 14 – Cycle to failure versus stress scatter plot of all the raw data. The light blue lines of cycles to failure versus stress based upon Miner's Rule.



Graph 15 – The plot uses IPL/Lognormal of stress versus cycles to failure. Separate estimates made below and above Tg due to preconditioning of 6x at 245°C below Tg.



Graph 16 – The plot uses IPL/Lognormal of stress versus cycles to failure. Separate estimates made below and above Tg due to preconditioning of 10x at 245°C below Tg.



Graph 17 – The plot uses IPL/Lognormal of stress versus cycles to failure. Separate estimates made below and above Tg due to preconditioning of 18x at 245°C below Tg. This plot includes <u>all</u> data points from testing with 18x preconditioning at 245°C including four outliers omitted from earlier analysis.

Table 7 – A comparison of CTF estimates using a number of analysis methods. Even with excessive preconditioning of 18x (>2.5x what is allowed on actual product with eutectic solder) the worst case estimate of cycles to failure is 3,500 cycles; equivalent to >9 years in the field at one thermal cycle/day.

Comparison of Cycles to Failure Estimates for a 95C Peak Field Life Tempeature Using the Various Methods		Preconditioning Cycles at 245C				
	Graph	2x	6x	10x	18x	T1%
Graphical Analysis of T1% from Lognormal Analysis of Temp vs CTF Data	Graph 5	-----	550,000	-----	-----	Yes
Graphical Analysis of Log/Log Scatter Plot of Temp vs CTF Data	Graph 6	250,000	35,000	35,000	4,200	No, but worst case data used for graph plot
Regression Analysis of CTF using Miner's Rule, then Monte Carlo, then Graphical Analysis of Monte Carlo Plots	Graph 10	260,000	87,000	48,000	2,800	No, but worst case data used for graph plot
Graphical Analysis of Log/Log Scatter Plot of Stress vs CTF Data (using Miner's Rule)	Graph 14	-----	240,000	-----	22,000	No
IPL/Lognormal Analysis of Stress vs CTF Data below Tg	Graph 15 & 16	-----	17,000	29,000	13,000	Yes
IPL/Lognormal Analysis of Stress vs CTF Data below Tg Including Outliers	Graph 17	-----	-----	-----	3,500	Yes

Comparison of Results

There is a wide difference in the results in Table 7. Some of this may be due to the inclusion of data with 18x preconditioning and the variability it adds. In general, the closer you get to the failure threshold during preconditioning, the wider the variability since a difference in one or two cycles to failure at the 245°C preconditioning temperature is equivalent to 170 to 3,000 cycles at thermal cycle temperatures. Looking at 6x preconditioning that is the equivalent to assembly and 2x rework, the lowest estimate is 17,000 cycles to failure from the various analysis methods. At 365 cycles per year, this is equivalent to 46 years of field life.

We need to discuss the resources needed to perform this type of thermal cycle testing. Those resources fall into three areas: 1) cost to fabricate test coupons, 2) cost of testing, and 3) cost of data analysis. The focus of this paper is to develop methods that can save cost in areas 1 and 2, even though it may add cost in 3. When we add the cost from these three areas together, our goal is a net cost reduction. Testing above Tg at multiple temperatures is fast and cost effective. For the 48 coupons tested above Tg, the average was 39 cycles to failure. In comparison, testing below Tg is slow and expensive. For the 138 coupons tested below Tg, the average was 3000 cycles to failure. In this paper, we looked at a number of variations in the amount of preconditioning and thermal cycle temperatures. Once we develop a valid method, then we can reduce the number of test conditions.

The method of using Miner's Rule and multiple regression followed by Monte Carlo simulation was complex and time consuming to develop, but does show promise. Nonetheless, with the proper statistical analysis tools multiple regression analysis is straight forward and fast. The Monte Carlo simulation was difficult the first time around, but lends itself to automation using a spreadsheet with macros or perhaps using a programming language like Matlab. The biggest issue we see with Miner's Rule is the need for a significant amount of data below Tg to make accurate predictions. The data below Tg is the most expensive to obtain due to the long to cycle to failure time.

Developing a method to merge TMA and DMA data to make a temperature versus stress curve was difficult the first time, but this method also lends itself to automation with a spreadsheet or Matlab. We feel that understanding the temperature versus stress curve is very important since it provides insight into what the laminate material is doing to the plated through hole. Understanding the temperature/stress relationship is also the key to performing testing in the Tg transition zone where test time should be fast, but where we can stay below the Tg where the PTH to POST interconnect failure mode shift occurs.

Conclusions and Summary

A number of data analysis methods for understanding plated through hole reliability versus temperature were developed, tested, and hold promise. In particular, we developed a method to produce a temperature versus stress curve from TMA and DMA testing of laminate material that is an important step forward. By understanding the stress applied to the copper plated through hole over a wide temperature range, we have more freedom to choose what temperatures we use to test. Since copper is stable in the temperature that we are interested in, knowing the stress on copper versus temperature means we no longer need to avoid testing in the laminate materials Tg transition zone.

Use of the data and analysis methods developed in this paper allow dropping the number of test conditions used to characterize a laminate material and pcb fab design. We would recommend testing above Tg, for example, 210°C, 235°C, 260°C, and 285°C to investigate failure mode shifts like the shift from PTH fatigue failure to POST interconnect separation, delamination, and in general, the laminate material safety margins at lead-free assembly conditions. This data is quick to get and provides insight into the plated through hole life that is useful for setting up test conditions for test below Tg. An example for test below Tg is 6x preconditioning at 245°C followed by thermal cycle to failure at 130°C, 180°C, and 210°C (50, 75, and 101 MPa). Assuming there is sufficient safety margin when extrapolating cycles to failure to field use conditions, this would be sufficient testing to estimate field life

There is an old saying "There is No Free Lunch" that is very appropriate here. The new analysis methods investigated in this paper hold the promise of reducing sample size and testing costs, but do require more advanced analysis expertise. So, in the short term the saying still holds true... Long term, these new analysis methods bring a much deeper understanding of plated through hole reliability at both assembly and in the field and this understanding is valuable to assist in making smarter business decisions and in reducing the amount of testing.

Future Work

Sun plans to perform additional thermal cycle life testing to understand plated through hole reliability in a lead-free assembly environment. In particular, we will continue to work on a couple of the most promising methods to improve them. We also plan to evolve from the 1st order stress on copper versus temperature model used in this paper to a model that incorporates the mechanical properties of both laminate material and the copper plating.

We encourage other parties to work in this area of plated through hole cycle to reliability and failure analysis and appreciate all constructive criticism of this work.

Acknowledgements

PWB Interconnect Solutions, Bill Birch, Neil Copeman, Jason Furlong
Sanmina-SCI, Owego, NY, Don Taylor
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University of Maryland-CALCE, Dr. Michael Pecht

Software Used in the Data Analysis
Microsoft Office Excel 2003
Minitab Release 14
Reliasoft ALTA Version 6
Sun Microsystems StarOffice Version 8

Acronyms Used
BGA – Ball Grid Array
CI – Confidence Interval
CPU – Central Processing Unit
CTF – Cycles to Failure
DMA – Dynamic Mechanical Analysis
DoE – Design of Experiment
HATS – Highly Accelerated Thermal Stress
IPL – Inverse Power Law
IST - Interconnect Stress Test
LCI – Lower Confidence Interval
PCB – Printed Circuit Board
PCB Fab – another name for a PWB
PTH – Plated Through Hole
PWB – Printed Wiring Board
Tg – T sub G or Glass Transition Temperature
TMA – Thermal Mechanical Analysis
UCI – Upper Confidence Interval

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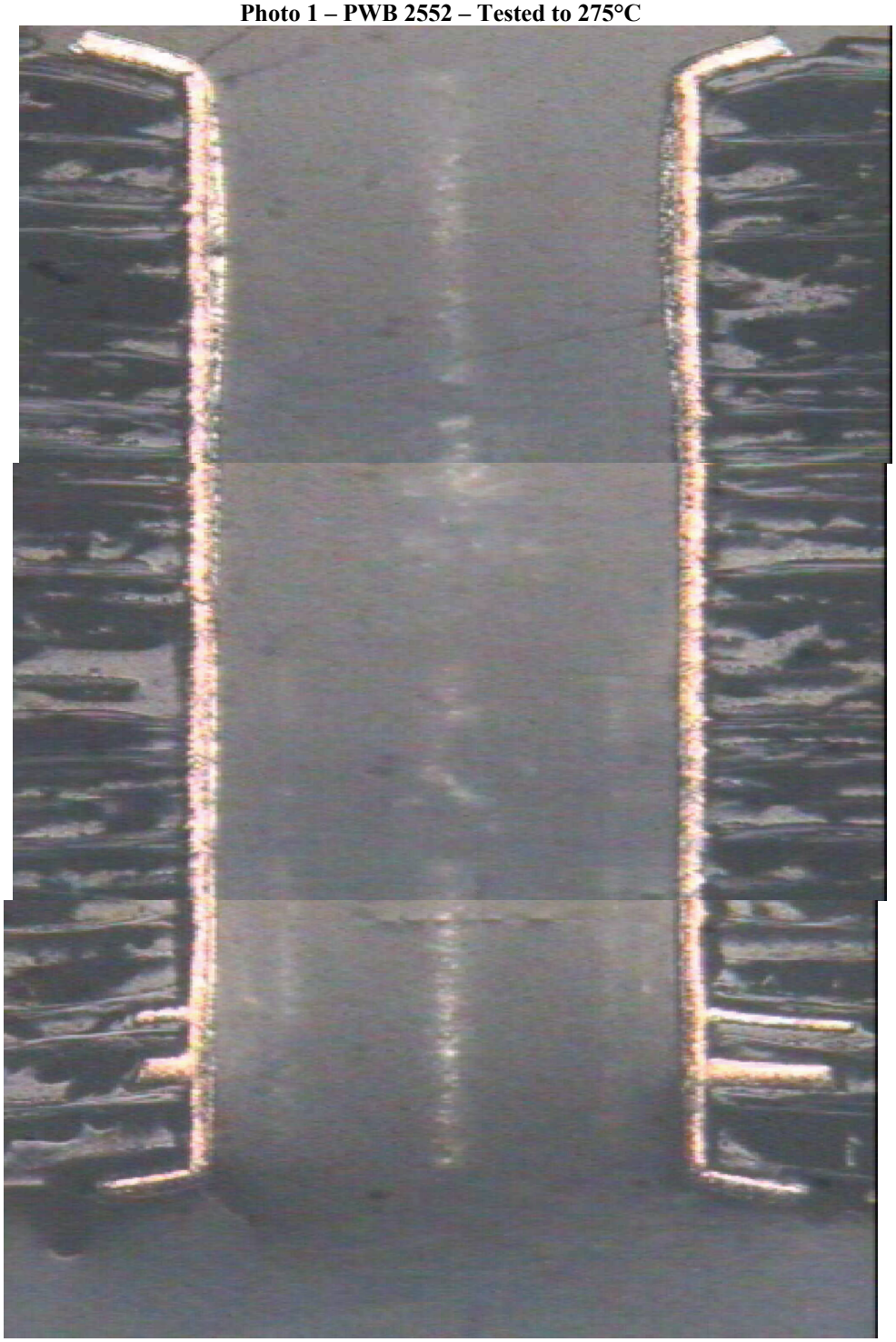
APPENDIX – Microsections of PTH and POST Interconnect Failure

Photo 1 – PWB 2552 – Tested to 275°C

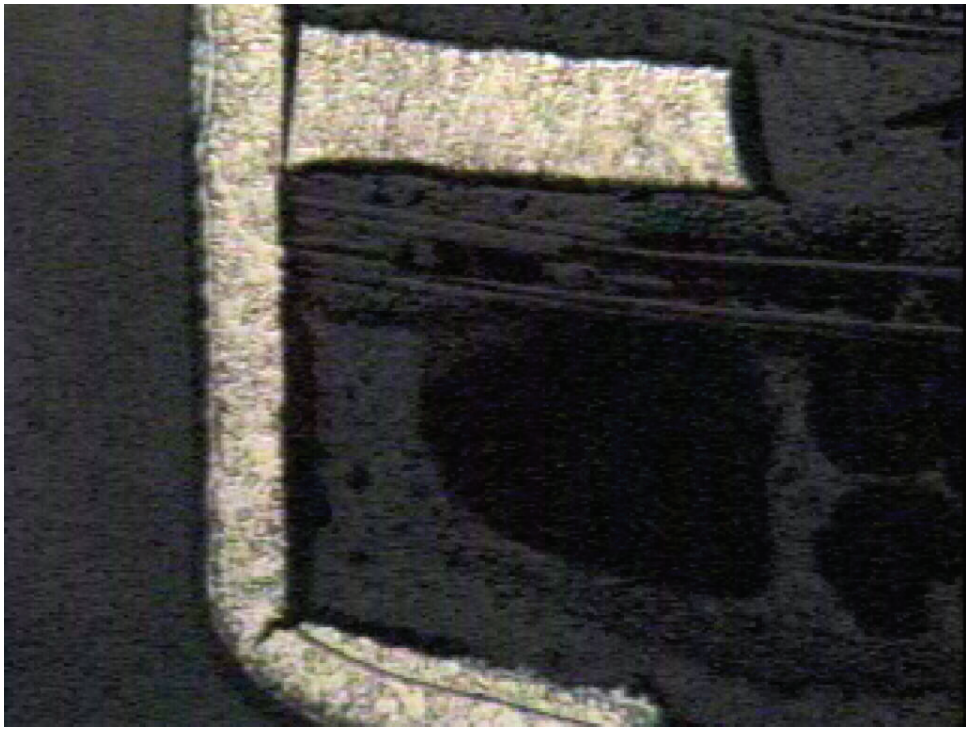


Coupon # 0805E-5849A - Mean Cu = .0012" – 20 Cycles – Post Failure

Photo 2 – PWB 2552 – Tested to 275°C

Coupon # 0805E-5849A - Mean Cu = .0012" – 20 Cycles – Post Failure

Photo 3 – PWB 2552 – Tested to 275°C

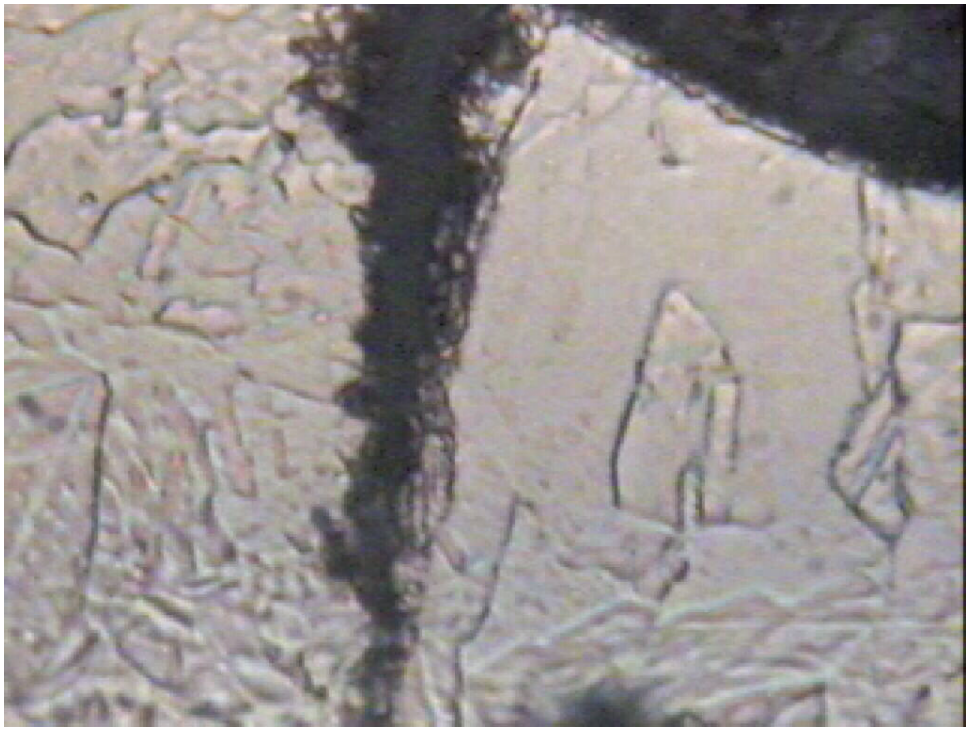


Coupon # 0805E-5849A - Mean Cu = .0012" – 20 Cycles – Post Failure

Photo 4 – PWB 2552 – Tested to 275°C

Coupon # 0805E-5849A - Mean Cu = .0012" – 20 Cycles – Post Failure

Photo 5 – PWB 2552 – Tested to 275°C

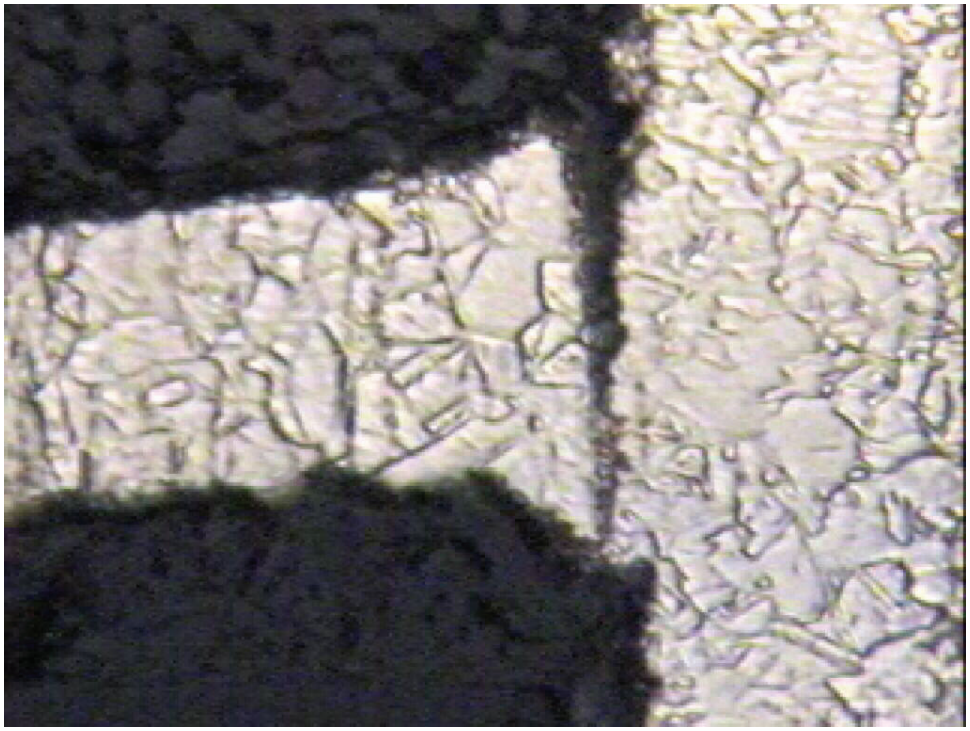


Coupon # 0805E-5849A - Mean Cu = .0012" – 20 Cycles – Post Failure

Photo 6 – PWB 2552 – Tested to 275°C

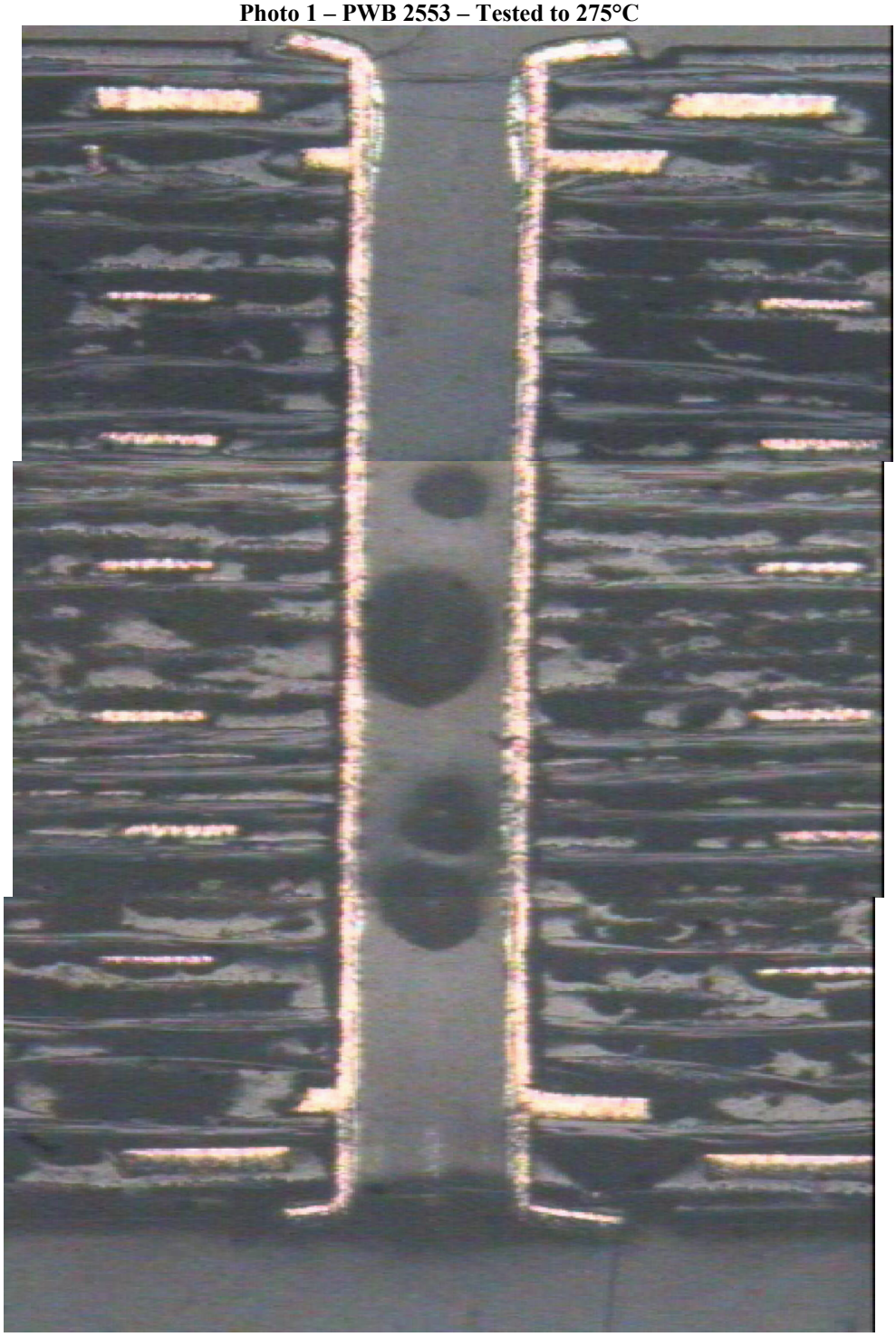
Coupon # 0805E-5849A - Mean Cu = .0012" – 20 Cycles – Post Failure

Photo 7 – PWB 2552 – Tested to 275°C



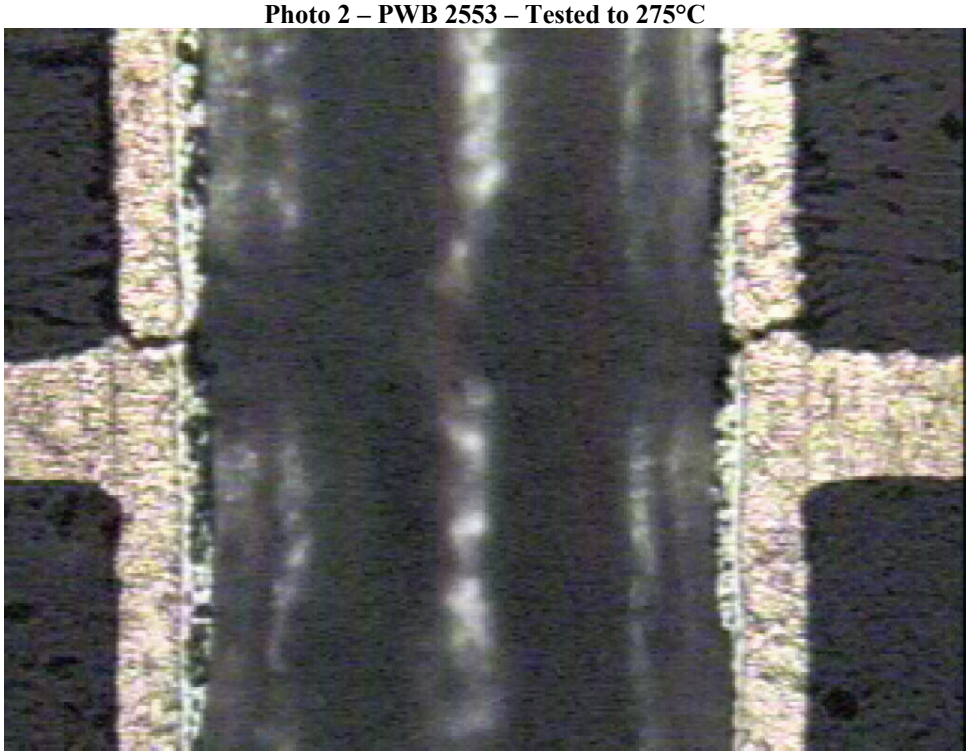
Coupon # 0805E-5849A - Mean Cu = .0012" – 20 Cycles – Post Failure

Photo 1 – PWB 2553 – Tested to 275°C



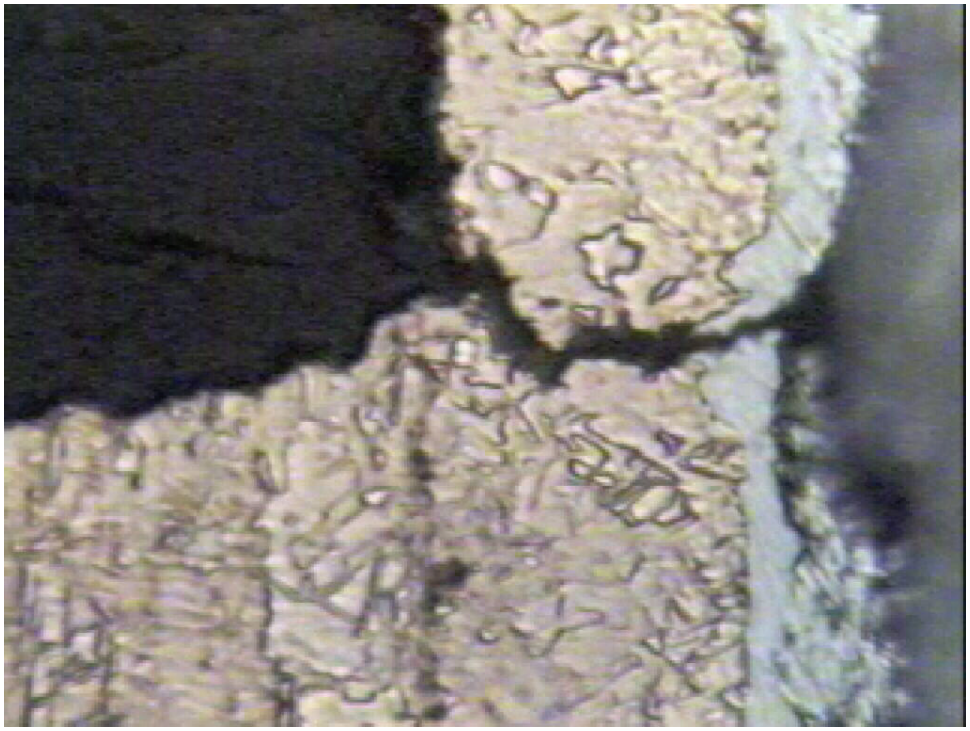
Coupon # 0405C-5769A - Mean Cu = .0013" – 13 Cycles – PTH Failure

Photo 2 – PWB 2553 – Tested to 275°C



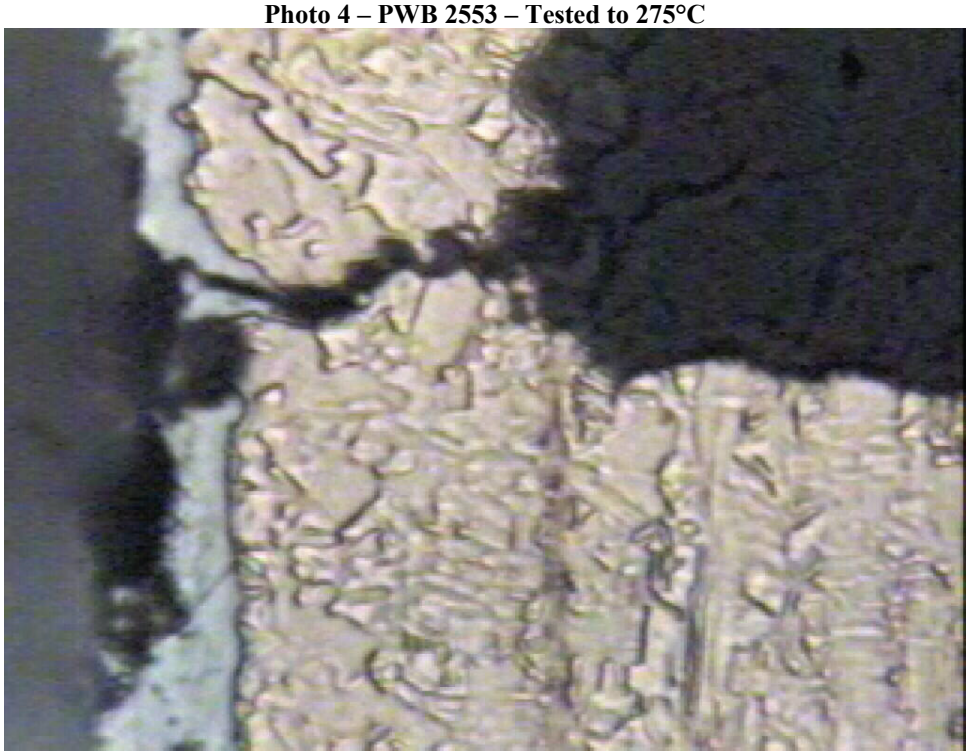
Coupon # 0405C-5769A - Mean Cu = .0013" – 13 Cycles – PTH Failure

Photo 3 – PWB 2553 – Tested to 275°C



Coupon # 0405C-5769A - Mean Cu = .0013" – 13 Cycles – PTH Failure

Photo 4 – PWB 2553 – Tested to 275°C



Coupon # 0405C-5769A - Mean Cu = .0013" – 13 Cycles – PTH Failure

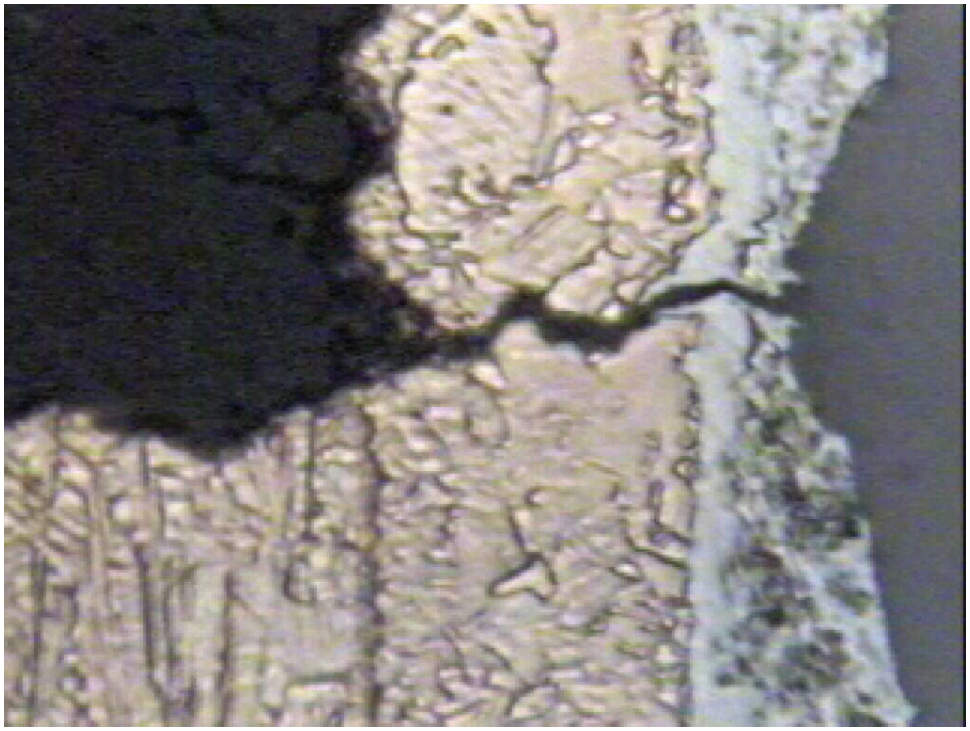
Photo 1 – PWB 2554 – Tested to 215°C

Coupon # 0405B-5647A - Mean Cu = .0013" – 71 Cycles – PTH Failure

Photo 2 – PWB 2554 – Tested to 215°C

Coupon # 0405B-5647A - Mean Cu = .0013" – 71 Cycles – PTH Failure

Photo 3 – PWB 2554 – Tested to 215°C

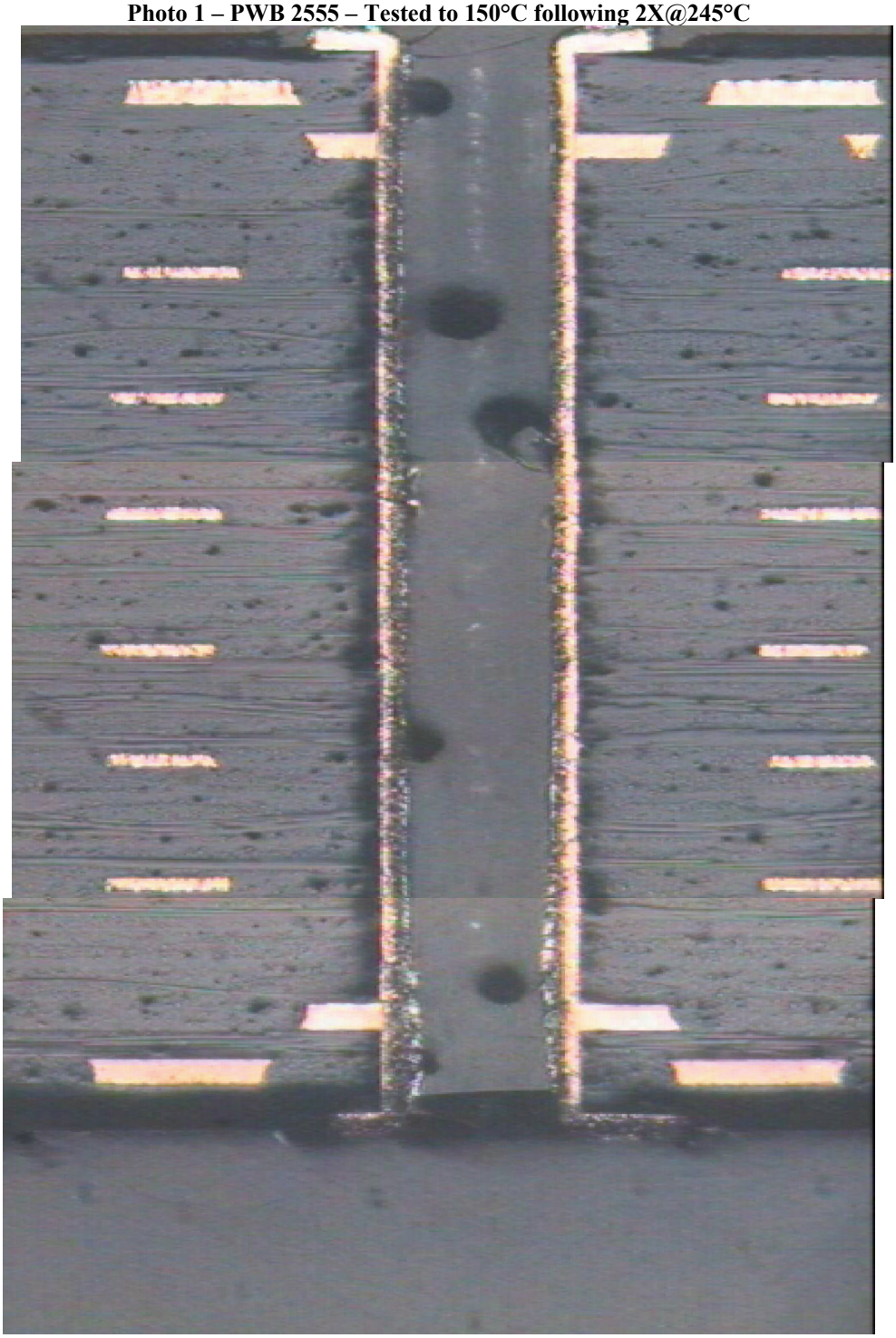


Coupon # 0405B-5647A - Mean Cu = .0013" – 71 Cycles – PTH Failure

Photo 4 – PWB 2554 – Tested to 215°C

Coupon # 0405B-5647A - Mean Cu = .0013" – 71 Cycles – PTH Failure

Photo 1 – PWB 2555 – Tested to 150°C following 2X@245°C

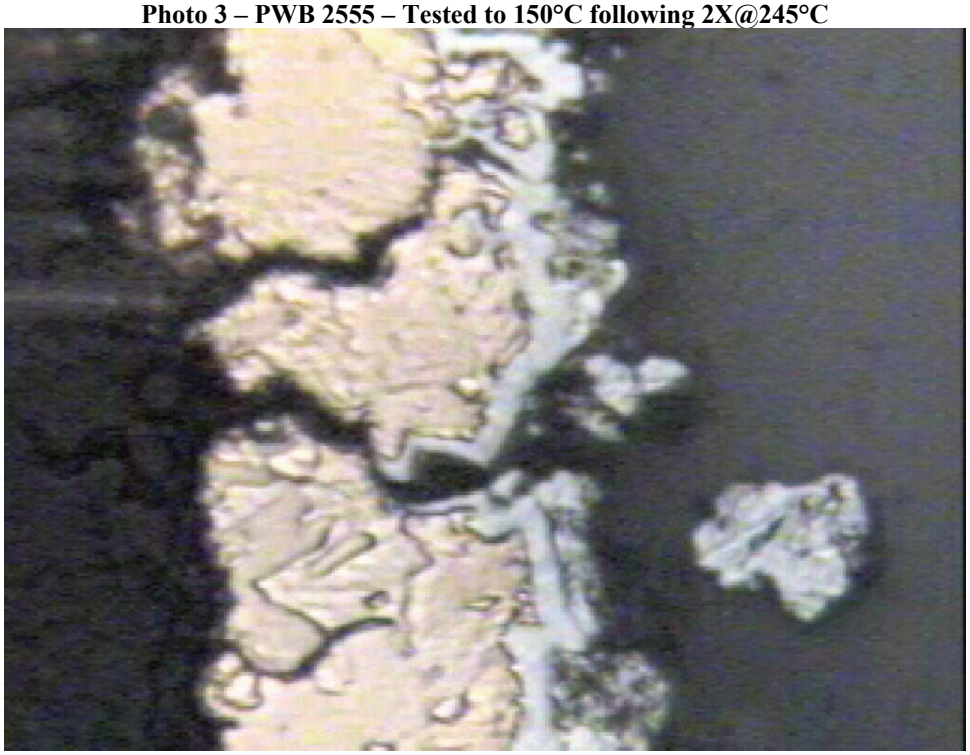


Coupon # 0805C-5989B - Mean Cu = .0013" – 1691 Cycles – PTH Failure

Photo 2 – PWB 2555 – Tested to 150°C following 2X@245°C

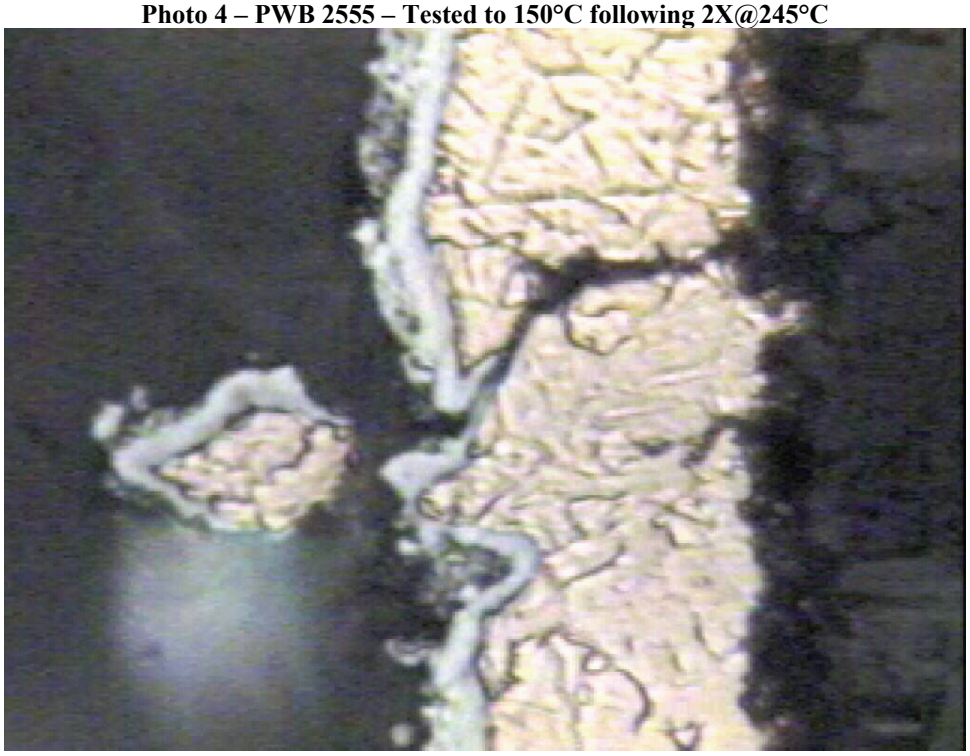
Coupon # 0805C-5989B - Mean Cu = .0013" – 1691 Cycles – PTH Failure

Photo 3 – PWB 2555 – Tested to 150°C following 2X@245°C



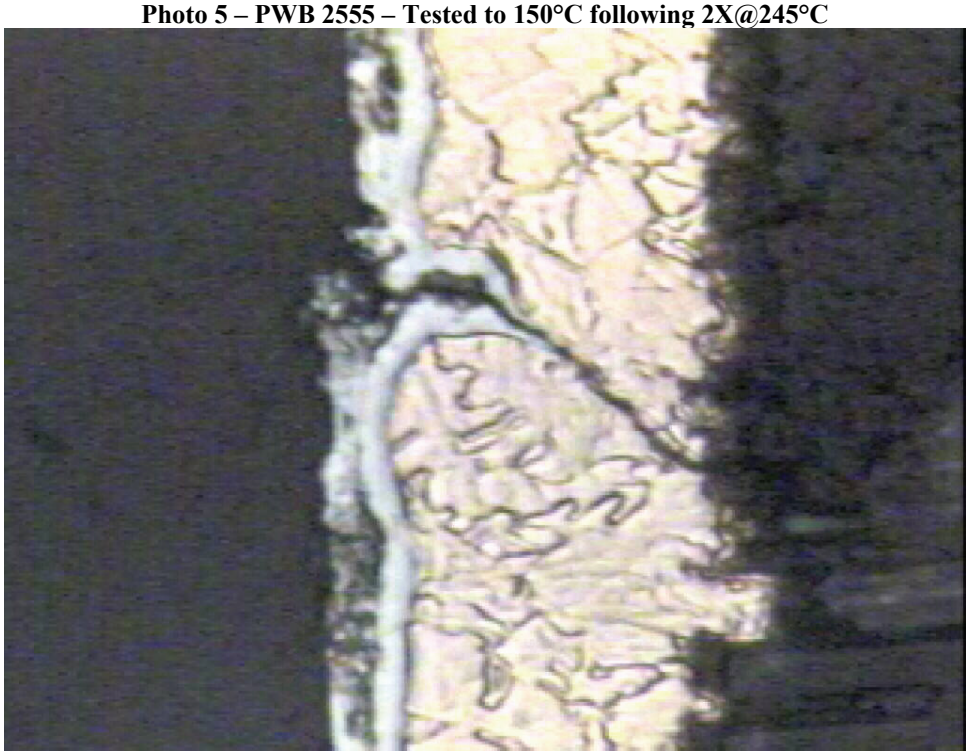
Coupon # 0805C-5989B - Mean Cu = .0013" – 1691 Cycles – PTH Failure

Photo 4 – PWB 2555 – Tested to 150°C following 2X@245°C



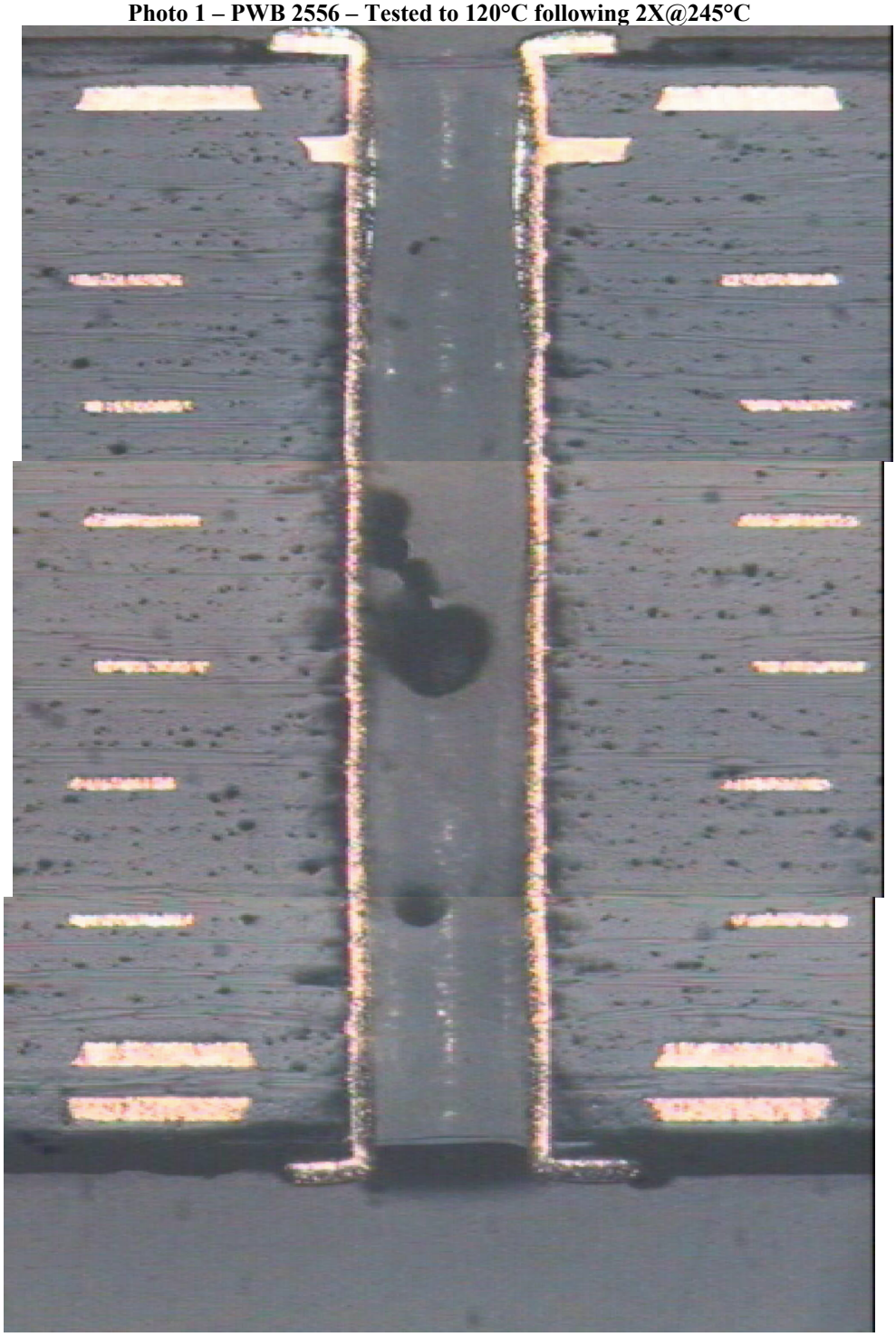
Coupon # 0805C-5989B - Mean Cu = .0013" – 1691 Cycles – PTH Failure

Photo 5 – PWB 2555 – Tested to 150°C following 2X@245°C



Coupon # 0805C-5989B - Mean Cu = .0013" – 1691 Cycles – PTH Failure

Photo 1 – PWB 2556 – Tested to 120°C following 2X@245°C



Coupon # 0805E-5890A - Mean Cu = .0013" – 3877 Cycles – PTH Failure

Photo 2 – PWB 2556 – Tested to 120°C following 2X@245°C

Coupon # 0805E-5890A - Mean Cu = .0013" – 3877 Cycles – PTH Failure

Photo 3 – PWB 2556 – Tested to 120°C following 2X@245°C

Coupon # 0805E-5890A - Mean Cu = .0013" – 3877 Cycles – PTH Failure

Photo 4 – PWB 2556 – Tested to 120°C following 2X@245°C

Coupon # 0805E-5890A - Mean Cu = .0013" – 3877 Cycles – PTH Failure

Photo 5 – PWB 2556 – Tested to 120°C following 2X@245°C

Coupon # 0805E-5890A - Mean Cu = .0013" – 3877 Cycles – PTH Failure