Thermal Stress Testing & Impact of High Thermal Excursion Pre-Conditioning on Cycles to Fail

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Abstract:
Today both Interconnect Stress Test (IST) and Highly Accelerated Thermal Shock (HATS) test methods are used to measure plated through hole via reliability. Both of these test methods have proved useful in their ability to quantify via reliability and have gained a wide level of acceptance and credibility within the industry.

This paper covers the use of HATS testing to determine the long-term reliability impact of simulated higher temperature assembly and rework thermal excursions. In particular, this paper will present data showing a complex relationship between higher temperature assembly processing and rework cycles, and subsequent HATS and IST cycles to failure (CTF). The Inverse Power Law (IPL) will be used to plot the via stress versus CTF relationship when cycling below the laminate material glass transition temperature (Tg).

Keywords:

IST, HATS, Lead-Free, Cycles to Failure (CTF)

Introduction:
Thermal Shock oven temperature cycling testing has a well established history as an indicator of the long-term field life of printed wiring board products. However, verified correlation with actual long-term field life has been difficult to achieve due to the long time required for testing and the associated expense. In the 1990's Interconnect Stress Testing (IST) was developed, and more recently Highly Accelerated Thermal Shock (HATS) testing has been developed, as a more practical indicator based upon the through hole via and internal interconnect reliability of printed wiring boards. Current printed wiring board technology trends, including the advent of higher lead-free temperature lead-free assembly processing, require a verified long-term reliability baseline. This baseline can best be based upon boards manufactured with historically standard FR4 laminate materials and eutectic tin-lead assembly alloy processing. This baseline is needed as the minimum acceptance standard for evaluating the long term reliability of more advanced printed wiring boards, including those manufactured using higher temperature lead-free assembly processing. It is preferred that the more cost effective HATS or IST test methodology can shown to be a good indicator of long term printed wiring board product reliability in the field.

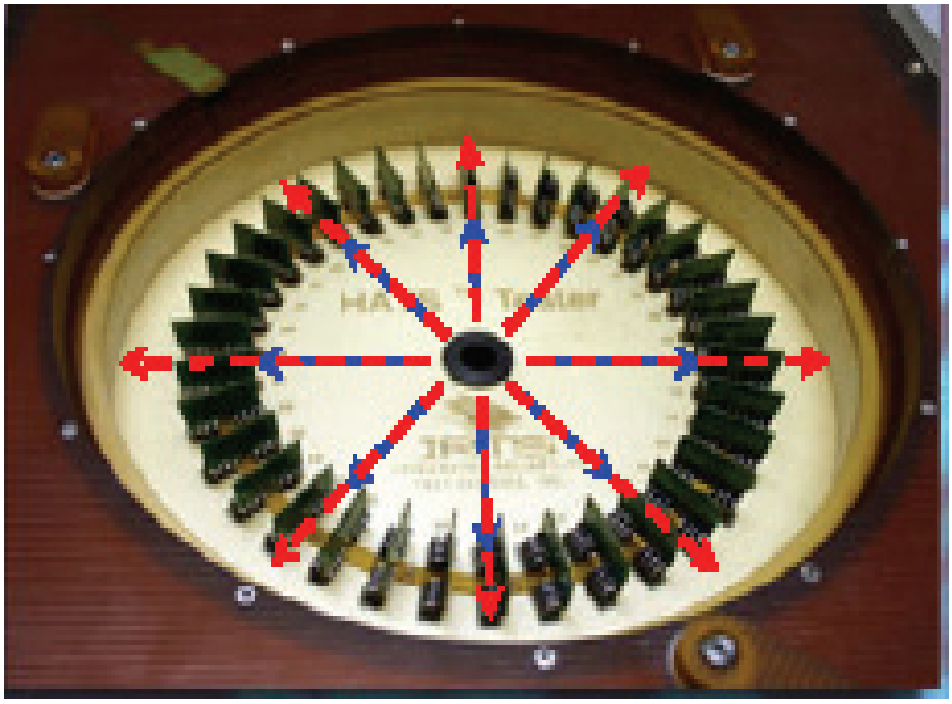
Background:
Although in many product applications the long term field life of printed wiring boards is not considered critical, in many telecommunications, enterprise systems, and other applications a 20 years or more product field life is required. New challenges to ensuring the required level of long-term product reliability include:

- Thicker printed circuit boards with higher aspect ratio plated through holes.
- Increasing use of large ball grid array devices that require filled and capped via-in-pads.
- Higher temperature lead-free assembly and rework processing (SnAgCu reflow alloy).

Thermal Shock Oven Testing: Measures cycles to fail (CTF) on actual functional production boards or appropriately designed test boards/coupons. The ovens are capable of air-air cycling over a potentially large temperature range (-40 to +145 C). Transition rates between 25 and 35 C per minute were used for this testing, with a 20 second dwell at both high and low temperatures.

IST Testing: Measures cycles to fail (CTF) on specially designed IST coupons that are thermally cycled using current flow through internal 'heating' circuits that heat the coupon and the adjacent plated through holes. Failure is defined as a 10 percent increase in the resistance of the plated through hole. Reference: IPC-TM-650, 2.6.26.

HATS Testing: Measures cycles to fail (CTF) on specially designed HATS coupons typically having 4 daisy chain nets each. There can be up to 36 coupons per chamber load that go through air-air cycling over a potentially large temperature range (-55 to +160 C). Transition rates for this testing are usually at least 25 degrees per minute up to 50 degrees per minute, depending upon the high and low temperature and the HATS equipment capability. Reference: www.Hats-Tester.com



ELEMENT	Thermal Cycling	IST	HATS
Stress – Temp Range	(-65, +125 C)	(+25, +250 C)	(-60, +160 C)
Temp Range >-20, <Tg	145 C	135 C	180 C
Characterization	Difficult	Easy (6 coupons)	Easy (36 coupons)
Failure Detection	Not Applicable	Early Detection	Early Detection
Cost of Ownership	High	Low	Low
Cost of Test	High	Low	Low
Data Collection	Optional	Integrated	Integrated
Capabilities	PTH	PTH & Post	PTH & Post
Time to Results	288 hrs	24 hrs	<24 hours
Installation	Hard Wired, Drainage, Compressed Air	AC Outlet	Compressed Air, AC
Microsectioning	Mass	Manual	Manual
Environmental	N2, CFCs	Friendly	Friendly
Cost (36 coupons, 500 cycles)	-	$2,700	$2,200

Sun Microsystems has several years of experience with IST testing as a comparative reliability monitoring tool. However HATS testing is being evaluated as perhaps more suitable for developing a stronger correlation with long-term field life.

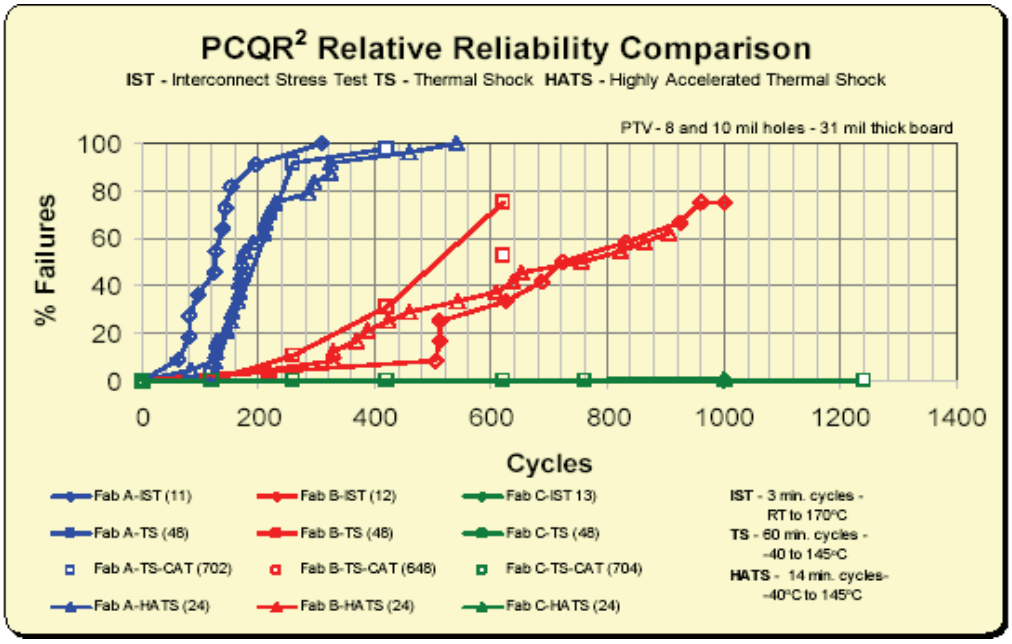
Comparison of Delphi Thermal Shock (TS), HATS, and IST Test Data:

The first milestone towards establishing a good long term reliability baseline for boards manufactured with standard FR4 laminate materials and eutectic tin-lead assembly alloy processing using HATS or IST testing is showing their correlation with the well established TS test results.

The IPC PCQR2 / CAT chart shown below demonstrates a reasonably good correlation of the Delphi HATS test results with the more established Thermal Shock oven temperature cycling testing over the same 185 C temperature range (-40 to +145 C). The test failure criteria was a 10 percent increase in resistance. The test results shown in blue are for a widely used standard dicyandiamide cured FR4 laminate material. The test results shown in red are for a commonly used phenolic-cured

FR4 laminate material.

IPC PCQR2 / CAT: Delphi Reliability Study (David L. Wolf, 14Apr2003)



The Delphi IST results are quite interesting. The lines in blue are for an established and widely used dicyandiamide cured FR4 laminate material. The lines in red are for a widely used phenolic cured FR4 laminate material. Due to the IST limitation of starting at ambient (room temperature of approximately 25 C), only a smaller 145 C temperature range was used in the Delphi Reliability Study (to stay below the laminate material Tg). Although the IST data for the phenolic-cured laminate material shows the expected higher IST 145 C cycles to failure compared with the HATS/TS 185 C cycles to failure due to the smaller cycling temperature range, the dicyandiamide-cured laminate material shows fewer IST 145 C cycles to failure with a smaller temperature range! Therefore a complex relationship between higher temperature thermal excursions and subsequent cycles to failure (CTF) is indicated, at least for some laminate materials.

HATS and IST Testing Goals:

Stage One
Establish a correlation between actual known long-term product field life and HATS test results. Achieve this goal by selecting hole sizes for the HATS daisy chain nets that are marginal for adequate long term field life using a well understood printed wiring board manufacturing technology. This will establish a HATS test baseline requirement.

Stage Two
Determine the comparative HATS reliability of test coupons made representing printed wiring board technology selected to withstand higher temperature lead-free assembly processing (printed wiring boards made using phenolic-cured FR4 laminate materials).

Stage Three
Identify a relationship or correlation between IST testing and HATS testing using IST coupons taken from the same test panels as the HATS test coupons used in Stage One and Stage Two.

HATS Testing:

Stage One
HATS test coupons were manufactured using standard dicyandiamide-cured FR4 laminate material with historically representative printed wiring board manufacturing technology including permaganate desmear, electroless copper plating, and pattern plating without prior panel plating and not utilizing reverse pulse plating. Each HATS test coupon was 1.0 x 2.0 inches in size having four daisy chain nets with the marginal hole sizes indicated:

> Net #1: Drilled Hole Size 13.5 mils Alternating Layers 1-26 182 Vias/Net

> Net #2: Drilled Hole Size 11.5 mils Alternating Layers 1-26 182 Vias/Net
> Net #3: Drilled Hole Size 13.5 mils Alternating Layers 4-23 182 Vias/Net
> Net #4: Drilled Hole Size 11.5 mils Alternating Layers 4-23 182 Vias/Net

A total of four (4) coupons from each of three (3) different working panels were tested for each test condition:

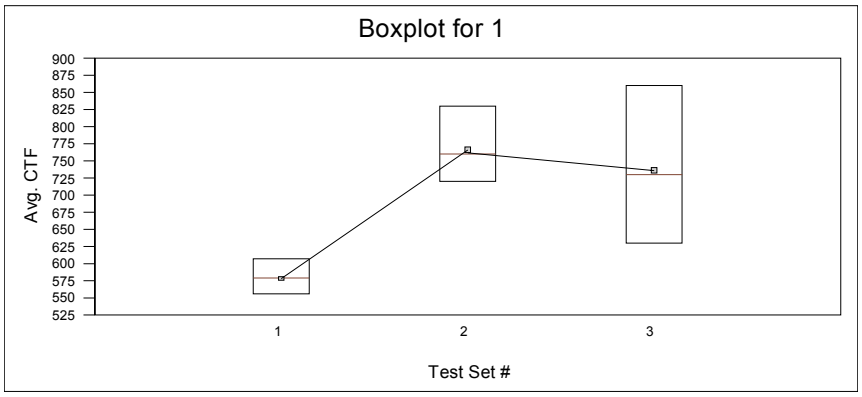
Test Condition	*Preconditioning 230 C (peak temp)*	*HATS Cycle*
> *1*	*8 X*	*0 to 160 C*
> *2*	*4 X*	*0 to 160 C*
> *3*	*0 X*	*0 to 160 C*
> *4*	*8 X*	*25 to 160 C*
> *5*	*4 X*	*25 to 160 C*
> *6*	*0 X*	*25 to 160 C*
> *7*	*8 X*	*0 to 135 C*
> *8*	*4 X*	*0 to 135 C*
> *9*	*0 X*	*0 to 135 C*

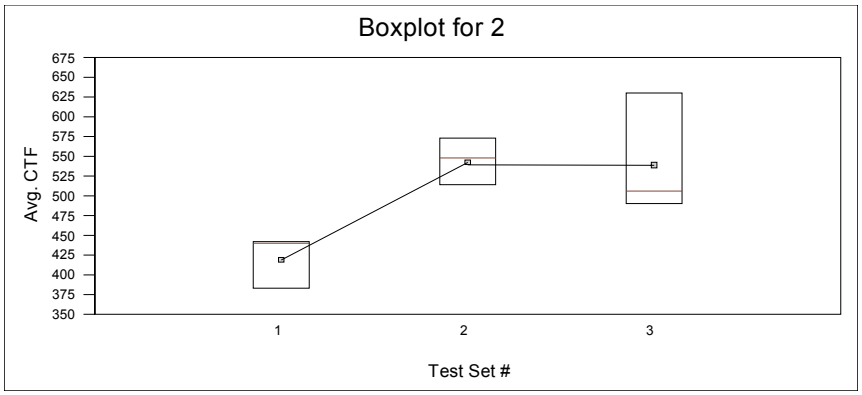
Stage Two - TBD
Manufacture HATS test coupons using FR4 laminate material selected for higher temperature lead-free assembly processing, including the utilization of phenolic-cured laminate material. The identical HATS test coupon design shall be used with four daisy chain nets and the same marginal hole sizes. The HATS testing will be done after simulated higher temperature SnAgCu reflow assembly and rework processing (preconditioning through assembly reflow profile with 260 C peak temperature instead of 230 C).

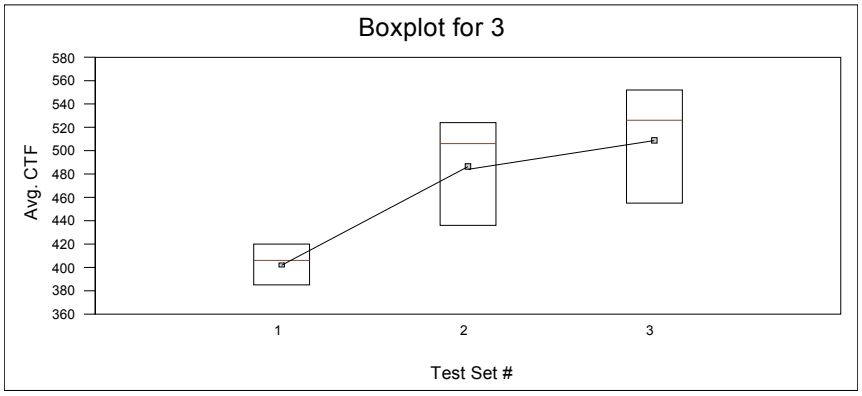
Stage Three - TBD
Perform Ambient to 160 C IST testing on IST coupons taken from the same test panels as the HATS test coupons used in Stage One and Stage Two, and compare with the Ambient to 160 C HATS test results for both dicyandiamide and phenolic cured laminate materials.

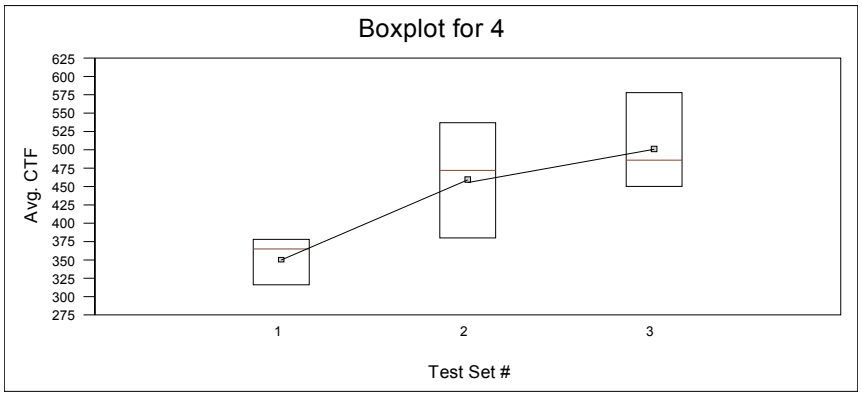
HATS Test Results – Stage One:

0 – 160 C HATS Cycling Test Results
The surprising results show that although there is not much change in reliability between the 0X (#3) and 4X (#2) 230 C preconditioning HATS test samples, there is a significant reduction in cycles to fail for the coupons that went through 8X (#1) 230 C preconditioning cycles. The following four separate box plots are for each daisy chain via hole type.



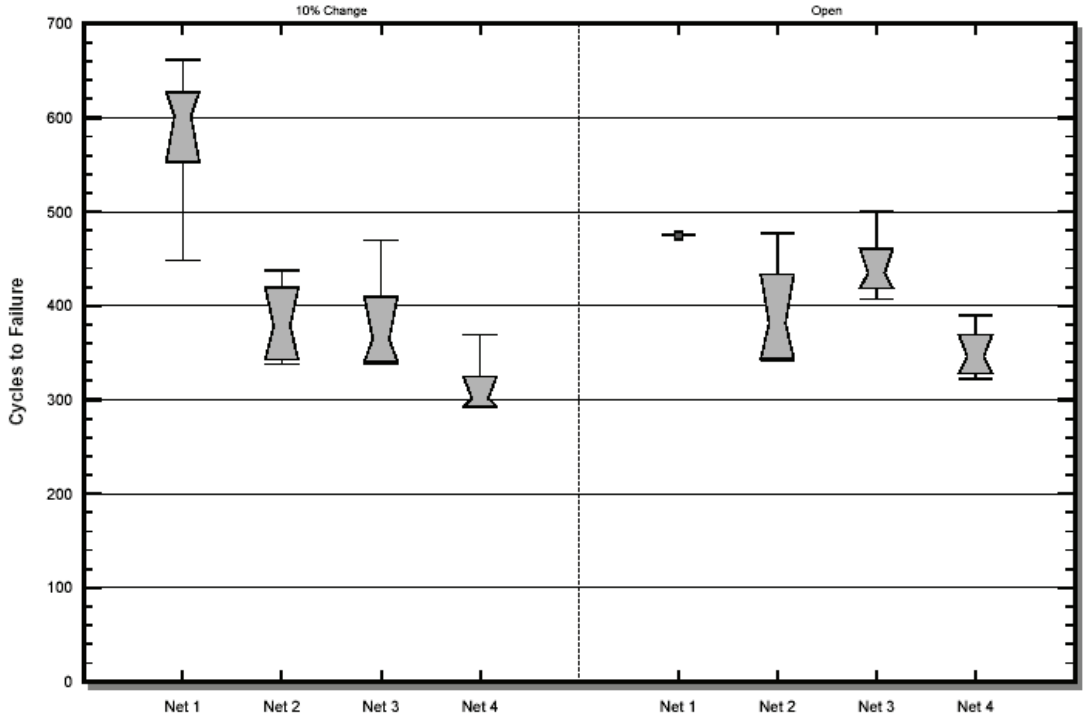




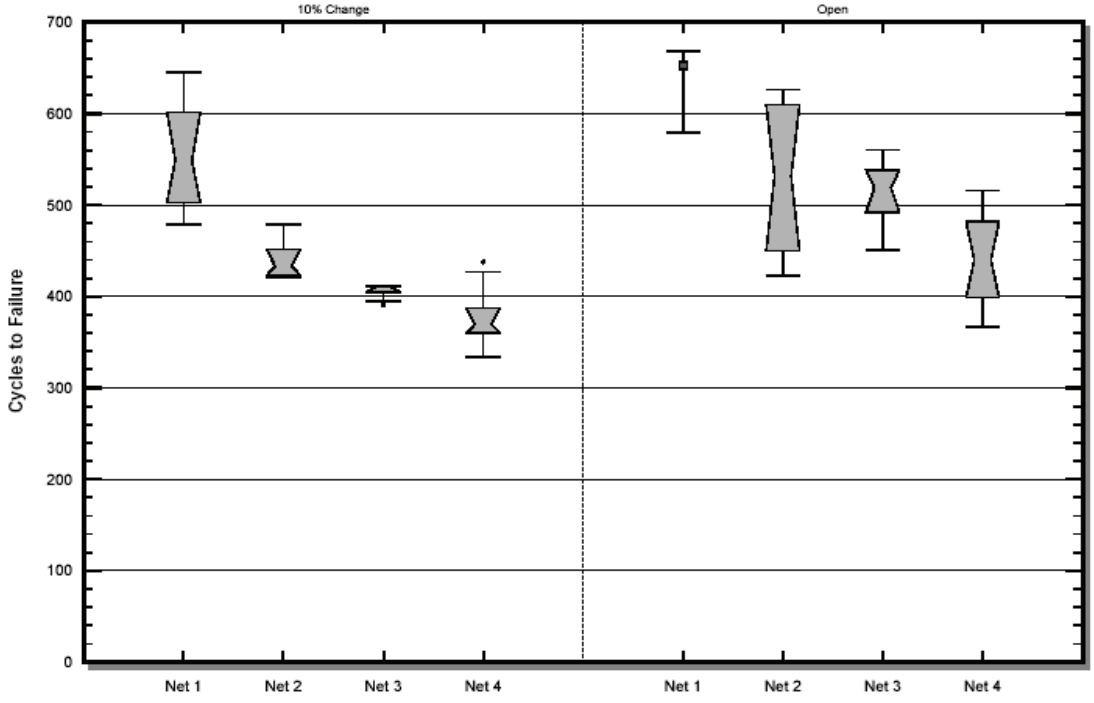


Initial Readings (0-160 C)	***DHS: 0.0135 inches***	***DHS: 0.0115 inches***
Daisy Chain: Layers 1 - 26	0.48 ohms	0.54 ohms
Daisy Chain: Layers 4 - 23	0.45 ohms	0.50 ohms

Test Condition #1 (Precondition 8X, 0 – 160 C HATS Cycling):
Panel #1



Panel #2



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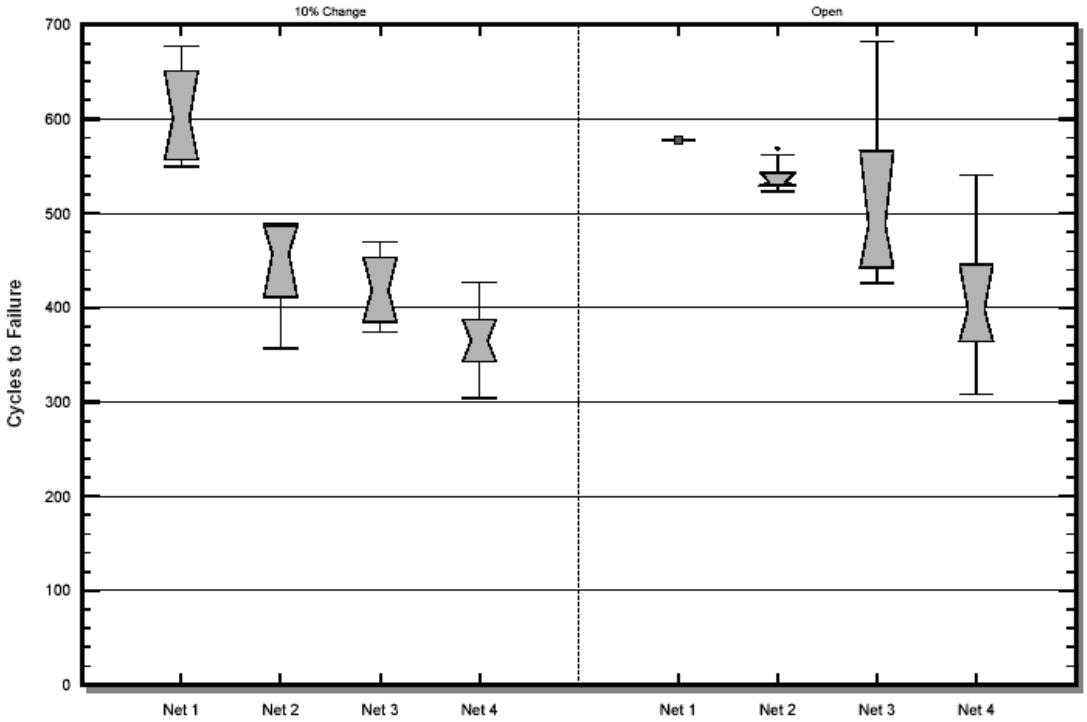
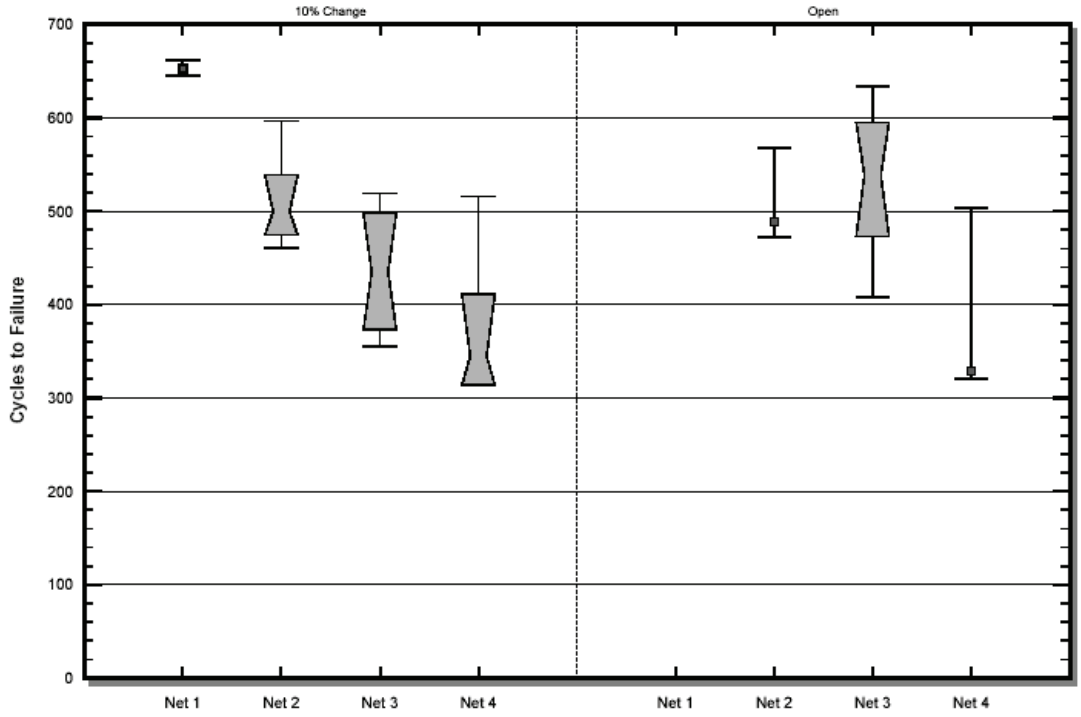
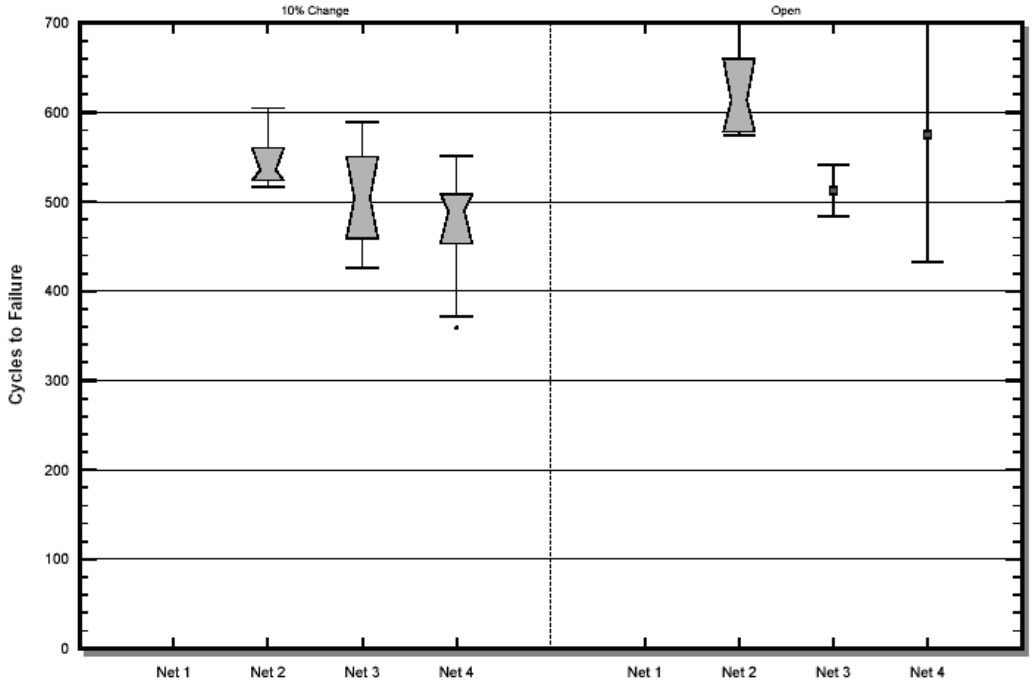


Test Condition #2 (Precondition 4X, 0 – 160 C HATS Cycling):

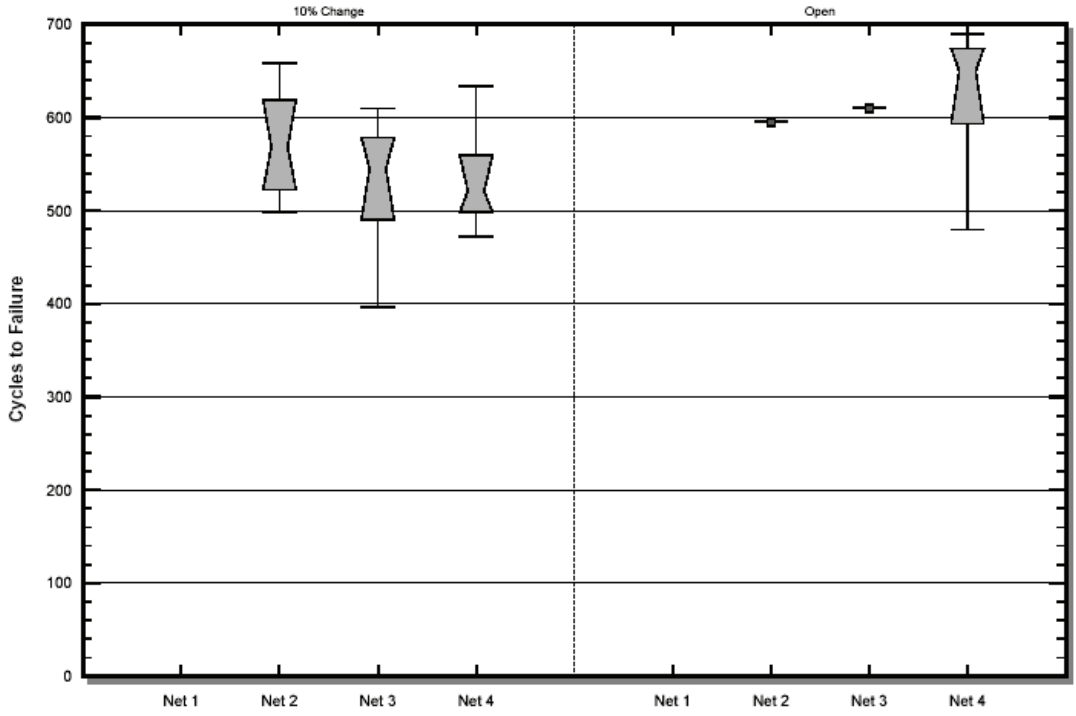
Panel #1



Panel #2

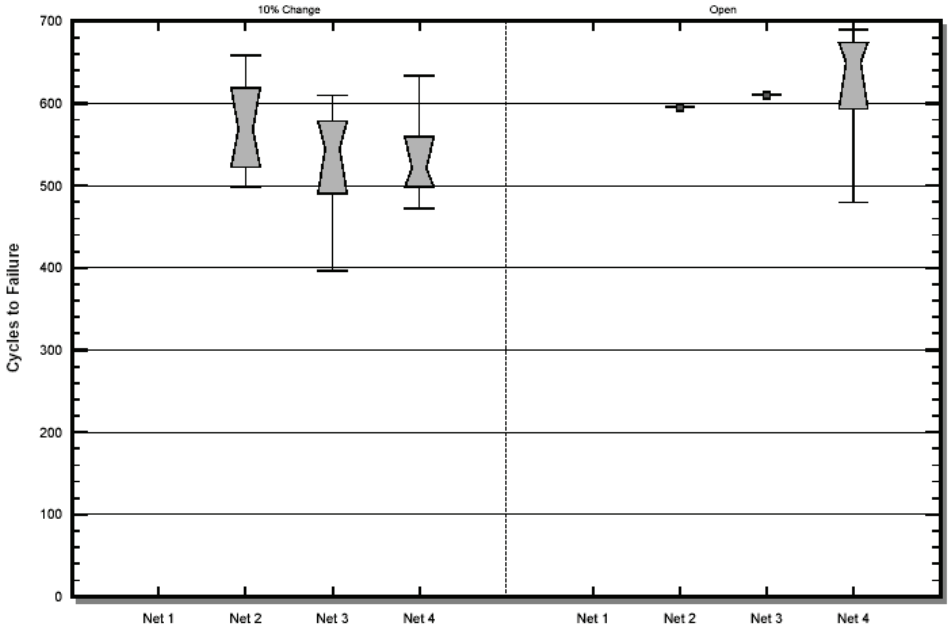

10% Change
Open
Cycles to Failure
700
600
500
400
300
200
100
0
Net 1
Net 2
Net 3
Net 4
Net 1
Net 2
Net 3
Net 4

Panel #3

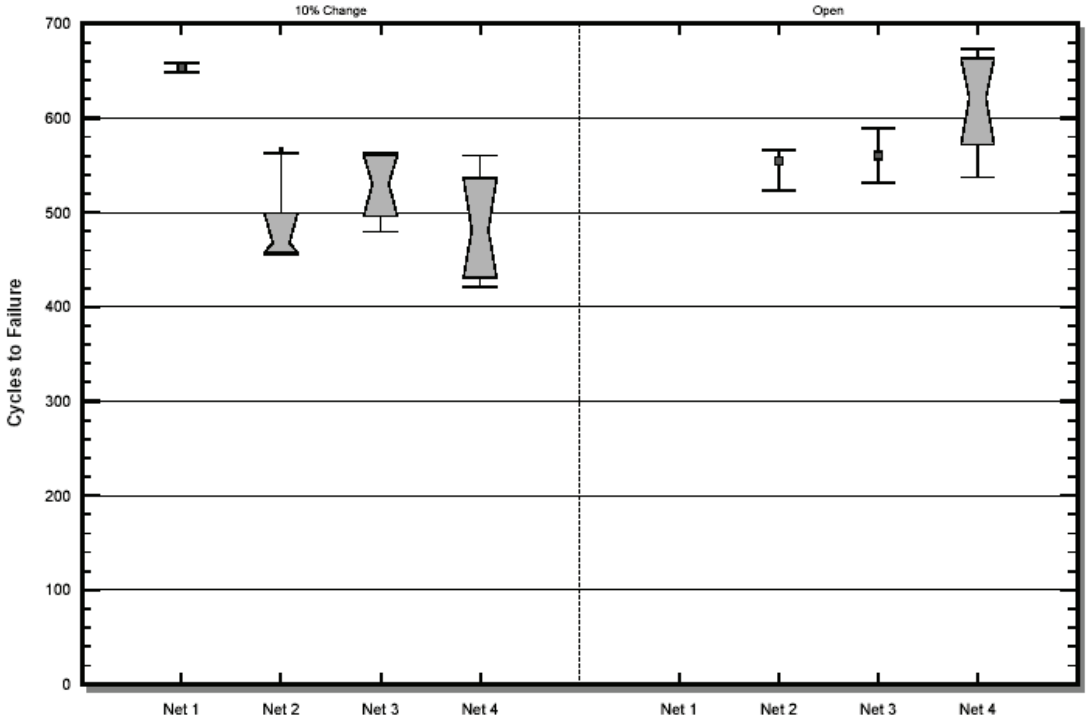

10% Change
Open
Cycles to Failure
700
600
500
400
300
200
100
0
Net 1
Net 2
Net 3
Net 4
Net 1
Net 2
Net 3
Net 4

Test Condition #3 (Precondition 0X, 0 – 160 C HATS Cycling):

Panel #1



Panel #2



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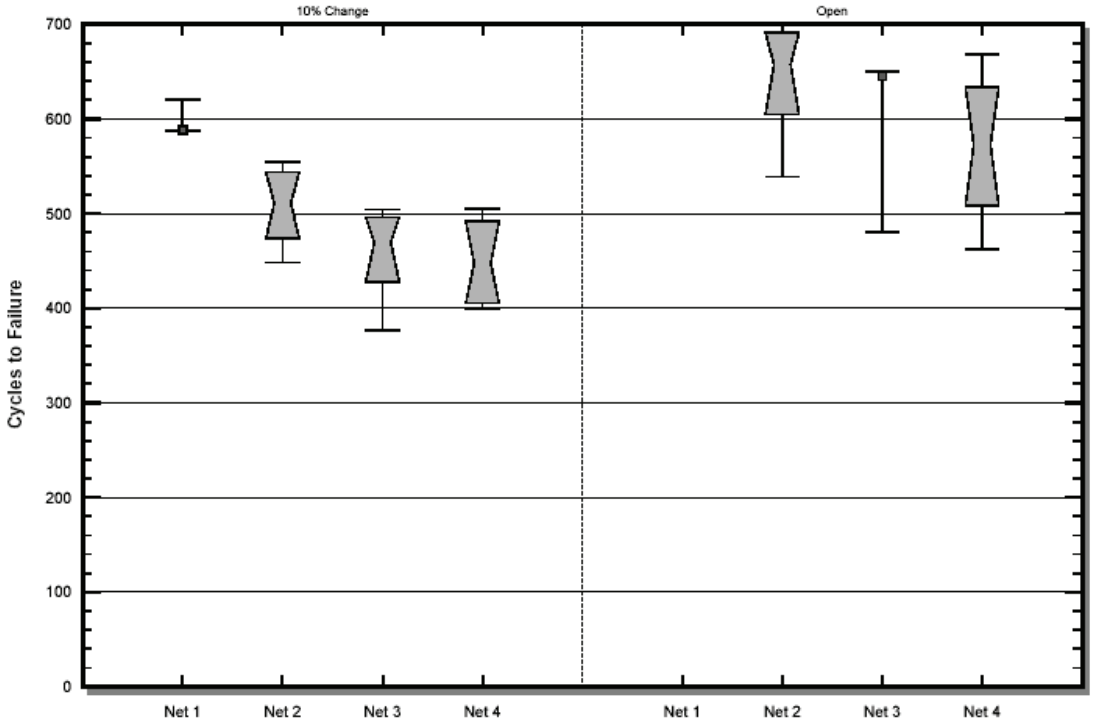
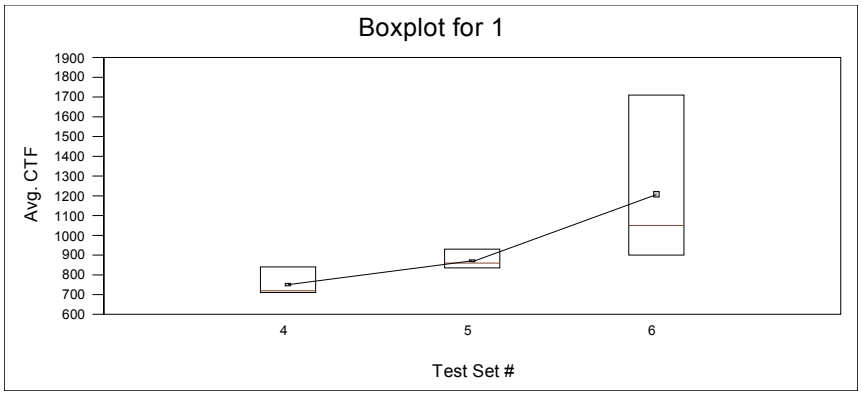
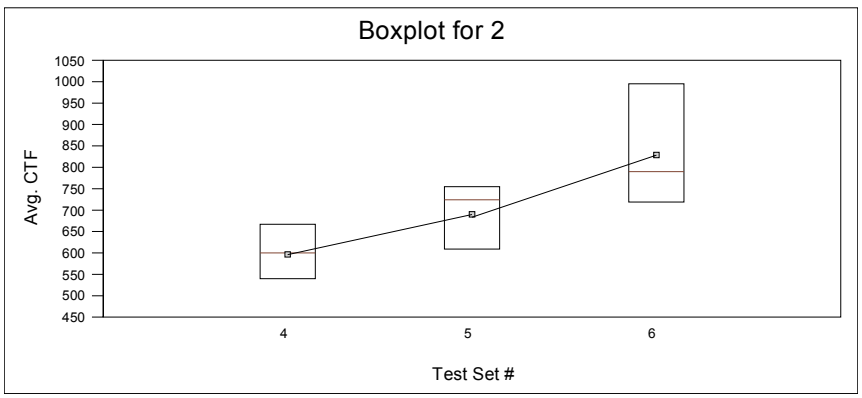
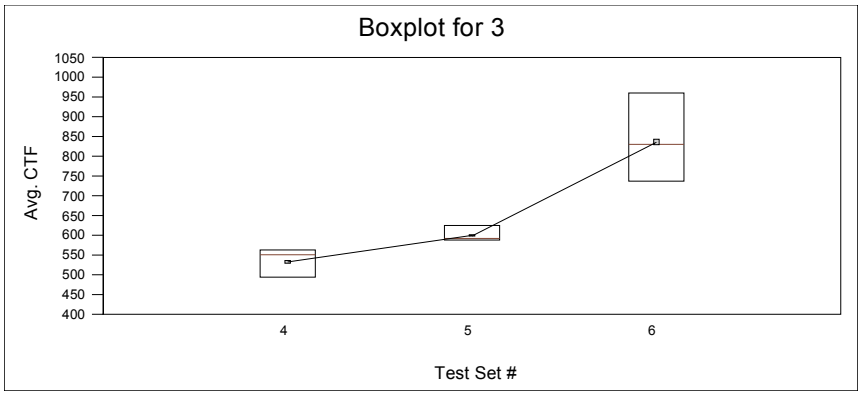


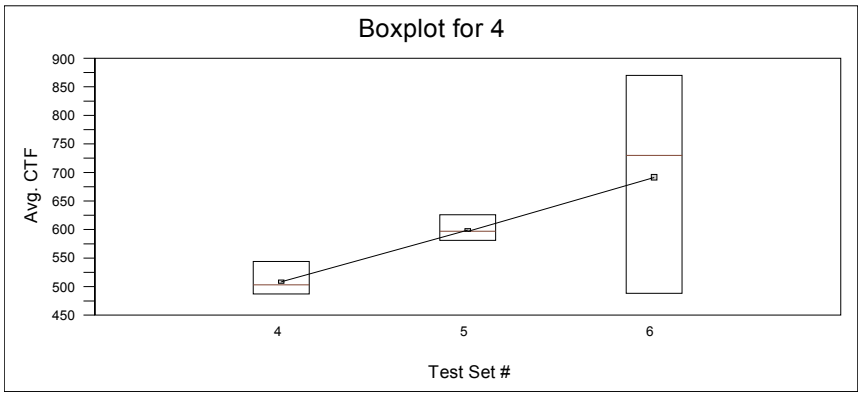
Ambient – 160 C HATS Cycling Test Results

These results show the expected gradual reduction in reliability moving from the 0X (#6) and 4X (#5) 230 C preconditioning HATS test samples to the 8X (#4) 230 C preconditioning cycles. The following four separate box plots are for each daisy chain via hole type.







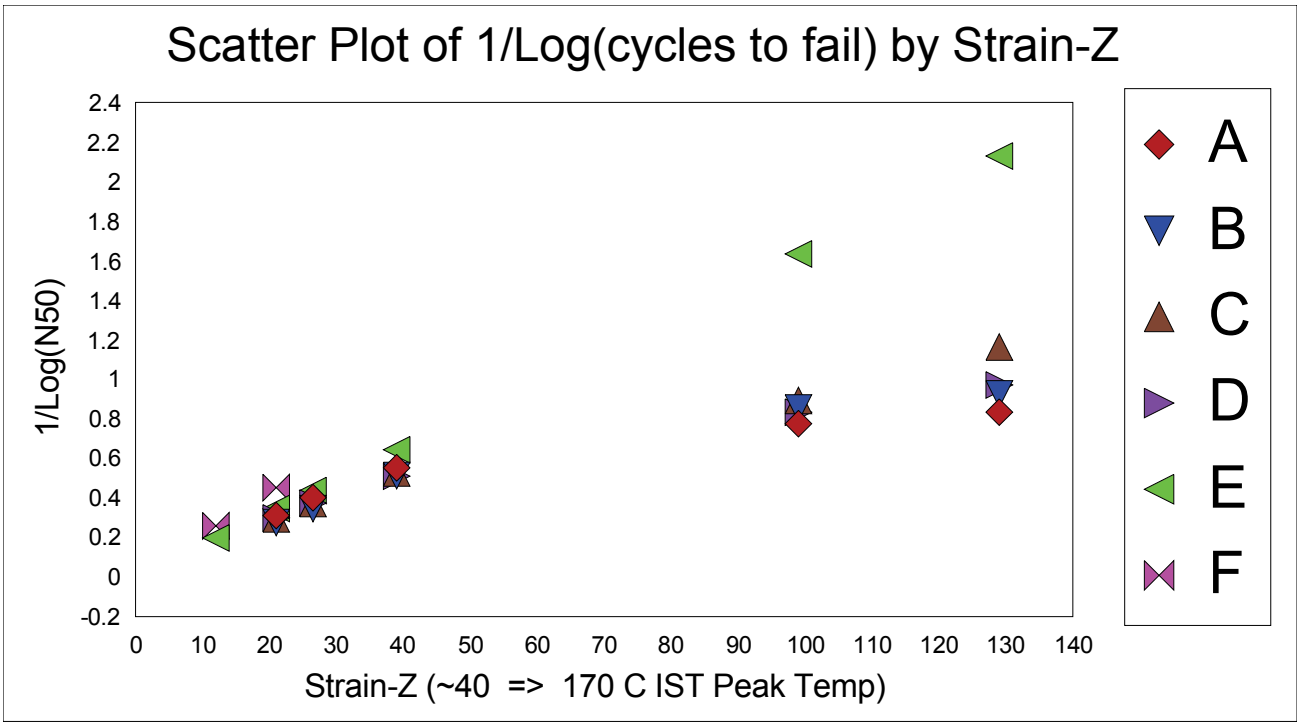


0 – 135 C HATS Cycling Test Results

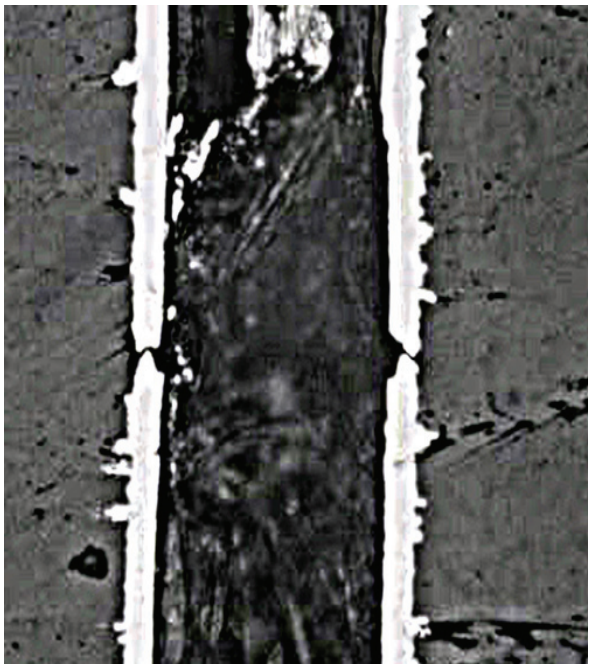
This testing is still underway at 1900 cycles with no failures to date. These results indicate that temperature cycling through the 0 and 25 C degree range has a lower magnitude effect on reliability compared with temperature cycling through the 135 C to 160 C degree range. Data is currently insufficient for any further analysis.

Initial Readings (25-160 C)	***DHS: 0.0135 inches***	***DHS: 0.0115 inches***
Daisy Chain: Layers 1 - 26	0.48 ohms	0.55 ohms
Daisy Chain: Layers 4 - 23	0.45 ohms	0.51 ohms

Long Term Reliability Analysis:
Plots of the via mechanical stress versus CTF relationship to show a good correlation with the Inverse Power Law (characteristic of copper fatigue failure) requires cycling with the high temperature well below the laminate material glass transition temperature (Tg).



Typical Via Reliability Failure:



This paper has covered how HATS testing can be used to determine the impact of simulated temperature assembly and rework thermal excursions on long term field life. In particular, the data has shown a complex relationship between higher temperature preconditioning and subsequent temperature cycling to failure (CTF). Based upon HATS test results to date, it should be possible to use the Inverse Power Law (IPL) and HATS test results to plot the via stress versus CTF relationship when cycling well below the laminate material glass transition temperature (Tg) and extrapolate to long term field life.