Electrodeposited Nanocrystalline Copper for Printed Wiring Board Applications

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Abstract
Nanocrystalline and ultra-fine grain copper can potentially offer increased reliability and functionality of printed wiring boards due to expected enhancements in strength and achievable wiring density by grain size reduction. In this research in-house synthesized nanocrystalline and ultra-fine grain-size copper foils produced by pulsed electrodeposition were compared with commercially available electronic grade polycrystalline electrodeposited (EG-ED) and cold rolled annealed (EG-CRA) copper foil. The microstructures of all materials were characterized by transmission electron microscopy (TEM). Nano-indentation and the four-point probe technique were used to evaluate their hardness and electrical resistivity, respectively. It is shown that grain size reduction results in significant increases in hardness at a moderate loss in conductivity.

Introduction
The manufacture of printed wiring boards (PWB) frequently involves the use of copper foil as the conductor for signal and current transport. Driven by more demanding customer needs, electronic devices today are much smaller in size, faster in processing and higher in capabilities. These improvements come from the advances of improved integrating circuits (ICs) and interconnect density. Components or ICs today are put closer together with decreasing packaging size. While the continuing trends in device miniaturization create increasing challenges to all electronic industries, the PWB manufacturers take the hardest hit because the performance capabilities and miniaturization of the integrated circuit devices are improving at a much faster rate than the PWB technology required to support them. The main method of device miniaturization is to increase the PWB wiring density. As electronic devices become more complex, the increase in wiring density and device miniaturization are compounding the risk of PWB failures. Considering that the circuits of a PWB comprise thousands of copper traces and interconnecting vias, failure of a single trace/via can ruin its entire function.

Thermal stress is the main contributor to PWB failure. Copper traces and vias are the most vulnerable components on PWBs to damage from thermal cycling and the leading cause of failure of PWBs in service. It has already been shown that microstructure control of copper can significantly enhance the performance and reliability of the PWB. This paper deals with the design, synthesis and characterization of nanocrystalline copper that would offer better performance over the conventional copper currently used in the electronics industry.

Nanocrystalline materials are generally defined as polycrystals with grain sizes below 100nm. As grain size decreases into the 100nm regime, materials will start to exhibit unusual properties such as increased yield strength, hardness and wear resistance[1,2]. Palumbo et al. explained these property improvements on the basis of the large intercrystalline (grain boundaries and triple junctions) volume fraction at such small grain sizes[3]. Their results showed that, as grain size decreases from 1μ to 2nm, the intercrystalline volume fraction increases from 0.3% to 87.5%. In other words, as grain size decreases, the structure of the material is changed from a crystalline-dominant to an intercrystalline-dominant solid.

Design Motivation
By reducing the grain size of copper, Considerable improvements over today's conventional polycrystalline copper are expected including: i) improved reliability by increases in mechanical and ii) higher achievable wiring density.

i) Reliability improvement by grain size strengthening
In order to consider the potential improvements in the reliability of PWB, it is important to address factors related to the coefficient of thermal expansion (CTE) and how these contribute to PWB failure. CTE is the physical expansion in the PWB over a specific range of temperature. The copper inside a multi-layer PWB, whether it is in the form of via (vertically) or trace (horizontally), is stressed, placing pressure onto the copper interconnect. With increasing thermal cycling, these stresses lead to foil cracking or layer/via separation; ultimately causing failure of the electronic device. In fact, copper foil/via cracking is one of the most common failures in electronic packages[4].

Grain size reduction increases the grain boundary volume fraction of the material. This provides constraints for dislocation movement and ultimately increases the strength of the copper foil. As the strength of copper increases, the circuit is expected to become more resistant to deformation, hence increasing the reliability of the PWB.

ii) Higher wiring density

One of the main methods in increasing PWB wiring density is to reduce the copper line width. Currently, the main drawbacks of this approach are the sharp decrease in manufacturing yield and increase in manufacturing costs. As a result of the isotropic dissolution characteristics of copper during the lithographic etching process, it is expected that the achievable wiring density can be increased through grain size reduction. Figure 1 shows schematic diagrams of circuit traces produced by lithography, using grain sizes of 1 μm and 100nm, respectively. A circuit trace that is etched into nanocrystalline copper is expected to have a better spatial resolution than a trace etched into polycrystalline copper foil. Improvements in spatial resolution, through grain refinement is expected to make traces straighter and more uniform, resulting in decreased localized stress fields, and thereby increasing the reliability of the PWB.

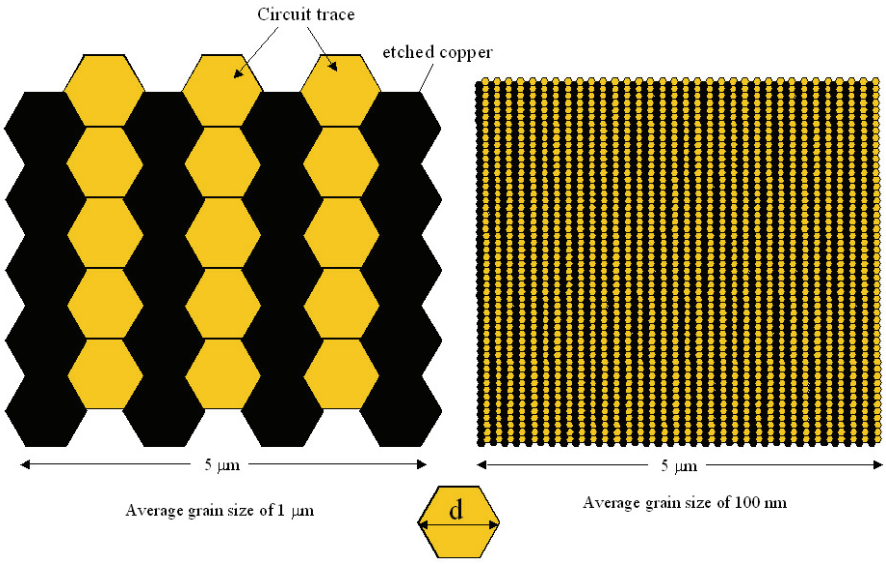


Figure 1 – Schematic representation of PWB's circuit trace after lithography and etching. Grain size reduction is expected to enhance trace resolution and achievable wiring density of the PWB.

It is important to realize that there is a physical limit in terms of minimum circuit width. Copper traces that are too narrow may limit the current-carrying ability, causing the circuit to overheat and ultimately damaging the PWB. Another potentially limiting factor is that the electrical resistivity also increases with decreasing grain size[5].

From the above discussion it is clear that a compromise must be made in selecting the grain size for PWB applications. The material should offer a significant increase in strength, yet with minimal decrease in ductility and electrical conductivity. A comparison of property changes with decreasing grain size for other nanocrystalline electrodeposit may give a good indication of what can be expected for copper. For example, for nanocrystalline nickel electrodeposits the yield strength is increased by a factor of 6 as the grain size is decreased from polycrystalline (50μm) to about 100nm. At 100nm, tensile elongation and electrical conductivity of Ni remain at about one-third and 90% of the values of the polycrystalline state[5,6].

Synthesis Method

Electrodeposition is frequently used in the manufacture of copper foils and vias. It is the synthesis method of choice because of its capability to produce fully dense, high purity copper foils. Electrodeposition is a very powerful synthesis technique with capability to produce materials with a wide range of property combinations in terms of strength, hardness, ductility, fatigue resistance and electrical resistivity[7]. Combinations of different electrolytes, plating bath additives and operating parameters yield a wide range of mechanical and physical properties for the resulting electrodeposits.

In this study, free-standing bulk copper foils with thickness of approximately 25μm were produced by pulse current electrodeposition from a bath containing copper sulphate, sulfuric acid and a proprietary grain refiner. An acid copper sulfate type plating bath was used because it is economical to prepare and operate, and is widely used in the electronic industries. The electrolyte was mechanically stirred and bath temperature of 25±2°C was maintained throughout the electrodeposition process. A 15% duty cycle was used as the pulsing parameter and samples were electrodeposited using various average current densities (from 150-550mA/cm^2) in order to achieve different grain sizes. A schematic representation of the experimental setup is shown in figure 2. Phosphorized copper rounds were used as the anode material. The cathode was made from a piece of titanium (30x30mm^2) which provides a stable electrically conductive oxide layer on the surface, which facilitates easy mechanical stripping of the copper electrodeposit after deposition.

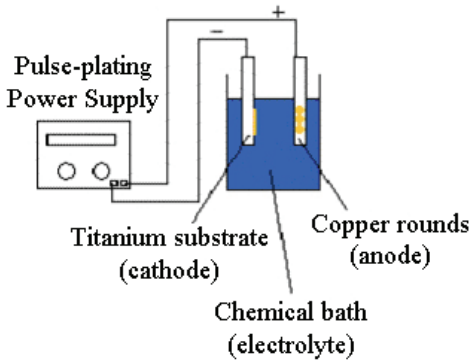


Figure 2 – Schematic representation of pulse current electrodeposition setup

The fundamental issue in nanocrystal electrodeposition is to promote grain nucleation and impede growth of existing grains. Glasstone et al., related activation energy for grain nucleation (A_k) and cathodic overpotential (Δg) by the following equation,

$$A_k \propto \left[\frac{1}{(\Delta g + [a'_{Me^+} / a_{Me^+}])^2} \right] \quad \text{---------- Eqn. 1}$$

where a'_{Me+} is the metal ion activity near the cathode (i.e. in the Nernst diffusion layer) and a_{Me+} is the metal ion activity of the bulk electrolyte[8]. This equation shows that high cathodic overpotential (Δg) will result in low activation energy for grain nucleation (A_k), ultimately promoting nucleation rate and assisting in nanocrystal electrodeposition. Pulse current electrodeposition can be utilized to allow high nucleation rates during electrolysis, which has been previously demonstrated by Erb and coworkers[9]. This is achieved by carrying out electrodeposition at high current densities (high overpotentials) for a short on-time (T_{on}). The peak current density (I_p) and on-time (T_{on}) determine the reduction rate of a metallic species during a pulse. However, since high nucleation rate strongly decreases the ion concentration near the cathode, an off-time (T_{off}) is used to allow ions to diffuse back into the ion depleted layer near the surface of the cathode.

A proprietary grain refiner was added to the electrolyte to further impede grain growth during electrodeposition. The organic grain refiner breaks down into polar molecules in the electrolyte. The refining power is primarily attributed to the adsorption of these polar molecules onto the electrode surface during electrodeposition.

Electrodeposited nanocrystalline (Lab-nc) and ultra-fine grain (Lab-UFG) copper foils were characterized by transmission electron microscopy (TEM) to determine average grain size and grain size distributions. Thin foils (3mm in dia.) for TEM analysis were prepared using electrolytic jet polishing in an electrolyte containing 30% phosphoric acid and 70% distilled water at room temperature and a voltage of 15VDC. In-house synthesized ultra-fine grain and nanocrystalline copper will also be compared to commercially available electronic grade electrodeposited (EG-ED) and cold-rolled annealed (EG-CRA) copper foils in terms of microstructure, mechanical and electrical properties.

Results and discussions

Copper foils with grain sizes ranging from 35 to 2000nm were produced by deposition carried out at current densities between 100-500mA/cm^2. Table 1 shows the In-house produced electrodeposited copper samples considered in this study[10].

Table 1 – Examples of In-house produced electrodeposited copper samples

Grain size (d), mm	Standard deviation (δ), mm
1048	1465
209	239
85	67
73	60
41	43

Microstructural Characterization

Figure 3 shows the TEM bright field and dark field electron micrographs for representative nanocrystalline (41nm average grain size) and ultra-fine grain (209nm average grain size) copper samples, respectively. To quantify the differences in grain structure between these samples, the average grain size (AGS) and grain size distributions (GSD) of the two samples are shown in figure 4. The two quantitative structure descriptors (AGS and GSD) were determined by first manually outlining more than 300 grains from dark field electron micrographs. Twin boundaries were ignored in grain size measurements, i.e. a grain that contained many twin boundaries was considered as only one grain. Using analytical software, Image J (version 1.31u, source code written by Wayne Rasband, National Institutes of Health, USA), and assuming that each grain is circular, the area and the diameter of each grain (d) were then determined. The GSD for both samples presented in Fig. 4 are lognormal distributions, similar to what has been previously reported for other electrodeposited nanocrystalline and ultra-fine grain metals[11,12,13]. Another observation that can be made from the grain size distributions is that ultrafine grain copper has a larger standard deviation than the nanocrystalline copper. As the grain size distribution narrows, properties of electrodeposited materials become more isotropic[14].

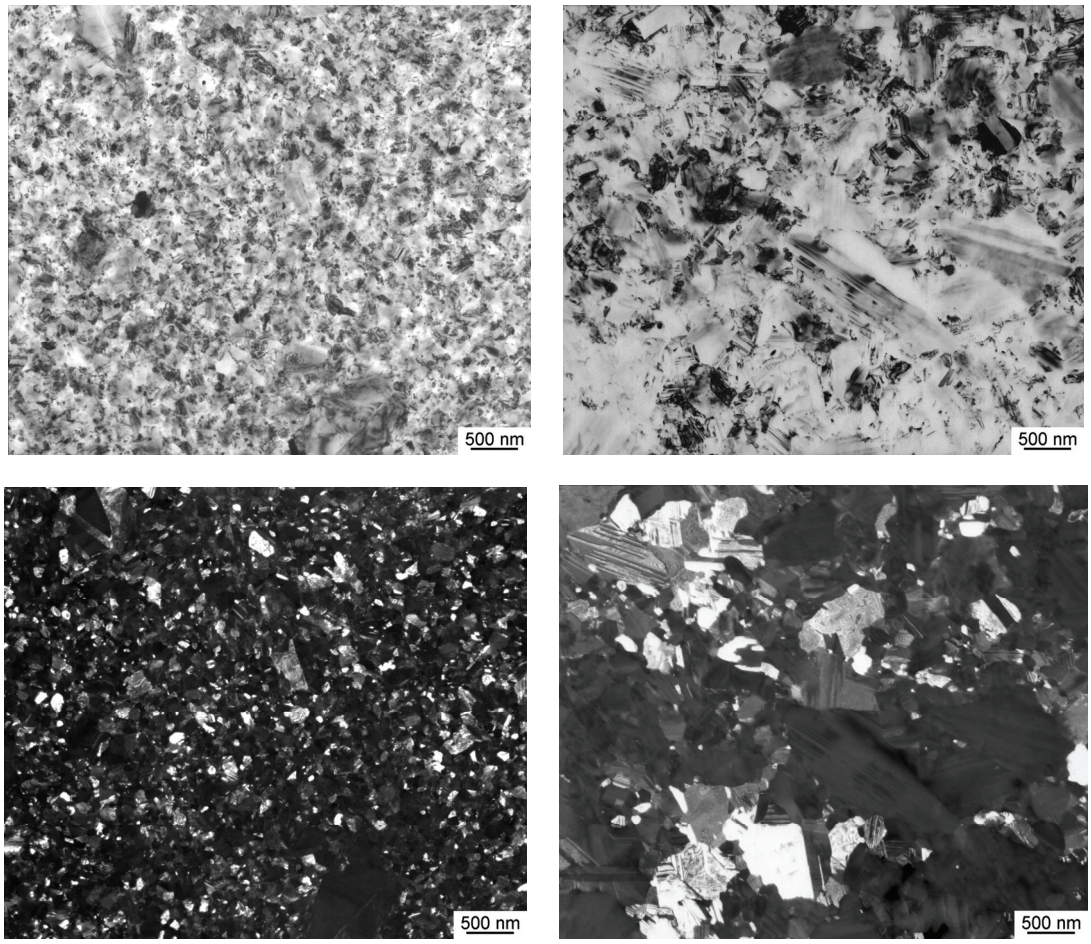


Figure 3 – TEM bright field (top) and dark field (bottom) micrographs showing typical microstructures of electrodeposited nanocrystalline (left) and ultra-fine grain (right) copper.

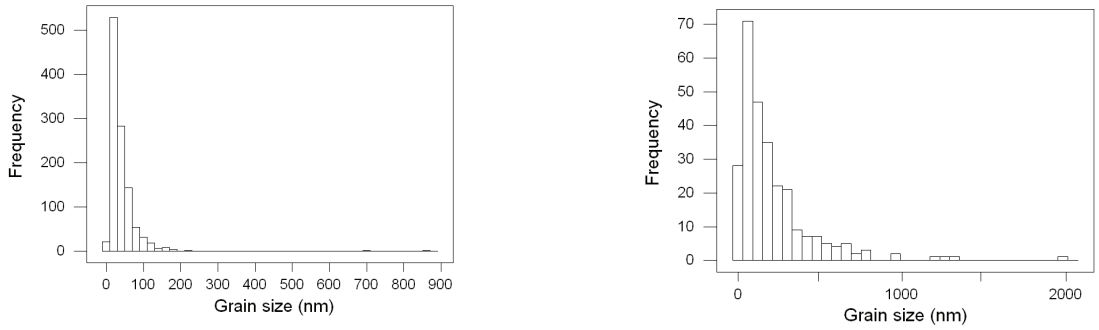
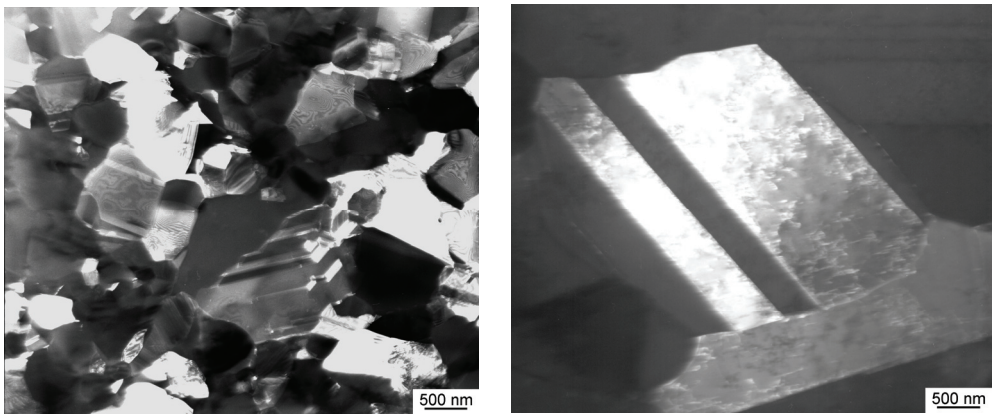


Figure 4 – Grain size distribution (GSD) for the nanocrystalline (left) and ultra-fine grain (right) copper shown in figure 3.

In comparison, figure 5 shows TEM dark field electron micrographs, together with data for average grain size (d) and its standard deviation (δ) for EG-ED (a) and EG-CRA (b) copper, respectively. Lab-nc copper samples have much smaller grain size; about 4 to 40 times smaller compared to EG-ED and EG-CRA copper foils (Table 1). Another observation is Lab-nc copper also has a higher density of twin boundaries per unit area compared to either EG-ED and EG-CRA copper foils. Twin boundaries are special grain boundary with much lower interfacial energy compared to normal grain boundaries[15]. Because of the low interfacial energy, twin boundaries are relatively chemically inactive and have a lower electrical resistivity compared to other grain boundaries[7]. Twin boundaries also have a high misorientation angle between the two neighboring crystals. Because of this high misorientation, twin boundaries are capable of impeding dislocation movement, providing the material with increased strength[16].



Commercially available EG-ED copper
d = 325nm, δ = 261.2 nm

Commercially available EG-CRA copper
d = 3238nm, δ = 1688 nm

Figure 5 – TEM DF micrographs for EG-ED (a) and EG-CRA (b) copper.

Mechanical Properties

The hardness of the in-house fabricated, as well as EG-ED and EG-CRA copper foils were determined by using a Shimadzu DHU-201S dynamic ultra-microhardness tester equipped with a 115° triangular pyramid (Berkovich) indentor. Nano-indentation measures the dynamic hardness of the material by measuring its indentation depth instead of the diagonal lengths of the indentation as in conventional hardness.

Dynamic hardness values for all samples as a function of grain size are shown in figure 6. Lab-nc copper samples exhibit significantly higher hardness than the polycrystalline EG-CRA copper. A nearly six-fold increase in hardness is observed as the grain size is reduced from 3.3μm to 41nm. EG-CRA copper has a hardness value of 43 kg/mm^2, while the hardness for Lab-nc copper with an average grain size of 41nm reached approximately 225 kg/mm^2. Nanocrystalline copper with grain size of 41 nm, showed an approximately 70% increase in hardness compared to today's smallest grained EG-ED copper foil. Similar observations of increasing hardness with decreasing grain size have been reported elsewhere by Nieh[17], Wang[18] and El-Sherik[19] for other nanocrystalline metals and alloys. This behavior can be explained by the classical Hall-Petch relationship[20,21].

Electrical Properties

Room temperature electrical resistivity measurements were performed using the four-point probe technique. Figure 7 shows electrical resistivity for all copper samples (Table 2 + EG-ED and EG-CRA) as a function of grain size. Polycrystalline EG-CRA copper has the lowest electrical resistivity, a value of 1.77 μΩ·cm. Lab-nc40, Lab-UFG and EG-ED copper show increases of respectively 32%, 10% and 7% in electrical resistivity compared to EG-CRA copper. The increase in electrical resistivity is due to the decrease in grain size. The increase in the grain boundary volume fraction increases the density of scattering centers for electrons, decreases the mean free path for electrons and, ultimately, increases the electrical resistivity of copper.

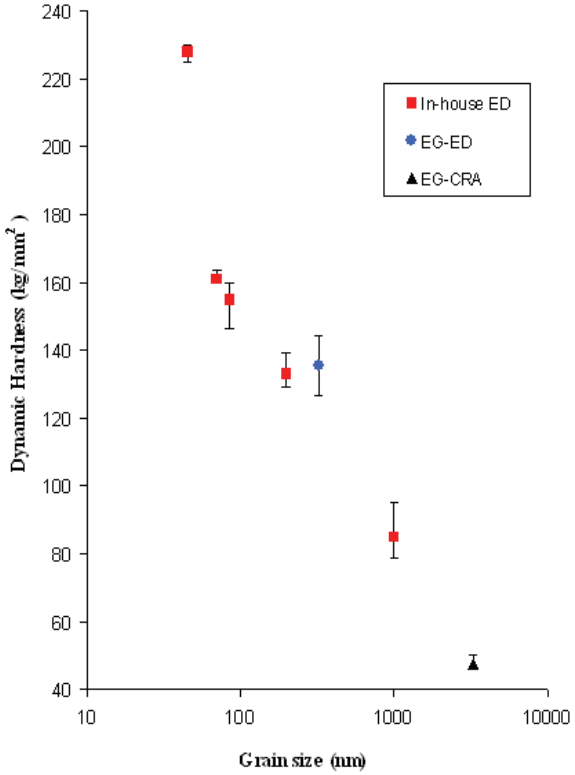


Figure 6

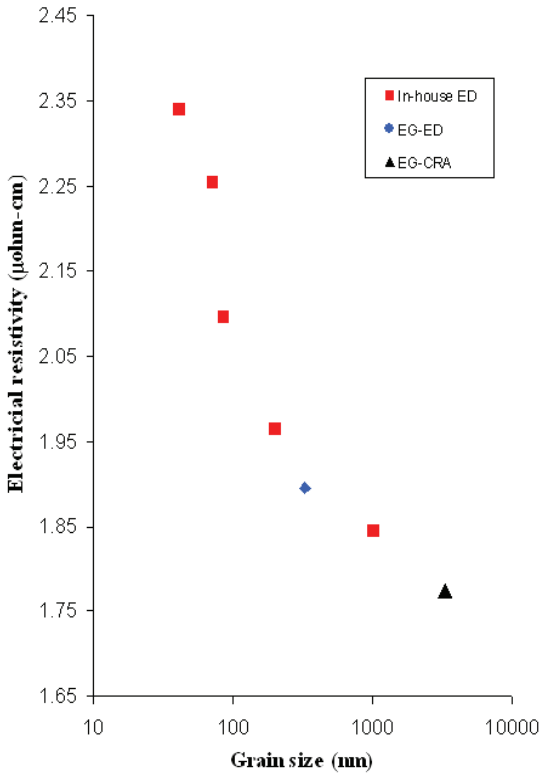


Figure 7

Figure 6 and 7 – Dynamic hardness and electrical resistivity results for in-house and Commercially available copper foil as function of grain size.

Conclusions

It has been demonstrated that nanocrystalline and ultra-fine grain copper foils can be produced by pulsed current electrodeposition. Nanocrystalline copper with an average grain size of 40nm showed an increase of over 500% in hardness compared to conventional polycrystalline copper with an average grain of about 3.3μm. However, this grain size decrease also resulted in an increase of electricity resistivity by about 30%. The results of this study are of considerable importance in the microstructural design for ultrafine grained and nanocrystalline copper which require a compromise between mechanical property enhancements and loss in electrical conductivity considerations.

Acknowledgements

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