The Effect of Plating Cell Configuration on the Quality of Copper Deposit for Printed Circuit Boards

H. Garich, J. Sun, L. Gebhart, M. Inman, E.J. Taylor,
Faraday Technology, Inc.
Clayton, Ohio

T. Dalrymple, N. Emami,
AFRL/SNDR
Wright-Patterson Air Force Base, Ohio

R. Smith, T. Berg, R. Thompson and W. Richards
Naval Surface Warfare Center – Crane
Crane, Indiana

Abstract
This paper addresses the effect of pulse plating of electronic interconnects for advanced electronic modules. This paper builds on earlier work by correlating plating cell and tank design issues and tank characterization studies with standard mechanical and reliability tests. The current work evaluates the resulting copper deposits in terms of throwing power, mechanical and reliability tests and compares the results to a current state-of-the-art process. The present work relies on electrical mediation for a highly controlled electrodeposition process that results in a very uniform and reproducible deposit; selection of the electric mediation parameters is based on considerations of mass transfer as well as microprofiles and macroprofiles related to current distribution. Data for plating industry test panels containing PTHs of approximately 5:1, 10:1, and 15:1 aspect ratios are presented. Using a pulse waveform sequence, throwing powers of approximately 90-100% are observed at plating rates of approximately 20 ASF.

Introduction
For years, printed circuit boards (PCBs) have been the platform for electronic devices, providing the electrical interconnection between components. The continuing miniaturization of electronic devices is driving the design of PCBs interconnects in the direction of finer pitch transmission lines, smaller diameter through holes and vias, and thicker boards with higher layer counts to provide increased circuit densities.[1,2] Plated through holes (PTHs) continue to provide most of the electrical connection on multilayer boards; the current trend is for multilayer boards containing PTHs with aspect ratios of 15:1[3] and higher. As the board thickness increases and the diameter of the PTHs decreases, the reliability of the PTH becomes a major concern. One of the greatest challenge facing PCB manufacturers today is plating the required copper thickness inside the high aspect ratio PTHs without overplating the surface of the board (i.e. good throwing power). In order to maximize the electroplating of high aspect ratio PTHs, without loss of throwing power and thickness distribution, the following parameters must be carefully considered and optimized:

- Current delivery mechanism
- Cell configuration, specifically flow conditions
- Anode design
- Electrolyte chemistry

To meet the plating challenge of advanced electronic interconnects, electrically mediated (periodic or pulse reverse) plating processes have recently received considerable interest.[4,5,6,7,8] Although pulse reverse plating has been reported to improve mechanical and physical properties of the deposits, to promote leveling and throwing power, and to increase plating speed in these previous studies,[4,5,6,7,8] these studies utilize brightener and/or leveler additives in the plating bath. Since these studies have not addressed the effects of pulse plating parameters in the absence of brightener/leveler additives, optimization of the pulse plating parameters is lacking. The proposed approach instead utilizes a sophisticated cell design coupled with optimized pulse reverse plating in the absence of brightener and leveler additives.

Electrically mediated electroplating causes concentration fluctuations near the electrode surface and reduces the effective Nernst diffusion layer thickness. Consequently, very high limiting current densities may be achieved with electrically mediated electroplating as compared to direct current (DC) electroplating. The Nernst-Fick equation[9] describes the limiting current, as a function of cathode diffusion layer thickness □□.

$$i_L = nFDC_b/\square_{\square} \qquad (1)$$

where D is the diffusion coefficient, C_b is the concentration of copper ions in the bulk solution, and $\square_{\square}$ is the Nernst diffusion layer thickness defined as shown in Figure 1.

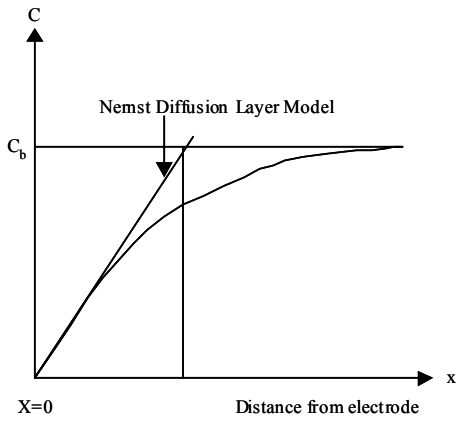

Figure 1: Variation of the Concentration of the Reactant During Non-Steady-State Electrolysis.

The model assumes that the concentration of metal ions has a bulk concentration C_b up to a distance $\square_{\square}$ from the electrode surface and then falls off linearly to $C_{x=0}$ at the electrode surface. At the distance $x \geq \square_{\square}$ mixing is uniform and efficient. Metal ions must diffuse through this layer $\square_{\square}$ to reach the electrode surface. In addition, at the limiting current density the metal ions are reduced as soon as they reach the electrode. At these conditions, the deposition rate is controlled by the rate of mass transport to the electrode. The limiting current density is of great importance to the copper deposition process, since the type and quality of copper deposits depends upon the deposition current and the limiting current for a given plating cell configuration[1]. Therefore, successful high copper deposition rate requires uniform and high solution agitation to reduce diffusion layer thickness and increase the magnitude of the limiting current.

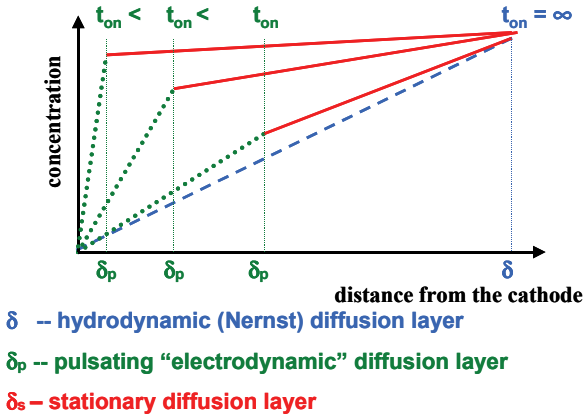

Figure 2: Schematic Representation of the Duplex Diffusion Layer.

In the electrically mediated approach, the Nernst diffusion layer is derived from the influence of a pulsating current on the hydrodynamic diffusion layer. As shown in Figure 2, during pulse plating a "duplex diffusion layer" develops. The duplex diffusion layer consists of a stationary layer and an inner pulsating layer. By assuming linear concentration gradients, Ibl[10,11] derived the following relationship between the pulsating diffusion layer and the on-time of the pulse

$$\delta_p \approx (2Dt_{on}) \qquad (2)$$

where D is the diffusion coefficient, t_{on} is the on-time of the pulse and δ_p is the pulsating diffusion layer. More recently, using a similar duplex diffusion layer approach the same relationship was derived for "pulse-with-reverse" plating[12] that affects both the mass and charge transfer in copper plating process. Under the duplex diffusion layer model, the boundary layer during pulse plating may be reduced relative to the boundary layer attained under DC plating. Consequently, instantaneous current densities during pulse plating can be much higher than those under DC plating.

Because of the coupling of the hydrodynamic layer and the "electrodynamic" layer, both the pulse waveform and cell hydrodynamic conditions are significant factors, which must be optimized in the copper plating process for PCBs. In pulse reverse copper plating, either with or without additives, the plating rate and throwing power are coupled to the waveform parameters, the feature dimensions, and solution flow conditions at the board surface and in the through holes. Some of the more recent research programs have suggested the use of solution agitation techniques,[4, 13,14,15] such as eductor flow. The direction of eductor flow relative to the plating tank walls and panel as well as solution velocity are likely to play an important role on the process.

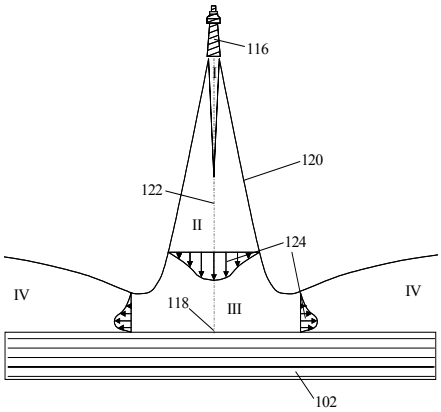

Figure 3: Velocity Profile of Eductor Placed Perpendicular to PCB Surface.[17,18,19]

We have developed a sophisticated cell design[16] that has undergone rigorous testing and optimization and has a host of unique features that allow control of the hydrodynamic conditions encountered during electroplating. The uniform flow distribution can be attributed to the following features: variable high velocity eductor-induced agitation, shaped guides, oscillation and vibration of the PCB, an anode chamber that includes shielding and baffles, and variable anode to cathode spacing. Typically, hydrodynamic control within a plating tank is achieved with air sparging or use of eductors, neither of which give absolute control of flow during plating. Use of eductors, alone or in conjunction with air sparging, in plating cell configurations has become common practice, although the placement and spacing of the eductors is often poorly utilized, resulting in variations in the solution flow velocity across the PCB surface and non-uniform copper deposit thickness. For example, eductors placed perpendicular to the PCB surface result in impinging solution flow, leading to variations in solution flow and copper thickness distribution. This phenomenon is represented schematically in Figure 3.[17,18,19] As seen in Figure 3, the velocity profile differs from the eductor nozzle to the PCB surface. Eductors placed below or to the side of the PCB surface result in a glancing effect from which the solution flow varies radially outward from the impingement point and also results in non-uniform solution flow and non-uniform deposition thickness, shown schematically in Figure 4.[20,21,22]

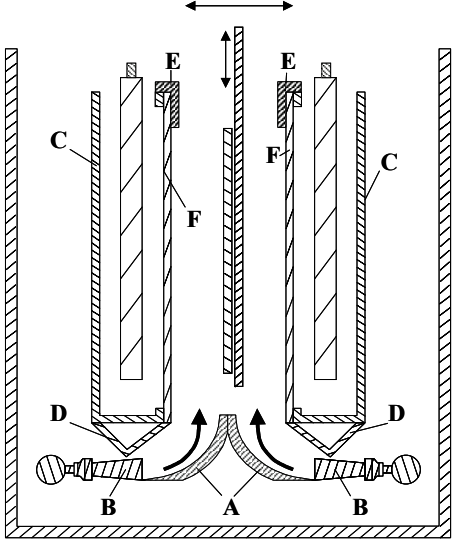

Figure 4: Velocity Profile of Eductor Placed at an Angle to the PCB Surface.[20,21,22]

In contrast, the cell utilized in the current work pairs eductors with a dampening member, which results in uniform laminar flow parallel to the PCB surface. A schematic of the cell is given in Figure 5, where the dampening member is designated as A and the eductors as B. The dampening member supresses any variations in solution flow, thus effectively decreasing any glancing effect. The cell contains three eductors on each side of the plating cell, which are located directly beneath the anode chambers. The anode chambers (C) are kept isolated from this flow by baffles located at the bottom of each anode chamber (D). The anode chambers are also equip with non-conductive shielding (E), preventing edge effects, and contributing to the uniformity of the copper deposit obtained by plating in this novel cell. The anode baskets hang in an anode chamber encased in a porous polymeric cloth (F) that spreads the current distribution such that the anode chamber behaves as a virtual anode, also contributing to high uniformity of the deposit. The cell is capable of accommodating varying anode to cathode spacing, however optimization studies have determined 210-220 mm to be the optimum spacing.

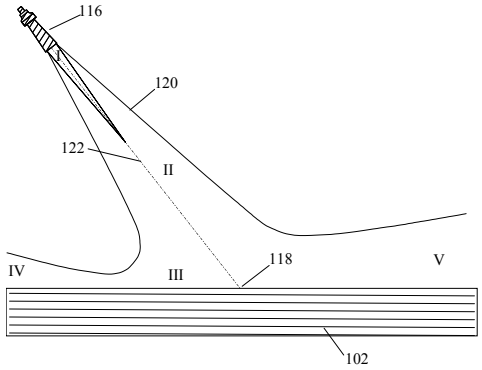

Figure 5: Schematic of Side View of Plating Cell.

Experimental

The aim of the current research is to explore the coupling of sophisticated cell geometry and optimized electrically mediated waveform parameters for the plating of high aspect ratio PTHs. Additionally, the present work will function to quantify the properties of the electrically mediated deposit in terms of tensile strength and reliability without the use of difficult to control organic additives.

As shown in Figure 6, the plating tank, which holds 1700 liters of bath electrolyte, is capable of accommodating one PCB, 45.72 cm by 60.96 cm (18x24 inch). Two 300 L/min pumps circulate electrolyte through six 19-mm eductors (three on each side) located horizontally under the anode chamber. Vibration of the PCB is accomplished by two horizontal eccentric rotating weights powered by variable speed motors and mounted to each end of the load bar. The frequency of vibration has a range of 0 to 2170 cycles per minute. Lateral oscillation is produced by a positive drive from a variable speed motor-reducer with crank arm and linkage. The frequency of oscillation can shift from 6 to 63 cycles per minute with a stroke of 25 mm. Experiments were conducted using a Power-Pulse pe 86D-6-212-480 rectifier supplied by Plating Electronics GmbH. Each plating experiment was conducted for 80 minutes.

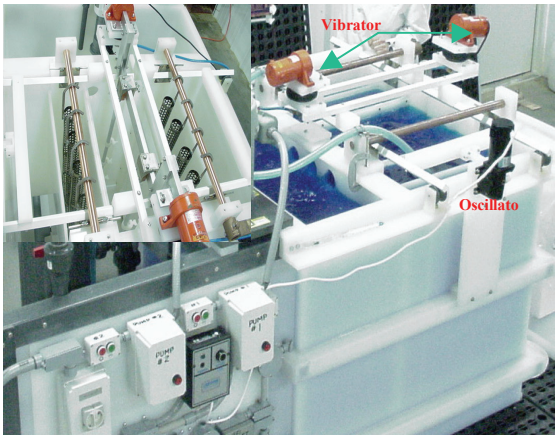

Figure 6: Plating Cell.

An acid copper sulfate electolyte containing 95-100 g/L $CuSO_4 \bullet 5H_2O$, 210-215 g/L of H_2SO_4, 60-70 ppm Cl^-, and 350 ppm polyethylene glycol (PEG) was used as the copper electroplating bath for all experiments. The chloride/PEG system acts as a suppressor and is not difficult to control.[23] The plating bath does not contain difficult to monitor/control additives such as brighteners and/or levelers and hence we consider the bath to be "additive-free." The plating bath temperature was maintained in the range of 22 to 25 ^oC.

Currently the tensile/elongation mechanical tests and IST reliability tests are being conducted; the results will be given during the 2006 IPC APEX/Expo presentation. The tensile/elongation tests are conducted in accordance to IPC –TM-650 2.4.18.1, Tensile Strength and Elongation, In-House Plating. The IST (interconnect stress test) reliability tests are conducted in accordance with IPC-TM-650 2.6.26, DC Current Induced Thermal Cycling Test. The results of these tests will be compared to "baseline" data. The baseline data is being generated with a "state-of-the-art" plating cell that utilizes pulse reverse plating with additives. The tank has been previously characterized.[24] The covariance values for cell characterization in the "state-of-the-art" cell versus the cell featured in the present work are 19.1% and 5.4% respectively. Therefore, the current cell plated a much more uniform deposit, which would lead to more uniform plating of high aspect ratio PTHs as compared to the "state-of-the-art" cell.

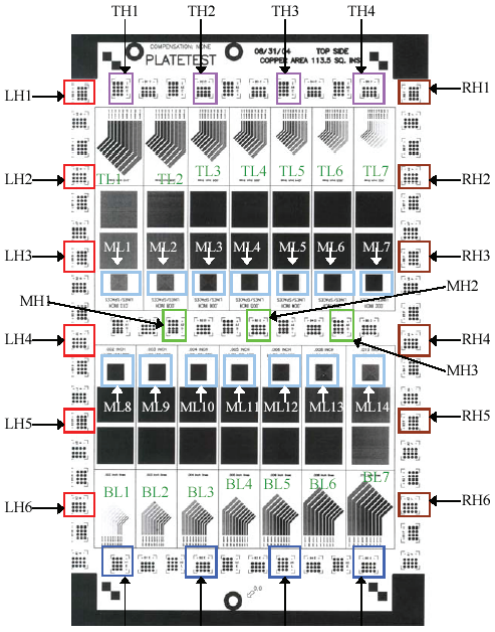

Figure 7: Schematic of Test Vehicle One.

Two test vehicles were used in the present work. The substrate for both boards is a double-sided FR4 epoxy, patterned on both sides with 50.8□m (2 mils) photoresist and 1/2 oz electroless copper seed layer. The first board, test vehicle one, was composed of line widths varying from 50.8□m to 254 □m (2 to 10 mils) and PTHs with diameters varying from 330.2 to 1600.2 □m (13 to 63 mils with approximate aspect ratios of 1:1 to 5:1). The second board, test vehicle two, contained only PTHs with diameters ranging from 262.5 □m to 692.8 □m (10 to 30 mils with aspect ratios of 5:1, 10:1 and 15:1). Figures 7 and 8 illustrate the layout of the test vehicle boards. Cross-section analysis was performed using a Nikon MM40 Measurescope with a DMX 1200F Imaging System.

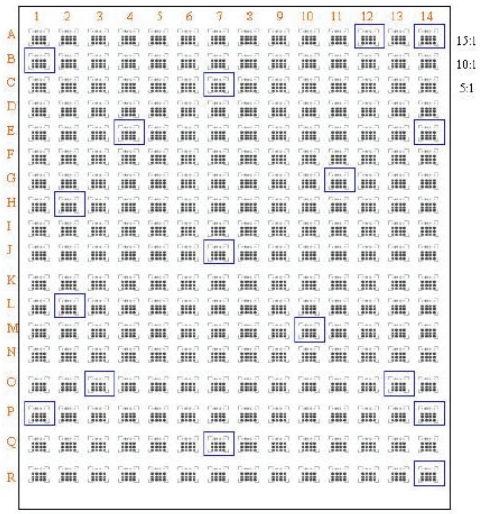

Figure 8: Schematic of Test Vehicle Two.

Results and Discussion

Previous work[25] focused on optimization of the following plating cell configuration parameters: eductor flow rate, oscillation speed, vibration frequency, and anode to cathode spacing. The results of these initial studies were obtained by plating stainless steel panels under DC conditions and then measuring the copper thickness uniformity of the obtained copper foil. This work achieved a covariance uniformity of approximately 5.4% across a 45.72 cm by 60.96 cm (18x24 inch) workpiece. The conclusion of this earlier work is that a uniform hydrodynamic boundary layer is required for uniform plating across a panel.

The current work focused on the plating of varying feature sizes with our novel cell using electrically mediated current and an "additive-free" electrolyte. An effective tank design is required for all plating processes, including those employing brighteners and levelers. This work explores the benefits of electrically mediated plating without the difficult to control additives. Sequences of waveforms were selected based on the test panel pattern heterogeneity and the electrodynamic boundary layer conditions. Extensive cross-section analysis was conducted on both test vehicles to determine the distribution of copper plating. Photographs of the cross-sectioned samples are provided.

Test Vehicle One

Photographs for coupons taken from Test Vehicle One are provided in Figures 9 through 16.

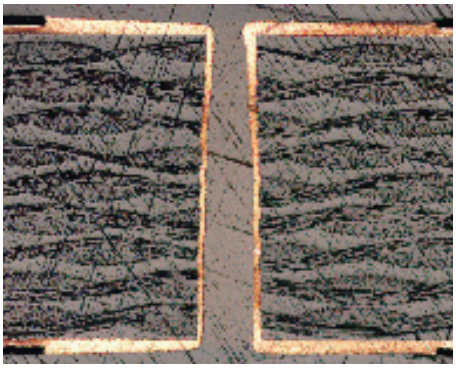

Figure 9: A 330.2 µm Diameter PTH with Aspect Ratio of 4.6:1.

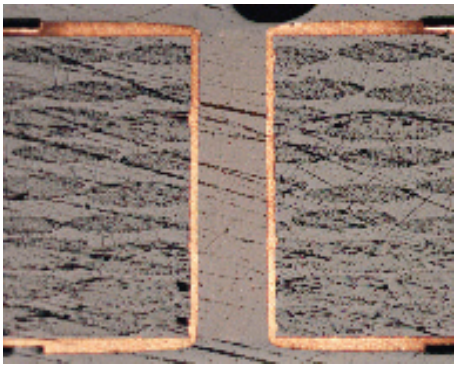

Figure 10: A 609.6 µm Diameter PTH with Aspect Ratio of 2.5:1.

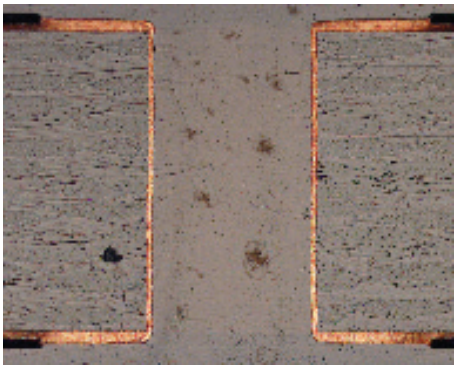

Figure 11: 889 µm Diameter PTH with Aspect Ratio of 1.7:1.

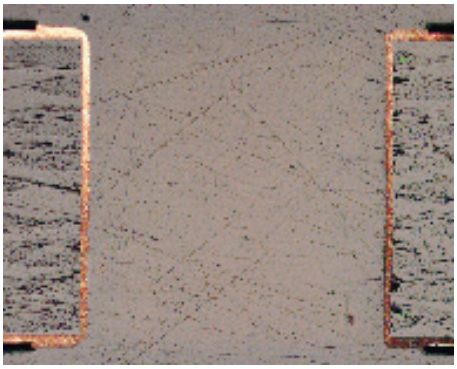

Figure 12: 1600.2 µm Diameter PTH with Aspect Ratio of 0.95:1.

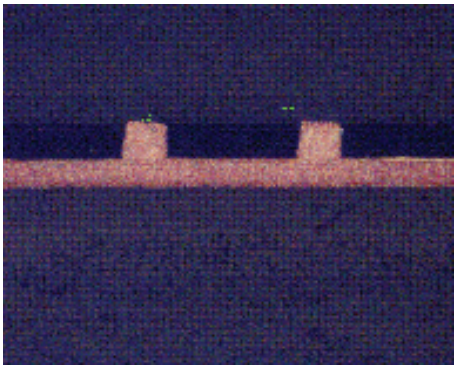

Figure 13: 50.8 µm Lines with 177.8 µm Spaces.

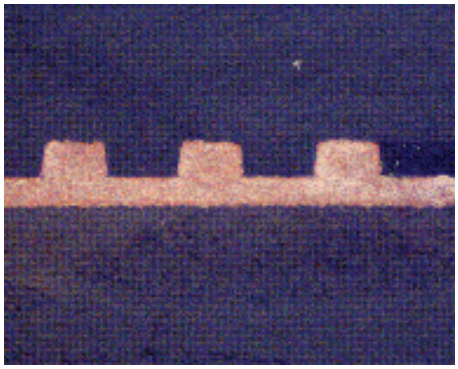

Figure 14: 76.2 µm Lines with 101.6 µm Spaces.

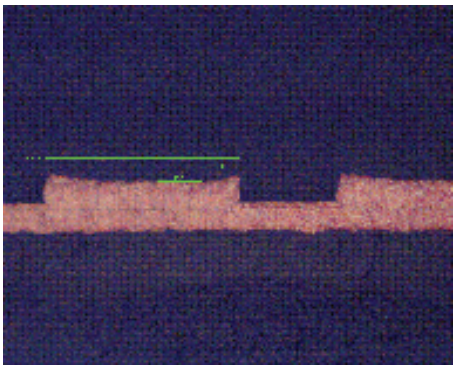

Figure 16: 254 µm Lines with 127 µm Spaces.

As illustrated in the above photographs, varying feature sizes may be uniformly plated on the same board using novel cell geometry and electrically mediated current, even in the absence of organic brighteners and levelers. Throwing power calculations were performed and are included as Table 1. As shown in Table 1, throwing power is very high, often exceeding 100%. In addition, the fine-tuned electrically mediated current parameters allow plating of the PTHs without a dog-boning

Table 1: Throwing Power Calculations for Test Vehicle One.

Diameter (µm)	Aspect Ratio	Average Wall Thickness (µm)	Average Top Thickness (µm)	Throwing Power %
330.2	4.6:1	31.51	33.34	94.5
609.6	2.5:1	37.93	37.47	101.2
889.0	1.7:1	27.84	36.10	77.1
1600.2	0.95:1	32.27	27.53	117.2

effect, commonly encountered with high aspect ratio PTHs.

Test Vehicle Two

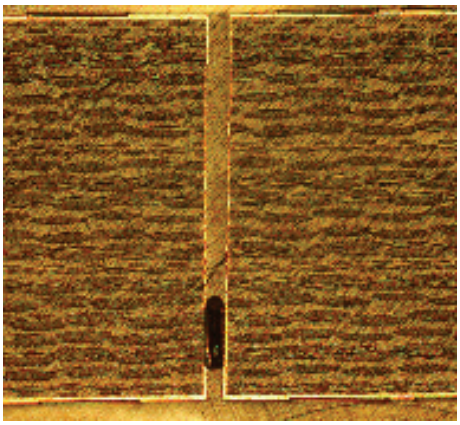

Figure 17: 262.5 µm Diameter PTH with Aspect Ratio of 15:1.

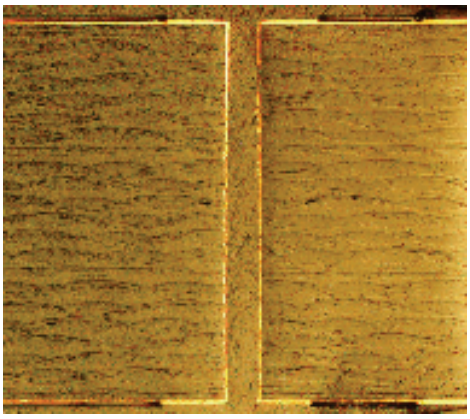

Figure 18: 358.4 µm Diameter PTH with Aspect Ratio of 10:1.

Photographs for coupons taken from test vehicle two boards are given as Figures 17 through 19. Figure 17 is a photograph of a 15:1 aspect ratio PTH. In the photograph, a small bubble is trapped in the hole and is a consequence of resin mounting and is not a defect in the plating of the PTH. In addition, there are slight drilling errors, as shown in Figure 19. The plating follows the contours of the PTH wall and uniform copper thickness is still obtained.

Tensile/Elongation Testing and IST Testing

The tensile/elongation mechanical tests and IST reliability tests are currently being conducted. The tensile/elongation panel and the IST panels were plated under the same waveform parameters as test vehicle boards one and two. The tensile/elongation panel and IST panels were plated under the same cell configuration parameters, i.e eductor flow rate, oscillation speed, vibration frequency and anode-to-cathode spacing as test vehicle boards one and two. The electrolyte, however, was different. The electrolyte used to plate the boards shown in this paper was from an aged bath. The electrolyte used to plate the tensile/elongation panel and IST panels was from a freshly prepared electrolyte bath. The concentration of species was held constant between the two electrolyte baths.

Conclusions

The PCB industry is continually pushing towards miniaturization of finer pitch traces and transmission lines and smaller diameter PTHs and vias, while maintaining low cost and high reliability. It is critical that technology keep pace with the miniaturization trends; manufacturers are concerned with whether their current production lines may be modified to plate higher aspect ratio PTHs with minimal cost. The technology presented here bridges this gap. The novel cell configuration circumvents the conventional problems of hydrodynamic control of the plating solution and can easily be retrofitted into existing production lines. Coupling the novel cell design with fine-tuned electrically mediated parameters allows for plating of high aspect ratio PTHs without the need for expensive and hard-to-control organic additives, thus reducing the cost of the process and the environmental liability of the plating process since additives represent a considerable cost of the PCB plating process and pose waste disposal issues.[26] The process is currently being quantified in terms of tensile strength and reliability; these results will be presented in comparison with that of copper plated in an additive-containing electrolyte.

Acknowledgments

The authors acknowledge the funding and support of the United States Air Force, specifically the AFRL/SNDR group for the current work. The work is supported under contract DASG60-01-C-0056. This paper was approved for public release by AFRL/WS as document number AFRL/WS-05-2476. Plating Electronic GmbH is also gratefully acknowledged for providing the rectifier for this work.

References

[1] M. Paunovic and M. Schlesinger, Modern Electroplating Wiley Inc. NY 2000.
[2] S. Coughlan, *Trans. IMF*. 73(2). 54. 1995.
[3] S. Kenny, B. Reents and J. Zosel, *Printed Circuit Design and Manufacture*, January 2005, pg. 23-29
[4] T. Pearson and J.K. Dennis, *J. Applied Electrochemistry*, 20, 196 (1990).
[5] S. Coughlan, *Institute of Metal Finishing*, May (1996).
[6] R. van't Wout Hofland, "Going in Reverse", *PC FAB,* November 2000.
[7] G. Milad and M. Lefebvre, "PPR Plating for HDI", *PC FAB,* September 2000.
[8] R. Blake, D. DeSalvo and R. Retallick, "Pulse Plating", *PC FAB,* January 2000.
[9] D. Pletcher and F.C. Walsh, Industrial Electrochemistry Second Edition, Chapman and Hall, Glasgow, 22, 1993.
[10] N. Ibl, *Surface Technology,* 10, 81 (1980).
[11] J-C. Puippe and F. Leaman, Theory and Practice of Pulse Plating, AESF, Orlando, FL (1986).
[12] K. Yin, *Surface and Coatings Technology,* 88, 162 (1996).
[13] A.J. Cobley and D.R. Gabe, *Circuit World* 27/3, 19-25, 2001.
[14] M. Ward, D.R. Gaba and J.N. Crosby, *Trans. IMF*, 76(4), 121, 1998.
[15] H. Williams, *Trans. IMF*, 79(3), B37, 2001.
[16] L. Gebhart, J. Sun, P. Miller, and E.J. Taylor, "Electroplating Cell with Hydrodynamics Facilitating More Uniform Deposition Across a Workpiece During Plating", Patent Pending, US Patent Application Number 10/804,841 (Publication Number US 2005/0205429 A1, Publication Date September 22, 2005), Application Date March 19, 2004.
[17] Chin, D-T. and Tsang, C-H. (1978), Mass Transfer to an Impinging Jet Electrode, *J. Electrochem. Soc*., 125, 9, pp 1461-1470.
[18] Hsueh, K-L. and D-T. Chin (1986a), Mass Transfer to a Cylindrical Surface from an Unsubmerged Impinging Jet, *J. Electrochem. Soc*., **133**, 1, pp 75-81.
[19] Hsueh, K-L. and D-T. Chin (1986b), Mass Transfer of a Submerged Impinging Jet on a Cylindrical Surface, *J. Electrochem. Soc*., **133**, 9, pp 1845-1850.

[20] Ward, M., D.R. Gabe, and J.N. Crosby (1998), Novel Agitation for PCB Production: Use of Eductor Technology, *Trans IMF*, **76**, 4, pp 121-126.
[21] Ward, M., D.R. Gabe, and J.N. Crosby (1999b), Exploitation of Eductor Agitation in Copper Electroplating, *Proc. SURFIN/99*, June 21-24, Cincinnati, OH.
[22] Chin, D-T. and M. Agarwal (1991), Mass Transfer from an Oblique Impinging Slot Jet, *J. Electrochem. Soc*., **138**, 9, pp 2643-2650.
[23] J. Reid, S. Mayer, E. Broadbent, E. Klawuhn and K. Ashtiani, "Factors Influencing Damascene Feature Fill Using Copper PVD and Electroplating", Novellus Systems Technical Paper.
[24] J. Sun et al, "The Effect of Plating Cell Configuration on the Uniformity of Copper Thickness Distribution", presented at IPC APEX/Expo February 2005.
[25] J. Sun, L. Gebhart, A. West and E.J. Taylor, "The Effects of Plating Cell Design on Pulse Plating of Electronic Interconnects in the Absence of brighteners and Levelers", IPC Printed Circuits EXPO, Long Beach, CA, March 2003
[26] P. Leisner, G. Bech-Neilson, and P. Moller, "Throwing Power in Pulse Reverse Plating from an Acid Copper Bath", Dynatronix Publication, http://www.dynatronix.com/copper.htm