Process Qualification Using the IPC-B-52 Standard Test Assembly

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Abstract
Many professionals in the electronics manufacturing industry have, or eventually will, face the issue of determining whether the materials of construction for printed wiring assemblies (PWAs) are compatible with each other for the products produced, and producing objective evidence of this compatibility. Such a determination may be a monitoring or changing of an existing in-house manufacturing process, the development of a new manufacturing process, or determining if assemblies produced by a subcontractor are acceptable. The concept of materials compatibility can be very broad, depending on what factors are chosen for examination, but is critical to understanding the reliability of manufactured hardware.

This paper focuses on the use of the IPC-B-52 standard printed wiring assembly as a test vehicle to meet these needs, with illustrative data from a high reliability avionics manufacturing process, including lead-free evaluations.

Process Qualification

The basic question to be answered in a process qualification exercise is "how do you demonstrate that your chosen combination of materials and processes are good enough?" The definition of "good enough" will vary depending on industry segment, the end item requirements, the end-use environment, consequences of failure, and which aspect of reliability is being discussed. "Good enough" for a commodity item may not be "good enough" for an airborne flight control computer.

When starting a qualification effort, the first question to answer is "qualification against what document or what standard?" Standards may include:

- Internal quality criteria or benchmarks
- A customer imposed set of tests and minimum criteria (e.g. Boeing)
- A standard common to a segment of the industry (e.g. Bellcore for telecommunications)
- A nationally accepted standard (e.g. MIL-STD-2000 or MIL-STD-883)
- An internationally accepted standard (e.g. IPC)

Reliability is a very broad and far reaching term, encompassing many different aspects of circuit function. Reliability can include items like solder joint integrity, integrity of polymeric compositions, component wearout, function in hostile environments, function in standard tests (vibration, thermal cycling), etc. This paper concentrates only on the aspects of electrochemical reliability, which is directly related to the residues present on a printed wiring assembly and the effects of those residues on electrical performance.

Even when a single aspect of reliability is decided upon, the choice of test vehicle is difficult because configuration and topology varies so greatly. The goal of this research effort was to develop a test vehicle, building upon successes and lessons learned from past test vehicles, which would represent mainstream electronics manufacturing, at a reasonable price, usable by many.

NPL-TB-57 Test Board

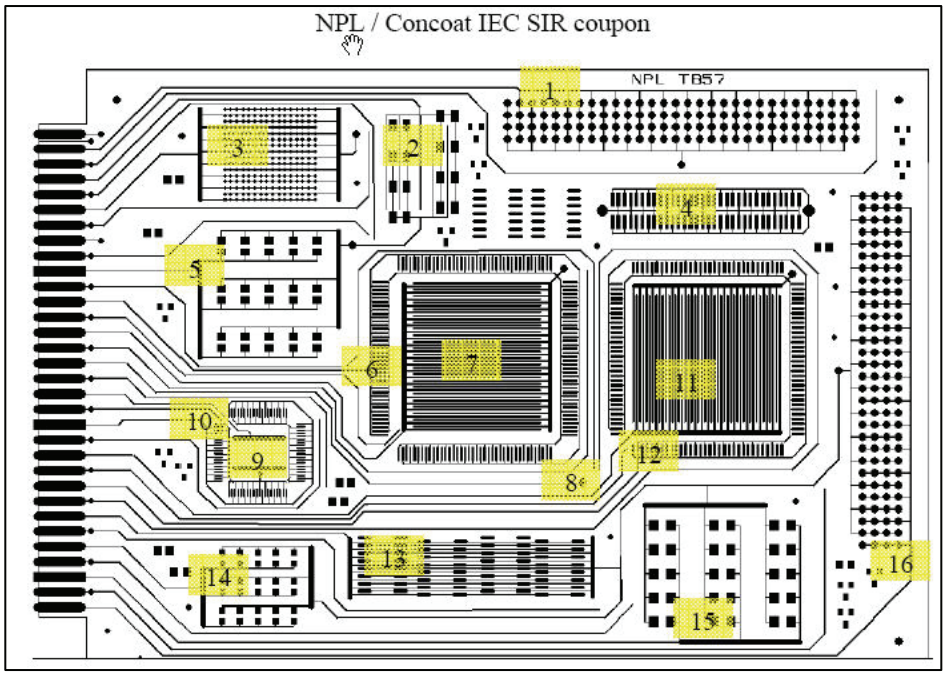
The primary drawback on almost all of the test vehicles used to date have been that they are either not designed for SIR testing, or are not a good representation of the material sets used in modern manufacturing. Further, many of the test vehicles did not contain components that would act as entrapment sites for deleterious process materials,

such as flux. Therefore, it was desired that a test vehicle be developed which was designed for SIR testing, and which contained common components.

References 1-3 show work done between the National Physical Laboratory (NPL) and Concoat Ltd., both in the United Kingdom, on development of such a test vehicle. This vehicle was designated TB57 and is shown in Figure 1. Information on the test patterns of the TB57 is shown in Table 1.

Figure 1 - Original TB57 Test Board (Top)

Table 1 - Original TB57 Bill of Materials



ID	Component	Min SIR Pitch [mm]
1	TH connector 4x30 pins horizontal	0.60
2	8 x SM Cap 1210	0.46
3	BGA256, 1mm pitch	0.4
4	SM connector IEEE 1386, 2 x 16 pins	1
5	15 x SM Cap 0805	0.6
6	QFP160 0.65mm pitch ISO	0.254
7	COMB under QFP160	0.2
8	COMB 45° bottom side (IPC-B-24)	0.5
9	COMB under QFP80	0.2
10	QFP80 0.5mm pitch ISO	0.2
11	COMB under QFP128	0.2
12	QFP128 0.8mm pitch ISO	0.3
13	4 x SOIC16 1.27mm pitch ISO	0.2
14	15 x SM Cap 0603	0.6
15	15 x SM Cap 1206	1.2
16	TH connector 4x30 pins vertical	0.60

IPC-B-52 Test Board Prototype Version

The TB57 represented a significant improvement over previous test vehicles such as the IPC-B-36 test board; however, to increase the utility of the test board, several features were changed during the Rockwell Collins revision efforts:

- The smallest component on the TB57 was a 0603 package. A 0402 package was considered to be more typical of mainstream challenges. The 1210 package was considered to be similar to the existing 1206 package, so it was converted to 0402 pads.
- The board was fully loaded with patterns (16). Nothing was left open for expansion for components such as chip scale packages or flip chips.
- The TB57 had three quad flat pack (QFP) packages of varying pitches. The 0.8 mm pitch was considered redundant and eliminated to open up board area for optional patterns, such as flip chips or chip scale packages.
- The author's experience with the CSL Umpire Board had showed that a fully masked comb pattern on the bottom side of the board did not often yield useful information. The TB57, as designed, had no components on the bottom side of the board. Such components can often entrap residues during wave soldering operations. The comb pattern on the TB57 was replaced with a series of 0805 passives to represent bottom side chips with solder joints formed during wave solder operations.
- Some of the connectors had no holes to support the molded pins of the connectors; so additional tooling holes were added.

Ion Chromatography (IC) Coupon

One drawback of process investigations that involve both ionic residue quantification, such as ion chromatography, and the effects of ionic residues, such as SIR testing, is that samples cannot be used for both tests. Two sets of fully populated SIR boards could be generated for IC and SIR testing, but would be very expensive and there are always questions of whether the two boards were manufactured under identical conditions. As a compromise, a break off coupon was added to the design, as shown in Figure 2.

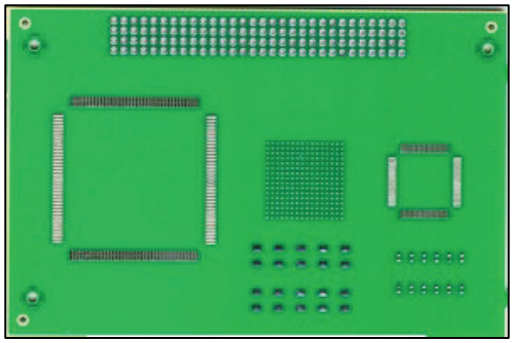


Figure 2 - IC Coupon

This IC Coupon was designed to contain those components most likely to entrap process residues and provide challenges to cleaning processes. The IC Coupon does not contain any active circuitry, only mounting pads. Room was left on the coupon for users to add components of their choice. The intent of the IC Coupon was to generate ionic cleanliness data as a correlation to SIR test data, on a test sample generated at the same time.

Solder Mask Coupon

Solder mask adhesion has been evaluated in a number of ways in the past. In general, adhesion testing has been done per Reference 4. This method involves scribing a checkerboard pattern into a sheet of solder mask, adhering tape over the surface and pulling the tape off. The amount of solder mask adhesion was measured by the number of squares removed by the tape pull. Unfortunately, there was a great deal of variability inherent in this technique, and it did not always predict the performance of solder mask features, such as solder mask dams.

The IPC [DuPriest 2221 committee] had proposed the use of an alternative coupon to test solder mask in a way that would be more representative of real world processing conditions. Two of these coupons, slightly modified for

automated testing, were added to the test vehicle design. One coupon can be used for as-received testing, and the other after exposure to the manufacturing process. Both coupons are tested using the standard tape test method (IPC-TM-650, method 2.4.28). The solder mask coupon is shown in Figure 3.

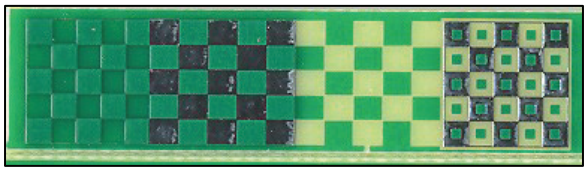


Figure 3 - Prototype Solder Mask Coupon

SIR Mini-coupons

Many OEMs represented at IPC meetings are often in the position of subcontracting assembly work, or having printed circuit boards made in remote locations. Having a quick acceptance test that could be run at a board fabrication site prior to acceptance, and again at the receiving site to verify a clean transport, was desired.

In the author's experience, SIR testing, with high resistance requirements, can quickly show if a bare board is clean or not. Work done by Brian Ellis [Ellis paper] showed that most long term SIR tests can be accurately predicted by an eight hour SIR test. In the course of running many SIR tests, the author has found the first 24 hours of the test to be the most telling.

Therefore, two mini-coupons were designed into the test vehicle and are shown in Figure 4. The comb patterns have 5 mil lines and 5 mil spaces. These lines and spaces were considered to be typical of most modern designs, but not at the cutting edge of technology (e.g. 3 mil lines and spaces). SIR professionals in the IPC SIR committees agree that covering the ends of comb fingers with solder mask leads to more stable test performance.

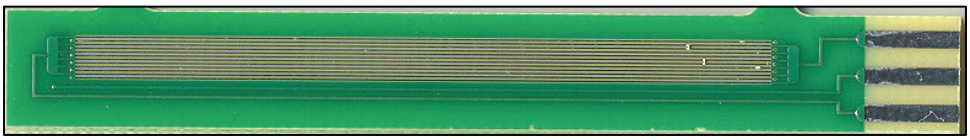


Figure 4 - SIR Mini-Coupons

IPC-B-52 Test Board Rev A

All of these features were combined into a single segmented test vehicle, which the IPC designated the IPC-B-52 test board. The first prototype of the IPC-B-52 is shown in Figure 5.

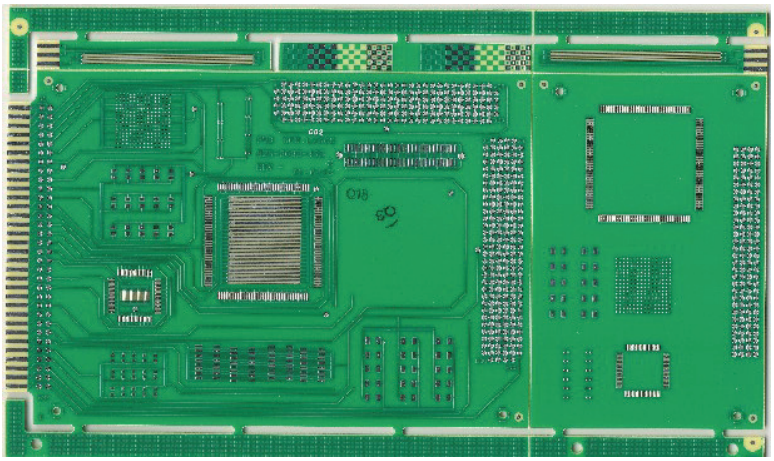


Figure5 - Prototype IPC-B-52 Test Boards

This prototype B-52 board was used for bare board studies and for studies of solder paste residues. Approximately 300 of these prototype boards were procured for initial studies. Approximate cost per board was $50. However, initial studies showed areas for improvement.

- After discussions with Rockwell Collins manufacturing personnel, the two solder mask coupons and the two SIR mini-coupons were moved to the ends of the test vehicles so that the rails would be intact for manufacturing. This also made the coupons more removable.
- One of the desirable aspects of the Bellcore test approach was the use of cross-hatched solder mask. This mask pattern provided an excellent entrapment site at the intersections of comb fingers and solder mask edge. If the solder mask imaging and developing process was improperly done, poor SIR performance was the result. Consequently, a cross-hatched solder mask pattern was added to the coupon design. Finally, the circuitry was routed to edge contact fingers, with incorporated through-holes, such that these coupons could be incorporated into automated test fixturing. The revised coupon is shown in Figure 6.
- After discussions with Don DuPriest, IPC-2221 chairman, the solder mask coupon was found to be incorrect. The correct coupon, slightly modified to make it more amenable to automated testing, is shown in Figure 7.
- Some of the mounting holes and circuit routings were changed to improve manufacturability.

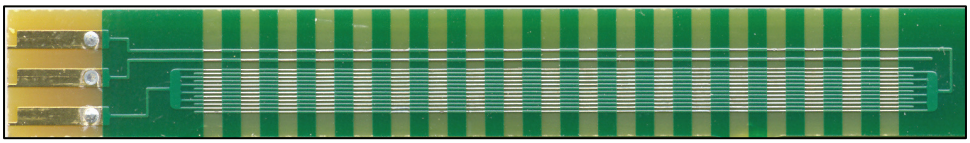


Figure 6 - Revised SIR Mini Coupon

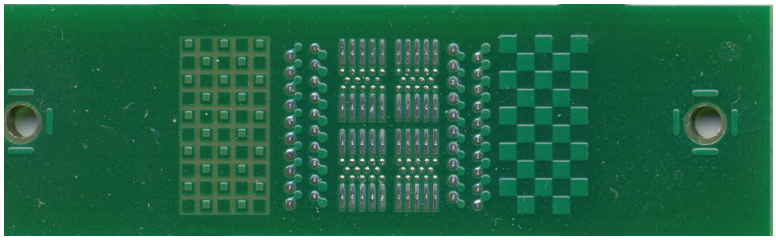


Figure 7 - Revised Solder Mask Coupon

Table 2 - IPC-B-52 Bill of Materials

Figure ID	Qty Needed	Ref Designator	Part Description	Component Name	Practical Components or TopLine PN	DigiKey PN
1	1	J2	TH connector 4x24 pins horizontal	AMP 536501-3		A3264-ND
2	20	C1-C8 C64-C75	CAPACITOR, 0.01uF, 0402			
3	2	U1, U9	BGA, 256 IO, 1 mm pitch, Isolated		TopLine: BGA256T1.0-ISO	
4	1	P1	SM connector IEEE 1386, 2 x 16 pins	Molex 74136-2164		WM17200-ND
5	25	C24-C38 C76-C85	CAPACITOR, 0.1uF, 0805 package			
6	2	U2, U8	QFP160 0.65mm pitch ISO		Practical Components: QFP160-28mm-.65mm-2.6 (isolated)	
7	2	U3, U10	QFP80 0.5mm pitch ISO		TopLine: A-TQFP80-12mm-.5mm-2.0 (Amkor)	
8	15	C9-C23	Capacitor, 0.01 uF, 0603 package			
9	4	U4-U7	SOIC16, 1.27 mm pitch, isolated		Practical Components: SO16GT-3.8mm	
10	25	C39-C63	Capacitor, 10 uF, 1206 package			478-1575-2-ND
11	2	J1, J3	TH connector 4x24 pins vertical	AMP 536510-3		A3276-ND

Of the materials in the BOM, only four have special requirements. Parts U1, U2, U3 and U4, correspond to test patterns which measure SIR between component leads. The presence of internal dies or internal wire bonding, even if purposely blown, can cause anomalous readings during SIR testing. Consequently, these four chips MUST be true mechanical dummies with no internal dies or wire bonds. If possible, the parts should be X-rayed prior to use. The mirror counterparts of U1-U4 (U7-U10) on the ion chromatography coupon do not have to be true isolated parts as SIR is not measured. The final version of the IPC-B-52 standard test vehicle is shown in Appendix A with the final Bill of Materials (BOM).

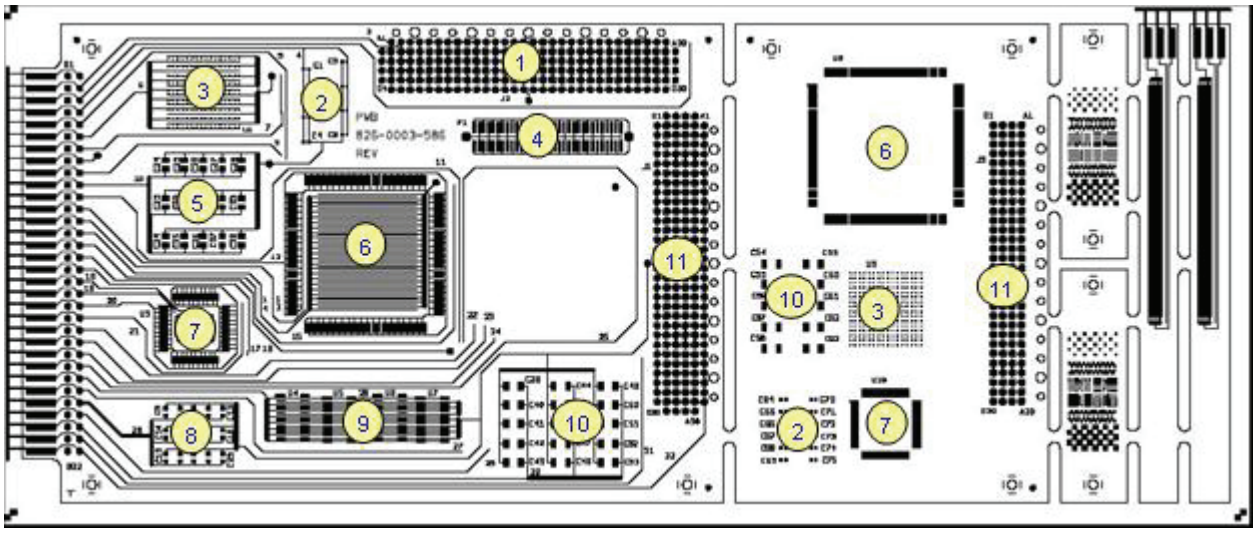


Figure 8 - IPC-B-52 Final – Top Side

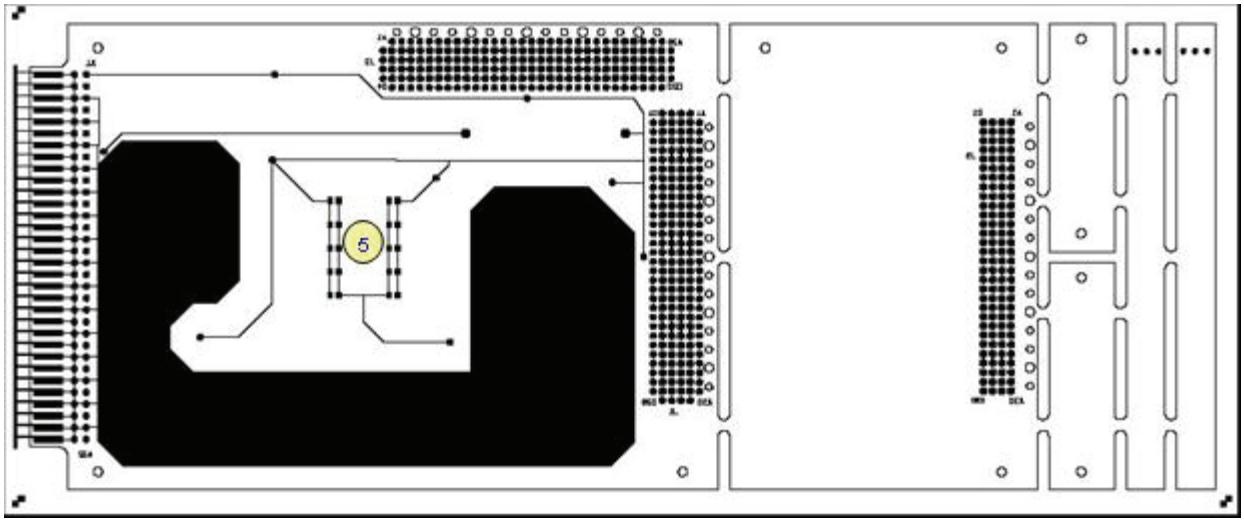


Figure 9 - IPC-B-52 Bottom Side

This finalized design was donated to the IPC by Rockwell Collins. The data file consisted of the following elements:

- Design file – Zuken format
- Rockwell Collins drawing – PDF and EPS formats
- Gerber Files for the bare board
- A Cover Note on the test board
- An Open Offer to IPC-B-52 Users

B-52 Test Patterns

The following sections illustrate and explain the various test patterns.

Horizontal Connector

The J2 through-hole horizontal connector is an AMP536501-3 4x24 pin configuration. The test pattern energizes alternate rows of plated through holes (PTHs) and measures the return current from the remaining rows of holes. If residues remain on, in or under the connector, the SIR will be impacted.

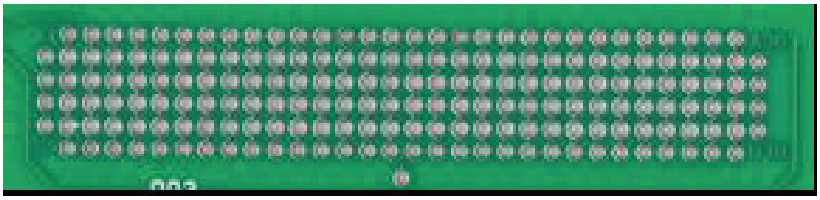


Figure 10 - Horizontal Connector Pattern

0402 Cap Field

The 0402 pattern contains eight 0402 package, 0.01 µF, ceramic capacitors. One side of each cap is energized and the resulting current measured on the opposite trace. If residues remain under, on or around the components, the SIR will be impacted.

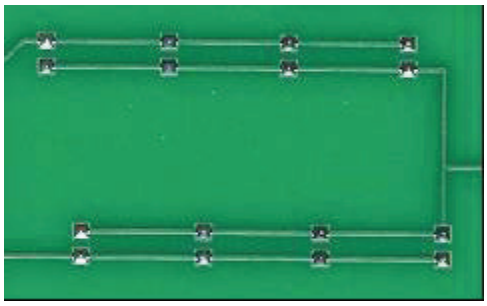


Figure 11 - 0402 Pattern

BGA

The ball grid array (BGA) is a 256 I/O full array, 1 mm pitch, configuration. The component for this pattern is a TopLine BGA256T1.0-ISO. This component must have no internal die or wire bonds as these will interfere with SIR measurements. Alternating lines of balls are energized, with the remaining lines used to detect resulting current.

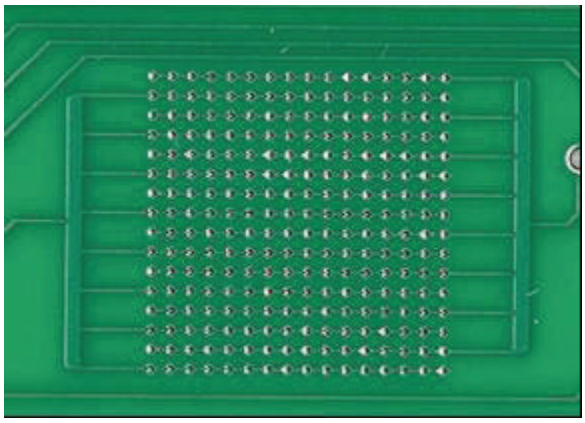


Figure 12 - BGA Pattern

SM IEEE1386 Connector

The IEEE1386 surface mount connector was designed around a Molex 74136-2164. This pattern measures resistance between pads. Alternate pads are energized and the remaining pads are used to measure resulting current.

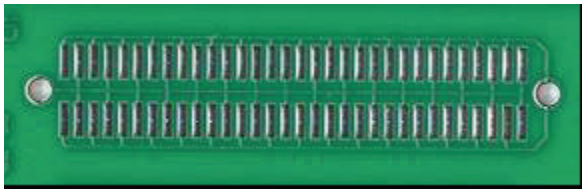


Figure 13 - IEEE1386 Pattern

0805 Cap Fields

The 0805 pattern contains fifteen 0805 packages, 0.1 µF, ceramic capacitor. One side of each cap is energized and resulting current measured on the opposite trace. If residues remain under, on or around the components, the SIR will be impacted.

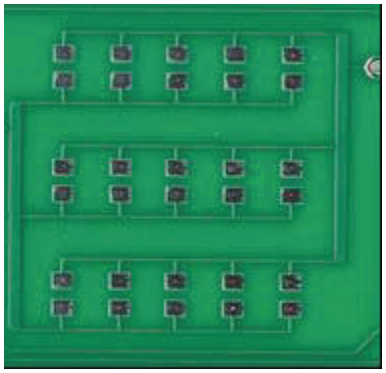


Figure 14 - 0805 Pattern

QFP160

The QFP160 area has two test patterns associated with it. The first test pattern measures the SIR between the 0.65 mm pitch component leads. The component used for this area is a Practical Components QFP160-28mm-.65mm-2.6 (isolated). This is another of the special components needed with no internal dies or wire bonds. The second test pattern is an interdigitated comb pattern under the QFP160. If residues are entrapped under the QFP160, SIR is impacted.

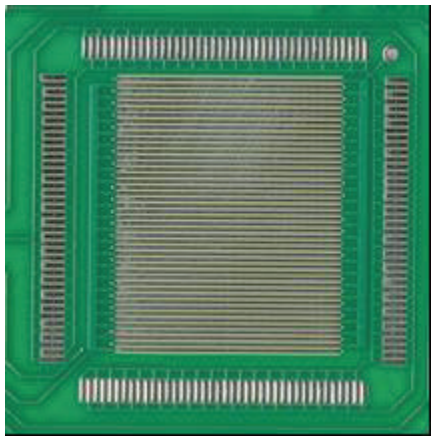


Figure 15 - QFP160 Pattern and Comb Pattern

QFP80

The QFP80 is similar to the QFP160 and has two test patterns. The component for this area is TopLine A-TQFP80-12mm-.5mm-2.0 (Amkor) QFP with no internal dies or wire bonds. The first test pattern measures SIR between the 0.5 mm pitch component leads. The second SIR test pattern is an interdigitated comb pattern under the component.

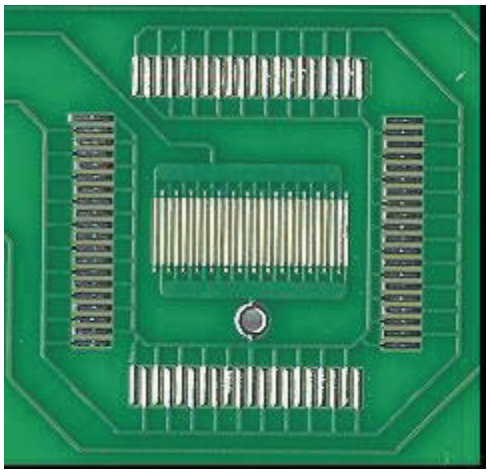


Figure 16 - QFP80 Pattern and Comb Pattern

0603 Cap Field

The 0603 pattern contains fifteen 0603 packages, 0.01 µF, ceramic capacitor. One side of each cap is energized and resulting current measured on the opposite trace. If residues remain under, on or around the components, the SIR will be impacted.

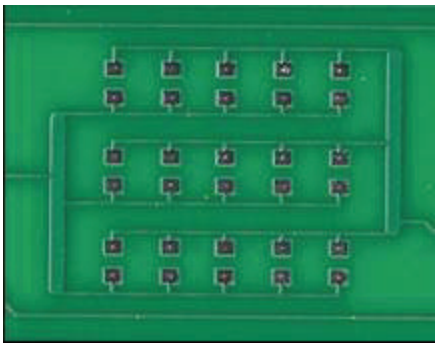


Figure 17 - 0603 Pattern

SOIC16 (U4-U7)

The SOIC16 pattern contains four 16 pin SOIC components, Practical Components SO16GT-3.8mm. The test pattern is setup to measure SIR between component leads.

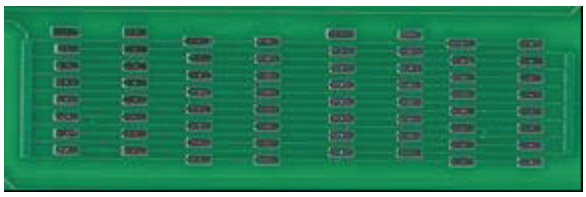


Figure 18 - SOIC16 Pattern

1206 Cap Field

The 1206 pattern contains fifteen 1206 packages, 10 µF, ceramic capacitor. One side of each cap is energized and resulting current measured on the opposite trace. If residues remain under, on or around the components, the SIR will be impacted.

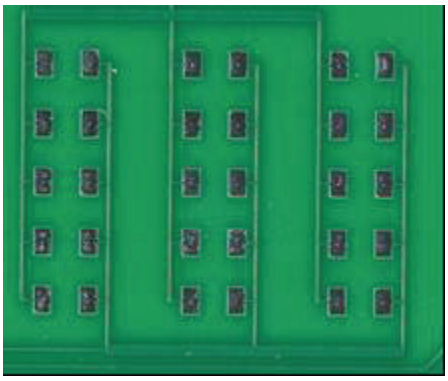


Figure 19 - 1206 Pattern

Vertical Connector (J1)

The vertical connector is similar to the horizontal connector and is designed around a 4x24 AMP 536510-3 connector. The layout is the same as the horizontal connector, but rotated 90 degrees.

Revised TB57 Board

The TB57 board had been proposed as a test vehicle for the International Electrotechnical Commission (IEC) process qualification specification 61189-5, with goals similar to J-STD-001. The IEC committee developing that specification, led by Mr. Graham Naisbitt of Concoat Systems Ltd., allowed a re-design for the TB57 test vehicle to match the Main SIR test vehicle, so that the SIR data generated by the TB57 and the IPC-B-52 would be comparable. However, the revised TB57 was not a mirror of the B-52. The revised TB57 is shown in Figures 20 and 21. The bill of materials (BOM) is shown in Table 3.

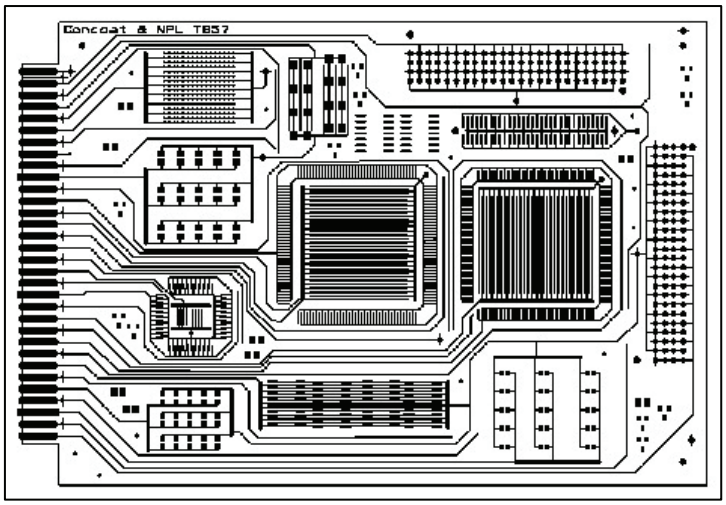


Figure 20 - Revised TB57 Top Side

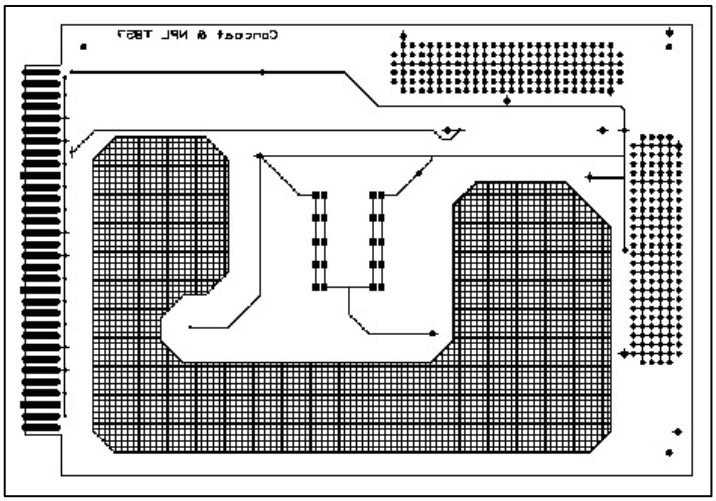


Figure 21 - Revised TB57 Bottom Side

Table 3 - BOM for Revised TB57

ID	Component	Min SIR Distance [mm]	Component type
1	TH connector 4x24 pins horizontal	0.6	24x4=96 way AMP: 536501-3
2	8 x SM Cap 1210	0.46	1210SMC-PL
3	BGA256, 1mm pitch	0.4	BGA256T1.0-ISO
4	SM connector IEEE 1386, 2 x 16 pins	1	1.00mm (.039") Mezzanine IEEE 1386 SMT, Dual Row, 71436
5	15 x SM Cap 0805	0.6	0805SMC-PA
6	QFP160 0.65mm pitch ISO	0.254	QFP160-28mm-.65mm-2.6 (isolated)
7	COMB under QFP160 (ID 6)	0.2	N/A
8	10 x SM Cap 0805	0.6	0805SMC-PA
9	COMB under QFP80 (ID10)	0.2	N/A
10	QFP80 0.5mm pitch ISO	0.2	A-TQFP80-12mm-.5mm-2.0 (Amkor)
11	COMB under QFP128 (ID12)	0.2	N/A
12	QFP128 0.8mm pitch ISO	0.3	QFP128-28mm-.8mm-2.6
13	4 x SOIC16 1.27mm pitch ISO	0.2	SO16GT-3.8mm
14	15 x SM Cap 0603	0.6	0603SMC-PA
15	15 x SM Cap 1206	1.2	1206SMC-PA
16	TH connector 4x24 pins vertical	0.6	24x4=96 way AMP: 536501-3

Phase 1: Bare Board Study

As part of the initial trials of the IPC-B-52, several studies were performed to determine performance of the test vehicle and if any modifications were needed. One of the desired uses of the test vehicle was to examine bare board fabrication processes and bare board cleanliness. The first phase of the study was to examine different laminate resin systems, different fabrication houses, and different surface finishes. Six groups of fifty test vehicles were procured representing the following combinations:

- Set 1: Fabricator A, FR4 laminate, tin-lead finish (HASL), solder mask A
- Set 2: Fabricator A, BT laminate, tin-lead (HASL) finish, mask A
- Set 3: Fabricator A, FR-4 laminate, Immersion tin finish, mask A
- Set 4: Fabricator A, BT laminate, Immersion tin finish, mask A
- Set 5: Fabricator B, FR4 laminate, tin-lead finish, mask B
- Set 6: Fabricator B, FR4 laminate, immersion tin, mask B

All of the Phase 1 studies were performed using the prototype B-52 vehicle. Each test board was handled with powder free latex gloves and broken into individual components. The components were placed in Kapak bags until ready for testing.

Phase 1 testing included ion chromatography (IC Coupon), SIR (SIR Main Board), solder mask adhesion (SM coupon), and short term SIR (SIR mini-coupon).

Ion Chromatography

Reference 5 is a good overview of setting up an ion chromatography laboratory. The Rockwell Collins IC laboratory is setup per this paper.

1. Each IC coupon was immersed in 70 ml of 10% isopropanol / deionized water solution in the Kapak bags.
2. The standard IPC ion chromatography test method, IPC-TM-650, method 2.3.28, uses a 75% isopropanol / 25% deionized water solution. Research studies performed at Delco Electronics and Rockwell Collins has shown the 10/90 solution to be as sensitive an extract media, but gentler to electronics.
3. The unsealed bags were suspended in an 80^{o}C water bath from an aluminum bar, clipped shut with binder clips. This arrangement keeps the extract solution in the Kapak bags, but does not completely seal the bag. Completely sealed bags tend to balloon as the extract solution heats up.
4. The coupons were allowed to extract for a total of 60 minutes. The bags were removed from the water bath and allowed to cool for 60 minutes with the IC coupons in the Kapak bags.
5. The IC coupons were removed from the Kapak bags using clean forceps. The solution was decanted into 25 ml Nalgene bottles that had been triple rinsed with 18 megohm-cm deionized water.
6. One sample set was analyzed by Rockwell Collins. The remaining sample sets were sent to volunteer laboratories for a comparative study in ion chromatography. Other volunteer laboratories included:

    - Precision Analytical Labs, Kokomo, IN
    - Trace Laboratories East, Hunt Valley, MD
    - Research in Motion, Waterloo, Ontario
    - Dionex, Sunnyvale, CA
    - Delphi Delco Electronics, Kokomo, IN

Rockwell Collins IC System

The Rockwell Collins ion chromatography system has the following configuration:

Cations

- Metrohm 761 Compact Ion Chromatograph
- Metrohm 766 Autosampler
- Method: Non-Suppressed Cation
- Eluent: 8.0 mmol/L d-tartaric acid , 0.75 mmol/L dipicolinic acid (DPCA)
- 1 ml/min flow rate
- Metrohm Cation2 column with guard column
- Sample loop: 20 µL
- Run time: 18 minutes per run
- Control cations: sodium, ammonium, potassium, magnesium, calcium

Anions

- Metrohm 761 Compact Ion Chromatograph
- Metrohm 766 Autosampler
- Method: Suppressed Anions
- Eluent: 2.8 mmol/L sodium bicarbonate / 1.4 mmol/L sodium carbonate
- 0.7 ml/min flow rate
- Metrohm ASUPP5-250 column with guard column
- Suppressor: Metrohm MSM
- Regenerant: 100mM sulfuric acid
- Sample loop: 20 uL
- Run time: 34 minutes per run
- Control anions: fluoride, chloride, bromide, nitrate, nitrite, phosphate, sulfate

IC Calibration

Prior to any test runs, the chromatographs were calibrated with National Institute of Standards and Technology (NIST) traceable calibration solutions. A four-point calibration scheme was used, covering 0.2 ppm – 20 ppm concentration levels for most anions and cations. Calibration solutions were made using dilutions by weight, measuring to the nearest 0.01 grams.

IC Integration Parameters

The value that chromatographic software reports as parts per million (PPM) concentration often depends on the background integration parameters. Such parameters are used to define minimum peak size, onset thresholds, and other values that allow the user to define what is and is not a peak. The integration parameters used in the RC system are shown in Figure 22.

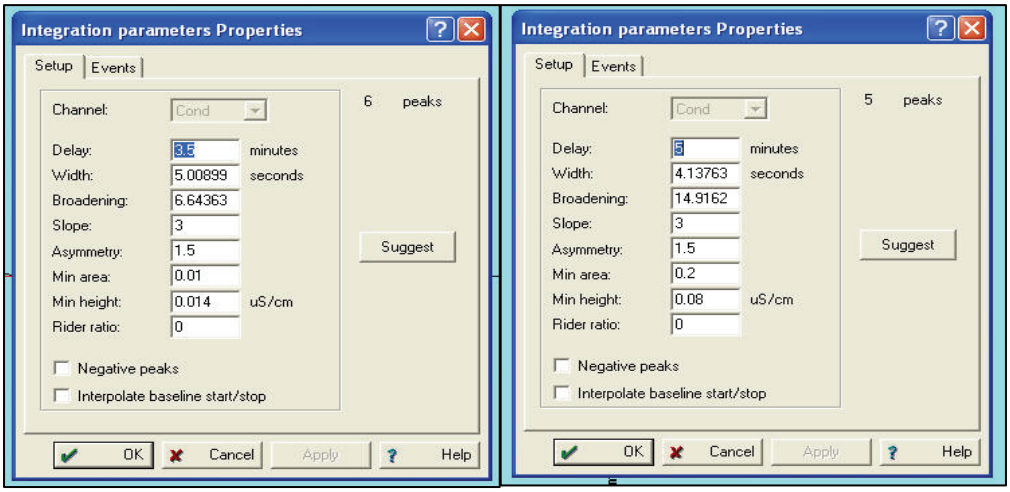


Figure 22 - IC Integration Parameters

Normalizing Results

The output of chromatographic software is a chromatogram showing conductivity vs. time, as shown in Figure 23.

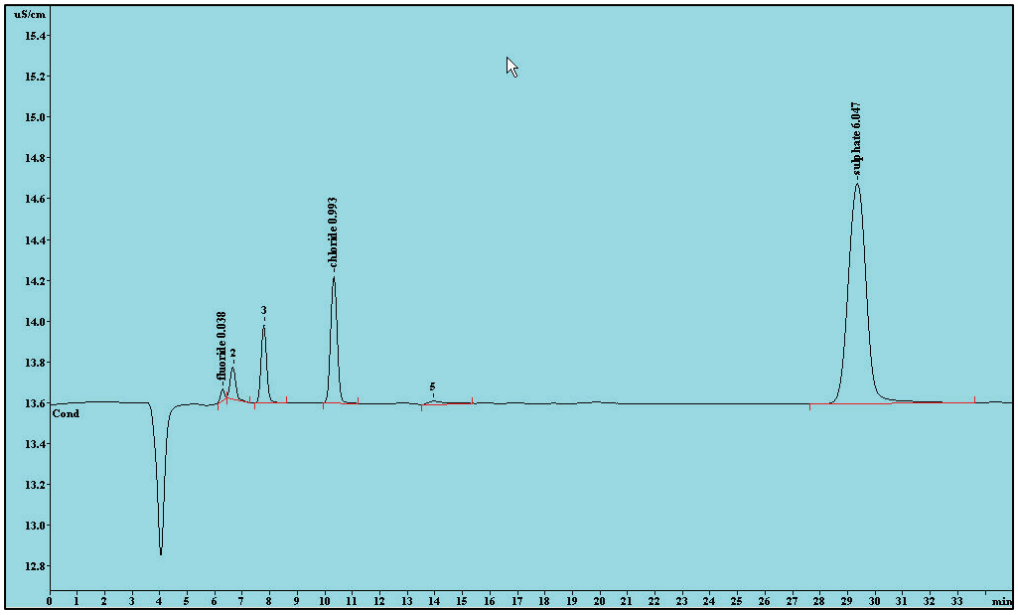


Figure 23 - Chromatogram

It is a common industry practice to convert PPM (or mg/L) concentration values from the chromatogram into a concentration of ions per unit area of extracted surface. The following formula (from method 2.3.28A) was used:

Value in PPM (in µg/mL) * Extract Volume (in mL) / surface area (in cm^2)

The IC coupon, with no components, had a surface area of 132 cm^2. It should be noted that parts per million (ppm) and micrograms per milliliter (µg/mL) are equivalent values.

Summary of IC Results

Table 4 - Chloride Levels (in µg/cm2)

Sample	RIM	Rockwell	Delco	Trace	PAL	Dionex
Ven A – FR4 – HASL	0.71	0.73	0.66	0.77	0.73	0.65
Ven A – FR4 – ImSn	0.98	0.99	0.89	0.95	0.94	0.95
Ven A – BT – HASL	0.82	0.80	0.69	0.81	0.79	0.64
Ven A – BT – ImSn	1.33	1.29	1.10	1.15	1.19	1.16
Ven B – FR4 – HASL	1.86	1.62	1.50	1.47	1.77	1.53
Ven B – FR4 – ImSn	0.13	0.17	0.09	0.36	0.09	0.10

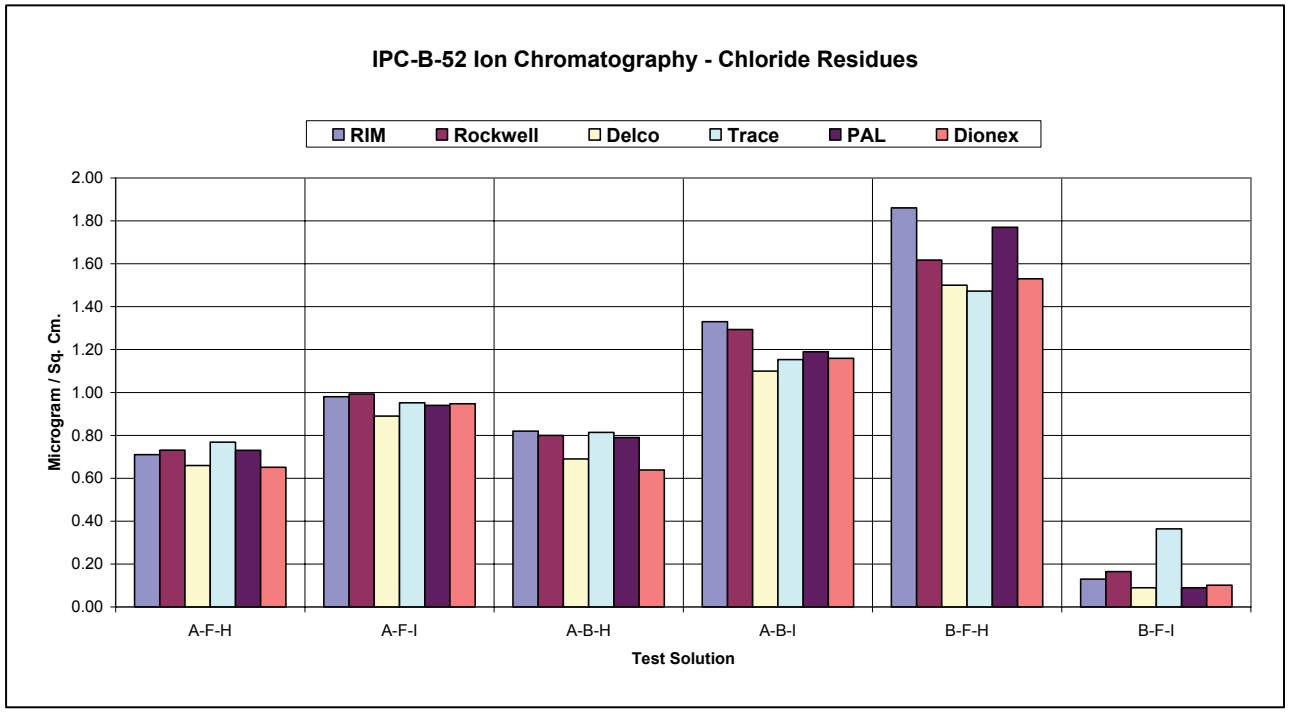


Figure 24 - Comparison of Chloride Values Between Labs

Table 4 shows the values found between the six different test laboratories participating in this phase of the study. The chloride values found were encouraging. Much of the published work within the IPC in the past few years, and much of the discussions within the Cleaning and Cleanliness Assessment committees has focused on the role of halide contaminants (primarily chloride and bromide) on electrochemical failure mechanisms. The higher the amount of chloride, the greater the risk of electrochemical migration (dendritic growth). References 9 -12 discuss generic recommended starting cleanliness conditions for ion chromatography data, although almost all of these recommended levels refer to finished assemblies and not bare, unpopulated circuit boards.

One of the goals of the IPC Ionic Conductivity / Ion Chromatography Task Group (ICTG) has been to develop a test methodology for determining ionic cleanliness that is both repeatable and reproducible. All of the test labs used completely different sets of equipment, different columns, different eluent structures, different calibration and integration parameters, and different software packages. Rockwell Collins was the only site using non-Dionex equipment. All sites used 3-4 point calibration schemes. The results for the chloride analyses show good agreement between the test labs. When this data was discussed in committee, technical experts agreed that a desirable level of agreement was obtained.

The data for chloride shows some surprising trends. In general, hot air solder leveling (HASL) is a “dirty” process when compared to other plated metalizations, such as immersion silver or immersion tin. Yet for all cases for chloride, the HASL boards had lower chloride levels than found for the immersion tin boards. The comparison between Vendor A and B for FR-4 and HASL was not surprising. From past experience, Vendor A has a much better post-HASL cleaning process than Vendor B.

Table 5 - Bromide Levels

Sample	RIM	Rockwell	Delco	Trace	PAL	Dionex
Ven A – FR4 – HASL	0.00	0.00	0.01	0.01	0.02	0.16
Ven A – FR4 – ImSn	0.00	0.17	0.01	0.01	0.01	0.00
Ven A – BT – HASL	0.00	0.23	0.01	0.01	0.01	0.00
Ven A – BT – ImSn	0.00	0.18	0.00	0.01	0.00	0.00
Ven B – FR4 – HASL	0.00	0.00	0.05	0.01	0.08	0.06
Ven B – FR4 – ImSn	0.00	0.18	0.01	0.01	0.01	0.00

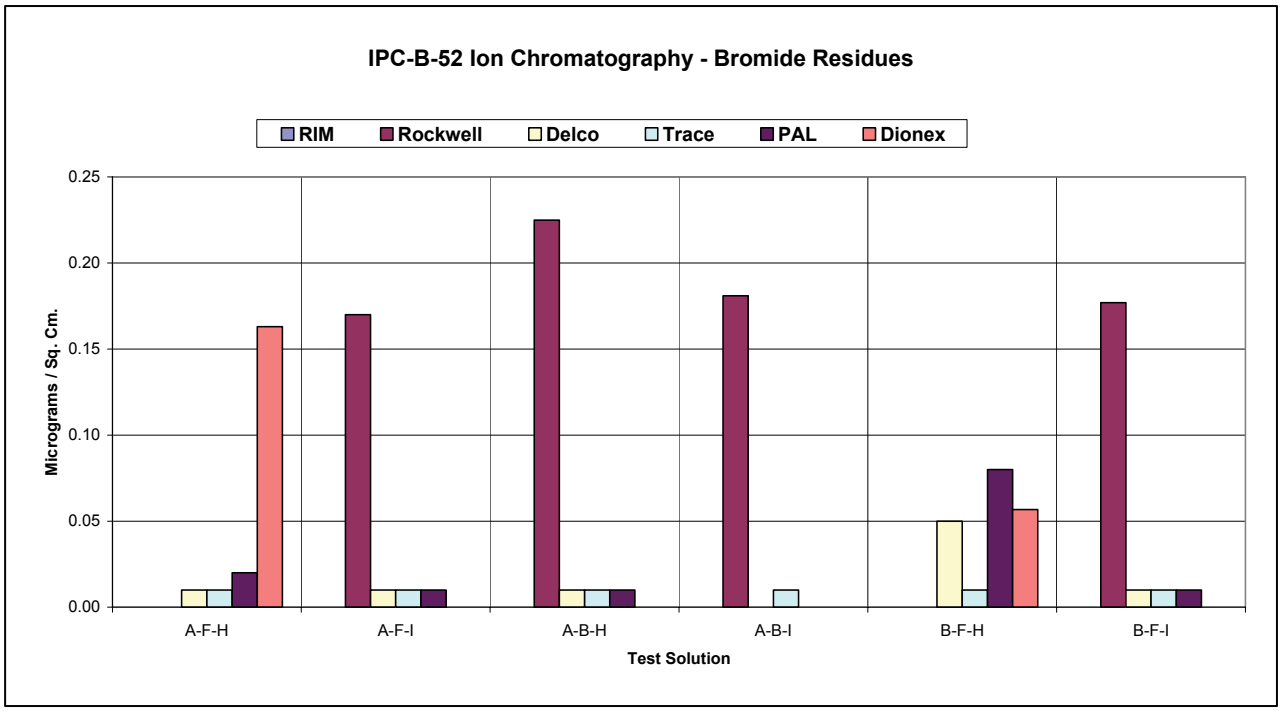


Figure 25 - Comparison of Bromide Levels between Test Labs

Table 5 shows the data for bromide residues for all test sites. Unfortunately, there is less agreement here between test labs. It should be pointed out that the scale in Figure 25 is much different from that in Figure 24 (chloride). From the author's published work in the past, a general guide for bromide residues has been approximately 2.0 ug/cm^2 as a maximum. The values observed here are far below that figure.

IPC-5701, Users Guide for Cleanliness of Unpopulated Printed Boards, gives an example of a Delphi Delco Electronics bare board specification in which bromide levels are recommended to be below 1.0 µg/cm^2. By that measure, all of the bare boards would be considered as acceptable from a bromide residue standpoint.

Good agreement was found between Delco, Trace and PAL, but Rockwell Collins and Dionex values are different. On a large scale, this difference is not expected to be significant.

Bromide residues come from one of two sources in bare boards; either from the brominated flame retardant in the laminate resin structure, or from the use of a brominated processing fluid, such as HASL flux. When bromide comes from the flame retardant, it does not initiate or support electrochemical failures. When bromide is from a flux residue, then dendritic growth is much more likely.

From a background knowledge of both Vendor A and Vendor B fabrication processes, neither use a brominated flux or plating solution. Hence, all of the bromide can be attributed to the laminate fire retardant.

Table 6 - Sulfate Levels

Sample	RIM	Rockwell	Delco	Trace	PAL	Dionex
Ven A – FR4 – HASL	0.91	1.19	0.90	0.84	0.97	1.19
Ven A – FR4 – ImSn	6.31	6.05	5.00	5.79	5.99	6.48
Ven A – BT – HASL	1.31	1.48	1.20	1.07	1.26	1.51
Ven A – BT – ImSn	5.13	4.92	4.10	4.48	4.74	5.26
Ven B – FR4 – HASL	0.99	1.30	0.97	0.90	1.07	1.19
Ven B – FR4 – ImSn	1.04	1.41	0.94	0.91	1.00	1.18

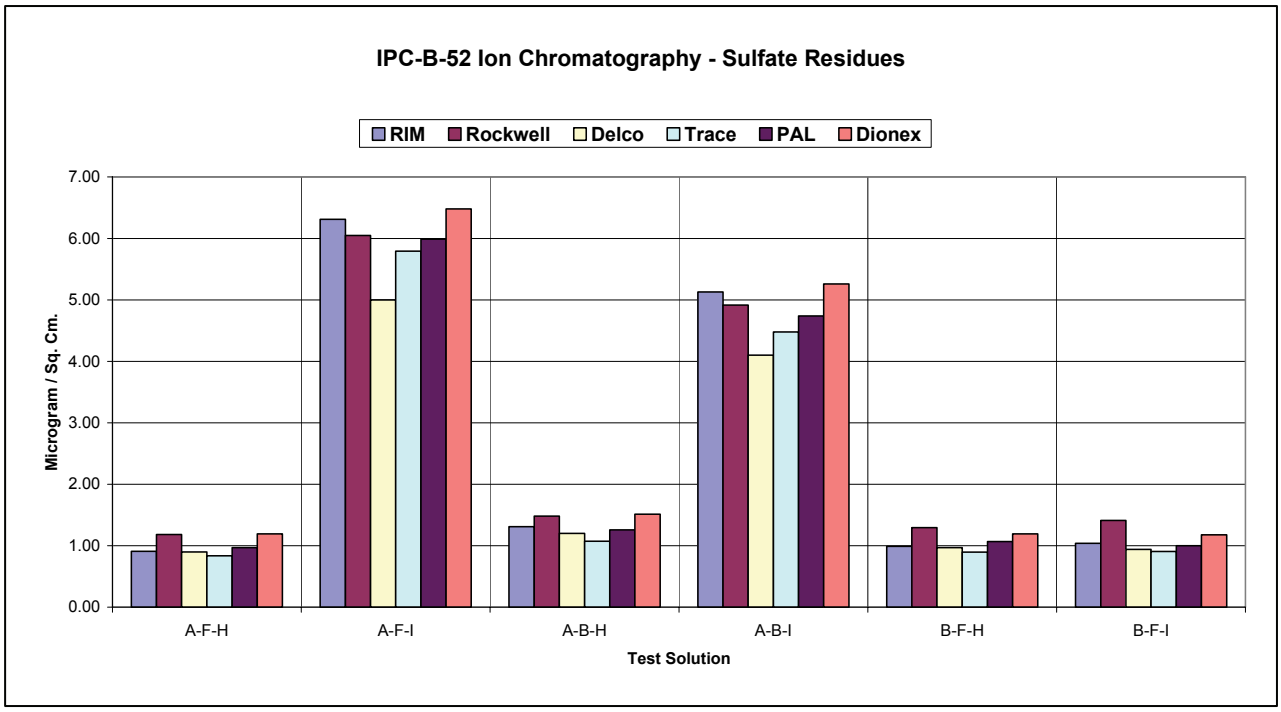


Figure 26 - Comparison of Sulfate Levels Between Test Labs

Table 6 shows the data for the sulfate residues. As seen with the chloride, there is good agreement between labs on the amount of sulfate. Sulfate can came from a number of sources, but are often found as constituent elements in many plating baths, such as sulfuric acid or sulfamate chemicals. Sulfur compounds are also common in solder mask imaging and developing processes in fabrication. Sulfur compounds are also added to municipal water supplies to help control bacteria, so if tap water cleaning was used during board fabrication, sulfates are expected on the finished boards.

For the data above, part of the sulfate residues come from the Kapak™ bags used as the disposable extraction vessels. While the Kapak bags are far cleaner than any other plastic bag on the market, there is a small amount of cornstarch based slip agent on the surface of the plastic, as an artifact of the bag manufacturing process. The amount is generally consistent at 0.2 – 0.3 $\mu g/cm^2$.

It is known that Vendor A uses a sulfur-containing chemistry as part of its immersion tin plating process. It is not known if Vendor B uses the same plating chemistry, but the data suggests they do not.

The amount of published information on the amount of acceptable sulfate is much scarcer than found for the halide materials. Some works suggest trying to keep sulfate residues under 0.5 – 0.7 $\mu g/cm^2$. In the author's experience, based on internal Rockwell Collins investigations, assemblies can tolerate higher levels of the divalent sulfate residues, where lower amounts of the monovalent, and more electroactive, halide species are desired.

Table 7 - Total Halide (Chloride, Bromide)

Sample	RIM	Rockwell	Delco	Trace	PAL	Dionex
Ven A – FR4 – HASL	0.71	0.73	0.67	0.78	0.75	0.81
Ven A – FR4 – ImSn	0.98	1.16	0.90	0.96	0.95	0.95
Ven A – BT – HASL	0.82	1.03	0.70	0.82	0.80	0.64
Ven A – BT – ImSn	1.33	1.47	1.10	1.16	1.19	1.16
Ven B – FR4 – HASL	1.86	1.62	1.55	1.48	1.85	1.59
Ven B – FR4 – ImSn	0.13	0.34	0.10	0.37	0.10	0.10

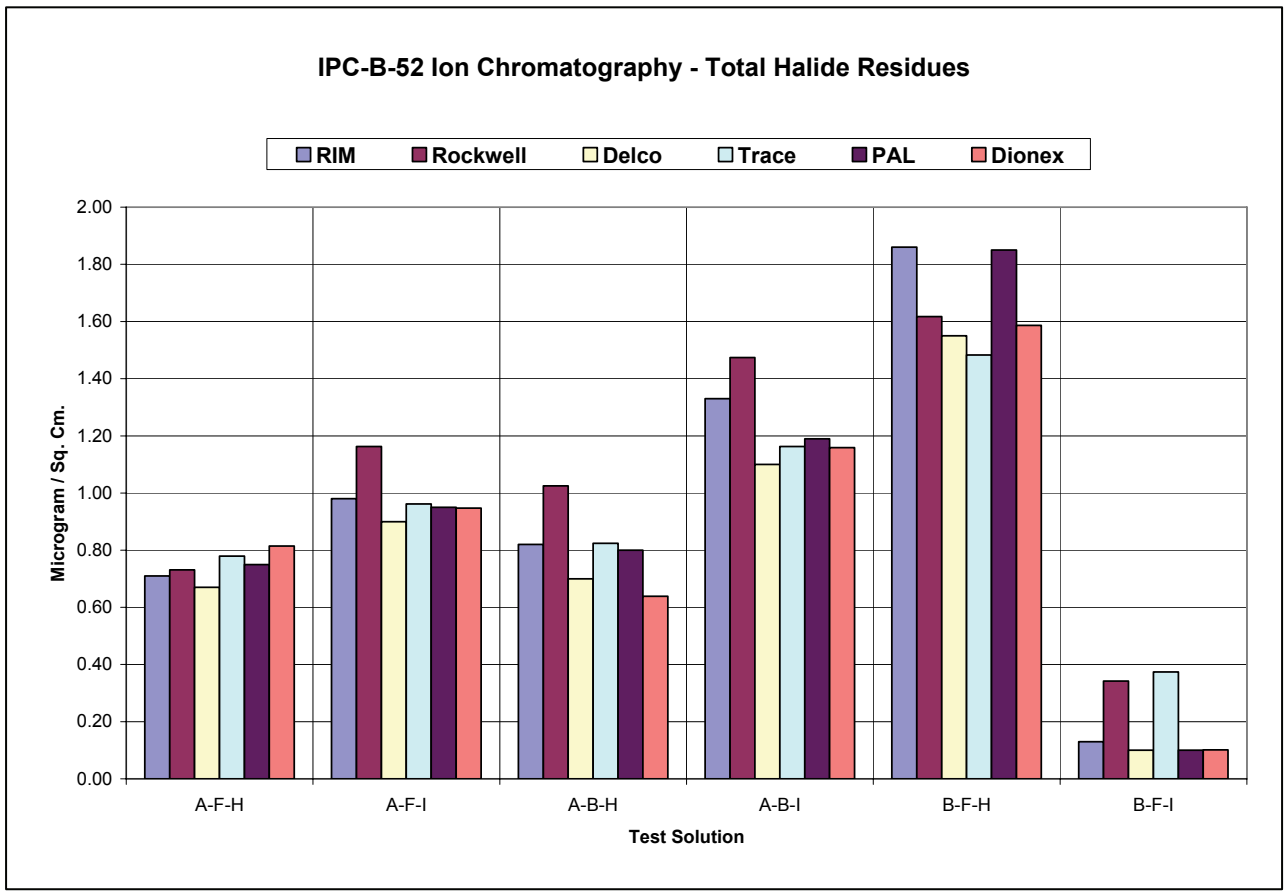


Figure 27 - Total Halide Between Test Labs

Table 7 shows a combination of the chloride and bromide values reported in Tables 4 and 5. There is reasonable agreement between test sites. Total halide has occasionally been used in some cleanliness studies as a good measure of overall cleanliness. Since the bromide levels were quite low for the bare boards studied, most of the combined data is chloride. However, if a brominated compound had been used in fabrication, the total of the two halide residues could be significant.

IPC-5701, Users Guide for Cleanliness of Unpopulated Printed Boards, gives an example of a Delphi Delco Electronics bare board specification in which a combined halide level of 1.75 µg/cm^2 is recommended. Using that metric, most of the bare boards would be considered clean, from a halide residue perspective.

Table 8 - Total Anion (Chloride, Bromide, Sulfate)

Sample	RIM	Rockwell	Delco	Trace	PAL	Dionex
Ven A – FR4 – HASL	1.62	1.92	1.57	1.62	1.72	2.01
Ven A – FR4 – ImSn	7.29	7.21	5.90	6.76	6.94	7.43
Ven A – BT – HASL	2.13	2.51	1.90	1.90	2.06	2.15
Ven A – BT – ImSn	6.46	6.39	5.20	5.64	5.93	6.42
Ven B – FR4 – HASL	2.85	2.91	2.52	2.38	2.92	2.78
Ven B – FR4 – ImSn	1.17	1.75	1.04	1.28	1.10	1.28

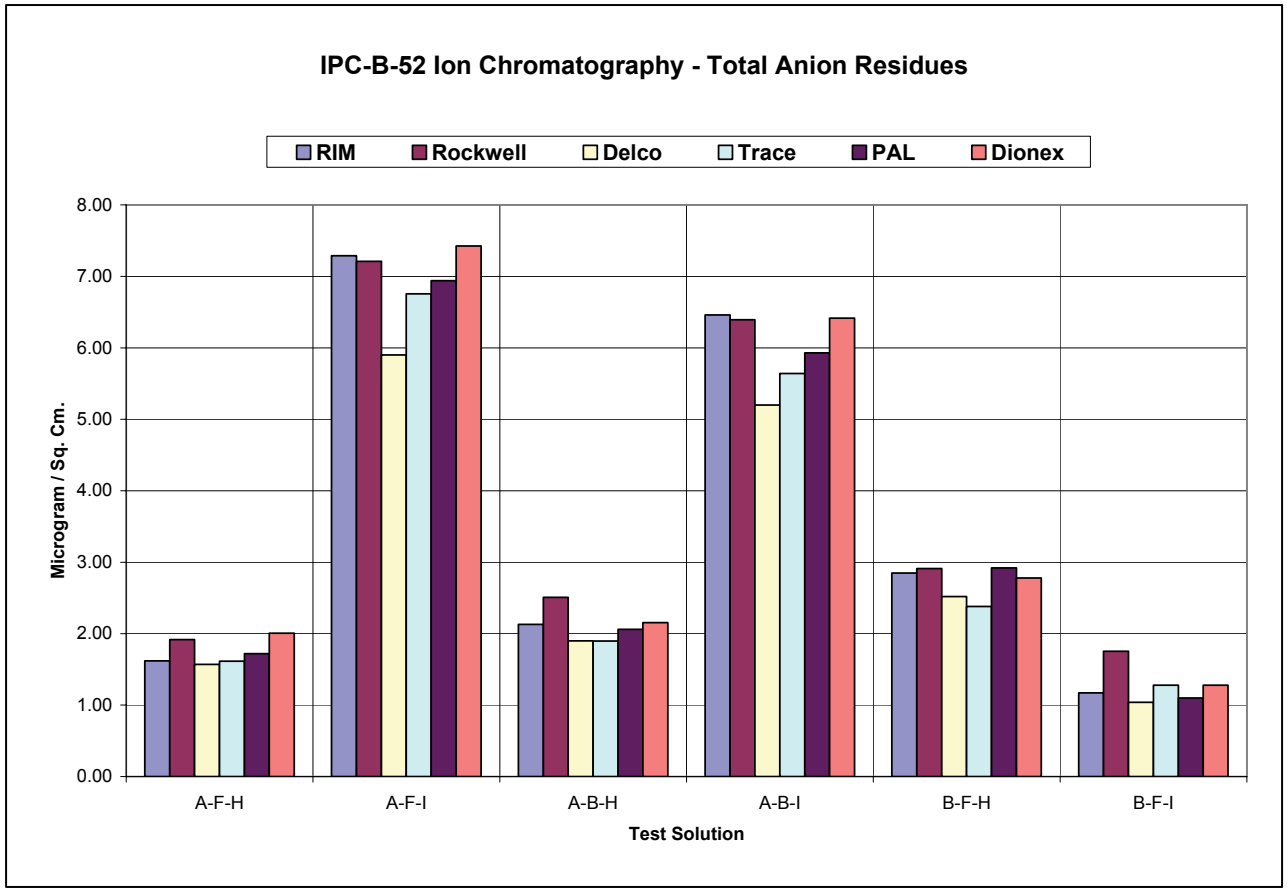


Figure 28 - Total Anions Between Test Labs

Table 8 shows the sum of the chloride, bromide, and sulfate residues. The term "total anions" is somewhat misleading as trace amounts of fluoride, nitrate, and nitrite were found on some samples. Those amounts were all considered to be low enough to be excluded from consideration. Much of the published work to date on electrochemical failures and the relation to cleanliness by IC has focused on "the usual suspects" of chloride, bromide, and sulfates.

As before, the good agreement with chloride and sulfate data translates to good agreement for this data. As a standard method, Rockwell Collins runs a standard anion spread of fluoride, chloride, nitrite, bromide, nitrate, phosphate and sulfate, with calibrated amounts between 0 and 20 ppm for each anion. Other test facilities may add or subtract other anions to this spread, depending on the application.

Table 9 - Sodium Levels

Sample	RIM	Rockwell	Delco	Trace	PAL	Dionex
Ven A – FR4 – HASL	0.04	0.32	0.14	0.18	0.21	0.37
Ven A – FR4 – ImSn	0.08	0.28	0.15	0.16	0.19	0.21
Ven A – BT – HASL	0.07	0.33	0.16	0.24	0.21	0.27
Ven A – BT – ImSn	0.05	0.00	0.01	0.01	0.09	0.15
Ven B – FR4 – HASL	0.13	0.34	0.07	0.26	0.41	0.31
Ven B – FR4 – ImSn	0.04	0.00	0.07	0.01	0.11	0.12

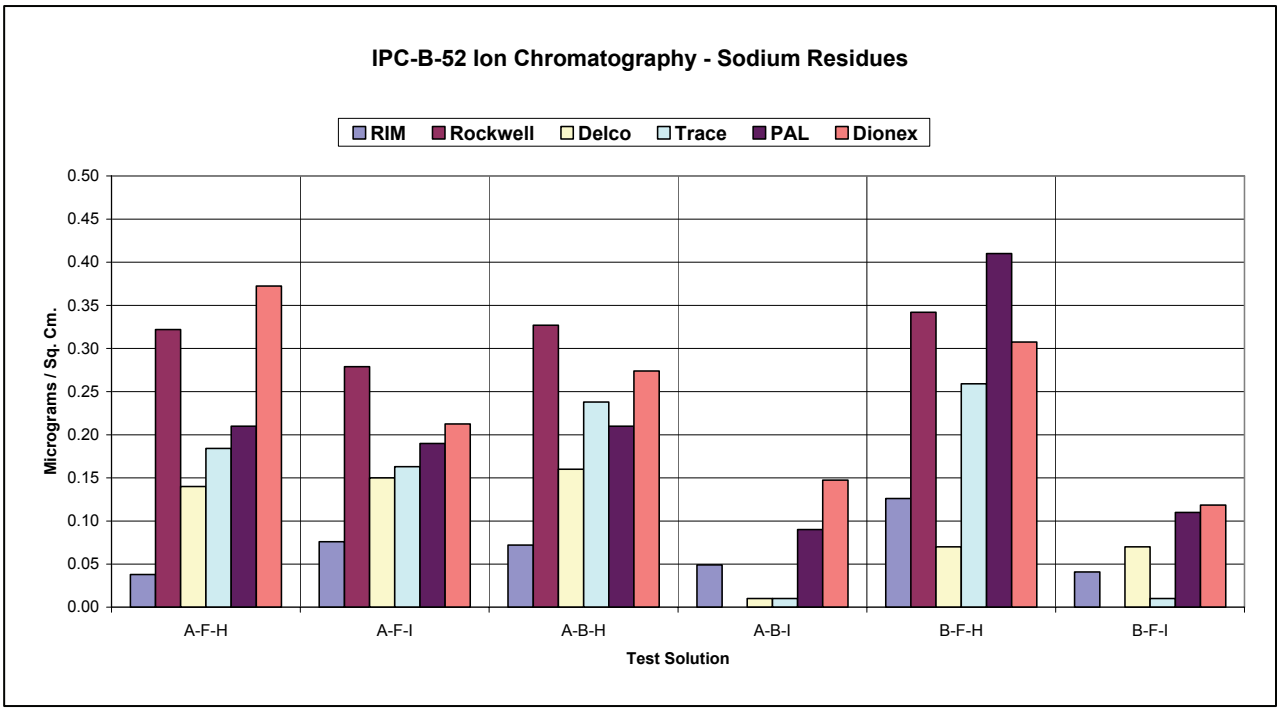


Figure 29 - Comparison of Sodium Between Test Labs

Table 9 shows the data for sodium. Far less has been published about acceptable or unacceptable levels of cation residues, compared to anion (halide) residues. Consequently, many of the test laboratories do not have methods for cation analysis as refined as those for anion analysis. This may be one contributing factor in the differences seen between test sites. In addition, some of the test sites ran suppressed cations, while others ran unsuppressed cations.

Sodium is a very common material on printed circuit boards and it is rare to see a chromatogram showing no sodium. The Delco bare board specification, shown in IPC-5701, lists a value of 2.0 µg/cm^2 for combined sodium and potassium. If one assumes an equal contribution for sodium and potassium, an "acceptable" range for sodium would be 1.0 µg/cm^2. If that can be assumed, all of the boards would have desirably low levels of sodium.

Table 10 - Potassium Levels

Sample	RIM	Rockwell	Delco	Trace	PAL	Dionex
Ven A – FR4 – HASL	0.00	0.00	0.18	0.18	0.28	0.00
Ven A – FR4 – ImSn	0.00	0.92	0.09	0.01	0.14	0.00
Ven A – BT – HASL	0.00	0.00	0.17	0.19	0.26	0.00
Ven A – BT – ImSn	0.00	0.71	0.00	0.01	0.07	0.00
Ven B – FR4 – HASL	0.00	0.00	0.02	0.01	0.19	0.00
Ven B – FR4 – ImSn	0.00	0.00	0.02	0.01	0.06	0.00

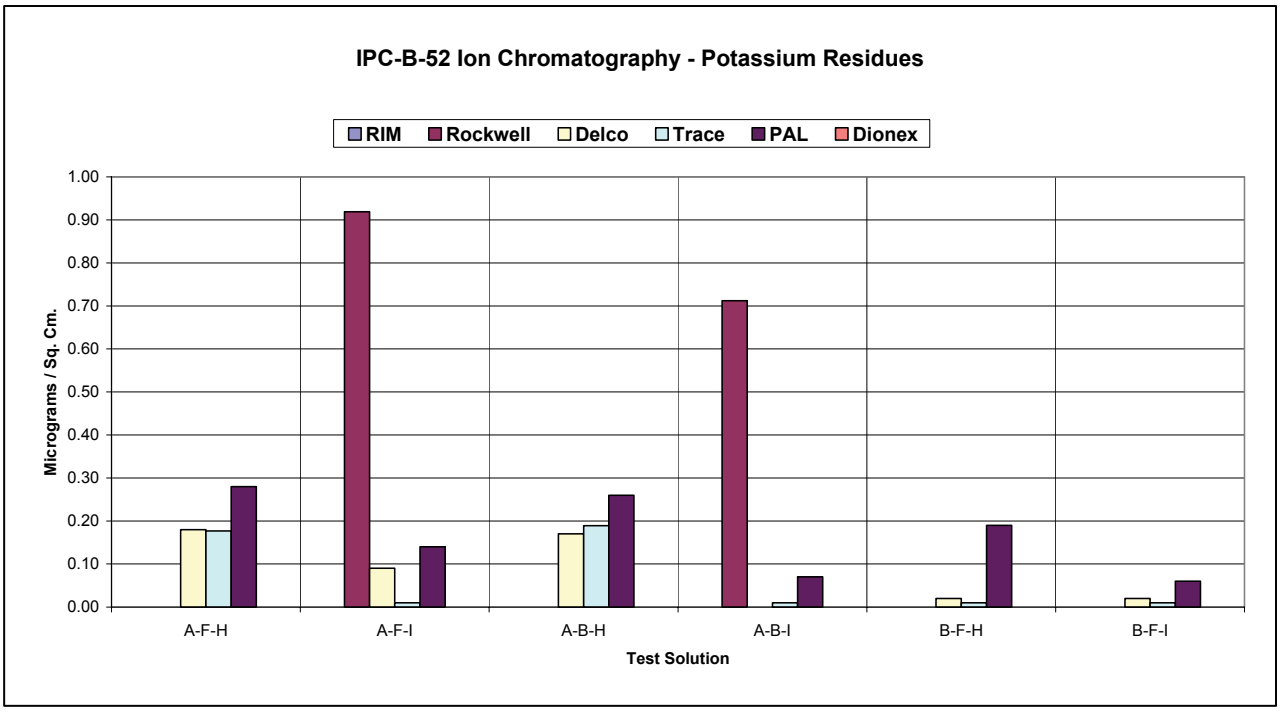


Figure 30 - Comparison of Potassium Between Test Labs

Table 10 shows the values for potassium residues, in which a wide difference was seen between Rockwell Collins and the other test laboratories. At present, the cause of the disparity is unknown. If the Rockwell Collins data is discounted, fairly good agreement is seen between Delco, Trace and PAL.

Table 11 - Calcium Levels

Sample	RIM	Rockwell	Delco	Trace	PAL	Dionex
Ven A – FR4 – HASL	0.09	1.03	1.10	0.73	0.58	0.61
Ven A – FR4 – ImSn	0.08	0.00	0.14	0.00	0.27	0.21
Ven A – BT – HASL	0.26	1.18	1.70	1.21	1.09	0.97
Ven A – BT – ImSn	0.11	0.24	0.08	0.00	0.19	0.17
Ven B – FR4 – HASL	0.23	0.51	0.53	0.40	0.59	0.42
Ven B – FR4 – ImSn	0.07	0.35	0.22	0.42	0.33	0.25

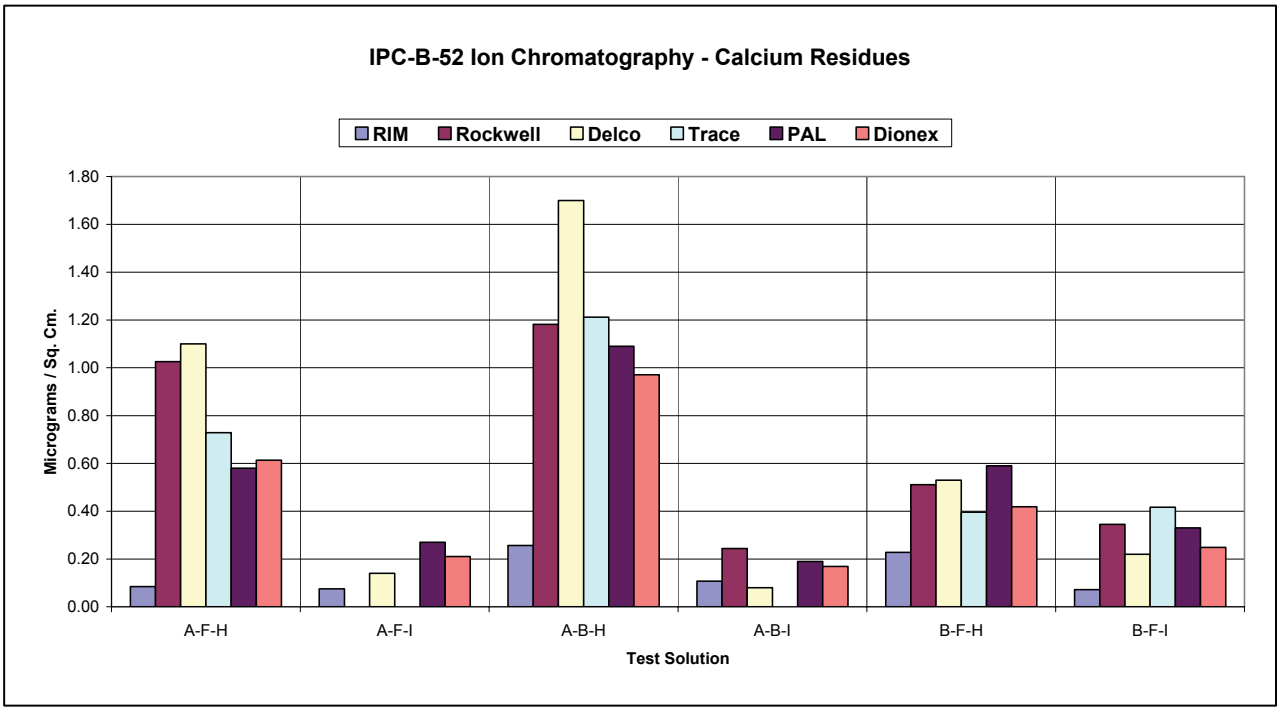


Figure 31 - Comparison of Calcium Between Labs

Table 11 shows the data for calcium residues. Calcium is a fairly common residue on bare boards and often comes from the solder mask itself, or sometimes due to processing solutions that were not adequately cleaned. The Delco specification recommends a value of less than 3.0 µg/cm^2 for combined calcium and magnesium (found only in trace amounts in this study).

Table 12 - Total Cation (Sodium, potassium, calcium)

Sample	RIM	Rockwell	Delco	Trace	PAL	Dionex
Ven A – FR4 – HASL	0.12	1.35	1.42	1.09	1.07	0.99
Ven A – FR4 – ImSn	0.15	1.20	0.38	0.17	0.60	0.42
Ven A – BT – HASL	0.33	1.51	2.03	1.64	1.56	1.24
Ven A – BT – ImSn	0.16	0.96	0.09	0.02	0.35	0.32
Ven B – FR4 – HASL	0.35	0.85	0.62	0.67	1.19	0.73
Ven B – FR4 – ImSn	0.11	0.35	0.31	0.44	0.50	0.37

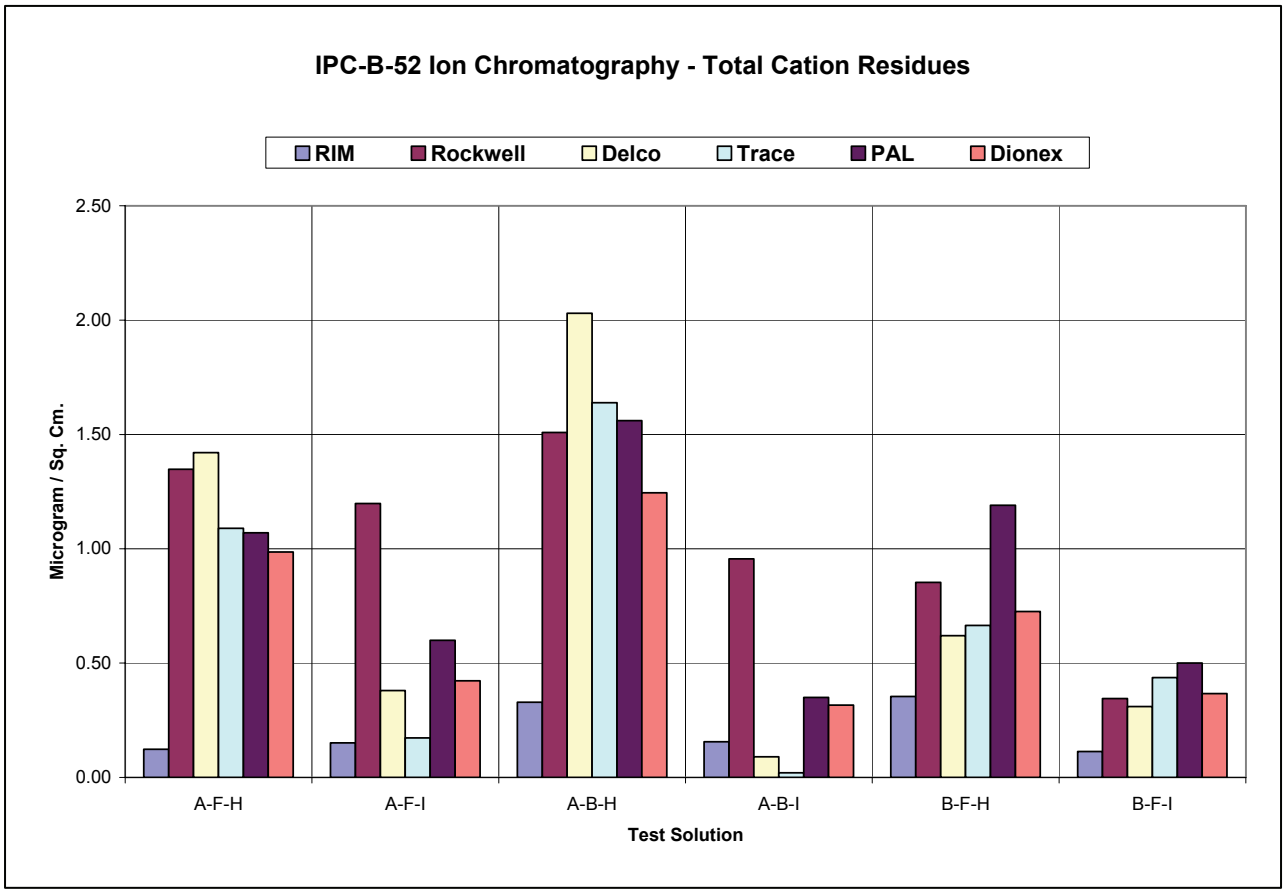


Figure 32 - Comparison of Total Cations Between Test Labs

Table 12 shows the additive sum of sodium, potassium, and calcium. Trace amounts of ammonium and magnesium were also found by most participating labs, but are not included in this sum.

For most of these cation species in this study, relatively low levels were found. Published data is very scarce on the role of cation species in electronics failures. The author's experience, based on internal studies at Rockwell Collins, indicate that none of the levels of these cations would be considered as a hazard. Rockwell Collins regularly tests with a cation spread of sodium, ammonium, potassium, calcium and magnesium, with concentrations between 0 and 20 ppm for these cations.

When high levels of cations are found, it can be indicative of a change in manufacturing materials or processes. Increases in ammonium can indicate a problem with mask developing. Increases in calcium can mean that water hardness or water purity in rinsing has significantly degraded. Increases in sodium or potassium can mean inadequate solder mask cure, such that sodium and potassium are leached from the mask during the IC extraction phase.

Surface Insulation Resistance (SIR)

Rather than use any of the traditional temperature-humidity profiles for the SIR test, a combination profile, using progressing levels of temperature and humidity was chosen for research purposes. The chamber was programmed with the profile outlined in Table 13 and illustrated in Figure 33.

Figure 33 - Temperature Humidity Profile

Table 13 - Temperature Humidity Profile

Segment	Temp (°C)	Humidity (% RH)	Duration (Hrs)
1	25	50	2
2	35	85-90	24
3	40	93	48
4	85	85-90	24
5	25	50	12

Work by NPL [Reference 6] has suggested that a low voltage, on the order of 5-10 volts DC, may be a more difficult electrification condition than the historical levels of 50-100 volts DC found in Bellcore or IPC test methods. The lower applied voltage levels tend to preserve the dendrites where higher applied voltages would have vaporized metal filaments. Consequently, a test voltage of 10 VDC was chosen. This voltage was applied to all test patterns throughout the test. This means that a different voltage gradient existed for all test patterns.

The NPL work has also indicated the need for frequent monitoring of SIR, on the order of every 30-60 minutes. A test interval of 60 minutes was chosen.

Test Procedure

1. A test fixture comprised of Teflon wiring, FEP resin edge card connectors, and stainless steel construction was developed for repetitive SIR testing of the SIR Main Board. A photo of this test fixture is shown in Figure 34. This test fixture was designed to interface to a Concoat Systems Ltd. AutoSIR64 test system.

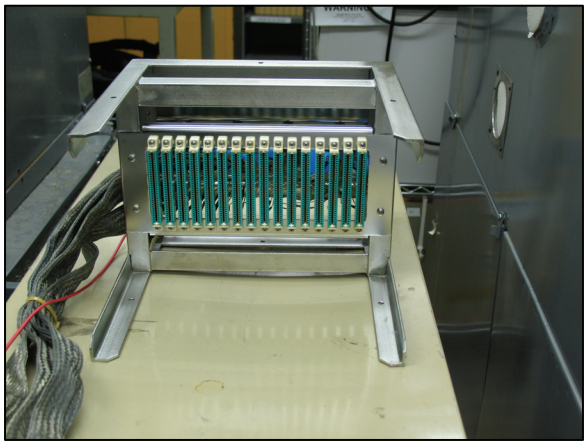


Figure 34 - SIR Test Rack

2. Prior to any testing, the test fixture was validated using a specially developed SIR calibration card, shown in Figure 35. This card matched the pinout of the SIR Main Board, with each corresponding circuit incorporating a high value resistor (Reference 7). Each resistor had been previously measured by the Rockwell Collins Metrology department. All fixtures were found to be within 1% of the measured value of the resistor for all fixtures tested.
3. The Main SIR boards were inserted into the validated test fixture and the chamber closed. The chamber was allowed to equilibrate at 25C and 50% RH for two hours prior to initial measurements.
4. Following initial measurements, the chamber profile was initiated and the AutoSIR data logging routing started.
5. The AutoSIR logs individual channels into a delimited text file, which was later imported into Microsoft Excel for analysis and graphing.

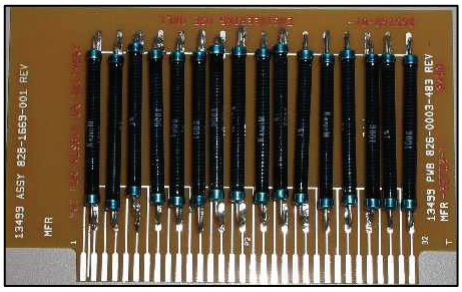


Figure 35 - B52 Connector Checker Assembly

Test Results – Visual

After completion of the SIR testing, each test board was visually examined for the presence of dendrites, corrosion, or other visual anomalies. Each test pattern was examined at 10-30X, with light incident from the top and with light behind the board (backlighting). The use of backlighting is effective when looking for dendrites.

Test Results – Numeric

Logging test data every hour over a five day period, on a large number of channels, generates a considerable amount of data, too great to show in this paper. The following figures show the logged SIR vs. Time. The Y-axis in each graph is in LogOhms, which is the base-10 logarithm of the measured resistance. A value of 6.0 is 1E+6 ohms; a value of 7.0 is 1E+7 ohms, etc. The full SIR data files are available from the author. The AutoSIR also has the ability to separately log temperature and humidity via a test probe, inserted in the area of the test boards. The resulting temperature-humidity log is shown in Figure 33.

It should be noted that some of the data has been edited. The AutoSIR occasionally demonstrates a "hiccup" in data acquisition, appearing as an open circuit for one reading across all patterns, and then returning to the baseline. Concoat has recently determined that this bug is due to a handshaking problem in the instrument and is developing a fix. Consequently, such data was deleted and appears in the following charts as a small gap in the lines.

Caution should be used when examining the SIR data in the following charts. SIR data is generally considered to be dependent on the geometry of the test pattern. Therefore, since all of the test patterns differ in geometry, the data from Pattern 1 cannot be directly compared to Pattern 2, etc.

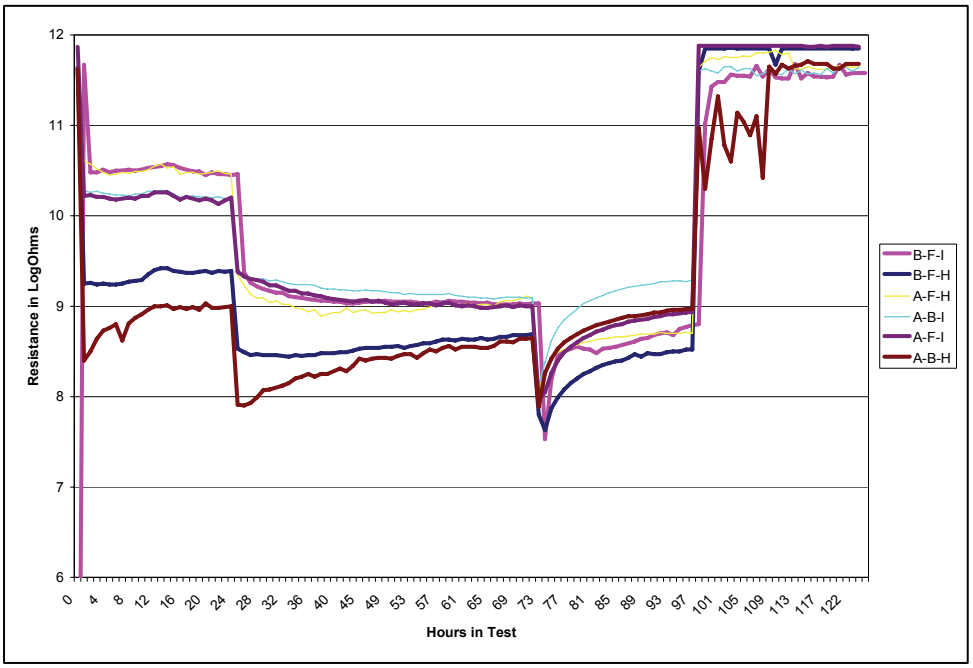


Figure 36 - SIR – Pattern 1
(A-B-I = Vendor A – BT – ImSn)
(B-F-H = Vendor B – FR4 – HASL)
No dendritic growth noted on this pattern on any test board.

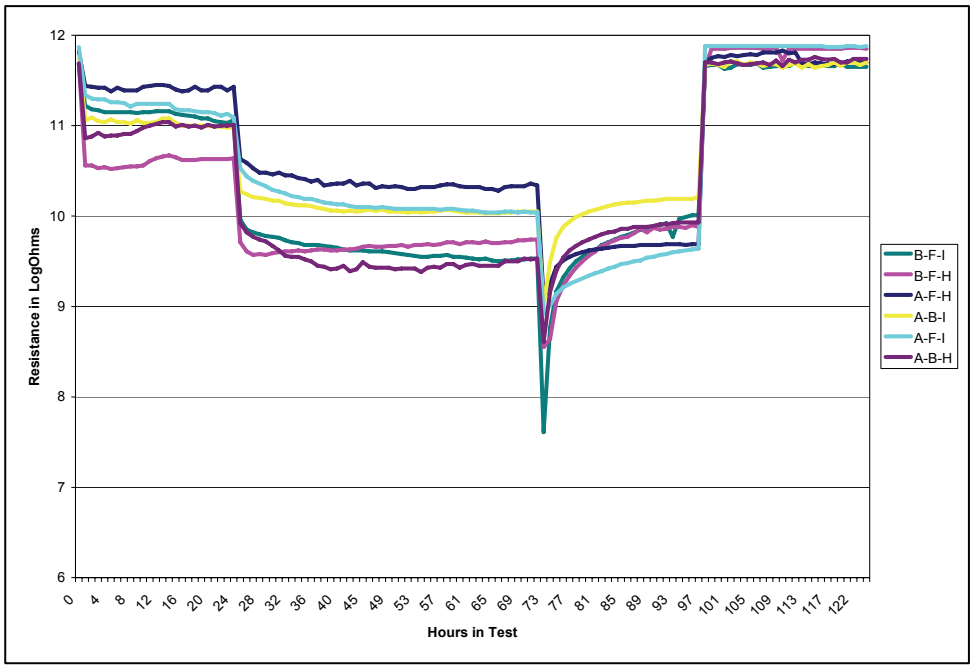


Figure 37 - SIR –Pattern 2
No dendritic growth noted on this pattern on any test board.

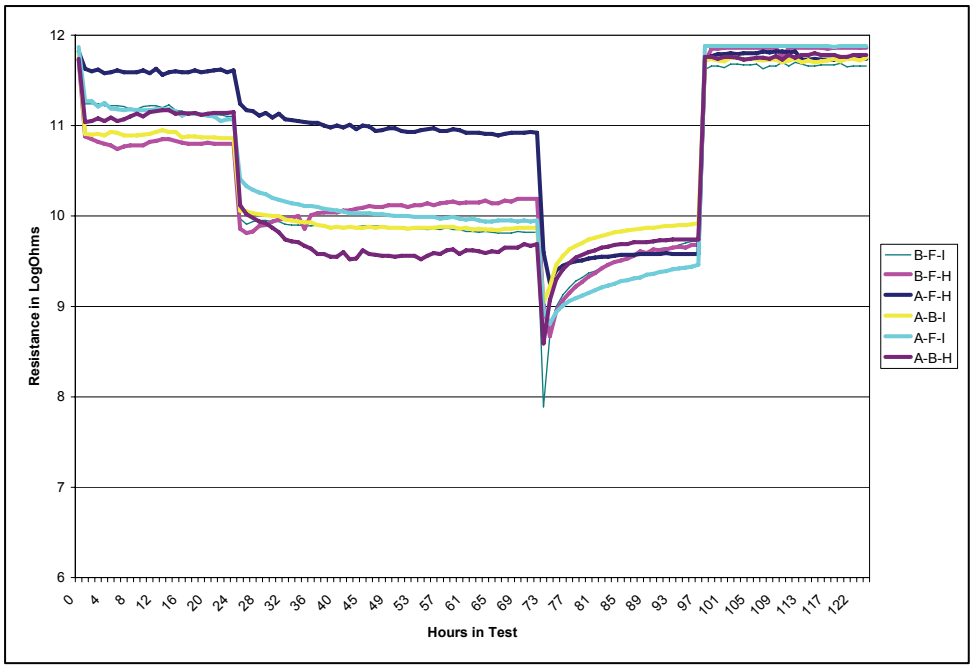


Figure 38 - SIR Pattern 3
No dendritic growth noted on this pattern on any test board.

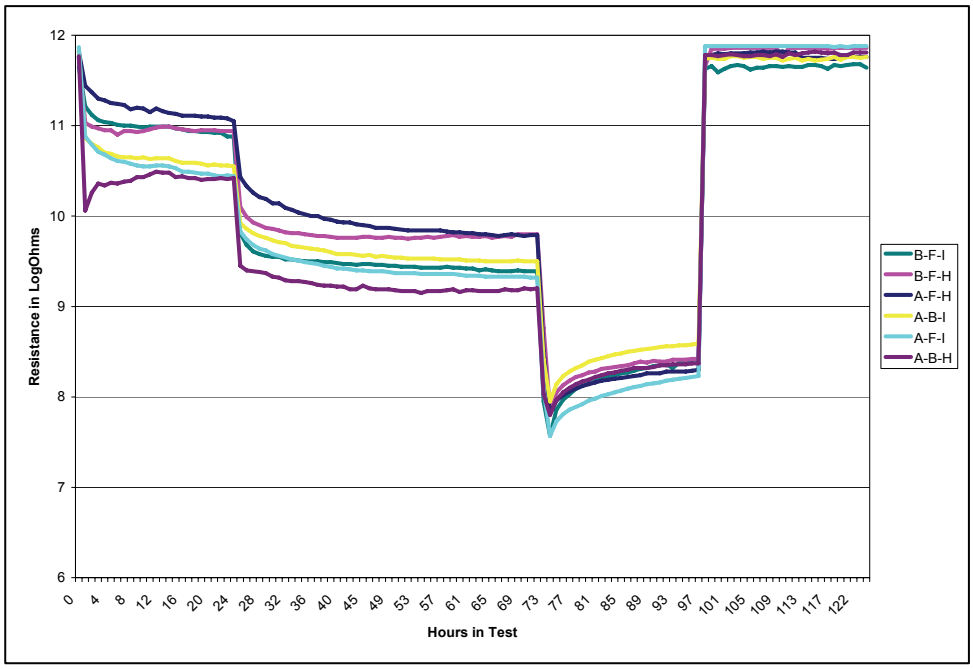


Figure 39 - SIR Pattern 4
No dendritic growth noted on this pattern on any test board.

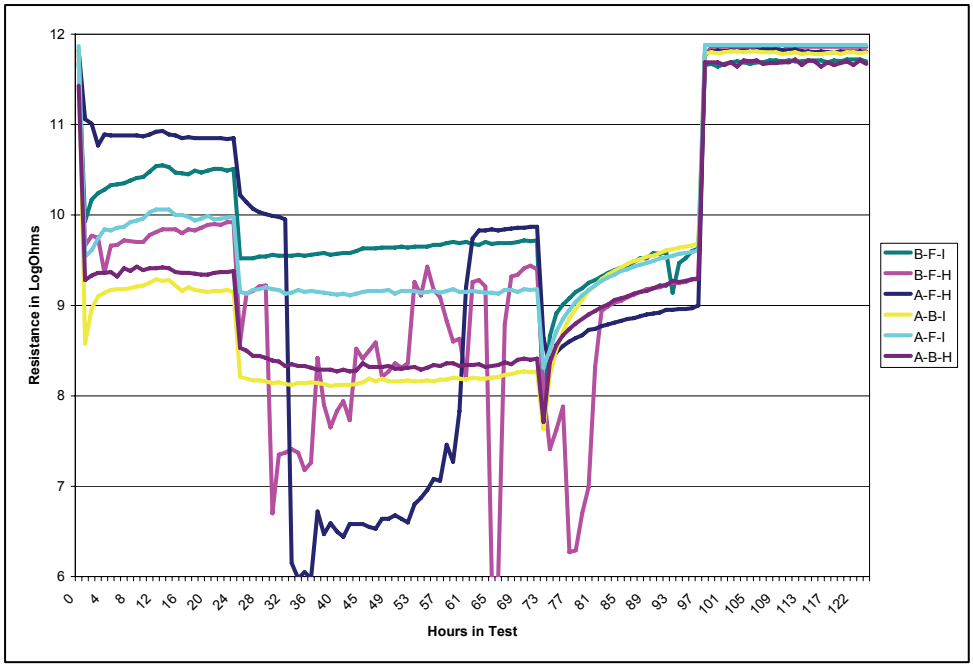


Figure 40 - SIR Pattern 7
(Patterns 5 and 6 are opens)
Dendritic growth found for this pattern on B-F-H and A-F-H

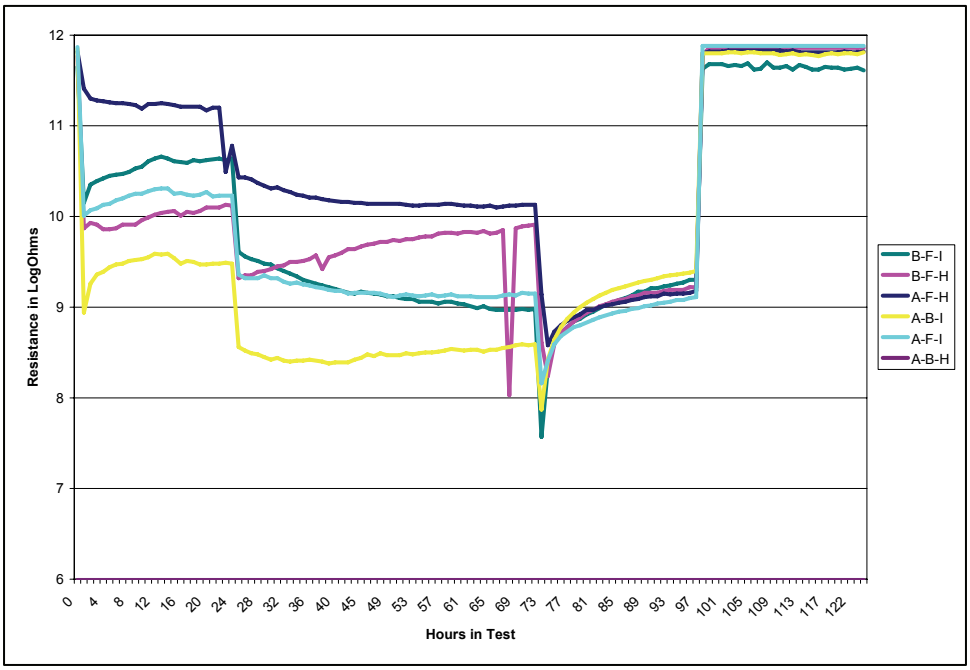


Figure 41 - SIR Pattern 8
Dendritic growth found for this pattern on B-F-H

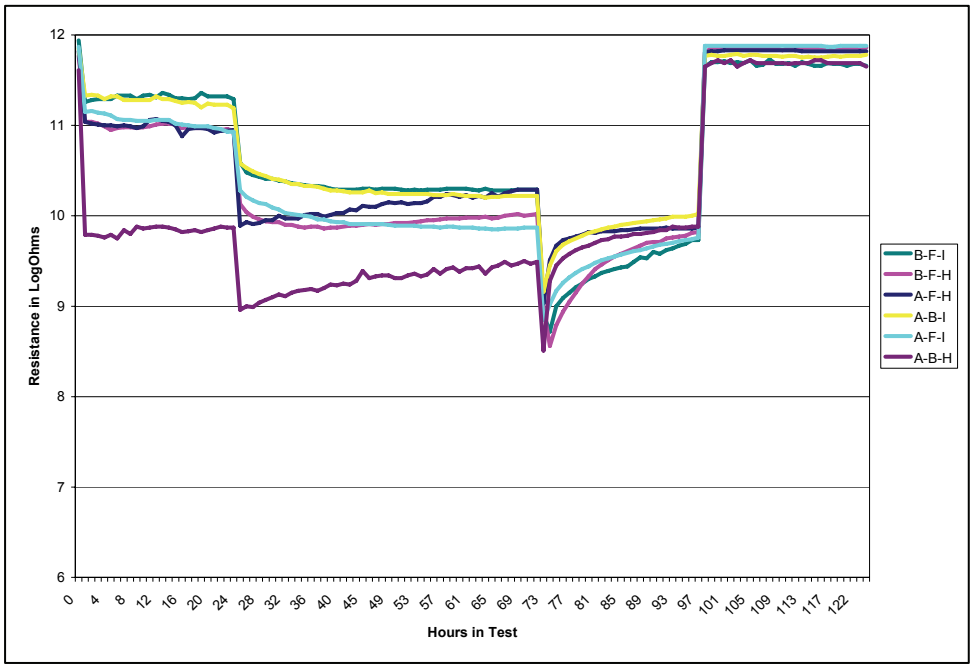


Figure 42 - SIR Pattern 9
No dendritic growth noted on this pattern on any test board

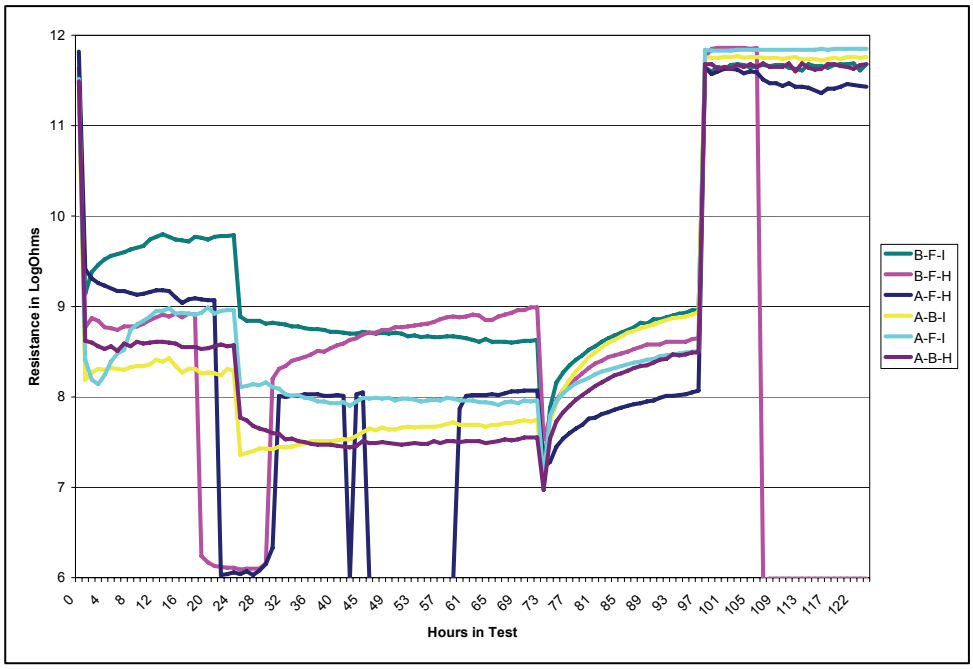


Figure 43 - SIR Pattern 10
Dendritic growth observed on B-F-H and A-F-H

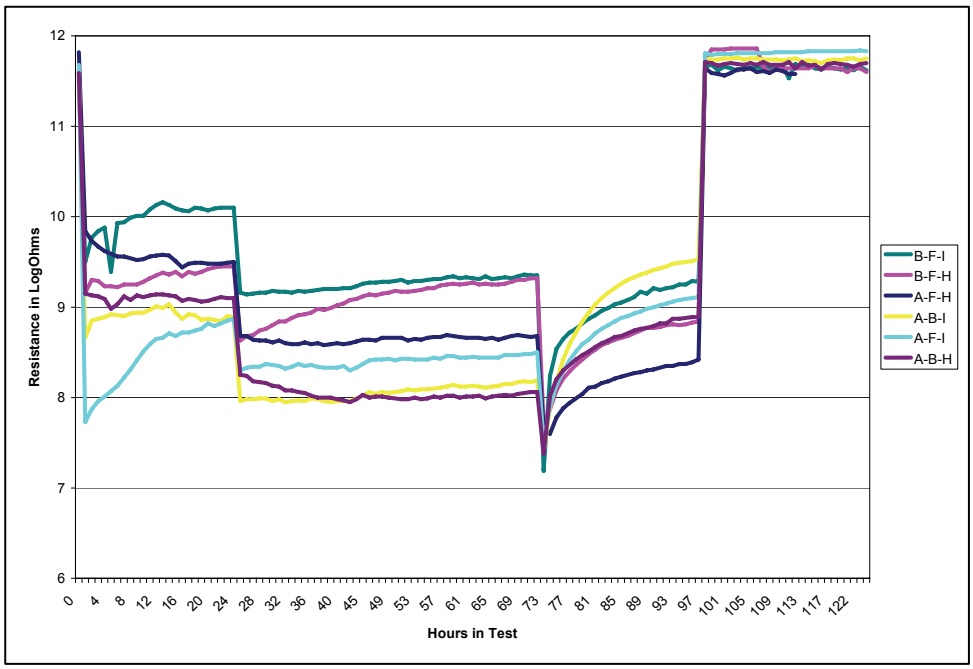


Figure 44 - SIR Pattern 11
No dendritic growth noted on any test board for this pattern

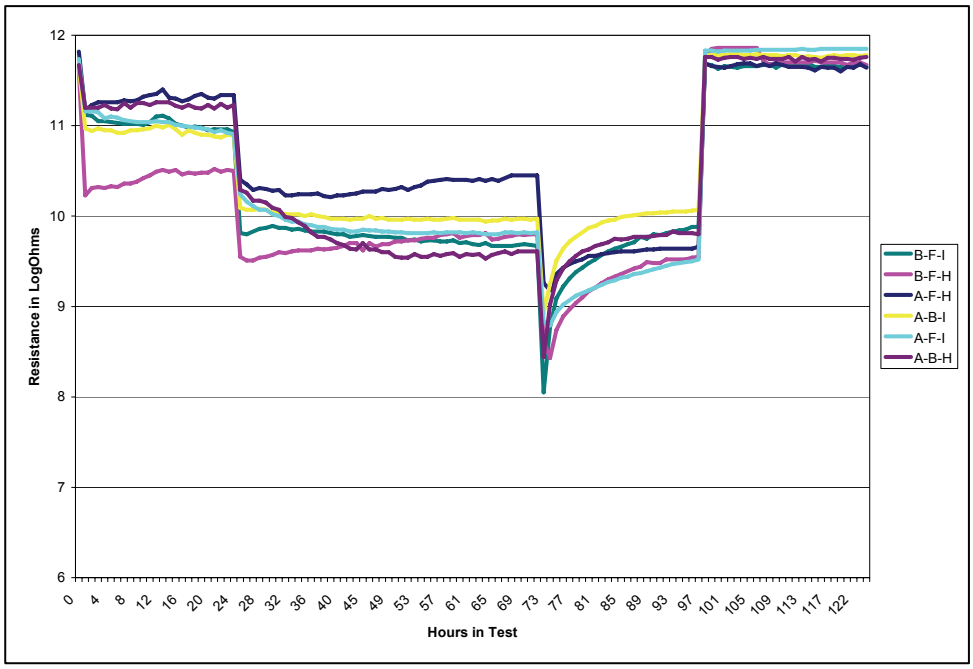


Figure 45 - SIR Pattern 12
No dendritic growth noted for any test board for this pattern

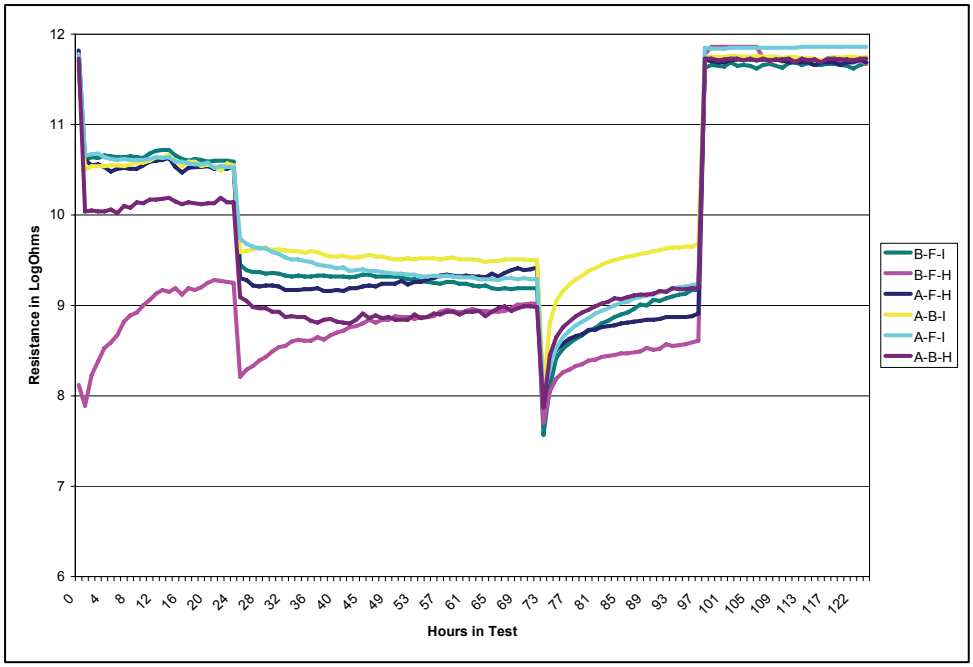


Figure 46 - SIR Pattern 13
Dendritic growth noted for this pattern for B-F-H

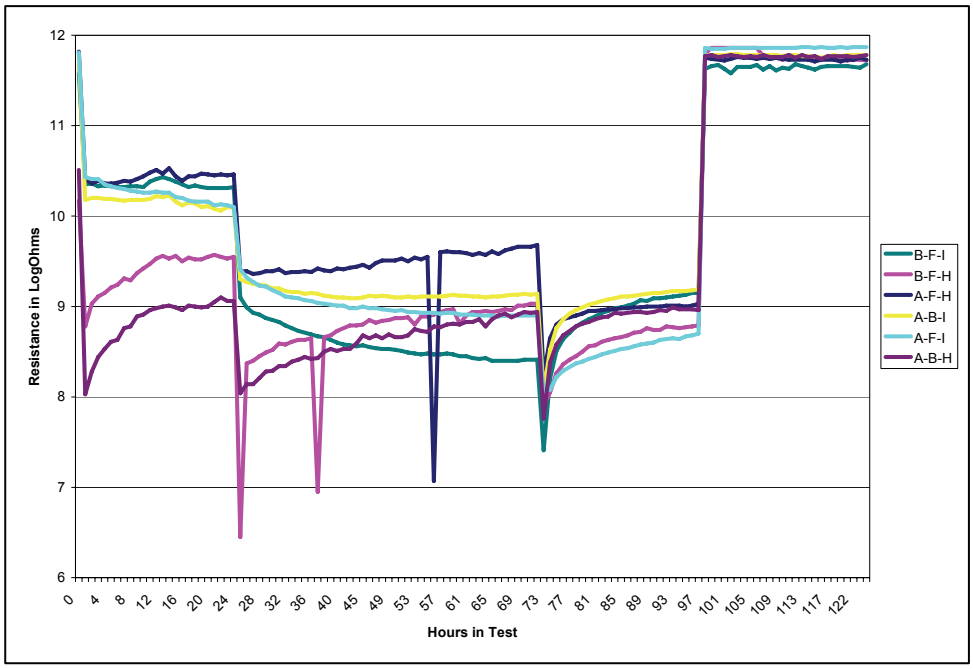


Figure 47 - SIR Pattern 14
Dendritic growth noted for B-F-H and A-F-H

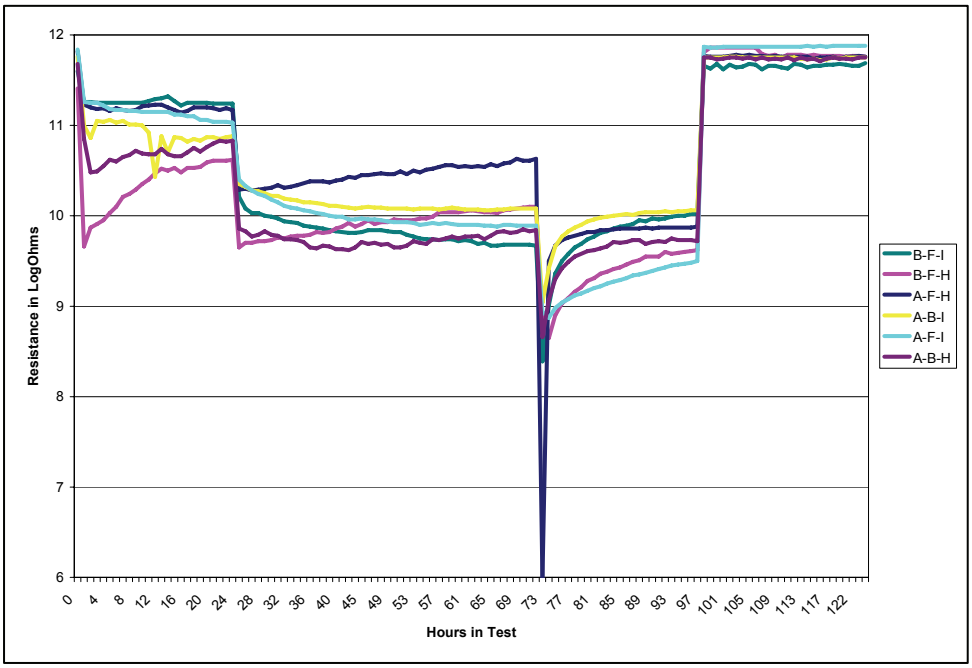


Figure 48 - SIR Pattern 15
No dendritic growth noted for any test pattern

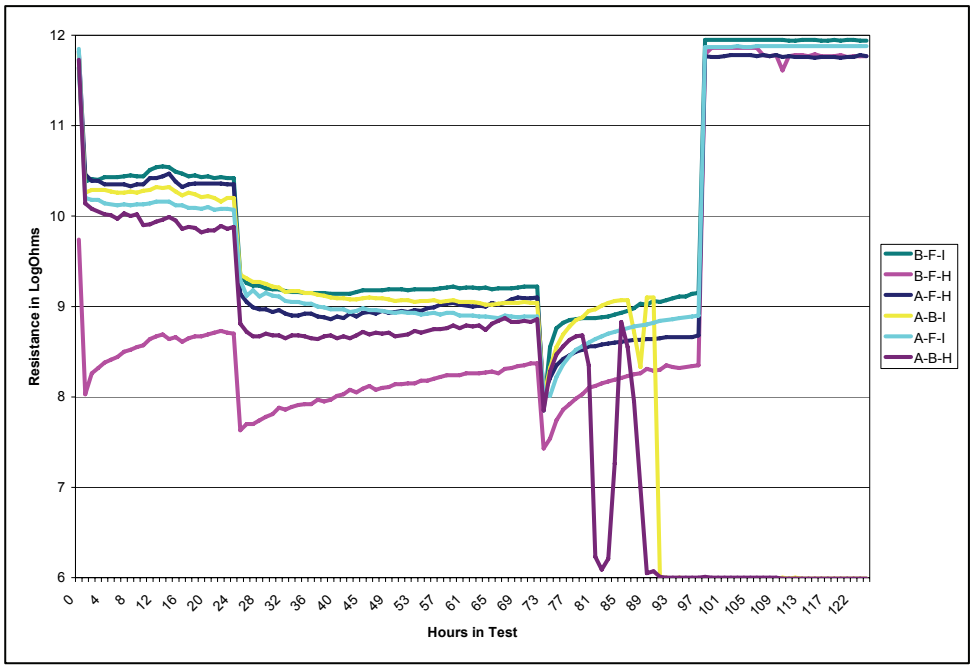


Figure 49 - SIR Pattern 16
Dendritic growth found on B-F-H, A-B-H, and A-B-I

Examples of Dendritic Growth

Figures 50 though 55 show examples of the dendritic growth found. In some cases, the dendritic growth was found only in the outline of a water droplet, as illustrated in Figure 50.

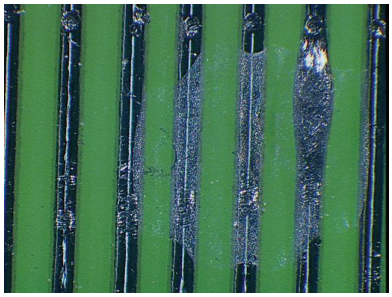


Figure 50.

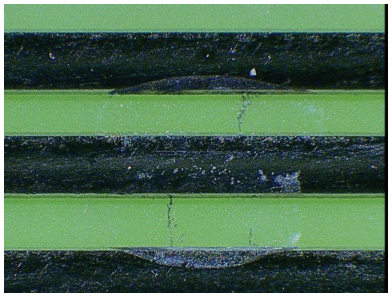


Figure 51.

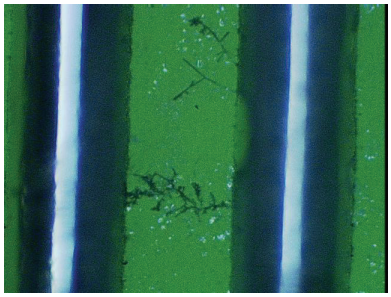


Figure 52.

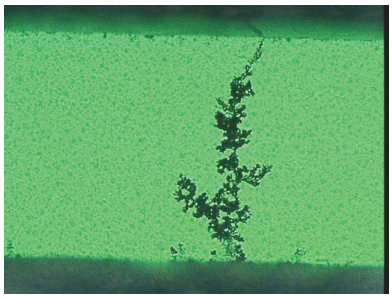


Figure 53.

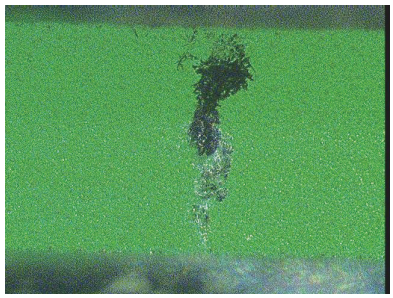


Figure 54.

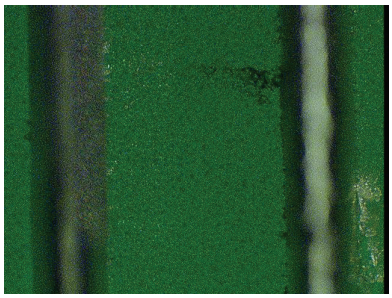


Figure 55.

SIR Mini-Coupon Tests

Test Procedure

A test fixture, comprised of Teflon insulated wiring and an FEP (a polymer of tetrafluoroethylene and hexafluoropropylene) resin edge card connector was developed to test multiple mini-coupons at one time. The test fixture is shown in Figure 56a and was designed to interface with a Concoat Systems Ltd; AutoSIR64 automated test system, shown in Figure 56b. The SIR testing was performed in an Espec temperature humidity chamber. The SIR coupons were tested with the comb patterns facing down, to minimize the possibility of water droplets falling on the energized test patterns.

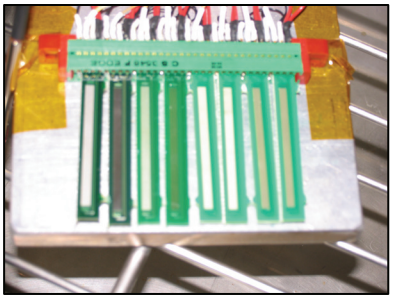


Figure 56a - SIR Mini Coupon Test Fixture

Figure 56b - Concoat AutoSIR

A number of temperature-humidity exposures have been used over the years for SIR testing. The SIR Handbook [Reference 8] goes into great depth on all matters relating to SIR testing.

Considering the historical success of the Bellcore method of monitoring fabrication houses (GR-78-CORE, section 14.4), a test environment of 35°C / 85-90% relative humidity (RH) was chosen. The following test parameters were used:

- Bias voltage: 10 volts DC
- Measurement voltage: 10 volts DC (same polarity as bias voltage)
- Measurement frequency: every 10 minutes
- Test duration: 24 hours

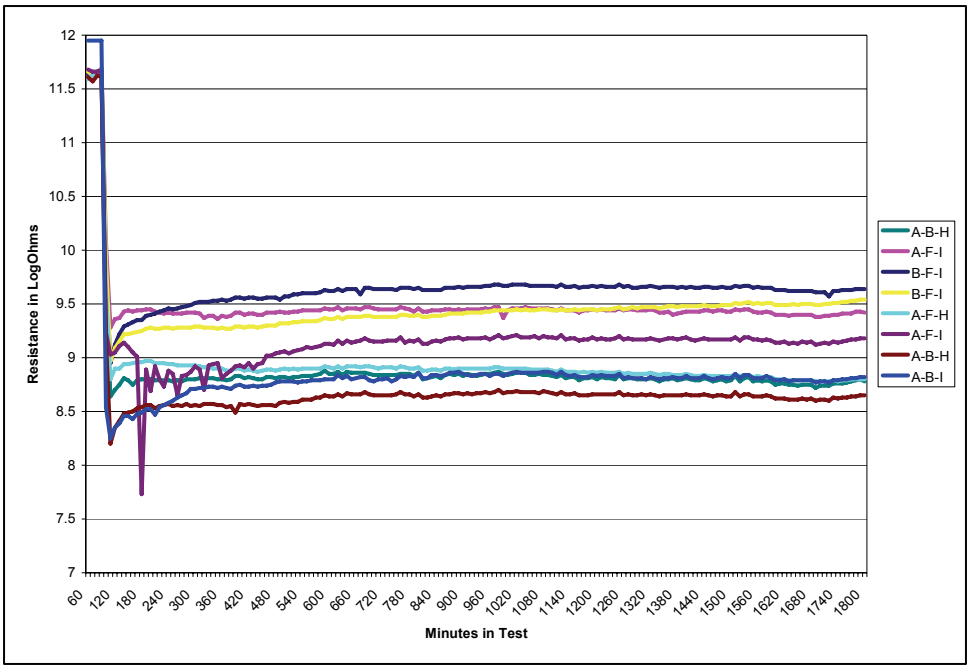


Figure 57 - SIR for prototype coupons having no solder mask stripes.

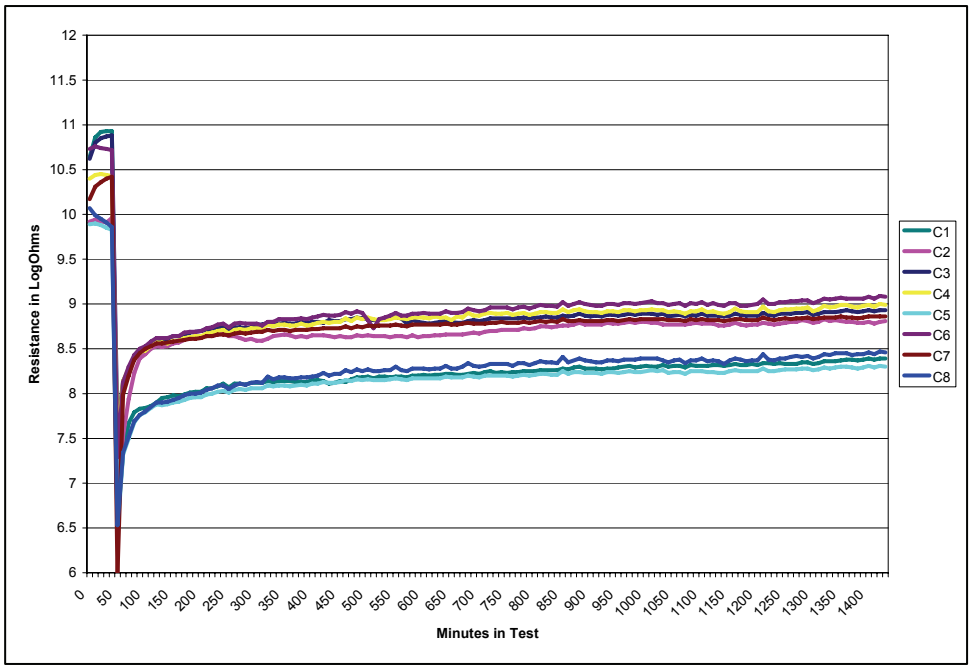


Figure 58 - SIR for revised coupons having the solder mask stripes.

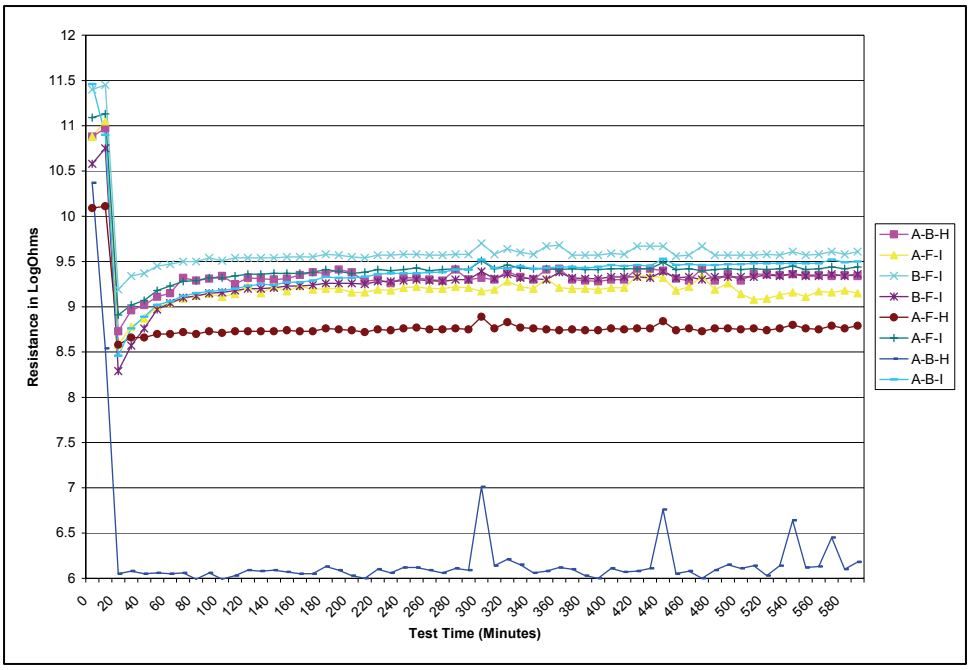


Figure 59 - SIR for cleaned prototype coupons having no solder mask stripes.

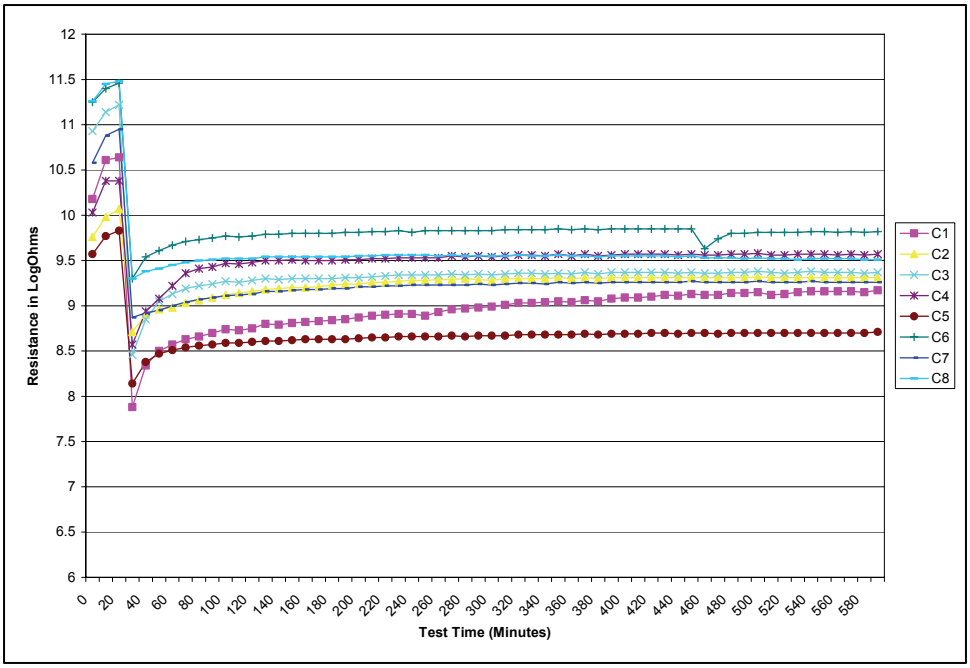


Figure 60 - SIR for cleaned revised coupons having the solder mask stripes.

As an experiment, following the SIR testing, each coupon was extracted using 10% isopropanol and 90% deionized water, for 60 minutes at 80°C. Each coupon was then dried for 30 minutes at 105°C. In the author's experience, this is a fairly effective cleaning method. Each coupon was then subjected to the same short term SIR testing to determine if cleaned coupons had higher levels of SIR.

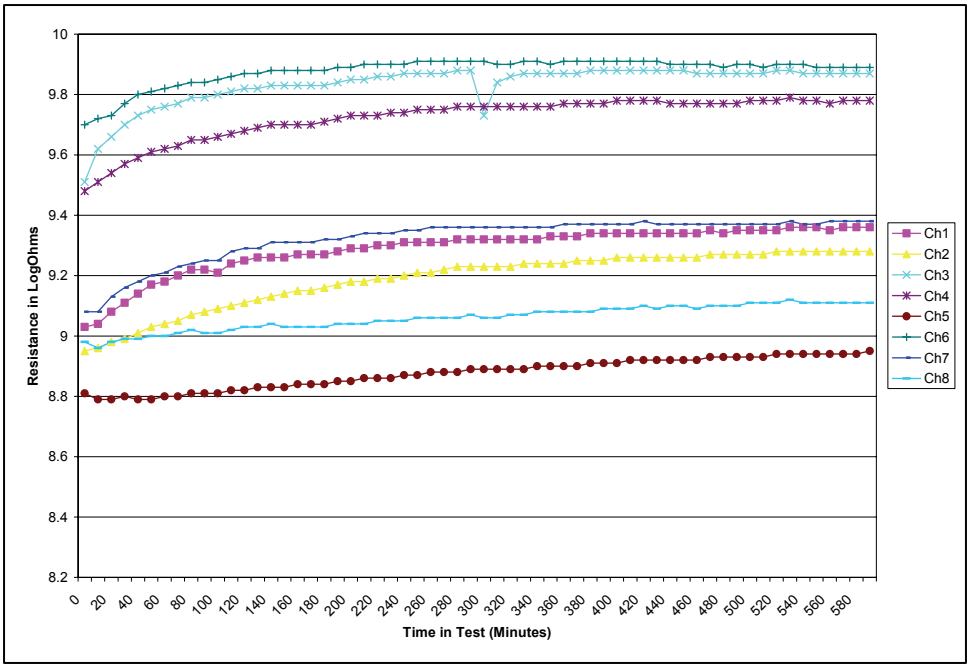
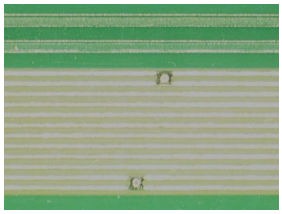


Figure 61 - Measured Resistance of Empty Fixture

Observations on SIR Mini Coupon Data

1. The resistance data taken on the empty fixture shows undesirable results. Ideally, a fixture should have channel-to-channel isolation resistance levels several orders of magnitude above the resistance being measured. At high humidity levels, resistance levels "should" be in the 11-12 LogOhm range or higher. In addition, the fixture resistance levels should be very consistent. As shown in Figure 61, there are 1-2 orders of magnitude differences between channels.
2. Consequently, it is impossible to separate out the "true" resistance readings of measured coupons, whatever the process combinations, from the leakage currents of the fixture.
3. Future testing will compare alternative fixture layouts with hardwiring (direct solder). If fixture testing will be used, a connector checker assembly will have to be developed.
4. In retrospect, the examination of the fixture leakage currents should have been the first examination, rather than the final check.
5. For the connector, one blank contact was left between coupons. Often times, the breakoff tabs of the coupons made straight insertion a challenge. If connectors are used in the future, more room should be left between coupons to accommodate the tabs.
6. In the final visual examination of the coupons, a defect was found on one of the comb patterns, in which a short had been removed from the coupon by cutting a metallic bridge. This is a common method of removing a short, though it damages the substrate. This was the source of the low resistance pattern seen in Figure 59.



7. In the examination of the coupons from the bare board study, most of the coupons from Vendor B had shorts in the mini-coupons for all HASL coupons. In the layout of the B52 board, the direction of the comb pattern of the mini-coupons is transverse to the comb patterns of the Main SIR test board. Since the direction of immersion for the board into the HASL bath is the long direction of the board, the yield on the mini-coupons would be a challenge due to the orientation. A possible re-design consideration would be to make the mini-coupons parallel to the long axis of the main board.
8. An observation made by Rockwell Collins wave solder operators is that the unsupported nature of the mini-coupon end of the test board could lead to that end of the board dipping down as it contacts the molten wave, flooding the surface patterns. Initial trials showed that the boards did not dip down, but if the board was re-designed, more support on this end of the board should be given.

Solder Mask Adhesion Testing

The solder mask coupons, both the prototype pattern (Figure 6) and the revised pattern (Figure 7) were tested for solder mask adhesion per IPC-TM-650, method 2.4.28. The tape used was 3M series 600 tape, 0.5 inch width, with adhesion strength of 15 ounces per linear inch. All testing was done by the same operator, using the same methodology. The tape was kept perpendicular to the coupon surface. All testing was done on Phase 1 boards, which had not been exposed to any manufacturing processes or any kind of conditioning.

None of the solder mask coupons, from either the original configuration or the revised configuration failed the tape pull tests. However, it is generally acknowledged within the IPC solder mask community that you have to have a serious process problem to fail the tape test, especially with the 15 ounces/inch tape strength. The data from Phase 2 and 3 of the test plan should yield more insight on the survivability of solder mask features in manufacturing processes.

Future Testing

At the time of publication of this paper, test data from Phase 2 (solder paste studies), and Phase 3 (full build), was not available. All of the data for Phases 1 – 3 will be published in an IPC technical report, sometime in 2006. A photograph of the IPC-B-52 test board, fully populated, is shown in Figure 62.

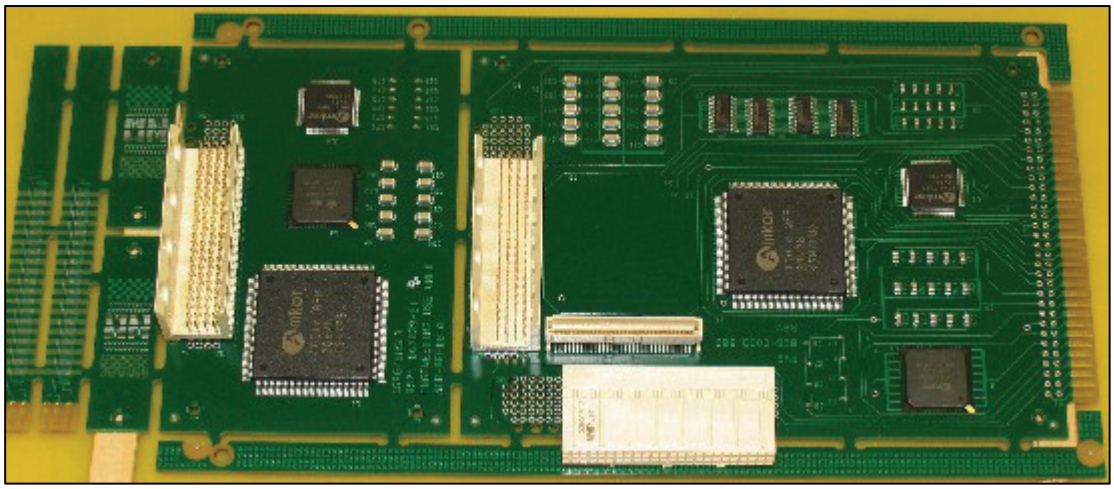


Figure 62 - Full Build IPC-B-52 Test Vehicle

From the first production run of this test board, the board was very manufacturable, with the exception of the vertical and horizontal connectors. These connectors, which work well on the TB57 test board, have mounting tabs molded into the undersides that interfere with the IC coupon and manufacturing rails along the side. These molded feet were clipped off for the first production run. Alternative connectors with the same spacing and style, but without the molded feet, are being investigated.

Conclusions

1. There is not yet enough data to correlate SIR performance with IC residue levels on a scale broad enough that recommendations can be made about acceptable or unacceptable levels of cleanliness for bare boards.
2. By historical / published values, the bare boards studied in Phase 1 would be considered as relatively clean.
3. The test labs seemed to have generally good agreement on ionic residues as determined by ion chromatography, even though all used different equipment and different methods. The IPC Ionic Conductivity Task Group is continuing to work on improvement of IC test methods and analyses.
4. Many of the failures in SIR testing seem to correspond with water droplets falling on the test samples. Even the cleanest of test boards will show dendritic growth when electrified patterns have water droplets fall on them. Greater precautions need to be taken to guard test boards from water droplets in subsequent testing.
5. The SIR mini coupons show promise, but the transverse orientation of the comb to the long axis of the B-52 leads to low board yields. If the board is re-designed, the orientation should be rotated. The SIR Mini-Coupon

fixture was not adequate for the testing. Additional development work must be done to get an attachment method that assures good channel-to-channel isolation and high overall insulation resistance levels. This may not be possible with an edge-connector arrangement.

6. The solder mask coupons showed no test failures; however, the low strength tape used in the tape method is not a challenging test and serious problems with the test boards would have to present to fail this test. The data from Phases 2 and 3, after exposure to manufacturing processes, will be more significant.
7. The data from all of the Rockwell Collins studies will be published as an IPC Technical Report when completed. The completion date is expected in the May-June time frame of 2006.

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- Mr. Phil Kinner, Concoat
- Dr. Chris Hunt and Dr. Milos Durek, National Physical Laboratory

It should also be noted that much of the preparation and physical testing efforts were done by Ms. Courtney Slach and Mr. Nathan DeVore, both material science engineering co-op students from Iowa State University. Without their hard work and dedication, the test samples would still be in the box waiting to be tested and you would not be reading this paper.

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